INTERFACE CONTROL DOCUMENT

Monitor and Control Bus Specification

ICD Document: **A25022N0091**

Revision: Draft

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List of Abbreviations and Acronyms

MCB – Monitor and Control Bus.

PCMC – PC/104 Monitor/Control Mezzanine Card.

FPGA – Field Programmable Gate Array.

DLL – Delay Locked Loop.

PLL – Phase Locked Loop.

1 Revision History

Revision	Date	Changes/Notes	Author
Draft	Feb. 22, 2005	Initial DRAFT release	Zhang Heng

2 Introduction

This document describes the electrical protocol for MCB (Monitor and Control Bus) that is used on the motherboards (Station Board, Baseline Board, Phasing Board and TIMECODE Generator Board) to monitor/control individual chips. The microprocessor can communicate with individual chips from this bus through PCMC (PC/104 Monitor/Control Mezzanine Card). Detailed information on PCMC can be found in [2] in Section 6 References.

3 Context

Figure 3-1 is a simplified diagram showing the connection of the PC/104-*Plus* mezzanine card, PCMC and the motherboard. MCB is located between PCMC and the motherboard.

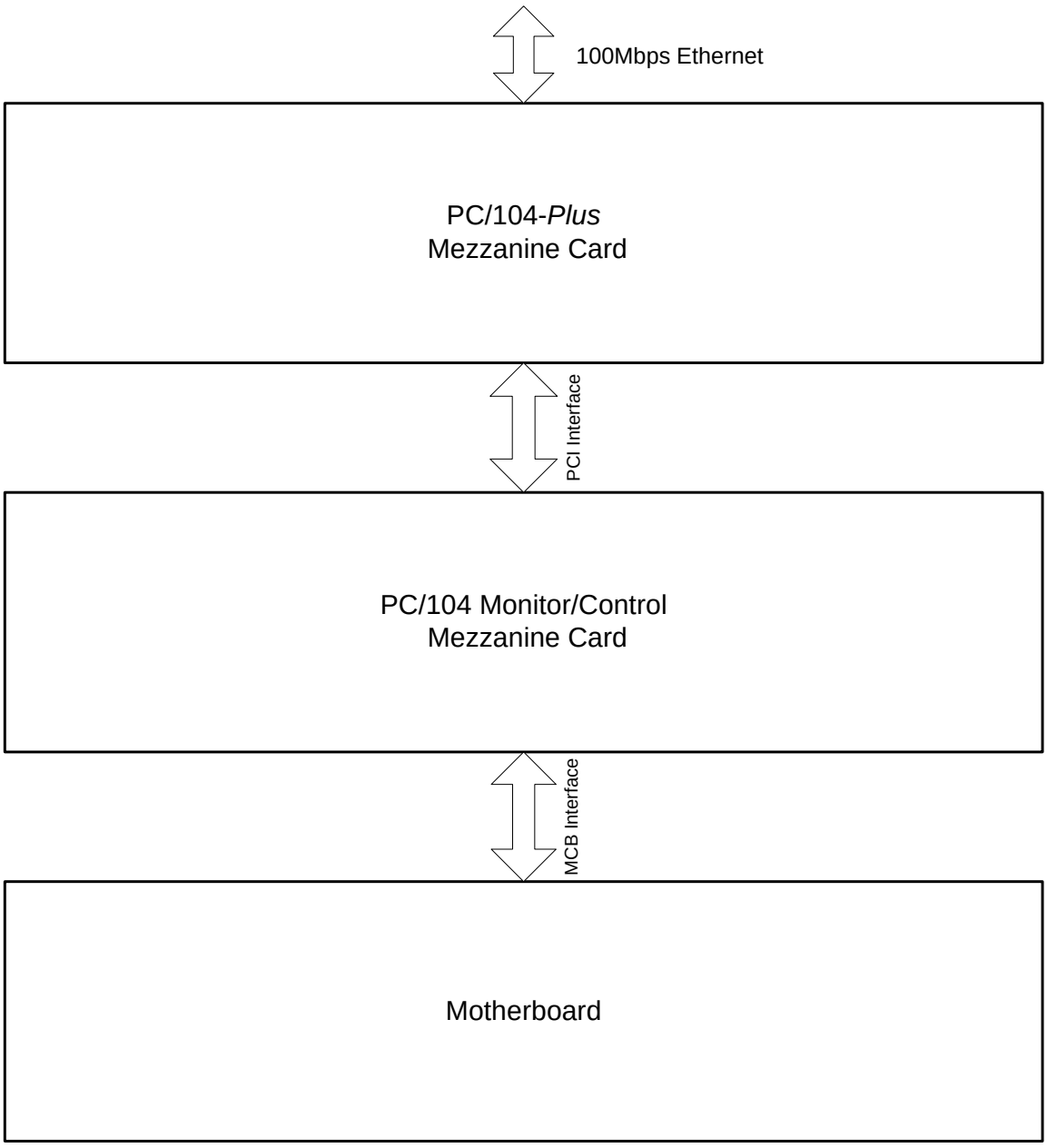

Figure 3- 1 Simplified diagram showing the connection of the PC/104-*Plus* mezzanine card, PCMC and the motherboard. MCB is located between PCMC and the motherboard.

4 Overview

The MCB interface is located between the PCMC and the motherboard. It contains MCB_CLK, MCB_BS*, MCB_RDWR*, MCB_DATA and MCB_ADDR signals. MCB_CLK is running at a maximum of 33MHz. This clock is derived from PCI_CLK. According to the PCI specification, a DLL or a PLL cannot be used on this clock, because of jitter of the PCI clock.

A simplified connection diagram of the MCB interface is shown in Figure 4-1.

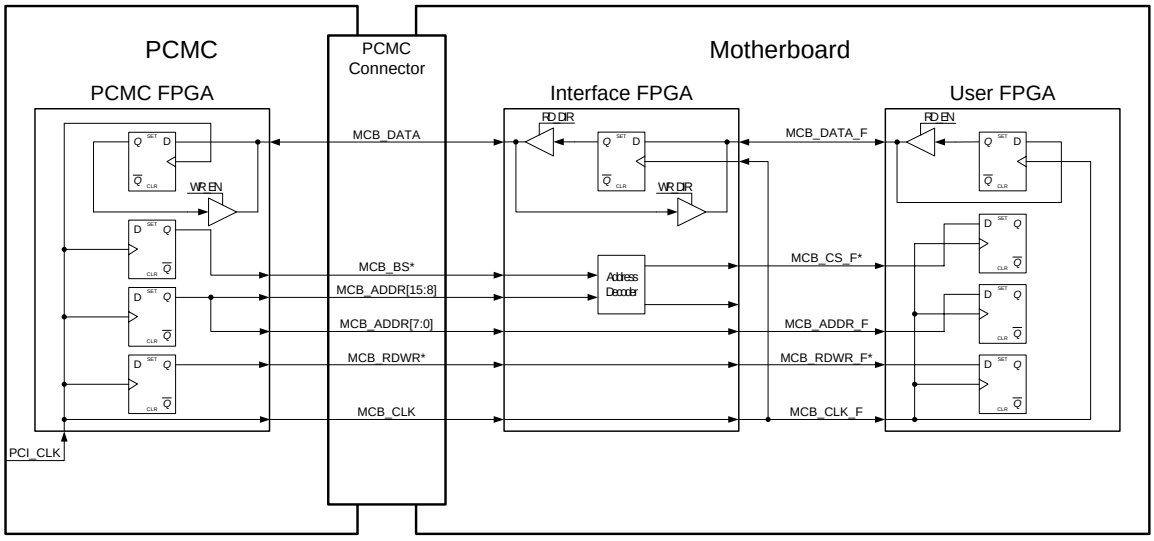

Figure 4- 1 Simplified connection diagram of the MCB interface. There is an interface FPGA between PCMC and the user FPGA. It serves as a fanout chip that generates multiple copies of the MCB on the motherboard.

The PCMC FPGA initializes the bus transactions by asserting MCB_BS*. When it is a write transaction, all MCB signals will pass through the interface FPGA and arrive at the user FPGA. The user FPGA will clock in MCB_DATA_F with MCB_CLK_F. When it is a read transaction, the user FPGA will drive data on the bus. It puts data on MCB_DATA_F, and the data will be re-clocked into the interface FPGA with MCB_CLK_F. The PCMC FPGA will clock in MCB_DATA with PCI_CLK. There is an address decoder in the interface FPGA. It is used to generate MCB_CS_F*s signals from MCB_BS* and MCB_ADDR[15:8].

The reason for adding 1 clock cycle delay on the read transaction is that there is not enough setup time for the PCMC FPGA to clock in the read data in 30ns (1 clock cycle), due to propagation delays of MCB_CLK and clock-to-output delays on the user FPGA.

5 Electrical Specification

The following sub-section defines the electrical specification on MCB interface.

5.1 Functional Specification

This section defines all functional transactions on MCB interface. The functional transactions on MCB interface include single write transaction, single read transaction, burst write transaction and burst read transaction. Each Functional transaction will be discussed here in detail.

5.1.1 Single Write Functional Transaction

Figure 5-1 illustrates a single write transaction.

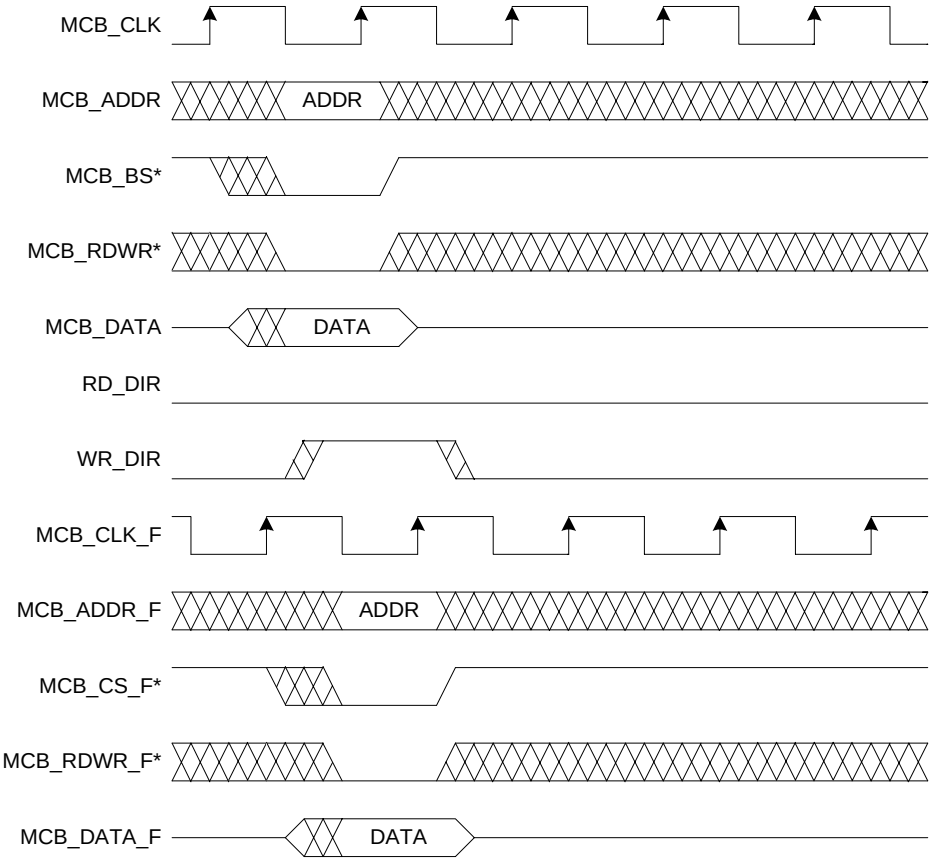

Figure 5- 1 MCB single write transaction. The transaction starts when MCB_BS* is asserted and MCB_RDWR* is low. The PCMC FPGA also provides MCB_ADDR and MCB_DATA on the bus.

In Figure 5-1, the PCMC FPGA drives MCB_ADDR, MCB_BS*, MCB_RDWR* and MCB_DATA signals on the bus. MCB_CLK_F, MCB_ADDR_F, MCB_RDWR_F* and MCB_DATA_F signals are the delayed versions of their original signals that pass

through the interface FPGA. MCB_CS_F* is generated from MCB_BS* and MCB_ADDR[15:8] in the interface FPGA.

RD_DIR and WR_DIR signals are the read/write direction control signals in the interface FPGA. They are generated from MCB_BS* and MCB_RDWR* signals.

5.1.2 Burst Write Functional Transaction

Figure 5-2 illustrates a burst write transaction.

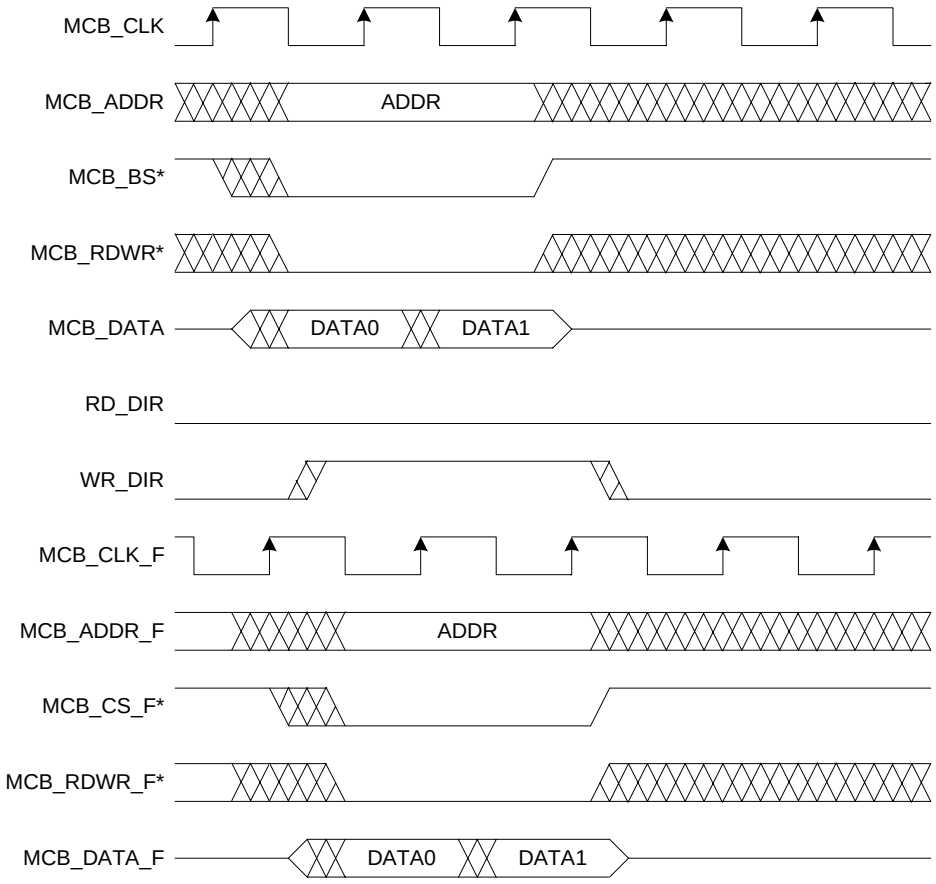

Figure 5- 2 MCB burst write transaction. The transaction starts when MCB_BS* is asserted and MCB_RDWR* is low. This diagram shows a burst of 2 write transaction on the bus.

Like the single write transaction, the burst write transaction starts when MCB_BS* is asserted and MCB_RDWR* is low. During burst write, MCB_DATA changes on every rising edge of MCB_CLK while MCB_ADDR stays the same.

In the user FPGA, implementation of the burst write function requires an internal write pointer that should increment when MCB_CS_F* and MCB_RDWR_F* are both low. Since the microprocessor may stop a burst write transaction and re-start it again later, this write pointer has to remain at its value when a burst write transaction stops and increments again when the burst write transaction re-starts. A clear bit through a MCB write is required to reset this pointer to 0.

5.1.3 Single Read Functional Transaction

Figure 5-3 illustrates a single read transaction.

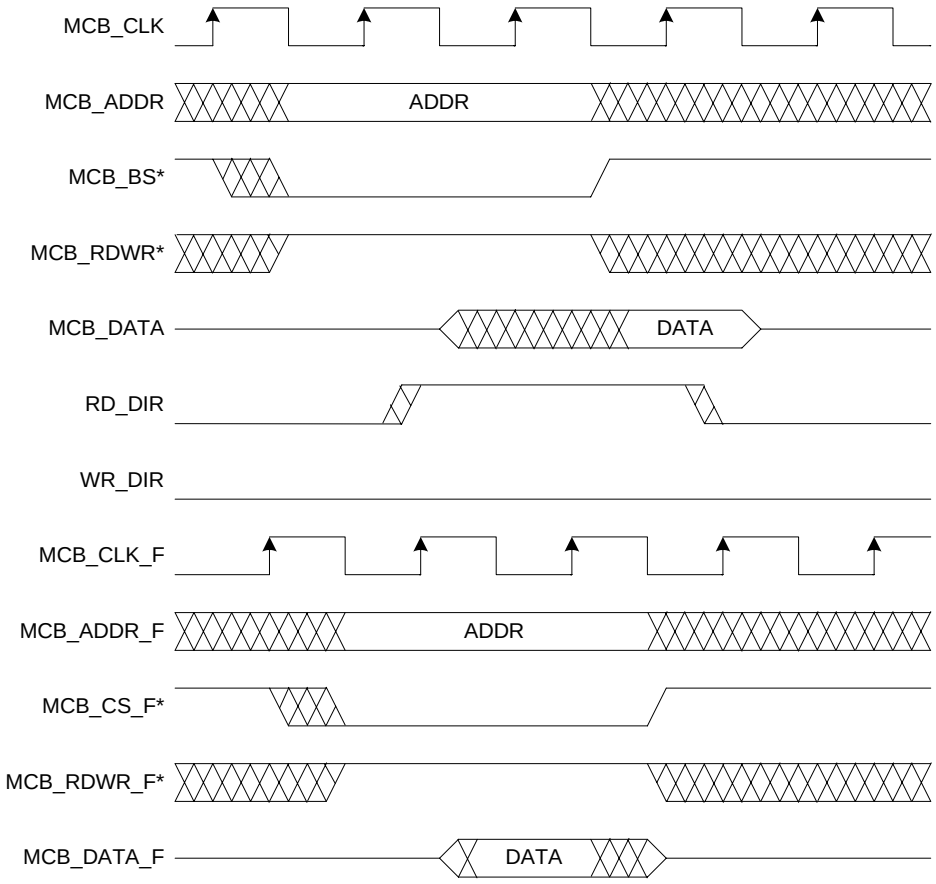

Figure 5- 3 MCB single read transaction. The transaction starts when MCB_BS* is asserted and MCB_RDWR* is high. The user FPGA provides the read data on the bus when it sees MCB_CS_F* is low and MCB_RDWR_F* is high.

In Figure 5-3, the PCMC FPGA initials a single read transaction by driving MCB_BS* low and MCB_RDWR* high. It also provides a read address on MCB_ADDR. When the user FPGA sees MCB_CS_F* is low and MCB_RDWR_F* is high, it will put read data on MCB_DATA_F. This data is re-clocked in the interface FPGA and the PCMC FPGA takes the data on the next clock.

5.1.4 Burst Read Functional Transaction

Figure 5-4 illustrates a burst read transaction.

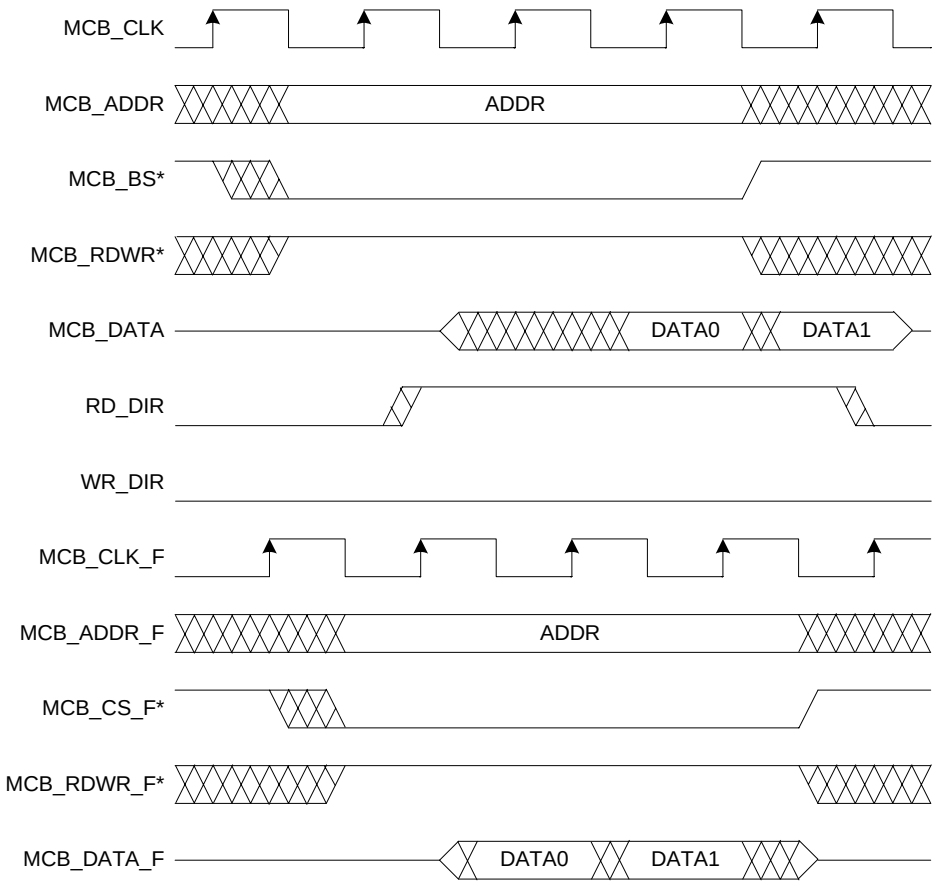

Figure 5- 4 MCB burst read transaction. The transaction starts when MCB_BS* is asserted and MCB_RDWR* is high. This diagram shows a burst of 2 read transaction on the bus.

Like the single read transaction, the burst read transaction starts when MCB_BS* is asserted and MCB_RDWR* is high. When the user FPGA sees MCB_CS_F* is low and MCB_RDWR_F* is high, it will put read data on MCB_DATA_F. During burst read, MCB_DATA_F changes on every rising edge of MCB_CLK_F.

In the user FPGA, implementation of burst read function requires an internal read pointer that should increment when MCB_CS_F* is low and MCB_RDWR_F* is high. Since the microprocessor may stop a burst read transaction and re-start it again later, this read pointer has to remain at its value when a burst read transaction stops and increments again when the burst read transaction re-starts. A clear bit through a MCB write is required to reset this pointer to 0.

Figure 5-4 is a functional diagram of a burst read of 2. In this diagram, there are 3 valid increments for the internal read pointer. But only 2 data have been read out for this transaction. The read pointer has to decrease by 1 at the end of this transaction to maintain the correct read address for the internal memory. A simple way to solve this problem will be discussed here.

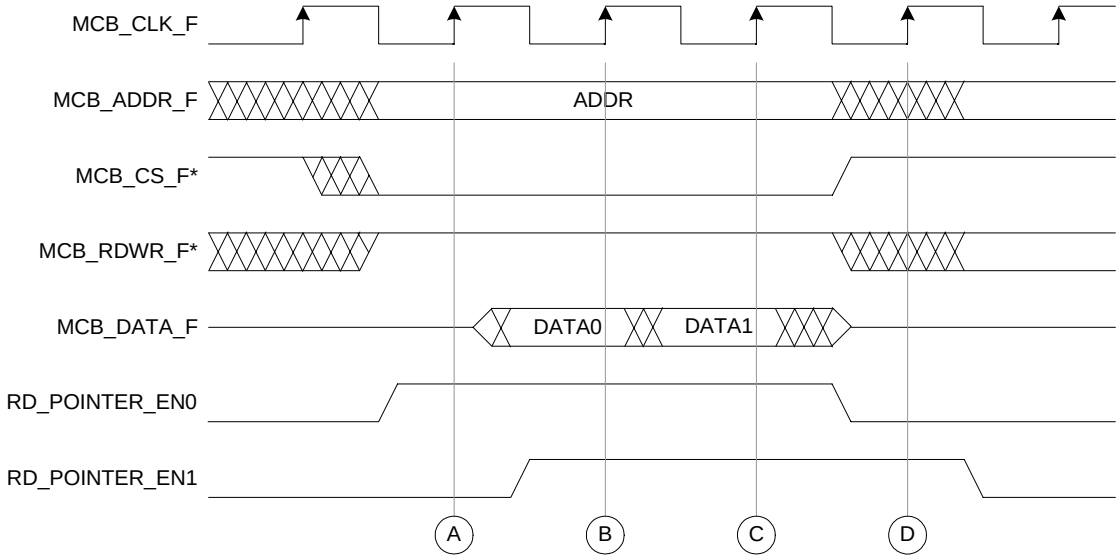

Figure 5- 5 Functional diagram to implement a read pointer for burst read transaction in the user FPGA.

In Figure 5-5, RD_POINTER_EN0 is asserted when MCB_CS_F* is low and MCB_RDWR_F* is high. RD_POINTER_EN1 is delay version of RD_POINTER_EN0 (1 clock delay). The read pointer increments at A, B and C when RD_POINTER_EN0 is high. It decrements at D when RD_POINTER_EN0 is low and RD_POINTER_EN1 is high. In this way, the actual increments of the read pointer will be 2 (increments by 3 and decrements by 1) and indicate 2 data have been read out from the memory.

5.2 Timing Specification

This section defines all timing requirements for MCB interface. The timing requirements include setup and hold time, clock-to-output time and pin-to-pin delay for each chip.

A timing diagram of MCB interface is shown in Figure 5-6.

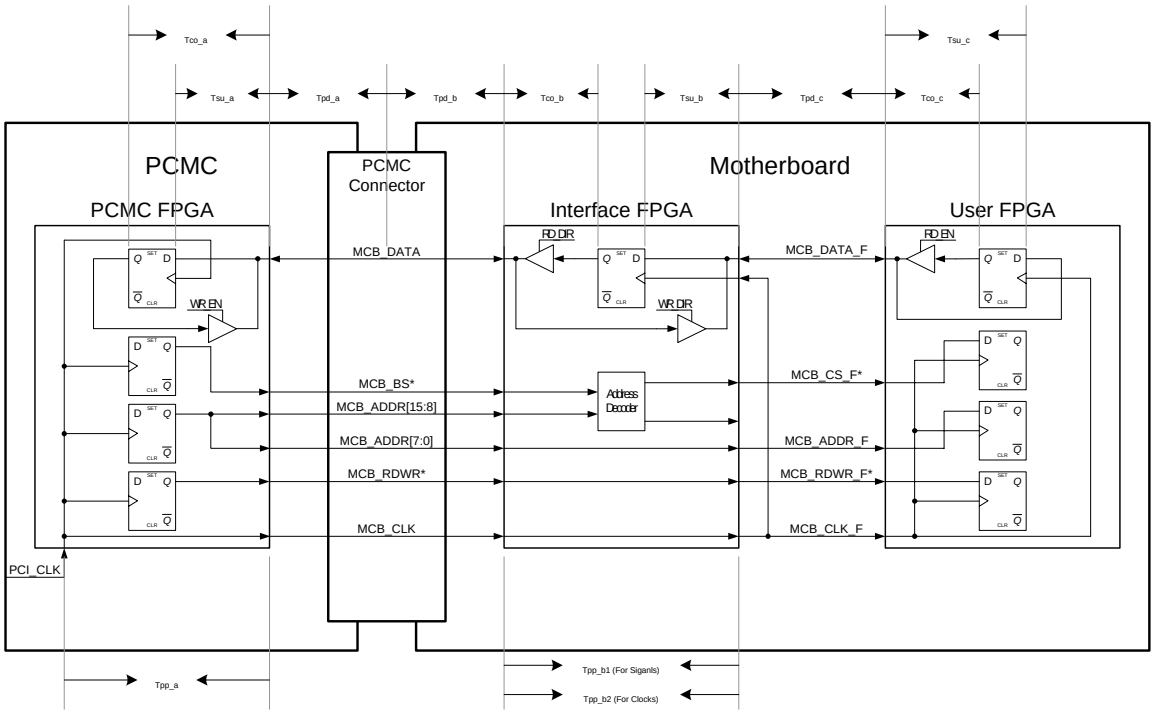

Figure 5- 6 Timing diagram of MCB interface. All setup time and clock-to-output time are referenced to their own clock at the input of the pin.

Table 5-1 provides the timing parameters for MCB interface. Refer to Figure 5-6 for the symbol names in Table 5-1.

Symbol	Parameter	Min	Max	Unit	Note
Tsu_a	Input setup time to PCI_CLK	2		ns	PCMC FPGA
Tco_a	PCI_CLK to signal output delay	9	12	ns	PCMC FPGA
Tpp_a	PCI_CLK to MCB_CLK pin to pin delay	3	5	ns	PCMC FPGA
Tpd_a	Propagation delay between PCMC FPGA and PCMC connector		0.25	ns	1.5” trace length on PCB
Tpd_b	Propagation delay between PCMC connector and interface FPGA		1.75	ns	10” trace length on PCB

Symbol	Parameter	Min	Max	Unit	Note
Tsu_b	Input setup time to MCB_CLK_F (local clock)		6	ns	Interface FPGA
Tco_b	MCB_CLK_F (local clock) to signal output delay	6	8	ns	Interface FPGA
Tpp_b1	Pin to pin delay for signals	8	12	ns	Interface FPGA
Tpp_b2	MCB_CLK to MCB_CLK_F pin-to-pin delay	6	8	ns	Interface FPGA
Tpd_c	Propagation delay between interface FPFA and user FPGA		3.5	ns	20” trace length on PCB
Tsu_c	Input setup time to MCB_CLK_F (local clock)		12	ns	User FPGA
Tco_c	MCB_CLK_F (local clock) to signal output delay		14	ns	User FPGA

Table 5- 1 Timing parameters for MCB interface.

Table 5-2 calculates the timing budget between the PCMC FPGA and the interface FPGA. Refer to Figure 5-6 for the symbol names in Table 5-2.

Tpp_a	Tpd_a	Tpd_b	Tpp_b2	Tco_b	Tpb_b	Tpb_a	Tsu_a	Sum	Margin
5ns	0.25ns	1.75ns	8ns	8ns	1.75ns	0.25ns	2ns	27ns	3ns

Table 5- 2 Timing budget between the PCMC FPGA and the interface FPGA.

Table 5-3 calculates the timing budget between the interface FPGA and the user FPGA. Refer to Figure 5-6 for the symbol names in Table 5-3.

Tpd_c	Tco_c	Tpd_c	Tsu_b	Sum	Margin
3.5ns	14ns	3.5ns	6ns	27ns	3ns

Table 5- 3 Timing budget between the interface FPGA and the user FPGA.

To analyze the setup time for the user FPGA, we have to know the maximum delay time on the signal path (Td_sig) and the minimum delay time on the clock path (Td_clk).

Table 5-4 calculates the maximum delay time on the signal path. Refer to Figure 5-6 for the symbol names in Table 5-4.

Tco_a	Tpd_a	Tpd_b	Tpp_b1	Tpd_c	Td_sig
12ns	0.25ns	1.75ns	12ns	3.5ns	29.5ns

Table 5- 4 Maximum delay time on the signal path.

Table 5-5 calculates the minimum delay time on the clock path. Refer to Figure 5-6 for the symbol names in Table 5-5.

Tpp_a	Tpd_a	Tpd_b	Tpp_b2	Tpd_c	Td_clk
3ns	0.25ns	1.75ns	6ns	3.5ns	14.5ns

Table 5- 5 Minimum delay time on the clock path.

Figure 5-7 shows the setup time for the user FPGA on MCB interface.

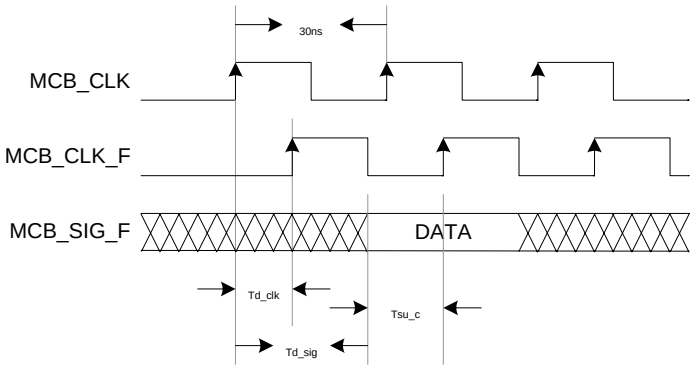

Figure 5- 7 Diagram for the setup time calculation on the user FPGA.

In Figure 5-7, the setup time for the user FPGA will be:

Tsu_c = 30ns + Td_clk – Td_sig = 30ns + 14.5ns – 29.5ns = 15ns

According to this calculation, the setup time for the user FPGA cannot be greater than 15ns (specification is set to 12ns).

5.2.1 Timing requirements for the PCMC FPGA

Table 5-6 defines the timing requirements for the PCMC FPGA.

Symbol	Parameter	Min	Max	Unit	Note
Tsu	Input setup time to PCI_CLK	2		ns	PCMC FPGA
Tco	PCI_CLK to signal output delay	9	12	ns	PCMC FPGA
Tpp	PCI_CLK to MCB_CLK pin to pin delay	3	5	ns	PCMC FPGA

Table 5- 6 PCMC FPGA timing requirements.

5.2.2 Timing requirements for PCB trace on the PCMC board

Table 5-7 defines the timing requirements for PCB trace on the PCMC board

Symbol	Parameter	Min	Max	Unit	Note
Tpd	Propagation delay between PCMC FPGA and PCMC connector		0.25	ns	1.5” trace length on PCB

Table 5- 7 Timing requirements for PCB trace on the PCMC board.

5.2.3 Timing requirements for the interface FPGA

Table 5-8 defines the timing requirements for the interface FPGA.

Symbol	Parameter	Min	Max	Unit	Note
Tsu	Input setup time to MCB_CLK_F (local clock)		6	ns	Interface FPGA
Tco	MCB_CLK_F (local clock) to signal output delay	6	8	ns	Interface FPGA
Tpp_sig	Pin to pin delay for signals	8	12	ns	Interface FPGA
Tpp_clk	MCB_CLK to MCB_CLK_F pin-to-pin delay	6	8	ns	Interface FPGA

Table 5- 8 Interface FPGA timing requirements.

5.2.4 Timing requirements for the user FPGA

Table 5-9 defines the timing requirements for the user FPGA.

Symbol	Parameter	Min	Max	Unit	Note
Tsu	Input setup time to MCB_CLK_F (local clock)		12	ns	User FPGA
Tco	MCB_CLK_F (local clock) to signal output delay		14	ns	User FPGA

Table 5- 9 User FPGA timing requirements.

5.2.5 Timing requirements for PCB trace on the motherboard

Table 5-10 defines the timing requirements for PCB trace on the motherboard.

Symbol	Parameter	Min	Max	Unit	Note
Tpd_1	Propagation delay between PCMC connector and interface FPGA		1.75	ns	10” trace length on PCB
Tpd_2	Propagation delay between interface FPFA and user FPGA		3.5	ns	20” trace length on PCB

Table 5- 10 Timing requirements for PCB trace on the motherboard.

6 References

[1] Carlson, Brent, Refined EVLA WIDAR Correlator Architecture, NRC-EVLA Memo#014, October 2, 2001.

[2] Heng, Zhang, PC/104 Monitor/Control Mezzanine Card RFS Document A25145N0000 Rev 1.1, May22, 2003.

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