TEST AND VERIFICATION PLAN

EVLA Correlator Manufacturing Test Plan

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1 Revision History

Revision	Date	Changes/Notes	Author
DRAFT	August 31, 2005	Initial DRAFT release	B. Carlson

2 Introduction

This document describes the baseline plan for post-manufacturing testing of printed circuit board (PCB) assemblies for the EVLA correlator. There are several hundred assemblies that will be fabricated and many of them are of sufficient complexity and cost that an effective method of testing is required to ensure high yield of delivered modules. It is the intent of testing to accept from the manufacturer only those modules that are in "working" order. It is thus necessary first to develop a plan to ensure that this goal is achieved in a cost-effective way, and then use this plan for any required implementation of hardware and software to achieve it.

This plan defines only those testing steps and procedures that are required *at the manufacturing site* and does not address additional steps and procedures required before completed assemblies are shipped to the final site(s) for installation.

There are several elements to this plan, and not all of them will be covered in detail in this document. The elements are as follows:

1. Pre-assembly bare board testing. We will leave this testing up to the manufacturer's discretion to ensure that the PCB meets all of the requirements defined in [1]. This testing is not within the scope of this document.

2. Pre-assembly component testing. For all components except for the custom correlator chip ASIC on the Baseline Board, it is assumed that sufficient testing has been done by the manufacturer before delivery. Since the assembly contract is full turn-key, we will leave it up to the manufacturer to process incoming components in a standard way to ensure that the correct components are mounted in the correct locations. We have no requirement for pre-testing of components.

3. Pre-assembly testing of the custom correlator chip ASIC. This is the subject of a completely separate test plan and testing procedure. Suffice to say that only fully tested correlator chips will be delivered to the manufacturer for mounting and soldering on boards.

4. Post-assembly X-ray inspection and other testing not under normal power. This is purely left to the manufacturer to define what testing is to be done to achieve acceptable yield and to meet the quality requirements defined in [1]. This testing is not within the scope of this document.

5. JTAG testing under power. All boards for which JTAG testing is feasible will undergo JTAG testing to test connectivity of chips on boards. This includes the Station Board, Baseline Board, Phasing Board, PCMC, Delay Module and Timecode Board. The Fanout Board and Feedthru Backplane do not have JTAG test capability. The "stage 1" prototypes [1], that is, the very first prototypes built, will not require JTAG testing (**is this true???**).

6. Complete assembly functional testing under power. All boards except the Feedthru Backplane will be functionally tested in a test bed at the manufacturer's site and must pass go/no-go tests before being accepted for delivery. The bulk of this document describes the details of this testing.

It goes without saying that during every phase of manufacturing and test, all surfaces, personnel, carrying, and storage devices must used proper ESD protection since devices on all assemblies use leading-edge technology and are ESD sensitive.

3 JTAG Testing

Where feasible and possible, the board assemblies for the EVLA correlator are designed with manufacturing test in mind, and the first line of testing is JTAG testing. The JTAG test chain on the board includes all components that have JTAG test ports—normally this means FPGAs and in some cases some memories. The custom correlator chip ASIC also has JTAG test ports and is included in the test chain for the Baseline Board it is mounted on.

The Station Board, Baseline Board, Phasing Board, and Timecode Board contain JTAG test ports and will require post-fabrication JTAG testing. The Feedthru Backplane and the Fanout Board do not have JTAG test ports and thus do not require testing.

Two mezzanine cards—the Delay Module and the PCMC—contain JTAG test pins as part of their functional interfaces but do not contain a separate JTAG test port that a tester could be plugged into. If these two mezzanine cards are to be tested separately from their motherboards, a separate test board for each one, complete with power supply, will be required. While this can be done it is likely that the easiest course of action is to install these mezzanine cards onto their motherboards, and then test the complete assembly with one JTAG chain.

To summarize, the following complete assemblies will require individual JTAG test sequences and tests.

- Station Board + PCMC mezzanine installed + 2 x Delay Module mezzanine installed.
- Baseline Board + PCMC mezzanine installed.
- Phasing Board + PCMC mezzanine installed.
- Timecode Board[1] + PCMC mezzanine installed.

To further complicate the situation, it is likely that the Delay Module for the stage 3 and stage 4 production modules (and thus the entire JTAG test sequence) will be different than the Delay Module for the stage 1 and stage 2 prototype modules. This module is going to be re-designed with a different FPGA for cost reasons, however, we wish to build prototypes with the existing design for schedule reasons. It is likely that a round of prototyping will be required for the new design of the Delay Module. In any case, the mezzanine card interface to the Station Board motherboard will not change, but the test sequence will.

[1] This module assembly may or may not be built under this contract. As there are only two of these in any system, the prototypes that already exist may suffice for our purposes, unless a design defect is found that requires a re-spin.

Note that it is part of the contract with the board assembly manufacturer (CM) to develop the JTAG test sequence for each board. We will provide all the information required for this, but we have not ourselves purchased the software or the tester for this purpose.

The connector on the front of each module is a Molex 87333-1420 2 mm 14-pin right-angle connector. A pinout diagram of this connector looking into the front edge of the PCB is shown in Figure 1.

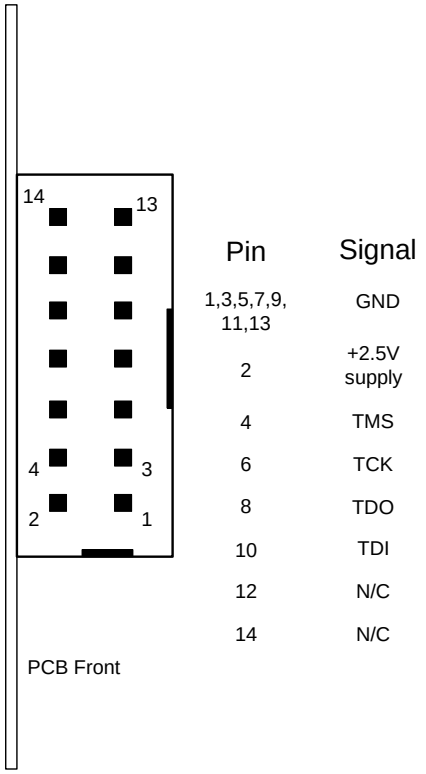

Figure 1 JTAG interface connector looking into the front of the PCB.

The boards must be supplied with –48 VDC power for JTAG testing. Power can most conveniently be provided by plugging the board into a test bed that contains mating Feedthru Backplanes with only their power connectors installed. This way, the insertion and extraction force of the board is minimal, and the bare assembly with installed mezzanine cards can be tested without installing heatsinks or front-panel hardware.

We will provide test bed(s) and –48 VDC power supplies with the proper power connectors for JTAG testing for the manufacturer. Presumably, only one slot of each type (e.g. 12U x 400 mm, 6U x 160 mm etc.) is required, and a single test bed could contain all required slots. No fan cooling for this test bed is anticipated since the tests are short and not at full speed.

4 Functional Testing

This section describes requirements and scenarios for full functional testing of completed assemblies at the manufacturer's site.

There are 4 assemblies that will require full functional testing:

- Station Board (c/w PCMC, PC/104+, Delay Modules, heatsink, front panel).
- Baseline Board (c/w PCMC, PC/104+, heatsink, front panel).
- Phasing Board (c/w PCMC, PC/104+, heatsink—if required, front panel).
- Fanout Board (c/w heatsink, front panel).

The PC/104+ board is a COTS embedded processor module that plugs into the PCMC card, which itself plugs into the motherboard (Station Board etc.). This module contains an Ethernet interface, boots from a host Linux computer, and itself contains a real-time Linux operating system. This embedded processor module is used to configure and test devices on the motherboard. The PCMC card contains an FPGA and an A/D converter and converts the PCI bus interface from the PC/104+ module to a simple synchronous interface on the motherboard for use by motherboard devices.

Each assembly contains its own power supply (-48 VDC to low voltage DC converter) and power switch so that it is possible to individually power-up and test each assembly, without affecting the other assemblies in the test bed. For any one assembly to be completely and properly tested requires that all of the other assemblies are powered up and configured and generating data. There is no additional specialized test hardware to test each assembly independently. Thus, when a particular set of assemblies of one type is to be tested, it is important that all of the other assemblies in the test bed are known to be good.

Real-time software Module Access Handlers (MAHs) (i.e. device drivers) will boot and be ready for use on the PC/104+ module. The boards themselves contain reasonably powerful hardware BIST (Built-In Self-Test) functions, driven by the MAHs. Additionally, powerful GUIs are being written that allow easy access to low-level on-board chip functions for configuration, debugging, and testing.

The intent is to develop an additional simplified GUI that, under the user's command, is able to run a go-no-go test to indicate if the selected assembly is functioning properly. From power up until an assembly go-no-go test is complete will likely take about 2-5 minutes. The go-no-go test will give a pass or fail, and if there is a failure will list, either graphically or textually, the devices that are detecting failures. It is possible that intelligent software could interpret these failures and nail down more carefully what is the likely cause of failure, but it is not possible to nail it down to one chip or one trace; a failure could be in the transmitter, the medium of transmission (the PCB/trace

connection), or in the receiver. Nevertheless, the graphical or textual indication will provide as much information as possible to narrow the location where defects are.

It is our intent to provide one or two technologists and/or engineers to assist with functional testing at the manufacturer's site. We will also build and provide the test bed, host computer, switch, and power supply for this purpose. The CM simply has to provide personnel to assist with plugging in boards, running tests, and fixing manufacturing defect problems. Completed assemblies are only accepted for delivery once the go-no-go test passes.

Figure 2 is a simplified diagram of a test bed for functional test. There are 6 boards in the test bed—1 Timecode Board, 1 Station Board, 2 Fanout Boards, and 2 Baseline Boards. Additionally, there is a –48 VDC power supply , with 3-phase Δ208 VAC in, an Ethernet switch, and a host computer. The host computer and Ethernet switch run off single-phase 110 VAC, and everything else runs off the –48 VDC supply.

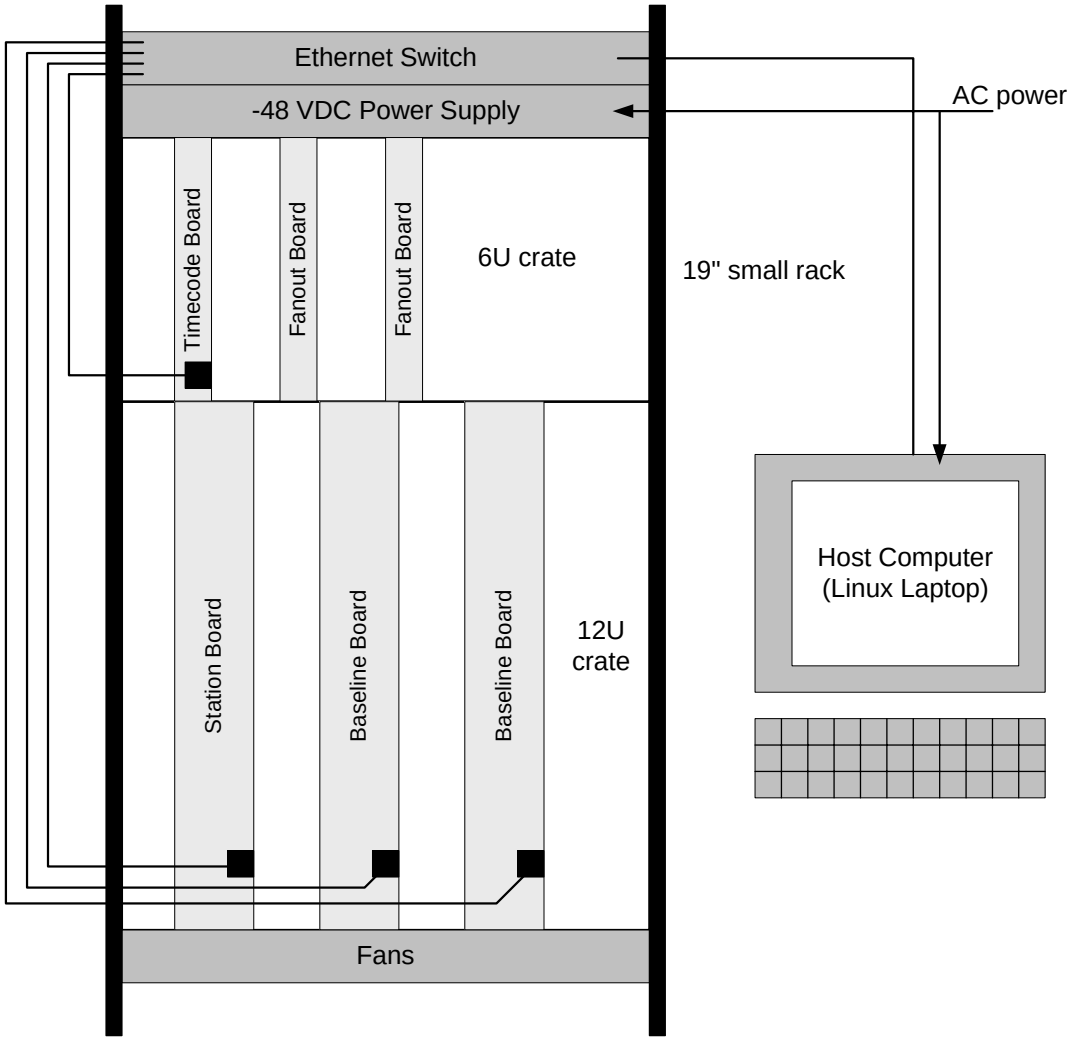

Figure 2 Functional test bed.

There are two crates—a 6U height crate and a 12U height crate, and the crates, fans, power supply, and Ethernet switch are mounted in a short 19" rack. Total rack height, including clearance for fans is about 4.5 feet (33 U). The rack is self-standing with roller wheels and will likely be mounted on the floor. The position of the –48 VDC power supply and the switch may be at the bottom to allow personnel easy access to plugging and unplugging boards. Boards are inserted and extracted with ejector handles (not shown) that are easily operated. The heaviest assembly, the Baseline Board, weighs about 12-15 lbs, mostly because of its monolithic heatsink. For these heavy modules, a handle on the front panel allows them to carried like a suitcase once removed from the system. Not shown in the figure is a number of cables connecting all boards via the Feedthru Backplanes at the back of the crates. These cables will be installed and secured as part of the test bed.

If yield is low, it may be desirable to run the test without the heatsink installed so that it does not have to be removed for board rework. Running the assembly, under power with fan cooling for a short period of time for the test is acceptable.

The total estimate power requirement for the 3 phase input for the –48 VDC supply is 2 kW. The 3-phase power connector for the –48 VDC supply is TBD. For the laptop host computer and Ethernet switch, the single-phase 110 VAC power requirement is about 700 W, with a standard AC plug/outlet. In this configuration, 1 Station Board can be tested at a time, however 2 Fanout Boards, and 2 Baseline Boards can be tested at once.

All tests will be run by starting a GUI on the host computer, pressing the appropriate button (i.e. "run test" for a selected board), and then waiting for the results. Once a test is complete, the particular UUT can be powered off with its front-panel power switch, removed, and a new UUT can be installed without power cycling the other boards in the test system. The new UUT is powered-up, boots, and the test sequence repeats.

5 References

[1] PWGSC Request for Proposal, Solicitation No. 31035-059127/A, “Printed Circuit Board Modules”, 2005-05-06.