

TEST AND VERIFICATION PLAN

EVLA Correlator Project Development and Test Plan

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List of Abbreviations and Acronyms

ASIC – Application Specific Integrated Circuit. This is a chip that is hardwired for a specific function. Sometimes this is referred to as a “custom chip”, or a standard-cell device. ASICs normally incur large NRE costs and require significant testing to maximize the probability that the chip will work the first time.

CDR – Critical Design Review. Formal review after which production prototypes, and then full production occurs.

CPCC – Correlator Power Control Computer. This is the host computer that is responsible for power monitor and control of the correlator system. The programs running on this computer are simple and designed to be very reliable.

DUMPTRIG – Internal signal that controls complex integration and binning functions in the correlator.

e-MERLIN – Expanded MERLIN radio telescope array, with central operations at JBO..

EVLA – Expanded Very Large Array near Socorro NM. This is the radio telescope array that the correlator is primarily being developed for.

FORM – Fiber Optic Receiver Module. This is the mezzanine card, developed by NRAO, that plugs into the Station Board and converts fiber signals to electrical signals for use by the Station Board. Also known as the **DTS receiver module**.

FPGA —Field Programmable Gate Array. A chip containing in-system programmable logic.

HVAC – Heating, Ventilation, and Air Conditioning.

JBO – Jodrell Bank Observatory near Manchester, England. This is the operations center for e-MERLIN.

JTAG testing – A method of tested the connectivity of chips on a circuit board, without knowledge of the board’s or the chips’ functionality. JTAG is an acronym for “Joint Test Action Group”.

MCCC – Master Correlator Control Computer. This is the host computer that communicates with the hundreds of embedded processors in the system, and is the primary interface to the EVLA Monitor and Control System.

NRAO – National Radio Astronomy Observatory, mainly referring to the group in Socorro NM that will take delivery of the correlator.

NRC – National Research Council of Canada. The NRC institute in Penticton is developing the correlator.

PCB – Printed Circuit Board.

PDR – Preliminary Design Review. Formal review after which the bulk of hardware prototypes are fabricated.

RTL (code) – Register Transfer Language. This is code that describes hardware functions. Also known as HDL (Hardware Description Language). The correlator development uses the Verilog HDL language.

VLA – Very Large Array near Socorro NM. This refers to the existing array and associated equipment.

Definitions

Crate – An enclosure—also known as a **sub-rack**—which is a carrier box into which PCBs can be installed by sliding them into guide rails, and mating with connectors at the back. The crate is rack-mountable, and normally is not a stand-alone piece of equipment

Rack – An enclosure into which crates are installed. Normally, the rack is floor mounted and is enclosed by side panels and front and back panels. A rack can be a stand-alone piece of equipment, or can be part of a larger overall system.

1 Revision History

Revision	Date	Changes/Notes	Author
DRAFT	Oct. 1, 2004	Initial DRAFT release for external review	B. Carlson

2 Introduction

The purpose of this document is to define an overall plan for testing and verification of the correlator system during each phase of development. Definition of a plan for testing and verification necessarily requires a plan for development. This development plan is contained within the project schedule [1], but will be reiterated and refined somewhat in this document. An early precursor to this document can be found in [2] and defines an overall development plan for the correlator.

This document is a top-level document that outlines, in the most concrete terms possible, a framework around which internal (NRC) and external (NRAO) test planning can be built. Test and verification procedural requirements are defined for FPGAs, custom chips, modules, sub-racks, racks, software and the system at various stages of development.

This is a working document that will evolve with time as more detailed information becomes available during each stage of development. This is a top-level document and necessarily relies on the development of detailed test plans for each of the many components of the system.

3 Overview

This section presents a brief overview of the plan for implementation and testing of the correlator system.

1. **Phase I: Design and development.** FPGAs are developed and tested with simulation, PCBs are developed and tested with simulation, the correlator chip ASIC is developed and tested, some key hardware is built and tested to demonstrate feasibility and help refine the design as necessary. A PDR (Preliminary Design Review) is held at the end of this phase before committing to first prototypes. According to the current schedule, the PDR will be held in Q2 2005.
2. **Phase II: In-house prototype testing.** The first prototypes are fabricated and tested in Penticton. Once successful, additional prototypes are fabricated, tested, and readied into prototype correlators for on-the-sky testing. According to the current schedule, this phase should be complete in early 2006.
3. **Phase III: On-the-sky prototype testing.** A limited number of boards are set up in a prototype configuration for testing at the VLA site and at JBO. Each prototype correlator will have 4-station capability, able to process 1 baseband pair, at the full baseband bandwidth (1 polarization), with 1024 spectral channels per baseline. Increased spectral resolution can be obtained at the expense of lower bandwidth with recirculation. The purpose of this testing is to qualify the hardware on the sky before proceeding with production. A CDR (Critical Design Review) is held at the end of this phase, and according to the current schedule will occur in mid 2006.
4. **Phase IV: Limited production and testing.** A full rack of Station and Baseline Boards are produced, configured, and tested in racks in what should be their final configuration. The primary purpose of this test is to find hardware bugs that may have gone undetected in the lower-volume prototypes before committing to full production. This system will facilitate more intensive system integration and testing with a more complete suite of software. According to the current schedule, this testing will be complete by the end of 2006 and this will free much of this hardware for installation at the VLA site for further integration and testing throughout most of 2007.
5. **Phase V: Full production and testing.** All hardware for the system is produced and tested in Penticton before being shipped to the VLA site for final installation and testing. According to the current schedule, full production and testing will occur in the first half of 2007.
6. **Phase VI: Installation and commissioning.** This phase has several steps associated with it including rack and cable installation starting in mid 2006, limited production board installation starting at the end of 2006, full production

board installation and testing beginning in the latter half of 2007, and final commissioning and handover of the system to NRAO in the latter half of 2008.

A simplified Gantt chart showing the above phases over the next several years is shown in Figure 3-1 below.

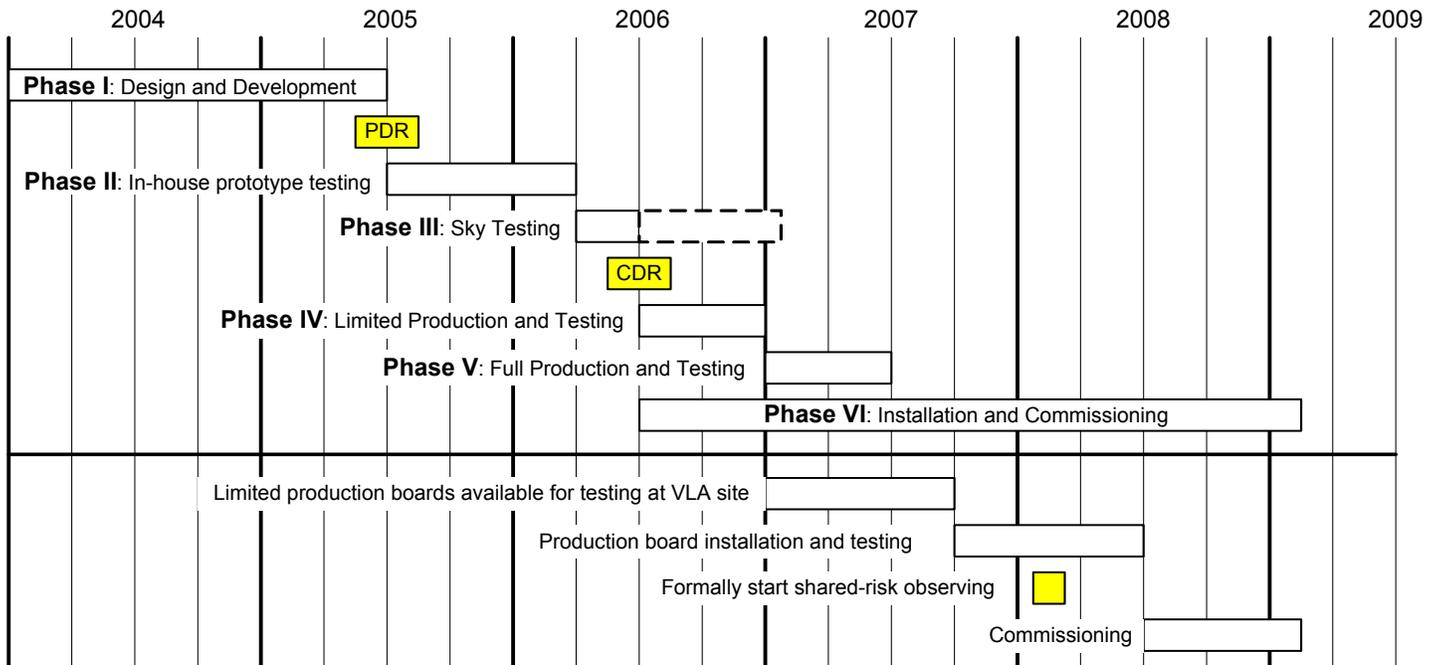


Figure 3-1 Simplified Gantt chart showing the phases of development, fabrication, and testing in the project. This schedule is developed from the current project schedule. Note that software development does not end with Phase I, but continues for most of the rest of the project.

It must be noted that this schedule is based on the current detailed project schedule and is largely hardware driven. That is, the schedule follows expected hardware development and fabrication, and software will “just have to be ready” when the hardware needs it. It is possible that this is exactly the opposite of what will actually be the case—the ability to test correlator functions and proceed to the next phase of development may be entirely driven by the availability of software. As the project proceeds, there will be less and less hardware development and debugging, and more and more focus on software development and debugging. Thus, engineers that are mostly focused on hardware development in the early phases of the project, will transition and focus on software development later on. It is believed that this, along with ample testing time, will help to mitigate the impact of increasing software complexity, increasingly complex interaction between software modules and associated bugs, and the time to find and fix them. Nevertheless, to our knowledge, a system of this size and complexity has never before been developed in radio astronomy, and it will take significant time before it is operational.

A detailed description of the activities associated with each of the phases of development is presented in the following sections.

4 Development Phase Description

This section describes each of the phases of development, fabrication, and testing in more detail.

4.1 Phase I: Design and Development

In this phase, the following activities, and associated testing will occur:

- **FPGA development and testing.** RTL code is written and functional simulation tests are performed on an incremental basis. Testing, through simulation, is performed on the RTL code and the place-and-routed design. Any functional bugs found after this are due to inadequate testing at this stage, or are due to PCB-level problems.
- **ASIC development and testing.** This primarily applies to the correlator chip, and perhaps the FIR filter. Since the design will reside in custom or semi-custom silicon, a highly rigorous level of testing must be performed at every stage of development to ensure that bugs are found and fixed before the next stage of major expenditure proceeds. The development of an ASIC is a complete sub-project that will have its own milestones, testing, and formal review requirements. There will be a separate CDR for each ASIC, before sign-off to the external contractor.
- **PCB development and testing.** PCB designs incorporate many different FPGAs, memories, and ASICs. It is the job of the PCB designer to ensure that the chips are connected to each other so that timing and signal integrity are within acceptable margin. Verification of timing and signal integrity is performed through simulation. Thermal analysis and testing is also important to ensure that the board will run within established thermal bounds. A test and verification plan and report must be generated for every PCB.
- **Preliminary prototype construction and testing.** This is construction and testing of real or mock physical models to study, verify, and ensure that the final design will meet requirements. This testing is required when it is not possible to absolutely guarantee that a particular design or choice of technology will work based on a manufacturer's specification or computer modeling. Full end-to-end testing of the Gbit/sec technology employed in the correlator, and construction of one or more rack thermal mock ups will undergo this kind of testing.
- **Software development and testing.** A top-down, bottom-up approach to design and implementation of the software for the correlator will likely be taken. As hardware designs are finalized, and descriptions of functions of chips and boards become clear and documented, development of device drivers and software design for embedded control proceed. At the same time, high-level descriptions of the functionality of host (MCCC) monitor and control software are developed,

with an underlying view of the functionality of the system. The focus for this phase of software development is to ensure that the required set of software is in place to facilitate prototype testing, once prototypes become ready. Higher level, more sophisticated software development continues after this phase for most of the rest of the project.

- **Reliability analysis.** A detailed reliability study of the correlator system components will be performed to find areas where reliability could be a concern. The aim of this analysis is to provide information that can be used to mitigate areas of concern, as well as eventually provide information required for system maintenance (spares etc). Commercially available software (Relex) capable of performing this analysis according to various standards (MIL HDBK 217F(2), Telcordia, PRISM) will be purchased and the study will be performed by NRC personnel.

Once this phase of development and testing is complete, the project is subject to a formal Preliminary Design Review (PDR). According to the current schedule, the PDR will be held at the end of Q2, 2005.

4.2 Phase II: In-house prototype testing

This phase is when full prototype modules, encompassing the results of all previous design and development activities, will be tested. Development and testing at this stage involves the following activities:

- **Construction and testing of 1st prototypes.** One module of each of the large boards (Station Board, Baseline Board) will be constructed, tested, and debugged, before construction of additional prototypes of the modules commences. This is to minimize cost and schedule risk if a design bug is detected that requires a full re-spin of the circuit board. At all times, circuit boards are fabricated and assembled at capable production facilities and thus are of a very high quality. The first prototypes may use sockets for some devices such as for the ASICs, to reduce risk and facilitate testing. One Fiber Optic Receiver Module (FORM) is required for this first prototype. A system PPS and 128 MHz signal generator are also required for this testing. Thermal cycling will be employed to help find areas where design margins are not sufficient.

Software must be in place to facilitate hardware testing—this means that device drivers and some way of accessing/executing device drivers must be available, and the backend must be capable of accepting frames and displaying them in text and graphical format. Software must be in place to allow the Station Board Delay Modules to be loaded with test vectors, and to set up and run delay tracking to be applied correctly to the data (i.e. repeating delay tracking with no cumulative delay error). Software must be able to set simple modes for DUMPTRIG to permit standard dump testing, phase binning, and recirculation.

- **Construction and testing of prototype correlators.** A number of modules will be constructed to meet the needs of on-the-sky prototype testing for all partners involved in this development. These will only be constructed once 1st prototype testing is complete, and it is mostly guaranteed that there are no “hard” design bugs in the PCBs¹. All of these modules will have to be integrated and tested in self-contained crates before they are shipped to telescope sites for further testing. Each crate is a prototype correlator. All crates will undergo thermal cycling and appropriate vibration testing to help to find marginal design bugs. It is likely that JTAG and functional testing is employed to ensure that there are no manufacturing defects.

The total prototype quantities that will be built, and who they are built for are defined in Table 4-1. For amplitude and phase closure tests, a minimum of 4 antennas are required for sky prototype testing.

¹ Hard bugs are those that require a PCB re-work or re-spin to fix. There can be “soft” hardware bugs that can be fixed by modifying FPGA firmware (a.k.a. FPGA “personalities”).

The table shows that only two Phasing Boards will be built. Because of the inherent uncertainty in the development schedule, and the complete focus on development of the Station Board and Baseline Board, it is unclear exactly when the Phasing Board prototype will be available. The current schedule indicates that the Phasing Board prototype will not be available until the end of 2006—likely well after on-the-sky prototype testing is complete.

Module	Qty for NRAO	Qty for JBO	Qty for Penticton	Totals
Station Board	4	4	4 (incl. 1 st prototype)	12
Baseline Board	1	1	1 (c/w corr chip BGA sockets)	3
Fanout Board (SDFB)	0	0	5	5
Common Backplane	16	16	16	48
TGB ²	2	2	2	6
PCMC	7	7	7	21
PC104+ (purchase)	7	7	7	21
FORM ³	4	4	4	12
1 m cable	16	16	16	48
10 m cable			10	10
12 U crate ⁴	1	1	1	3
Phasing Board	1		1	2
Host computer (MCCC/PCCC)	1	1	1	3
100 Mbps Ethernet Switch	1	1	1	3
Backend computer c/w Gbit Fiber in	1	1	1	3
48 VDC power supply	1	1	1	3

Table 4-1 Prototype quantity requirements. This does not include some small additional numbers of spares of boards and components that will be acquired.

² It is likely that the TGBs will be mounted in a 12 U crate.

³ Fiber Optic Receiver Module provided by NRAO.

⁴ This assumes that a full rack is not required for each crate. Some minor mechanical modifications will be required to table-mount a crate.

4.3 Phase III: On-the-sky prototype testing

This phase begins when prototype correlators and associated software are sufficiently debugged and tested to connect to real antennas. The purpose of this test is to finally verify that fringes can be detected on the sky, that there are no “hard” hardware bugs in the design, and that there are no long-term systematic biases in the data. According to the current schedule, **this testing will start in Q2 2006 and take a few months to complete.** Once testing is complete, hardware will remain at the sites where prototype testing occurred to allow for continued integration and testing.

This phase will require a set of software that will allow reasonably easy configuration, control, monitor of the correlator, and processing of correlator data. Most likely this means that close to the full set of embedded software is working and that it is possible to configure and monitor the correlator in a quasi-automatic way independent of the higher-level EVLA monitor and control system. The following software elements are essential for this phase of testing:

- Delay model generation and tracking.
- Phase model generation.
- Correlator monitor and control via a host GUI that allows configurations to be manually set, and status information to be displayed.
- Real-time control of DUMPTRIG for normal dumping, phase binning, and recirculation.
- Back-end that can produce files that can be read by AIPS and fringe analysis software. The current plan is that the backend will be able to produce UVFITS files, according to the current UVFITS format standard. Although this standard is restrictive and will not allow output from the correlator in its full suite of configurations, it should be adequate for this level of testing.
- Software for analysis of UVFITS files. NRC has a graphical analysis tool called “ccvis” and a fringe search analysis tool called “cgff” that can be used for this purpose. NRAO has a similar set of fringe analysis tools.

Due to the limited availability of Baseline Boards and prototype correlator chips, it will only be possible to concurrently process a portion of the full bandwidth that is available to the Station Board. The following figure shows how the Station Board outputs could be connected to the Baseline Board inputs in the prototype correlator.

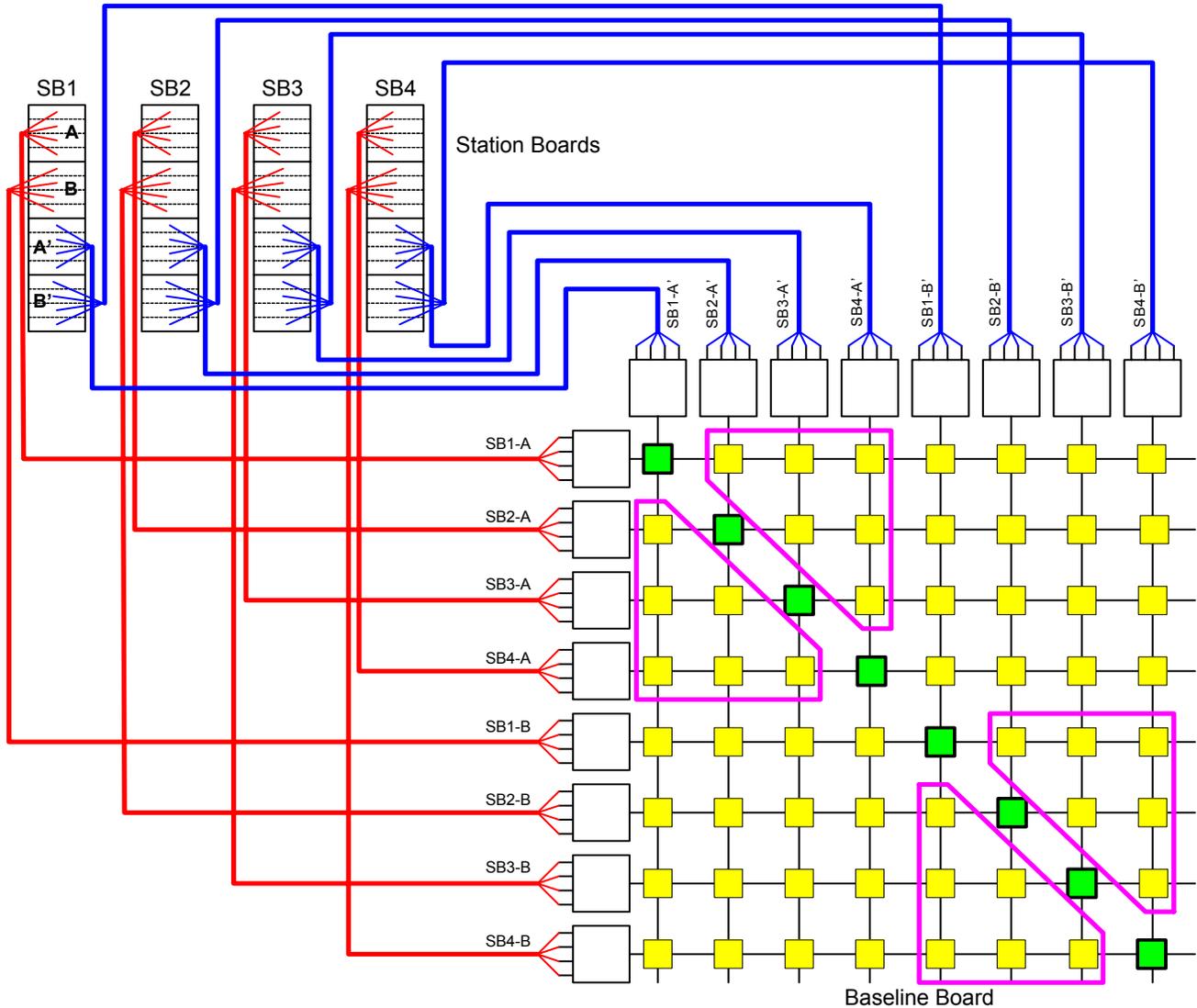


Figure 4-1 Prototype correlator connection diagram. Four sub-band pairs from each Station Board are connected to one Baseline Board input. Two sets of four sub-bands (e.g. SB1-A and SB1-B) can be correlated against duplicated outputs (e.g. SB1-A' and SB1-B'). This arrangement allows all of the bandwidth to be correlated with 1 polarization product, and ½ of the total bandwidth (8 sub-band pairs) to be correlated with 2 or 4 products. 2048 lags per baseline are available—more with recirculation. Other correlator chips can be tested with a suitable arrangement of sub-band allocations to the A, B, and A', B' outputs.

In Figure 4-1, it is possible to correlate all of the bandwidth⁵ with one polarization product, and ½ the total bandwidth with all polarization products at maximum sub-band bandwidth with 2048 lags. With “static” recirculation on, it is possible to acquire 4096

⁵ By making use of the Station Board “Input Chip” cross-bar switch.

lags by obtaining the “lead” lags in the lower triangle and the “lag” lags in the upper triangle. However, only 4 streams can be correlated like this because of the limited width of recirculation memory, and thus only $\frac{1}{2}$ of the above bandwidth can be correlated. Refer to [3] and [4] for background information on the many ways the Baseline Board and correlator chip can be configured.

The nomenclature in the diagram is as follows: **SB_n-A** is 4 sub-band pairs (or 8 sub-bands, 1 polarization) for station “n”, fed into the “Y” inputs of the Baseline Board. **SB_n-A'** is the identical 4-sub-band pairs, duplicated by the output cross-bar switch on the Station Board, only they are fed into the “X” inputs of the Baseline Board. The **B** and **B'** outputs are the second set of 4-sub-band pair outputs. Thus, a total of 8 sub-band pairs can be processed, yielding $\frac{1}{2}$ the total bandwidth available to each Station Board. Double this bandwidth—16 sub-bands—is available with one polarization.

It is clear that software will have to be sufficiently agile to be able to handle this hardware configuration to the best possible advantage for testing. Since it is necessary to test the results from all correlator chips on the Baseline Board, it will likely be necessary to establish software configurations that are not the same as any planned implementation. For example, it makes no sense to correlate SB1-A with SB4-B', and so to test the correlator chip at that intersection, it is necessary to ensure that all sub-bands that are to be correlated are consistent in frequency and bandwidth. One way of allowing these seemingly redundant or unnecessary configurations to be tested is to allow for automatic or manual software configurations of the hardware.

4.3.1 Prototype correlator science testing

A key input to the test plan for on-the-sky testing is from project scientists. Experience indicates that likely the best way to test the prototypes to ensure that all functions are exercised is to correlate a variety of science experiments. The goal is to put the correlator in as many different configurations as possible, and analyze the output data for correctness.

It may be effective to solicit proposals from a subset of scientists with a number of different science goals to best exercise the prototype correlator. The following factors should be considered when generating and selecting proposals:

- Only 4 stations will be available. This is enough to obtain amplitude and phase closure. If it is highly desirable, 8 stations may be processed by using the 4 Station Boards allocated for Penticton, but these boards would likely have to be returned to Penticton once sky testing is complete (i.e. they would likely not be left at the VLA site indefinitely). If 8 stations are processed, only 4 sub-band pairs from each station can be accommodated.
- A variety of continuum and spectral-line observations must be processed.
- One or more deep integrations must be performed.

- Configurations that use recirculation and pulsar phase binning must be performed.
- Radar mode, pulsar gating, tone extraction must be tested.
- Real-time FIR filter interference mitigation (blanking) must be tested.
- It should be possible to independently verify that the output data products do not exhibit any unusual behaviour. This can be accomplished by comparison with the existing correlator, expected results from a known radio source, expected results from a different instrument, or a combination thereof.

Nevertheless, a detailed test plan will be developed for this phase of testing, since this is the last opportunity to find hard bugs before going into limited and full production.

At the end of on-the-sky prototype testing—and what exactly constitutes the end of this testing remains to be define—a Critical Design Review (CDR) will be held. The CDR is the last milestone before limited and full production, and the current schedule indicates it will be held in Q3, 2006. These prototypes will remain at the telescope sites for further testing.

4.4 Phase IV: Limited production and testing

Once the CDR is complete and there are no major design issues that need to be resolved, we will proceed with limited production and associated testing—also sometimes referred to as production prototype testing. The limited production run is one last step in an attempt to find hard bugs that may have slipped through prototype testing due to the limited number of boards that have been built for the prototypes. Additionally, it is used to test most of the final rack wiring configurations that will be used in the full correlator installation, and to verify correct and adequate thermal performance. Boards will undergo a combination of JTAG and functional testing to find manufacturing defects before being accepted from the manufacturer. This will likely require a special test bed and test software for speed and ease-of-use.

The plan is to build one full rack of Station Boards and one full rack of Baseline Boards so that these racks can be operated in their final (or close to final) configurations—the rest of the system is a replication of these racks and their contents. As much as possible, the racks will be wired like the final racks, but some modification will be necessary to ensure that all hardware is stimulated as much as possible.

The Baseline Rack will be wired for 32-station (or 40-station), all baselines, and as one sub-band correlator. Since there are only 4 station “quads” in one Station Rack, multiple sub-band outputs from the quad will be used to provide the full stimulus needed for the Baseline Rack. That is, outputs from the Station Rack that would normally go to different sub-band correlators will be used to function as different “stations” into the test Baseline Rack. In this case there are actually 64 outputs that can stimulate up to 64 inputs in the Baseline Rack (even though there will be only 32 or 40 inputs to the Baseline Rack). The purpose here is not to wire the correlator for maximum scientific use, but rather to wire the correlator for maximum test coverage. This test setup will never be used at the VLA site—it is only intended for use in Penticton.

Figure 4-2 is a simplified diagram showing some wiring connections for the limited production test racks. Each of the inputs (40 are shown) to the Baseline Rack is a “station input”, but is wired to different sub-band pair outputs of the limited Station Rack.

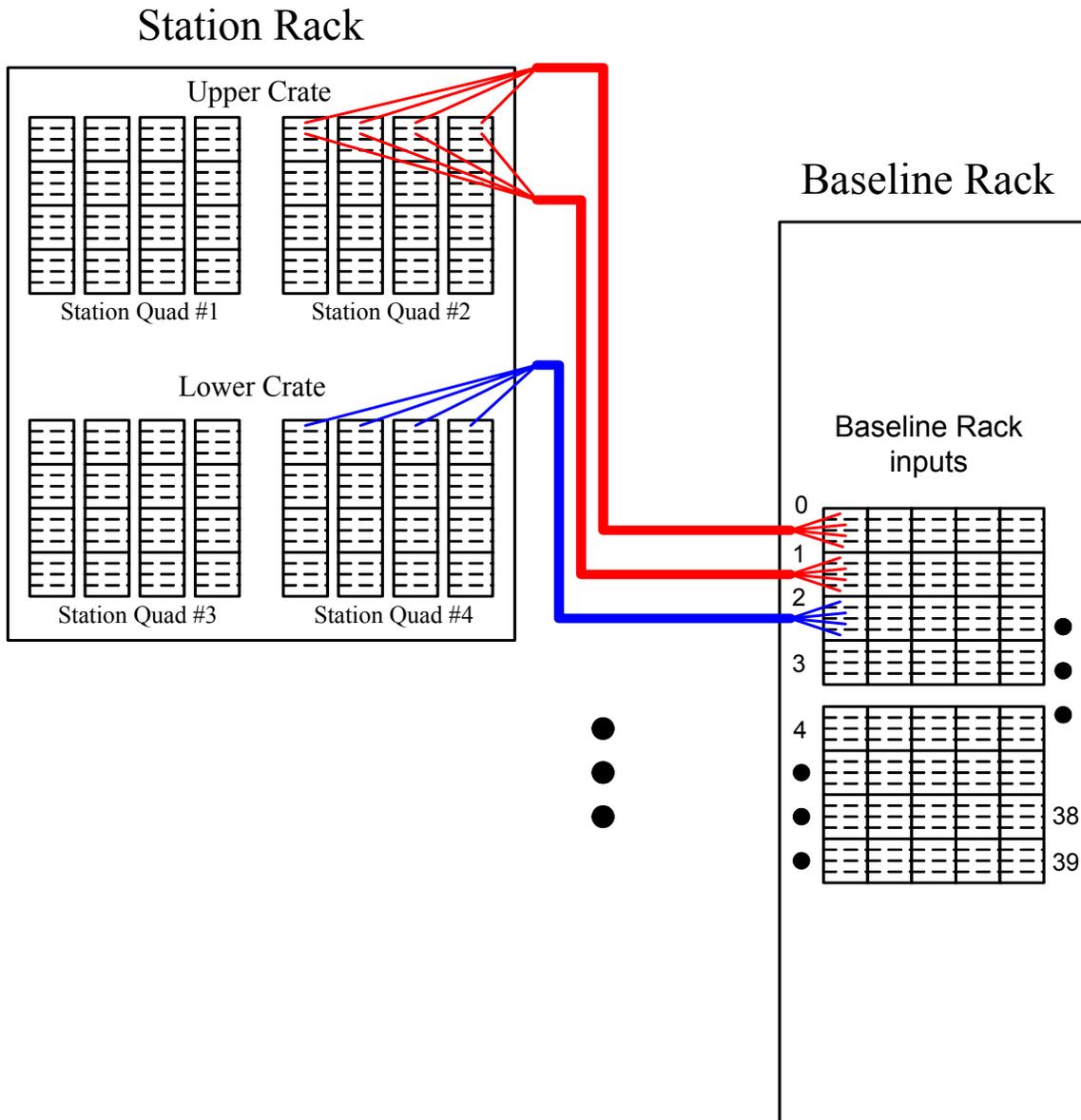


Figure 4-2 Limited production run Station Rack to Baseline Rack wiring configuration. Only a few wiring connections are shown. Internally, the Baseline Rack is wired as one sub-band correlator for 32 or 40 stations, including fan out boards. All inputs to the Baseline Rack can be stimulated by connecting the available outputs of the four station quads to Baseline Rack inputs.

This limited production correlator will undergo thermal testing to try to find and eliminate hard and soft bugs. Most if not all testing will use Station Board-generated test vectors for stimulation of all hardware.

According to the current schedule, limited production testing will be complete by the end of 2006. Once testing in Penticton is complete, the modules can be delivered to the VLA site and JBO for further integration and testing. The configuration of these modules at

the VLA site can be to maximize the number of antennas (up to 20 antennas, including the initial prototype modules already there) or to maximize bandwidth coverage. Further thoughts on configuration for this preliminary correlator testing are included in section 4.6.2.

A list of modules required for limited production testing is shown in Table 4-2 below.

Module	Qty
Station Board	16
Baseline Board ⁶	10 or 15
Phasing Board	1
Common Backplane	132 or 160
TGB	2
Fanout Board (SDFB)	32 or 40
PCMC	27 or 32
PC/104+	27 or 32
1 m cable	160 or 240
10 m cable ⁷	32 or 40
24" rack	2
12 U crate	4
6 U crate ⁸	2
100 Mbps Ethernet switch	2
1 Gbps Ethernet switch	1
Back-end computer c/w Gbit Ethernet in	2
Host computer (MCCC/CPCC)	1
48 VDC power supply	1 (20 kW capacity)
Water chiller ⁹	1

Table 4-2 Limited production run quantity requirements

Software should be much more advanced at this point and it will be a critical element in successful testing of these boards in this configuration. Due to the larger number boards, configurations, and data products the software must be more automated in configuration and data handling, but still with sufficient flexibility to allow the hardware engineers to put the correlator in configurations to facilitate full testing.

⁶ i.e. for a 32-station or 40-station installation.

⁷ It is likely a good idea to use a variety of the long, equalized cable lengths here so that all possibilities are tested.

⁸ One of the 6 U crates is needed for the TGBs, one is required for the fanout boards.

⁹ Only if a rack with closed-cycle air cooling, and liquid cooling is used.

4.5 Phase V: Full production and testing

In this phase the main thrust is to produce and test production quantity boards in preparation for final installation at the VLA and JBO sites. It is believed not to be feasible to try to construct the entire correlator in Penticton, because of the size of the system and the sheer volume of cable required. Nevertheless, a “slice” of the correlator – probably a complete rack of each type—will be constructed in Penticton and used for continued system integration and testing before boards are shipped to the VLA site. All boards undergo JTAG and functional testing before being accepted from the manufacturer. All boards will be burned-in¹⁰, tested, and qualified before being shipped to their final destination.

According to the current schedule, the full production run is expected to be complete by the end of Q2 2007, with system integration and testing continuing in Penticton for a few more months.

¹⁰ And/or temperature cycled—further detailed investigation is required to determine the most effective testing methods to find infant mortality failures.

4.6 Phase VI: Installation and commissioning

This is the final phase of the project. At the end of this phase, the correlator system will be completely handed over to NRAO, with NRC continuing to play a consultative role on an as needed basis. Also included is the handover of all documentation, computer files, and drawings that will be needed by NRAO for long-term maintenance and support of the system.

There are several steps to this phase, as described in the following sub-sections.

4.6.1 *Rack and cable installation*

There will be 24, and perhaps as many as 26 racks (40 station correlator) installed in the correlator room at the VLA site. A preliminary rack layout plan is shown in Figure 4-3 below. In this figure, there are enough racks for 40 stations, including 16 Phasing Boards. In a 32-station configuration, the same layout should be used except that two of the Station Racks would not be populated. The nominal rack footprint is 2.7 ft wide x 3 ft deep, and there is 2.5 ft of front/back clearance for each rack.

The baseline plan is to install the racks and cables at the VLA site in advance of the arrival of limited production and full production boards. According to the current schedule, limited production boards could be installed at the VLA site at the beginning of 2007. Thus, rack and cable installation should start well in advance of this time—likely beginning in mid or early 2006.

It is not yet known what the final rack configuration will be, what the final power requirements for each rack will be, and what the cooling method will be. However, as indicated in section 4.1 it is likely that one of two methods will be used for correlator cooling:

1. All air cooling. In this case, the room HVAC system will have to supply enough cold air for all of the racks. For a 32-station correlator, the HVAC system could have to have enough cooling capacity for about 200 kW (estimated¹¹, based on 400 W per Station Board, and 600 W per Baseline Board, and 50 kW extra capacity for everything else). For a 40-station correlator this could increase to about 270 kW. It is currently estimated that the ambient temperature of the air fed into the racks not exceed 15 °C.
2. Closed-cycle air/liquid cooling. In this case, the room HVAC system will only have to supply enough cold air for the auxiliary racks (MCCC etc, fiber, backend, power plant), and the correlator racks will be supplied with intake and exit water

¹¹ Note: these are preliminary numbers and depend heavily on the final power dissipation of the correlator chips and the FIR filter chips.

lines. The room HVAC system need only have ~50 kW cooling capacity. The water supply line temperature and volume flow requirements are TBD.

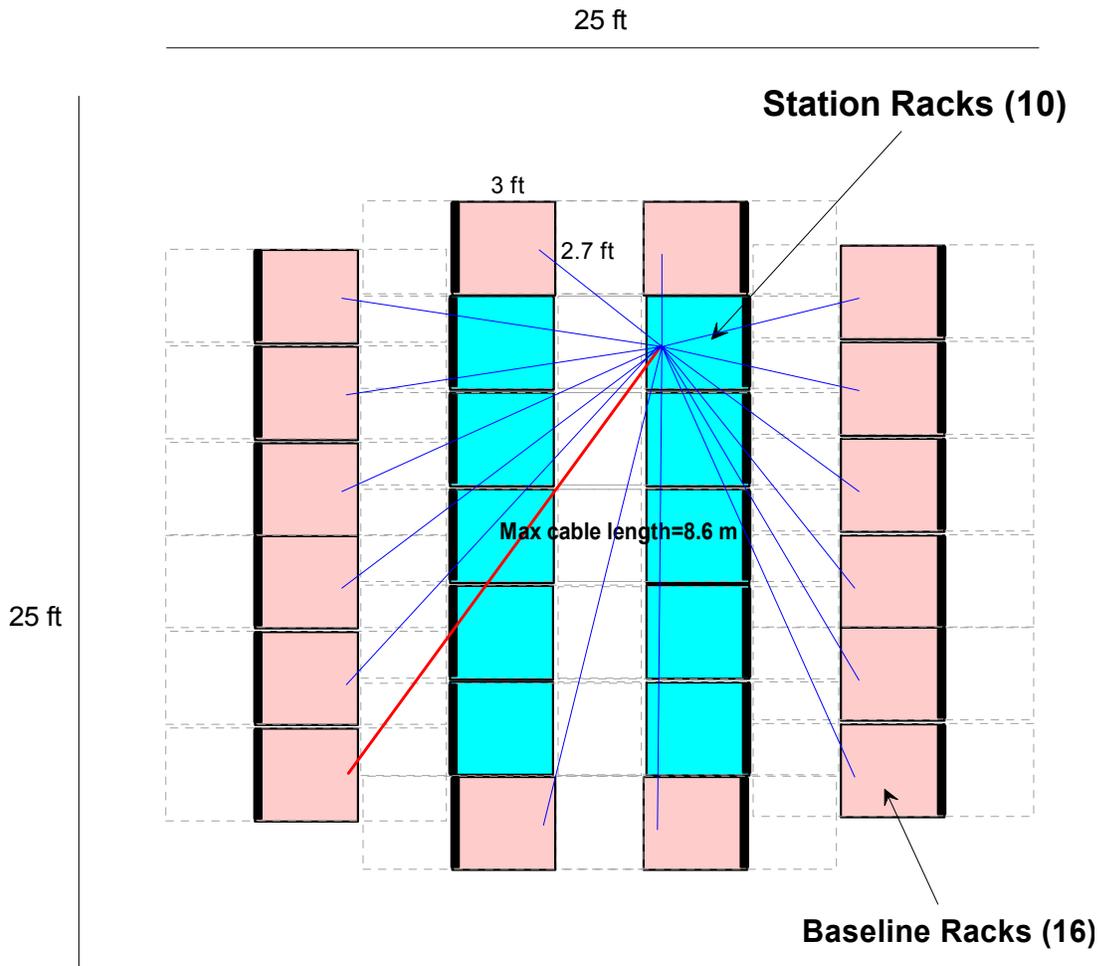


Figure 4-3 Preliminary footprint of the correlator's Station and Baseline Racks showing wiring connections from one Station Rack—note that from every Station Rack, there are 4 cables routed to each Baseline Rack. Not included in this diagram is a rack required for the MCCC, CPCC, and the Timecode Generator crate, as well as racks for fiber optic equipment, the 48 VDC power plant or the backend computers.

Rack and cable installation entails the following basic components and installation steps:

- Install bare racks on pedestals mounted to the concrete floor of the correlator room.
- Install the 48 VDC power plant and additional AC UPS. Consultation and assistance from the power plants' manufacturers is likely necessary.
- If closed-cycle liquid cooling is used, install room supply and return cooling lines, and connect to rack heat exchangers. Test all connections and operation.

- Install all “below-the-floor” rack-to-rack signaling cables, and 48 VDC and AC power supply cables.
- Install the raised tile computer floor grid.
- Install crates and any necessary fans in the racks. If closed-cycle liquid cooling is used, it is likely that the racks come equipped with fans.
- Install common backplanes in the crates, and connect 48 VDC power. Test all 48 VDC power connections for correct polarity.
- Connect signal cabling to all common backplanes. Check and verify cable connectivity. Install computer floor tiles.
- Install all additional computers, switches, fiber equipment, associated wiring, room protection systems etc. Check power and connectivity of all equipment.

At this point, the correlator rack and cable installation is complete and ready to accept the first correlator circuit boards from the limited production run.

4.6.2 Limited production run installation and test

As indicated in section 4.4 there will be 16 Station Boards, 16 Baseline Boards, and associated support boards and computers available for initial testing in advance of full production modules. According to the current schedule these boards, the result of a limited production run, could be available at the beginning of 2007. For simplicity, and to minimize complex wiring changes, it is likely that the installation of these boards will be within the wiring framework of the full correlator. (It is important to note that during this sort of testing, any fan out board (SDFB) outputs that are not in use must be terminated otherwise the output from other bit-stream channels can be adversely affected. It is feasible that this can be done with simple dummy plug-in terminators, however the cost of these terminators is currently unknown.)

The installation scenario that seems to offer the best tradeoff between science capability and testing is one in which each of 8 station “quads” are populated with 2 Station Boards, and each of the 16 sub-band correlator racks (i.e. Baseline Racks) is populated with one Baseline Board.

In this configuration, a total bandwidth of 8 GHz (2 GHz on 2 baseband pairs) is available with full correlation ability on 8 stations. There are 32,768 lags¹² available per baseline and this could be doubled to 65,536 lags per baseline if the “static” recirculation configuration is employed similar to that indicated in Figure 4-1.

¹² Recirculation can be used at narrower bandwidths for more channels. I.e. the baseline plan is to provide recirculation capability with the prototype and this installation.

According to the current schedule, this configuration will be in place until nearly the end of 2007. With this complement of boards it should be possible to perform significant system integration and testing at the VLA site and by the time full production boards show up many of the hardware and software bugs in the system should be resolved.

Testing during this time should focus on system integration with the EVLA monitor and control system, and on integration with the correlator backend and image processing system. The ability of the correlator is likely to be dominated by software ability, and it is likely that there will be a transition from manual, to semi-automated, to automated observations as integration testing and debugging proceeds.

It will be important during this time to schedule a variety of science experiments with the aim of using the experiments to help to shake down the system. As with the prototype correlator, this could come from observing proposals that are rated based on the ability to test the system, and on science ability. Contrary to the current schedule, some “shared-risk” observing is likely to occur during this time, although there is no guarantee that data will be available and that it will be of the desired quality.

4.6.3 Production board installation and testing

Starting near the end of 2007, more production-qualified boards will arrive at the VLA site, ready for installation and testing. It is envisioned that an incremental install and test strategy will be used, in an effort to shakedown the system one step at a time to maximize debugging effectiveness. While there are many ways this can be done, one possible scenario is as follows (assuming the required number of EVLA antennas are available):

- Install 16 production Station Boards, beside the existing complement of 16 Station Boards. Thus, a full 8-station correlator is available at full bandwidth. This step will be used to ensure that all fiber connections, configurations, and EVLA monitor and control are possible with 8 stations.
- Install 32 more production Station Boards and 32 production Baseline Boards to bring the correlator up to a full complement of 16 stations, full bandwidth, all baselines. If testing in all previous steps was thorough and successful, it should be easy to test and verify this configuration. A series of science observations will be needed to help find and shake out problems. Nevertheless, there are more embedded CPUs to control, more data going to the backend etc. and so it could take some time to find and fixed bugs. Formally, according to the current schedule, this is the start of “shared-risk” observing.
- Install and test all remaining Station Boards and Baseline Boards. This should essentially be a formality if all previous testing is rigorously performed and it likely will mostly reveal installation and configuration bugs.

4.6.4 Commissioning

Formally, this phase begins once the new correlator system is completely operational and tested to the point where sufficient confidence in its operation has been obtained and it is trusted with processing all observations. The old correlator is turned off at the beginning of commissioning. According to the current schedule, commissioning begins in mid 2008 and NRC personnel provide direct support on an as-needed basis for the next 8 months or so, at which time commissioning is officially complete. During this time, it will be important that key NRAO personnel become familiar with correlator system components so that they are able to completely take over long-term system management and maintenance.

5 References

- [1] EVLA Correlator project schedule:
(http://www.drao.nrc.ca/science/widar/private/Management/EVLA_Project_asof_21Jul2004.pdf)
- [2] Carlson, Brent, EVLA Correlator Development Plan, prepared for the Nov. 2, 2001 CoDR, October 11, 2001.
(http://www.drao.nrc.ca/science/widar/private/Management/CorrelatorDevPlan_Oct11-01.pdf)
- [3] Carlson, Brent, Two Correlators for the Price of One: How a VLBA Correlator Could Fit Within the Proposed 40-Station WIDAR EVLA Correlator, NRC-EVLA Memo# 006, September 28, 2000.
- [4] Carlson, Brent, EVLA Correlator Chip RFS document A25082N0000, Rev. 2.1, September 27, 2004.