INTERFACE CONTROL DOCUMENT

External Timecode (ext-TC) and

128 MHz Clock Interface Specification

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B. Carlson, October 30, 2007

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1 Revision History

Revision	Date	Changes/Notes	Author
Draft	Jan. 20, 2005	Initial release for review.	Zhang Heng
1.0	Feb. 22, 2005	Add a simplified diagram of TIMECODE interface. Add CRC-4 circuitry.	Zhang Heng
2.0	Oct. 30, 2007	Changes to reflect new method of Timecode delivery; this document specifies ONLY the external Timecode delivered to the correlator from external EVLA systems.	B. Carlson

2 Introduction

This document describes the external Timecode and 128MHz clock interface at the correlator. Both of these signals are provided to the correlator from the EVLA system, and form the foundational reference for correlator processing.

The external Timecode (**ext-TC**) interface is a fiber MT-RJ receptacle connector utilizing the Agilent AFBR-5903Z fiber-optic transceiver module.

The 128 MHz clock interface is a 50-ohm terminated SMA female connector, which expects a single-ended 0 dBm (223 mV RMS, or about 600 mV pk-pk swing), 128 MHz CW or square-wave input signal.

To provide fault-tolerant operation, the correlator requires two redundant signals of each type, although it can operate with just one. Timing (phase matching) between redundant signals is not critical; however, they should be reasonably matched (~<100 nsec) to minimize switchover time should one signal disappear.

3 Overview

ext-TC and 128 MHz CW signals are provided to the correlator via the front-panel of select X-bar Boards installed in the middle 6U crate of correlator Station Racks.

A simplified diagram showing signal entry to the correlator is shown in Figure 3-1 below:

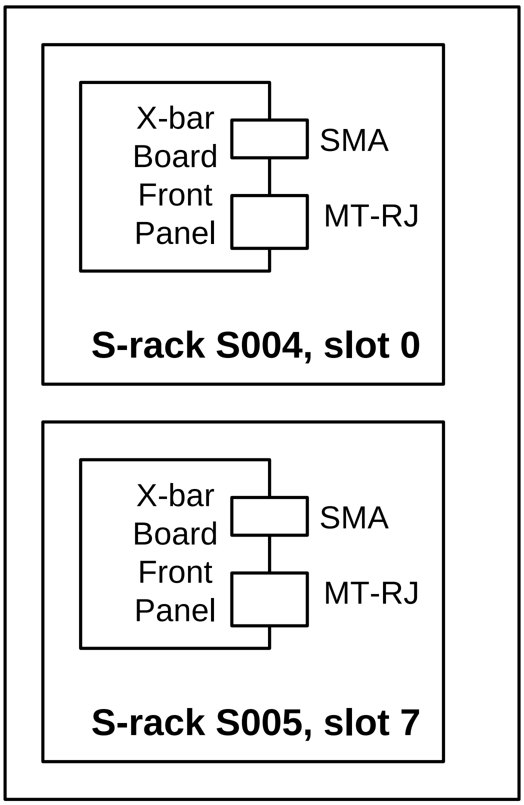

Figure 3-1 External Timecode and 128 MHz CW entry to the correlator.

Cable entry access points are provided through the rear of the racks, and cabling should be routed to these points accordingly. Racks are labeled in a specific sequence in the room, according to Figure 3-1 of [1].

The two X-bar Boards then distribute a "station Timecode" (**st-TC**) to all Station Boards in the correlator [2] according to the distribution plan defined in [4]. The **st-TC** signal contains an additional "hop count" field that helps to ensure that the final TIMECODE signal [3] distributed to downstream Baseline Boards by Station Boards is roughly synchronized (to within delay difference absorption FIFOs on the Baseline Board).

4 Interface Requirements

The following sub-section defines interface requirements for the ext-TC and the 128MHz clock signals.

4.1 ext-TC Signal

The ext-TC frame is shown in Figure 5-1. A “101010…” preamble is continuously present, until the Start Bit (2 zeros in a row) marks the beginning of the frame. There is one frame per second. The signal operates at exactly 128 Mbps, frequency locked to the 128 MHz clock signal, and the EVLA H-maser. Phase of this signal compared to the 128 MHz clock is not important, as long as it is stable and doesn’t change by more than ~±0.1 UI (±1.5 nsec).

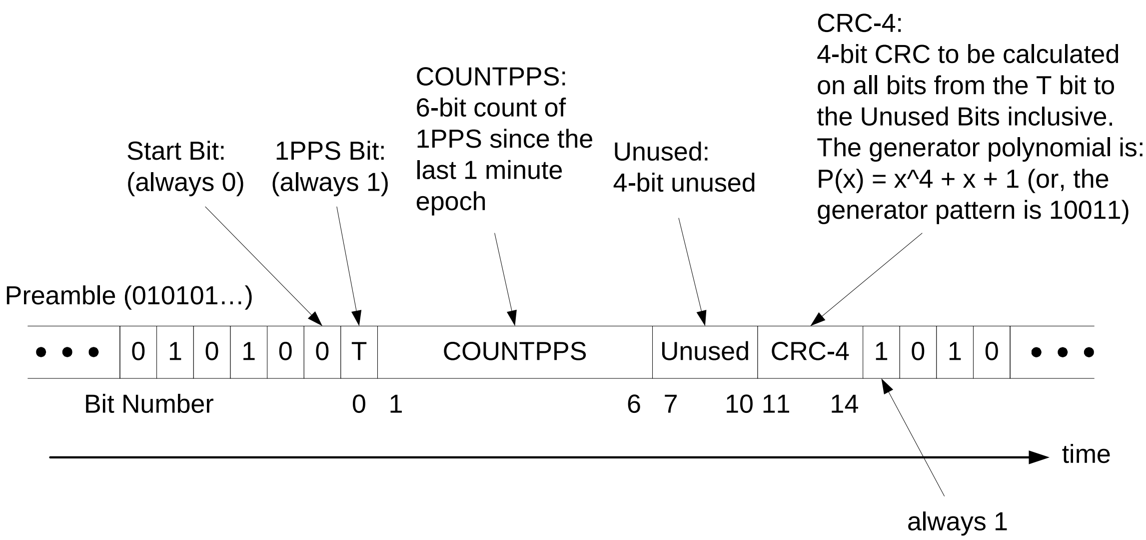

Figure 4-1 The ext-TC frame.

Each of the ext-TC bits is as follows:

Bit[0] (1PPS Bit) – Always 1 at every second epoch. This is the fundamental epoch in the Time Tick input.

Bit[1:6] (COUNTPPS Bits) – Counts of 1PPS time tick since last 1 minute epoch. This 6-bit counter increases by 1 for every 1PPS time tick, and is 0 on every 1 minute epoch. Bit[1] is the LSB, and Bit[6] is the MSB.

Bit[7:10] (Unused Bits) – 4 unused bits. Bit[7:10] should always be set to 1010.

Bit[11:14] (CRC-4 Bits) – 4-bit CRC that is calculated on all bits from Tick Bit to the Unused Bits inclusive. The generator pattern is 10011. Refer to the Appendix for the CRC-4 generation circuit.

4.2 ext-TC Physical Interface

The ext-TC physical interface is an MT-RJ fiber receptacle connector, provided by the Agilent AFBR-5903Z fiber-optic transceiver module. As this connector is on the front panel of the X-bar Board, a grommetted entry port is provided in a panel in the 6U crate accessed at the back of the rack. Fiber must be routed through this grommet and into the correct X-bar Board according to Figure 3-1, depending on which rack is accessed.

4.3 128MHz Clock Signal

The 128 MHz clock signal is a single-ended 0 dBm (223 mV RMS) CW or square-wave signal terminated into 50 ohms. Maximum cycle-to-cycle jitter is ± 100 psec.

4.4 128 MHz Clock Physical Interface

The front panel of the X-bar Board contains a right-angle SMA connector (e.g. Johnson Components part # 142-0701-501) that mates with standard semi-rigid or flexible coaxial RG-142 50 ohm cable and male connector. This connector is terminated on board, and so no external termination is required.

For convenience of installation, this front panel connector is connected to a feed-thru bulkhead connector mounted beside the ext-TC fiber entry grommet at the back of the 6U crate. The external 128 MHz clock can connect to this bulkhead connector at the rear of the rack.

5 Appendices

5.1 CRC-4 Circuitry

Hardware calculation of a CRC is a simple, efficient, and straightforward process at both the transmitter and receiver. The basic schematic for the CRC-4 with generator pattern 10011 required by this interface is shown in Figure 5-1. For the transmitter, the following steps are required:

- Reset all of the DFFs.
- Input the transmit bit sequence, LSB first, into the INPUT.
- Append 4 zero to the end of the transmit bit sequence – once the last zero is clocked to position C0, then the calculated CRC is C0 … C3.
- C0 … C3 is transmitted as the CRC-4 code, LSB (C0) first.

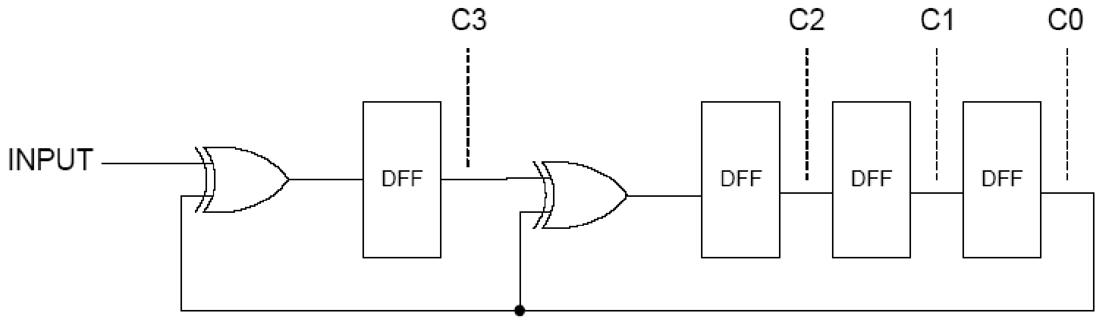

Figure 5-1 CRC-4 circuitry with generator pattern 10011. the coefficients C0, C1, C2, C3 represent the calculated CRC for the transmitter, 4 clock cycles (zero padded) after the transmitted bit stream enters the INPUT. For the receiver, the entire input and the 4-bit CRC should yield an all zero result (C0 … C3) if there was no transmission error.

For the receiver, the following steps are required:

- Shift the entire received bit sequence and appended 4-bit CRC code into the INPUT, until the last bit is shifted through to the C3 location. If there was no transmission error, then C0 through C3 should all be zero.

Example: The transmitted bit sequence (LSB … MSB) 010111001011101 results in a CRC code of 0111. Receiving the sequence and CRC 0101110010111010111 results in all zeros in locations C0…C3.

6 References

[1] Carlson, B., LOGISTICS AND DIRECTIONS: EVLA Correlator Room Station Rack-to-Baseline Rack High-Speed Cable Installation Plan, LAD Document A25005N0001, Revision DRAFT3, October 25, 2007.

[2] Carlson, B., PROTOCOL SPECIFICATION: Station Timecode ("st-TC") Protocol and Physical Interface Specification, PROTOCOL Document A25022N0043, Revision DRAFT2, October 31, 2007.

[3] Carlson, B., PROTOCOL SPECIFICATION: HM Gbps Cable Signaling Specification, PROTOCOL Document A25022N0041, Revision 1.3, November 2007.

[4] Carlson, B., LOGISTICS AND DIRECTION: EVLA Correlator TIMECODE Cable Installation Plan, LAD Document A25005N0004, Revision DRAFT, October 24, 2007.