

## **PROTOCOL SPECIFICATION**

### **Station Timecode (“st-TC”) Protocol and Physical Interface Specification**

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## **List of Abbreviations and Acronyms**

**LVDS** – Low Voltage Differential Signaling. A high-speed digital differential transmission standard.

**CRC-4** – 4-bit “Cyclic Redundancy Check”. The CRC uses a linear feedback shift register (LFSR) to calculate a code that takes into account all input bits. The generator polynomial defines the LFSR configuration, and different generator codes have different error detection capability. A CRC-4 will catch about 95% of all types of errors.

**HM Wafer** – a 4-pair connector that plugs into one row of an 8-pin HM (hardmetric) header. Wafers can be stacked side-by-side to allow various wiring configuration in the correlator.

**HM** – Hard Metric, 2.0 mm connector system. This connector system is most often utilized in Compact PCI systems, and is an industry standard.

## 1 Revision History

<b>Revision</b>	<b>Date</b>	<b>Changes/Notes</b>	<b>Author</b>
Draft	Apr. 15, 2004	Initial DRAFT release	Zhang Heng
DRAFT2	Oct. 31, 2007	Major definition change. This now describes the “st-TC” Timecode distribution amongst X-bar Boards and Station Boards. The st-TC signal contains a hop count.	Brent Carlson

## 2 Introduction

This document describes the signaling protocol and physical interface of the station Timecode signal (“**st-TC**”) distributed to Station Boards via X-bar Boards in the EVLA correlator.

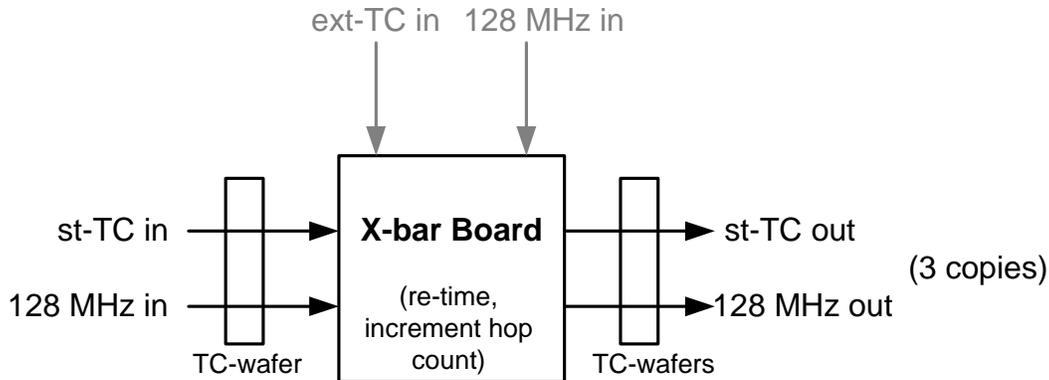
This signal is different than the ext-TC signal described in [1]. The st-TC signal contains an additional 8-bit field, which is the “hop-count” indicating the number of hops/repeats the signal has undergone since its source. This hop-count is used by the Station Board to implement appropriate delays, such that subsequent signaling from Station Boards arriving at Baseline Boards is approximately matched in time.

Each board that receives the st-TC signal, and then repeats it, increments the hop count. The maximum number of hops expected in the EVLA system is 16, but the hop count can support up to 256 hops.

st-TC signals travel to and from X-bar Boards and Station Boards on Meritec 2 mm hardmetric 4-pair wafers. Each wafer contains the st-TC signal, and a 128 MHz clock. A complete cable installation plan for st-TC is in [2].

### 3 Overview

As shown in Figure 3-1, the X-bar Board receives the input st-TC signal and 128 MHz clock on the Meritec wafer, re-times the clock, and generates 3 copies to its output with the hop count incremented. If ext-TC into the X-bar Board is present, then it and its associated 128 MHz input is used instead, with the output st-TC having its hop count set to 0.



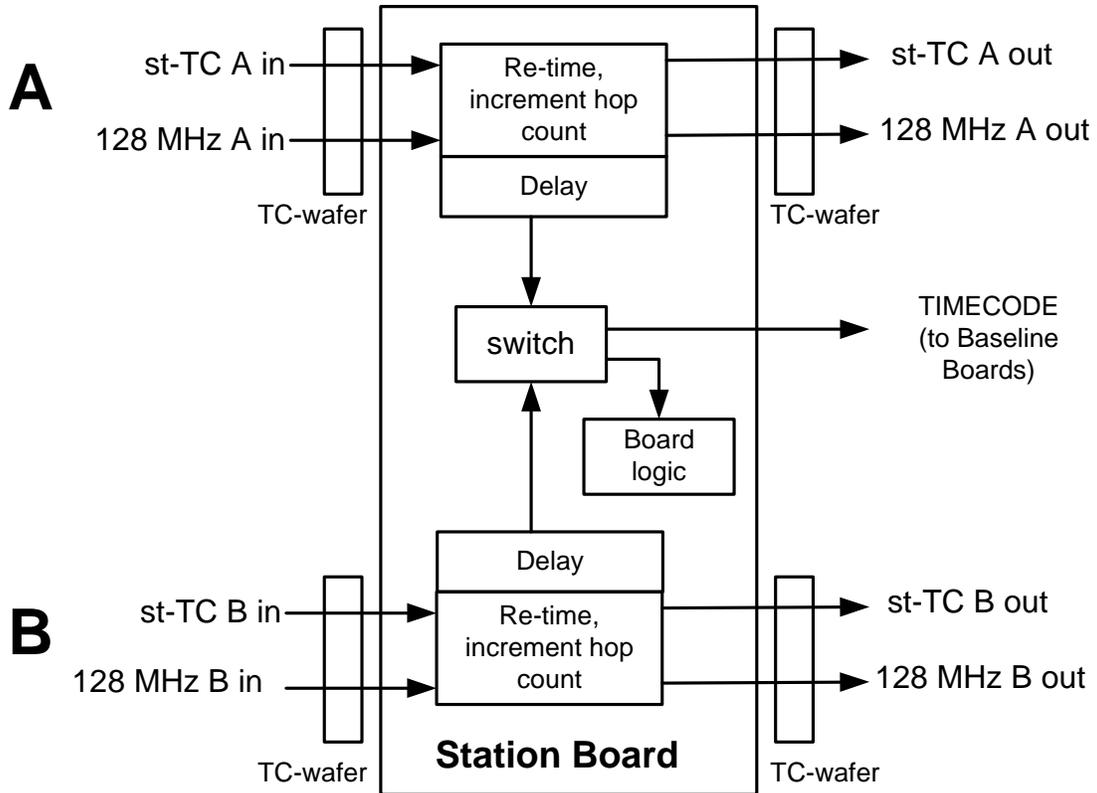
**Figure 3-1 st-TC and 128 MHz clock inputs and 3 copies of outputs of the X-bar Board. If ext-TC input is active, it is used instead.**

The Station Board functions in a similar manner. As shown in Figure 3-2; it receives the st-TC and 128 MHz inputs, re-times them, increments the hop count, and re-generates them on the output wafer. Since fault-tolerant operation is required, the Station Board has two receivers, **A** and **B**. The hop count for A and B could be different and so a different delay is inserted in the A and B path before a switch selects which input will be used for on-board logic, and TIMECODE to the Baseline Board.

The st-TC in to st-TC out delay is a fixed value of 16, 128 MHz clock cycles + I/O delay for a total of ~135 nsec<sup>1</sup>. The Delay used on the Station Board is maximum when the hop-count is minimum, and minimum when the hop count is maximum. This requires that the system knows what the maximum hop count is. The maximum Delay on the Station Board is likely to be 16 hops, at ~135 nsec/hop = 2.16 usec. Station Board circuitry should synchronize A and B inputs into the switch as well as possible, to minimize switchover time to the other input, if it is required.

*Since the CRC-4 code can miss about 6 % of the errors, Station Board and X-bar Board circuitry should be designed to learn the hop count over some period of time, and not instantaneously change it, or the Delay (on the Station Board), if the hop count suddenly changes.*

<sup>1</sup> This number will be refined through empirical tests.



**Figure 3-2 st-TC and 128 MHz clock inputs and outputs of the Station Board. The Station Board develops TIMECODE and transmits it to Baseline Boards.**

## 4 Protocol and Physical Interface

### 4.1 st-TC Signaling Protocol

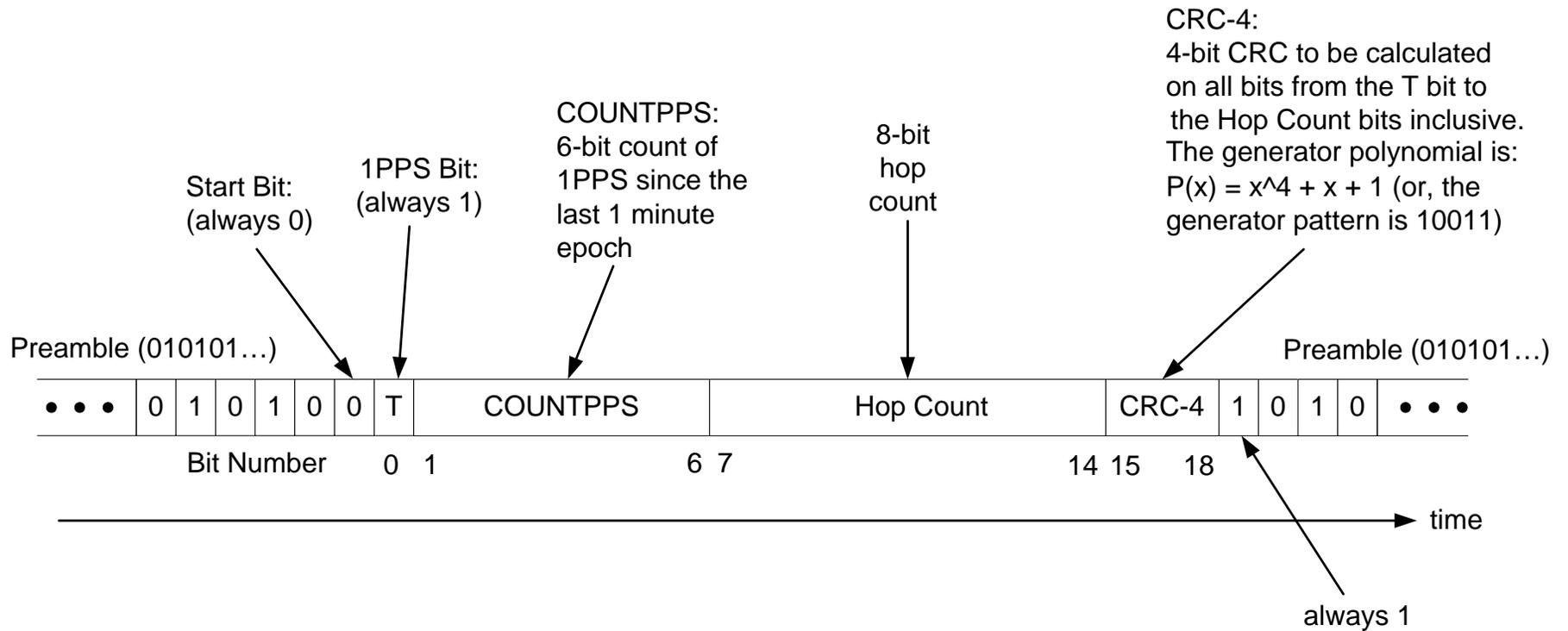
The st-TC frame is shown in Figure 4-1. There is one frame per second. Bits in the frame are as follows:

**Bit[0]** (1PPS Bit) – Always 1 at every second epoch. This is the fundamental epoch in the Time Tick input.

**Bit[1:6]** (COUNTPPS Bits) – Counts of 1PPS time tick since last 1 minute epoch. This 6-bit counter increases by 1 for every 1PPS time tick, and is 0 on every 1 minute epoch. Bit[1] is the LSB, and Bit[6] is the MSB.

**Bit[7:14]** (Hop Count) – Count of the number of hops since the source. Each receiver increments this count before re-transmitting the signal. Bit[7] is the LSB, Bit[14] is the MSB.

**Bit[15:18]** (CRC-4 Bits) – 4-bit CRC that is calculated on all bits from Tick Bit to the Hop Count bits inclusive. The generator pattern is 10011. Refer to [1] for details of the CRC-4 generation circuit.



**Figure 4-1 st-TC frame format.**

## 4.2 Physical and Electrical Interface

Each X-bar Board and Station Board reserves several rows of the 2 mm hardmetric connector for the st-TC signal and the 128 MHz clock. Rows are numbered 1-36 [3], with row 1 at the top. All signals are differential 100 ohm LVDS, AC coupled out of the transmitter.

For the **X-bar Board** the following **row** assignments are used:

- TOP connector: row 35 INPUT; row 36 OUTPUT.
- BOTTOM connector: rows 35 and 36 are both OUTPUTs.

For the **Station Board**, the following row assignments on the MIDDLE connector are used:

- Row 22: INPUT A; row 23: OUTPUT A.
- Row 24: INPUT B; row 24: OUTPUT B.

Refer to [2] for X-bar Board and Station Board Timecode row assignment diagrams.

For BOTH boards, within the wafer row, and looking into the connector (or Common Backplane), the 128 MHz clock is the right-most pair in the row, and the st-TC signal is the pair immediately to the left of the clock, as shown in Figure 4-2. That is, the connector pin **column** assignments are:

- Connector pin columns A and B – 128 MHz clock pair.
- Connector pin columns C and D – st-TC signal pair.
- Connector pin column E, F, G, and H are not connected.

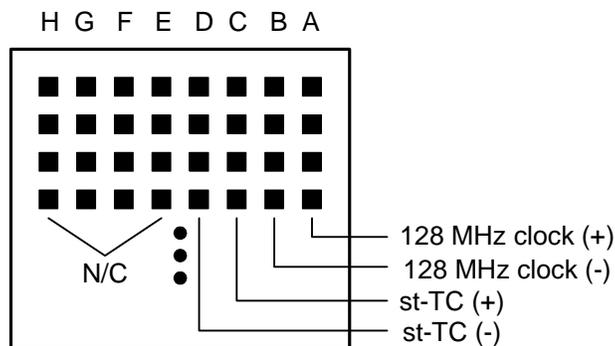


Figure 4-2 ERNI connector column pin assignments.

## 5 References

[1] Carlson, B., INTERFACE CONTROL DOCUMENT: External Timecode (ext-TC) and 128 MHz Clock Interface Specification, ICD Document A25022N0090, Revision 2.0, October 30, 2007.

[2] Carlson, B., LOGISTICS AND DIRECTIONS: EVLA Correlator TIMECODE Cable Installation Plan, LAD Document A25005N0004, October 24, 2007.

[3] Zhang, Heng., INTERFACE CONTROL DOCUMENT: HM Gbps Cable Physical Specification, ICD Document A25022N0040, April 13, 2004.