INTERFACE CONTROL DOCUMENT

HM Gbps Cable Physical Specification

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List of Abbreviations and Acronyms

PECL – Positive Emitter-Coupled Logic

HM Connector – 2mm Hard Metric Connector

SDFB – Station Data Fanout Board

Gbps – Giga bit per second

1 Revision History

Revision	Date	Changes/Notes	Author
Draft	Apr. 13, 2004		Zhang Heng

2 Introduction

This document describes detailed physical requirements for the HM Gbps cable. The Gbps cable provides the high-speed interconnect between the station-based systems, and baseline-based systems in the correlactor. It contains high-speed data, timing, control, and model information that is generated on the Station Boards and used by the Baseline Boards and Phasing Boards. For detailed signaling information of this cable, refer to HM Gbps Signaling Specification (document number A25022N0041).

Background information on the correlator design, and the role of the HM Gbps cable in the system can be found in [1]. This document further refines the physical requirements of the cable and is a reference for designs that interface to the cable/connector and is a reference for cable and connector specifications.

3 Context

The HM Gbps cable provides the primary high-speed interconnects in the correlator. It resides in two places in the correclator system. The “Long” HM Gbps cable resides between the station rack and the baseline rack. The “Short” HM Gbps cable resides in the baseline rack. Each type of the HM Gbps cables will be described in more detail in this document.

A block diagram of the context of the HM Gbps cable is shown in Figure 3-1.

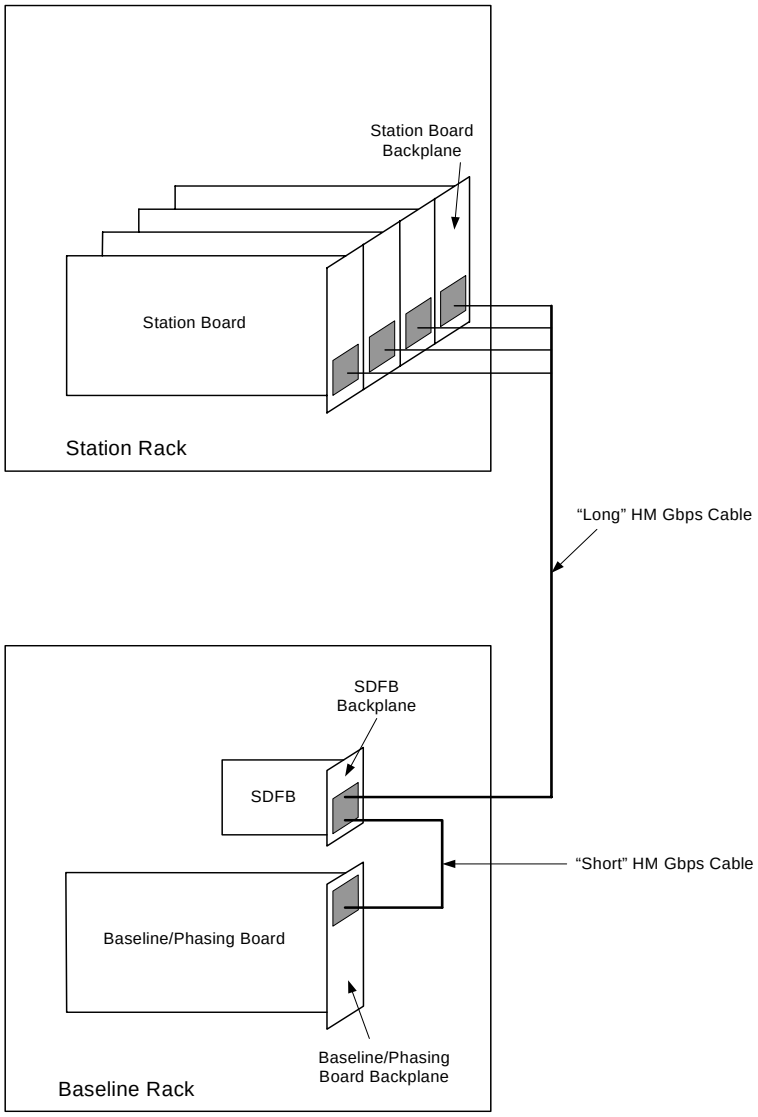

Figure 3- 1 Context diagram of the HM Gbps cable. Both “Long” HM Gbps cable and the “Short” HM Gbps cable contain 16 differential signals in 4 cable stacks. For the “Long” Gbps cable, 4 stacks are split and connected to 4 Station Boards. The SDFB generates 8 copies of input signals, and sends them to the Baseline/Phasing Boards.

4 Overview

In the correlator system, a common backplane has been designed for use of every functional board. This backplane contains 2 HM shrouds on the back, and the HM cables can plug into the shrouds directly from the back of the backplane. A physical diagram of the two shrouds is shown in Figure 4-1.

Rear view of the backplane shrouds (i.e. viewed from the cable side).

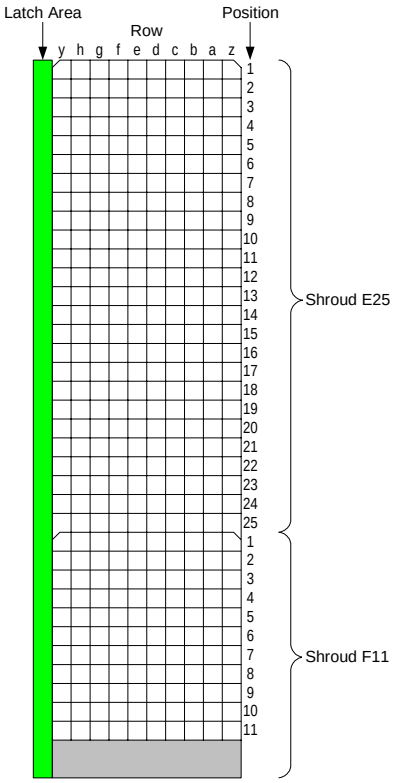

Figure 4- 1 Rear view of the backplane shrouds (i.e. viewed from the cable side). There are two HM shrouds on the back of the backplane: Shroud E25 and Shroud F11. Shroud E25 has 25 positions and Shroud F11 has 11 positions. They are sitting on the backplane next to each other. The shrouds have 10 rows. Row a to h are signal rows; row z and y are ground rows. The left side of the shrouds is the latch area.

There are two HM shrouds on the back of the backplane: Shroud E25 and Shroud F11. Shroud E25 has 25 positions, and Shroud F11 has 11 positions. The shrouds have 10 rows. Row a to h are signal rows; row z and y are ground rows. Each position in the shrouds is shown in Figure 4-2.

Rear view of a single position of the backplane shrouds (i.e. viewed from the cable side).

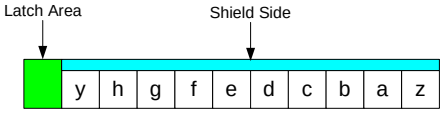

Figure 4- 2 Rear view of a single position of the backplane shrouds (i.e. viewed from the cable side). Row a to h are signal rows; row z and y are ground rows. The latch area is on the left, and the shield plate of the cable stack is on the top.

A single position of the backplane shrouds contains 10 rows. Row a to h are signal rows; row z and y are ground rows. The latch area is on the left, and shield plate of the cable stack is on the top. A double-ended cable stack that connects two of single position shrouds is shown in Figure 4-3.

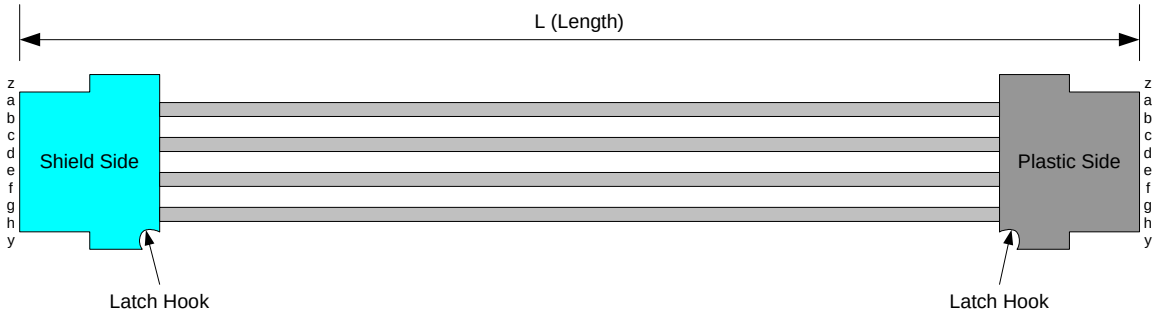

Figure 4- 3 Diagram of a double-ended cable stack. It contains 4 differential pairs. In each pair, line-to-line impedance is 100 ohms, and line-to-ground impedance is 50 ohms. This is the basic element to assemble the HM Gbps cable. Both "Long" HM Gbps cable and the "Short" HM Gbps cable are assembled with this cable stack.

As mentioned before, there are two types of the HM Gbps cable in the correlator system: the "Long" HM Gbps cable and the "Short" HM Gbps cable. The sub-band data signals from the Station Boards are transferred to the SDFB Board through the "Long" HM Gbps cable. On the SDFB, 8 copies of input signals are generated and sent to the Baseline/Phasing Boards through the "Short" Gbps cable. Both "Long" HM Gbps cable and the "Short" Gbps cable will be assembled with the same cable stack shown in Figure 4-3. Each type of the HM Gbps cable will be discussed in more detail in following section.

5 Requirements

The following is the list of the HM Gbps cable requirements.

5.1 Physical Requirements

5.1.1 "Long" HM Gbps Cable Physical Requirements

As shown in Figure 3-1, the "Long" HM Gbps cable resides between the Station rack and the Baseline rack. The sub-band data from 4 Station Boards are transferred to the SDFB through this cable. On the SDFB side, 4 stacks of the HM cables are combined together and plugged into the SDFB backplane. On the Station Board side, 4 stacks will be split and plugged into 4 Station Board backplanes. The requirements of this cable assembly are shown in Figure 5-1.

Side view of the "Long" HM Gbps cable assembly (i.e. viewed from the side of the latch hook).

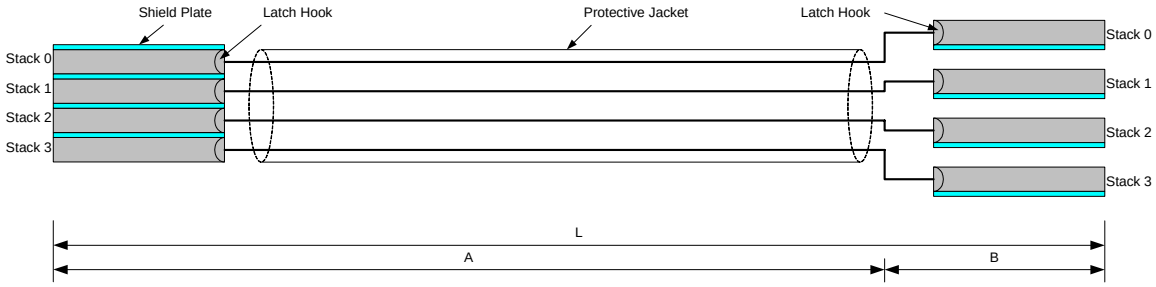

Figure 5- 1 Side view of the "Long" HM Gbps cable assembly (i.e. viewed from the side of the latch hook). On the SDFB side, 4 stacks of the HM cables are combined together and plugged into the SDFB backplane. On the Station Board side, 4 stacks will be split and plugged into 4 Station Board backplanes.

The pin assignment of this cable is defined as follows.

Row	Y	H	G	F	E	D	C	B	A	Z
Stack 0	GND	BB1-	BB1+	BB0-	BB0+	CTR0_1-	CTR0_1+	CLK-	CLK+	GND
Stack 1	GND	BB3-	BB3+	BB2-	BB2+	CTR2_3-	CTR2_3+	CLK-	CLK+	GND
Stack 2	GND	BB5-	BB5+	BB4-	BB4+	CTR4_5-	CTR4_5+	CLK-	CLK+	GND
Stack 3	GND	BB7-	BB7+	BB6-	BB6+	CTR6_7-	CTR6_7+	CLK-	CLK+	GND

Table 5- 1 Pin assignment of the "Long" HM Gbps cable.

5.1.2 "Short" HM Gbps Cable Requirements

As shown in Figure 3-1, the "Short" HM Gbps cable resides in the Baseline rack. The SDFB receives the sub-band data inputs from the Station Boards, generates 8 copies of the input signals, and sends them to the Baseline Boards and the Phasing Boards. The pin assignment of this cable is the same as the "Long" HM Gbps cable, refer to Table 5-1 for the detailed definition. The requirements of this cable assembly are shown in Figure 5-2.

Side view of the "Short" HM Gbps cable assembly (i.e. viewed from the side of the latch hook).

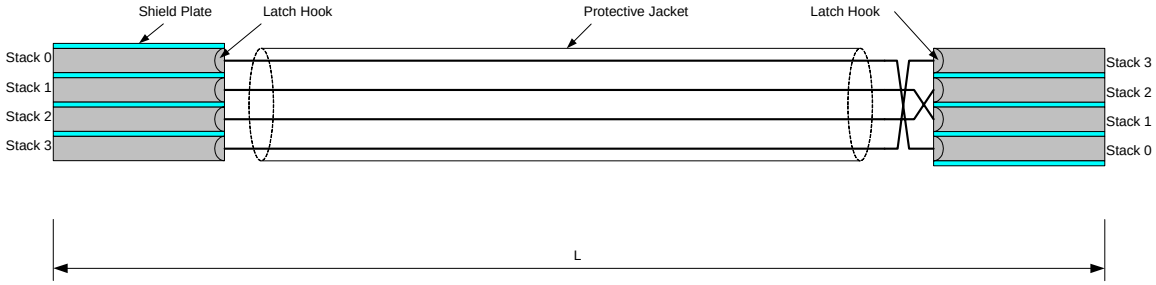

Figure 5- 2 Side view of the "Short" HM Gbps cable assembly (i.e. viewed from the side of the latch hook).

5.1.3 Summary of the HM Gbps cable Physical Requirements

The following table shows the summary of the HM Gbps cable physical requirements.

Cable Name	No. of Stacks	Length (M)			Equalization	Reference
		L	A	B		
"Long" HM Gbps Cable 1	4	5	4.8	0.2	Yes	Figure 5-1
"Long" HM Gbps Cable 2	4	7	6.8	0.2	Yes	Figure 5-1
"Long" HM Gbps Cable 3	4	10	9.8	0.2	Yes	Figure 5-1
"Short" HM Gbps Cable	4	1	NA	NA	No	Figure 5-2

Table 5- 2 Summary of the HM Gbps cable physical requirements.

5.2 Performance Requirements

The performance requirements of the HM Gbps cable are based on some assumption and analysis on the high-speed signal path. See Appendices 8.1 for detailed information.

1. The "Long" HM Gbps cable with equalization shall have the following performance characteristics[1]:
    a. 100 ohm differential impedance ±5 ohms. 50 ohm line-to-ground (+/-2.5 ohm).
    b. Leg-Leg skew within differential pair: <10ps per cable.
    c. Leg-Leg skew between different pairs: <30ps per cable.
    d. Near-End Cross-Talk: <2% (tr = 100 psec).
    e. Attenuation: <7 dB per cable at 1.024GHz.
    f. Peak jitter: <25ps.
2. The "Short" HM Gbps cable without equalization shall have the following performance characteristics[1]:
    a. 100 ohm differential impedance ±5 ohms. 50 ohm line-to-ground (+/-2.5 ohm).
    b. Leg-Leg skew within differential pair: <10ps per cable.
    c. Leg-Leg skew between different pairs: <30ps per cable.
    d. Near-End Cross-Talk: <2% (tr = 100 psec).
    e. Attenuation: <1 dB per cable at 1.024GHz.
    f. Peak jitter: <25ps.

5.3 Environmental Requirements

1. The cable and connectors will be operated in a room temperature, controlled office environment. However, many hundreds of long (up to 10 m) cables will be installed under a raised floor in arbitrary orientations, and so it is necessary to ensure that the cable is robust enough to not suffer physical damage over time (i.e. with many cable lying on top of each other in arbitrary orientations).
2. The floor where the cable is to lie must not contain any protrusions or sharp edges that could damage the cable under normal self-loading conditions as described above.

5.4 Interface Requirements

1. All signals are differential. The driver and receiver must use appropriate source/termination values for a point-to-point link. The driver is the Altera Stratix Gx PECL driver, and the receiver is the Altera Stratix Gx LVDS receiver. The termination impedance is 100 ohm line-to-line and AC coupling is used.
2. All signals are operating at 1.024Gbps except the clock signals. The clocks are running at 128MHz.

[1] Note: these specifications are preliminary and require testing of the actual cable build to verify.

6 Functional Specifications

Since this document represents a cable physical specification, this section is intentionally left blank.

7 References

[1] Carlson, Brent, Refined EVLA WIDAR Correlator Architecture, NRC-EVLA Memo#014, October 2, 2001.

[2] Carlson, Brent, Requirements and Functional Specification, MDR-80 Cable and Interface, Revision 1.4, July 4, 2003.

[3] Altera Stratix GX FPGA Family Data Sheet, Ver. 2.0, November 2003.

[4] Motorola MC100ES6220 Technical Data Sheet, Rev 1, November 2002.

8 Appendices

8.1 Gbps Signal Path Analysis

The performance of the HM Gbps cable has significant impact on the high-speed data transfer from the Station Board to the Baseline/Phasing Board. In order to specify the HM Gbps cable's performance requirements, a simplified diagram of the high-speed signal path is shown in Figure 8-1.

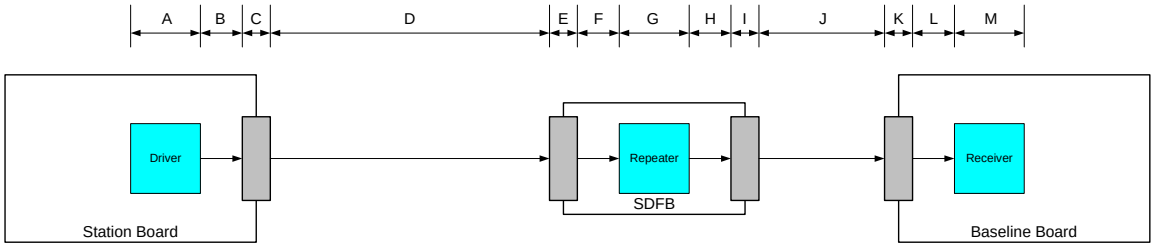

Figure 8- 1 A simplified diagram of the high-speed signal path.

The high-speed Gigabit signal path contains a PECL driver, a PECL repeater, a LVDS receiver, 4 HM connectors, and few-inch PCB traces on the Boards. An analysis of this signal path is shown as follows.

8.1.1 Jitter Budget Analysis

A summary of the jitter budget analysis is shown in Table 8-1.

Path	A	B	C	D	E	F	G	H	I	J	K	L	M	Sum	Budget
Jitter (ps)	160	12	5	25	5	12	3	12	5	25	5	12		281	416

Table 8- 1 Jitter budget analysis of the high-speed Gigabit signal path.

More explanations of the Table 8-1 are as follows.

- A: Altera Stratix Gx PECL driver. The maximum output jitter of this driver is 160ps that is specified in Table 139 on page 266 of the Stratix Gx FPGA family data sheet.

- B: 4" output PCB trace on the Station Board. Assume that the PCB trace will introduce 3ps of jitter per inch, and total 12ps of jitter will be added to the signal.

- C: Station Board output HM connector. Assume that the HM connector will introduce 5ps of jitter to the signal.
- D: “Long” HM Gbps cable with equalization. According to the simulation result from Meritec, the maximum jitter that this cable will introduce is less that 25ps.
- E: SDFB input HM connector. Assume 5ps of jitter will be introduced here.
- F: 4” input PCB trace on the SDFB. Assume 12ps of jitter will be introduced here.
- G: Motorola PECL repeater. According to the answer from Motorola, this chip may introduce maximum 3ps of jitter.
- H: 4” output PCB trace on the SDFB. Assume 12ps of jitter will be introduced here.
- I: SDFB output HM connector. Assume 5ps of jitter will be introduced here.
- J: “Short” HM Gbps cable without equalization. Assume that maximum 25ps of jitter will be introduced by this cable (Should ask Meritec).
- K: Baseline Board input HM connector. Assume 5ps of jitter will be introduced here.
- L: 4” input PCB trace on the Baseline Board. Assume 12ps of jitter will be introduced here.
- M: Altera Stratix Gx LVDS receiver. Minimum eye opening for this receiver is 560ps that is specified in Table 139 on page 265 of the Stratix Gx FPGA family data sheet.

According to this jitter budget analysis, there are 135ps of jitter budget left. But since we haven’t count crosstalk and system noise impacts on the signal, the actual jitter margin might be less 100ps.

8.1.2 Signal Loss Analysis

A summary of the signal loss analysis is shown in Table 8-2.

Path	A	B	C	D	E	F	Sum	Budget	G	H	I	J	K	L	M	Sum	Budget
Loss (dB)	0	-0.6	-0.2	-7	-0.2	-0.6	-8.6	10	0	-0.6	-0.2	-1	-0.2	-0.6		-2.6	8.5

Table 8- 2 Signal loss analysis of the high-speed Gigabit signal path.

More explanations of the Table 8-2 are as follows.

- A: Altera Stratix Gx PECL driver. The minimum output level of this driver is 525mv that is specified in Table 69 on page 206 of the Stratix Gx FPGA family data sheet.

- B: 4” output PCB trace on the Station Board. Assume 0.15dB/inch loss on PCB trace, 4” PCB trace will have 0.6dB loss.

- C: Station Board output HM connector. Assume 0.2dB loss on the HM connector.

- D: “Long” HM Gbps cable with equalization. Maximum signal loss on this cable must be less than 7dB.

- E: SDFB input HM connector. Assume 0.2dB loss on the HM connector.

- F: 4” input PCB trace on the SDFB. Assume 0.15dB/inch loss on PCB trace, 4” PCB trace will have 0.6dB loss.

- G: Motorola PECL repeater. According to Motorola MC100ES6220 data sheet, the input voltage of this chip is 100mv-1300mv. If we assume the output of A (Stratix Gx PECL driver) is 500mv, and we want the minimum input voltage at G (Motorola PECL repeater) is 150mv. We will have 10dB budget from A to G. the minimum output level of this repeater is 400mv.

- H: 4” output PCB trace on the SDFB. Assume 0.15dB/inch loss on PCB trace, 4” PCB trace will have 0.6dB loss.

- I: SDFB output HM connector. Assume 0.2dB loss on the HM connector.

- J: “Short” HM Gbps cable without equalization. Assume the attenuation on this cable is less that 1dB.

- K: Baseline Board input HM connector. Assume 0.2dB loss on the HM connector.

- L: 4” input PCB trace on the Baseline Board. Assume 0.15dB/inch loss on PCB trace, 4” PCB trace will have 0.6dB loss.

- M: Altera Stratix Gx LVDS receiver. It requires minimum 560ps eye opening over 100mv peak-to-peak. We will have 8.5dB budget from G (Motorola PECL repeater) to M (Stratix Gx LVDS receiver), if we want the minimum input voltage at 150mv.

According to the signal loss analysis, the high-speed signal path from A (Altera Stratix Gx PECL driver) to G (Motorola PECL repeater) has 10dB budget, and loss on the “Long” HM Gbps cable must be limited to maximum 7dB.

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