USER MANUAL

EVLA Correlator System

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List of Abbreviations, Acronyms, and Definitions

100Base-T – Refers to 100 Mbps ("Fast") Ethernet, running on twisted pair, using an RJ-45 connector.

1000Base-T – Refers to 1 G Ethernet, running on twisted pair, using an RJ-45 connector.

ASIC – Application Specific Integrated Circuit. In this document, it often refers to the Correlator Chip.

BDF -- Binary Data Format. Format of data output from the CBE.

BlB – Short form for "Baseline Board".

BlB Pair – Baseline Board Pair. In the EVLA, a pair of Baseline Boards are required to correlate all polarization products, for 32 antennas, 128 MHz/pol'n.

BLF – Binary Lag Format. Raw binary file format containing LTA lag frames.

BB0, BB1 – The HM Gbps code stream which carries sampled DATA streams to the Baseline Boards.

CBE – Correlator Back End. Refers to the cluster of computers which accept and process Ethernet "lag frames" from Baseline Boards.

CDR – Clock Data Recovery. PLL circuit/receiver that recovers the data clock from the data.

CMIB – Correlator Monitor Interface Board.

COTS – Commercial Off-The-Shelf.

CPCC – Correlator Power Control Computer.

CRM -- Correlator Resource Monitor.

DIN – German standards body.

DPA – Dynamic Phase Alignment. The Altera-FPGA scheme for automatically selecting and tracking the clock edge, in source-synchronous clocking/communication.

DRAO – Dominion Radio Astrophysical Observatory.

DTS Receiver – Digital Transmission System Receiver. Referring to the fiber receiver mezzanine card that plugs into the Station Board.

DUMPTRIG – The HM Gbps code stream which controls Correlator Chip integration.

ECO – Engineering Change Order.

ERNI – One manufacturer of "2 mm Hard Metric" connectors.

FDDI – Fiber Distributed Data Interface. A somewhat obsolete communications standard.

FIFO -- First In First Out (memory).

FORM -- Fiber Optic Receiver Module. Referring to the fiber receiver mezzanine card that plugs into the Station Board.

FPGA -- Field Programmable Gate Array. XBB functions are implemented in FPGAs.

FPGA boot binary – Binary file generated by FPGA compile software, which gets loaded (booted) into the FPGA to enable the FPGA to perform designed functions. Also known as a "configuration" file or a "personality" file.

HM Gbps – Refers to the inter-board data transmission protocol used in the EVLA correlator system. Refer to A25022N0041.

HVAC -- Heating, Ventilation, and Air-Conditioning.

IEEE 802.3 – The Ethernet frame standard, which defines the Ethernet frame (preamble, start, addresses, payload, FCS).

I/F pair -- Intermediate Frequency pair. Refers to a wideband polarization pair signal from the antenna receiver.

jitter – Refers to randomization of arrival time of waveform edges from where they ideally should be.

JTAG – Joint Test Action Group, developer of IEEE Standard 1149.1-1990, a board connectivity test scheme, which does not require normal functioning of chips.

LED – Light Emitting Diode.

LTA – Long-Term Accumulator.

LVDS – Low Voltage Differential Signaling.

M&C – Monitor and Control.

MCAF – Metadata Capture and Formatting.

MCB – Monitor Control Bus. Refers to the simplified synchronous read/write CPU interface, used on the Baseline Board.

MCCC – Master Correlator Control Computer.

MITR – Module Instance Tracking and Reporting.

NRAO – National Radio Astronomy Observatory.

PCB – Printed Circuit Board.

PCS – Physical Coding Sub-layer. Codes between Ethernet packets, specific to a given standard.

PHASEMOD – The HM Gbps code stream which carries antenna-based phase models to the Baseline Boards.

PHASERR – The HM Gbps code stream which carries phase corrections to the Baseline Boards, to implement sub-sample delay tracking.

PC/104+ -- Refers to an industry-standard embedded CPU form factor, which is a PC on a 3.5" x 3.5" card.

PCI bus – Peripheral Component Interconnect bus. A bus standard for personal computers.

PCMC – PC/104+ Mezzanine Card. This card is part of the CMIB stack, and is sandwiched between the COTS PC/104+ CPU card and the motherboard.

PCU – Power Conversion Unit. Refers to SMPS in the -48 VDC power plant.

PLL – Phase-Locked Loop.

RAM – Random Access Memory.

Recirc -- Refers to the Recirculation FPGAs on the board.

RFI -- Radio Frequency Interference.

RFS – Requirements and Functional Specification.

RJ-45 – Registered Jack – 45. Standard 8-wire connector used in networking.

RPM -- Revolutions Per Minute.

RPMIB -- Remote Power Monitor Interface Board.

RXP -- Refers to one of two RXP FPGAs on the Baseline Board. "Re-timing", "X-bar", and "Phasing".

SERDES – Serializer/Deserializer.

SMA -- SubMiniature version A. Small form-factor high-frequency coaxial connector.

SMPS – Switch Mode Power Supply.

SDM -- Science Data Model.

SCSI – Small Computer System Interface standard.

SFP – Small Form Factor Pluggable.

SNMP – Simple Network Management Protocol.

SSB – Single Side Band.

StB -- Short from for "Station Board".

STP – Shielded Twisted Pair.

TCP/IP -- Transmission Control Protocol/Internet Protocol.

Timecode -- General term referring to reference time in the correlator. Could refer to ext-TC, st-TC, or TIMECODE, depending on context.

TIMECODE – The specific HM Gbps code stream which carries the current time epoch.

TTL – Transistor-Transistor Logic. Generally means ~4 V (high), and <0.8 V (low) voltage levels.

UDP/IP – User Datagram Protocol/Internet Protocol. A connectionless, packet-based protocol defined by RFC 791 and RFC 768.

UPS -- Uninterruptable Power Supply.

USB – Universal Serial Bus.

UTP – Unshielded Twisted Pair.

VCI protocol – Virtual Correlator Interface protocol.

VDIF – VLBI Data Interchange Format. Refer to the GigE FPGA RFS A25092N0001 for more information.

VLBI -- Very Long Baseline Interferometry.

W0/W1 – A distinct pattern inserted in the BB0, BB1 sampled DATA streams to help with receiver synchronization.

Wafer – Refers to a ~2x17 mm plastic connector space or cable header for intra-correlator high-speed data transport.

WIDAR -- Wideband Interferometric Digital ARchitecture.

WDM – Wavelength Division Multiplexing.

w.r.t. – "with respect to".

XBB -- Short form for "Cross-Bar Board".

XPAK – Expansion Pack; industry-standard form factor, for 10G Ethernet.

XML– Extensible Markup Language. ASCII-encoded messaging used for peer-to-peer communications.

1 Revision History

Revision	Date	Changes/Notes	Author
DRAFT	August 25, 2011	Initial release for review.	B. Carlson

2 Introduction

This document is the User Manual for the EVLA Correlator System. It contains information relevant and pertaining to the entire system, tying together all lower-level documentation to provide a complete picture of the correlator. It is written to give the interested reader some insight into the layout and operation of the correlator, and contains details documenting specific wiring and setup configurations crucial to the operation of the system. As much as possible, items that might be considered peripheral to the correlator, but nevertheless essential for its operation, are included and in these cases input from other experts' domains are included for completeness.

The correlator system is a 32-antenna, 8 GHz per polarization "spectral-line" cross-correlation spectrometer. The correlator contains antenna (or "station")-based processing elements, antenna-pair or baseline-based cross-correlation elements, station-to-baseline connection/cross-bar switching elements, monitor and control elements, output data processing elements, the power delivery system, the HVAC (Heating, Ventilation, and Air Conditioning) and system protection systems, and finally the software, operating at various levels, to drive it all.

The correlator "core" consists of 16, 24-inch x 7 ft racks. Eight of the racks—"Station racks"—contain Station Boards and cross-bar switches, and 8 of the racks—Baseline racks—contain Baseline Boards. The Station Boards are where antenna/station-based processing occurs. The cross-bar switches, implemented in Cross-Bar Boards contained within Station racks, facilitate configuration of the correlator to allow for flexible allocation of cross-correlator resources. The Baseline Boards are where cross-correlation, and phased-array (a.k.a. "tied-array") processing occurs.

To process all of the bandwidth (8 GHz/polarization), 4 Station Boards are required for each antenna, resulting in a total of 128 Station Boards for all 32 antennas[1]. Each Station Board processes 2 GHz/polarization in 3-bit[2] sampling mode, or 1 GHz, one polarization, in 8-bit sampling mode. The latter limitation is imposed not by the correlator, but by the sampler modules in the antennas and the fiber-optic data transport system to the correlator.

Along with other necessary interferometer array functions, each Station Board contains 36 independently configurable multi-stage digital filters, 18 per "data path" (in 3-bit initial sampling mode each data path is a polarization). Normally, only 16 per data path are used, and cross-correlator resources exist for only 16. The output of each filter can be configured for bandwidths ranging from 128 MHz to 31.25 kHz, in binary steps. The

[1] Although the EVLA has only 27 antennas, the correlator is designed and built for 32 antennas, allowing for some additional capacity for expansion and redundancy. This is also because the correlator "numerology" is set for 32 antennas.

[2] The data paths on the correlator allow for 4-bit samples; 3-bit samples are imposed by minimizing the cost of the antenna-to-correlator fiber transmission system.

output of each Station Board is therefore 16 sub-bands, each with a potentially different bandwidth, and from a different antenna for a particular baseband or I/F pair. Four boards per antenna, therefore, mean there are 64 sub-band polarization pairs that must be correlated.

The cross-bar switch between the Station Boards is a distributed cross-bar switch, which comes close to functioning as a full cross-bar switch but with some limitations. Collectively, it allows sub-band outputs from Station Boards to be routed to cross-correlation resources (Baseline Boards) in flexible ways, allowing tradeoffs between number of sub-bands and I/F pairs and number of spectral channels per sub-band cross-correlation. The cross-bar switch is implemented as 8 Cross-Bar Boards in each Station rack; each Cross-Bar Board contains two independent devices, each one implementing a switch for a particular sub-band. Wiring in the Station rack from the Station Boards to the Cross-Bar Boards establishes sub-band switching granularity for this part of the system.

The Baseline Boards are arranged as "Baseline Board pairs", abbreviated "BlB-pairs", which consist of two Baseline Boards in adjacent slots in a rack. Each BlB-pair is able to form all cross-correlation products (1, 2, or 4) for one sub-band. Therefore, 64 BlB-pairs are required to cross-correlate all 16 sub-band pairs from the 4 I/F pairs fed into the correlator. Baseline Boards are grouped in "quadrants" (Q1-Q4), where each quadrant (consisting of 2 Baseline racks) contains 16 BlB-pairs, or 32 boards. Baseline Boards in a BlB-pair are intricately linked; data from the cross-bar switches feeds one board—the board in the odd slot of the pair—and an identical copy of that data is fed to the 2nd board of the pair, albeit re-arranged (mirror-imaged) due to connection routing constraints.

Each Baseline Board contains an 8x8 array of Correlator Chips, each of which contains 2048 "lags", divided into 16, 128-lag sections, which may be connected and configured in various ways. The array of chips are fed by various levels of receiving and cross-bar switching chips, and a specific cross-bar switch setting allows all polarization pairs for 32 antennas, for one sub-band to be correlated in a BlB-pair. "Static" and "dynamic" "recirculation" on the board, along with the cross-bar switch, enable one or more BlB-pairs to be allocated to a sub-band, providing aforementioned flexibility. Antenna sub-arrays can also be independently correlated, and can be formed with 4-antenna granularity.

Cross-correlation coefficients are output from Baseline Boards on 1 Gigbit Ethernet, and route to the Correlator Back End (CBE)—a cluster of computers—via a monolithic network switch (the "CBE switch"). The CBE performs required processing ("data gathering", FFT, optional RFI excision, optional further integration, formatting, labeling, and meta-data insertion) preparing data ultimately destined for the image processing/archive system. Phased-array processing is performed on each Baseline Board and the resulting real-time time-domain data stream, packaged in the "VDIF" format, is output on a 2nd 1 Gigabit Ethernet link, for routing to VLBI recorders or other phased-array data processors. The Baseline Board also allows for phased-data to be simultaneously routed to the board's correlation matrix for auto (or cross-correlation); this same data is also output from the board's rear connector in raw format for direct

connection to other processing equipment. The phased-array delay center is identical to the interferometer delay center, for the particular sub-band being processed. There is no possibility of intentionally or inadvertently offsetting these delay centers, are both are forced to use the same phase and residual delay models.

Each Station Board and Baseline Board contain an embedded computer (PC/104+ CPU module—"PC/104+" is an industry-standard embedded module form factor), running a real-time Linux OS. These are referred to a "CMIBs"—Correlator Monitor Interface Boards. CMIBs talk to the boards they are plugged into via a standard PCI-bus interface (translated by another mezzanine card—the "PCMC"—to a simple synchronous read/write bus for the board), and connect to central control computers, and sometimes the outside world, via 100 Mbps Ethernet switches. The PC/104+ and PCMC combination is sometimes referred to as the "CMIB stack". The CMIBs contain all of the real-time, and quasi-real-time software required to perform necessary functions, and they communicate with the outside world using the XML protocol, on TCP/IP. The Station Board contains the DTS receiver (a.k.a. Fiber-Optic Receiver Module—FORM) mezzanine card, which also contains a CMIB, but this module and its own CMIB are not formally considered to be part of the correlator, although they reside within the correlator racks.

There are two main central control computer types. The first type is the "MCCC"—Master Correlator Control Computer. The MCCC's primary function is to translate high-level correlation requests from the EVLA Executor to low-level configurations understood by the CMIBs— the so-called "Configuration Mapper" function. This is no small feat considering the plethora of ways the correlator can be configured. Generally, there is not a one-to-one mapping between Executor configuration requests and actual correlator configuration. The MCCC also gathers and distributes alerts coming from the CMIBs. The protocol that the Executor uses to talk to the Configuration Mapper running on the MCCC is referred to as the "VCI" protocol, an acronym for "Virtual Correlator Interface". The VCI protocol is a specific set of XML schema, which the Configuration Mapper and Executor understand.

There is only one hot-running MCCC, and a cold-standby is available in case of failure; the problems of handling a hot-standby were deemed too great to be worth the effort of implementation; if the MCCC dies, the correlator is effectively down until it is replaced. The MCCC communicates with the CMIBs via 100 Mbps Ethernet switches. These switches also contain routing paths to allow CPCCs to talk to the CMIBs, and allow Baseline Board packets to be routed to the MCCC for testing by the CRM (Correlator Resource Monitor).

The second type of central computer is the CPCC—Correlator Power Control Computer. There are two of these computers in a 1+1 redundant hot-running configuration. Either one of the computers (known as "CPCC-1" and "CPCC-2") could completely fail, and the correlator would still keep running; if both CPCC computers fail—something with a very low probability—the entire correlator will shutdown instantly. The primary role of the CPCC computers is to directly control and monitor the power enable and monitor lines for each Station Board, Cross-Bar Board, and Baseline Board in the system, as well

as monitor and control rack fan speeds. Control and monitor lines for the boards and the fans are hard-wired connections directly between the boards and the CPCCs (one separate cable path for each CPCC), independent of any network switches. Thus, as long as at least one CPCC computer is up, and it has a network connection, it is possible to access these control+monitor lines.

CPCCs run autonomously, monitoring AC-mains power fail status from the -48 VDC power plant, monitoring board temperatures (via the network), and controlling rack fan speeds. CPCCs are programmed to autonomously take action to protect (shutdown) the correlator if need be. (It should be noted that as a final backup, each board in the correlator contains dual redundant thermal-overload protection devices, which will protect the boards from thermal damage in the worst case situation. Thus, inaction on the part of the CPCC is unlikely capable of damaging the correlator.) The CPCCs also monitor smoke/fire alarm and HVAC system status, and take appropriate action to cut power and protect the system if required.

Correlator racks are powered by a central -48 VDC power plant system, located in the correlator room. This is a high reliability/high availability commercial-off-the-shelf (COTS) system built for use in telecom central offices. The power plant is fed by 3-phase 480 VAC from the site mains supply, contains 2 racks of PCUs (Power Conversion Units) and central distribution bus-bars/breakers, and a bank of telecom-quality batteries. This system provides the correlator with enough backup power so that in the event of short power outages no interruption of operation occurs and with enough backup time to allow backup diesel generators to kick-in and restore the AC-mains supply. The power plant's PCUs and batteries, along with mains-AC transient suppressors, provide the correlator with a nice and well-protected -48 VDC supply to reduce the probability of "power bumps" damaging the boards (the boards themselves contain dual transient suppressors—transorbs—on their -48 VDC lines as well). The power plant contains the smarts to automatically cut output power (independent of the CPCCs) if the voltage drops below a certain programmable level to prevent an undervoltage and/or excessive battery drain condition. The CPCCs are programmed to gracefully shut down the correlator well before this point.

The power plant contains N+1 PCUs (Power Control Units—total 20 at 200 A each), built for hot-servicing. The total output power capacity of the power plant is ~190 kW, but normally only about 150 kW of power is used, allowing for some headroom. The power plant provides dual 200 A services, each with its own breaker (located in the power plant racks), to each rack. Two sets of two wires, routed in overhead cable trays, connect each rack to -48 VDC. Each rack contains a dual-leg breaker panel, further routing -48 VDC to each board in the rack. Each Station Board and Baseline Board is protected with its own breaker, and all 8 Cross-Bar Boards are on one breaker in each Station rack. -48 VDC delivery to the correlator is completely isolated, thus ensuring deterministic routing of high-current DC paths. The -48 V return (a.k.a. neutral) is only connected to room shielding/earth ground in the power plant distribution panel.

The correlator room contains several cooling systems, which provide enough cooling capacity to remove the ~150 kW of heat generated by the correlator. There are 2 high-

capacity chilled water units, and 2 lower-capacity air conditioning units. In the event of mains AC failure, the cooling units continue to circulate air, however, they are no longer actively dissipating heat to an exterior unit, and so only the existing chilled water heat capacity can be used for cooling. Thus, in the event of a prolonged power failure, and diesel backup generator failure, the correlator can run only for ~5 minutes at full capability before the CPCC puts it into sleep mode (de-configures all of the FPGAs and power down the ASICs), and then finally shuts it down.

A picture of the complete correlator system, primarily showing correlator racks is in Figure 2-1 below. All associated network switches and control computers are out of view on the other of side of the racks in the picture.

Figure 2-1 The EVLA Correlator System installation at the VLA.

2.1 Acknowledgements

The entire EVLA correlator system is the result of the direct and indirect work of many people at DRAO Penticton and at NRAO Socorro for many years.

Several people have contributed directly to the content of this document, without which it would have been impossible to put together. Kevin Ryan provided details regarding

CPCC functionality and connectivity to HVAC and smoke detector systems. Bob Broilo provided information on the HVAC systems, building UPS, and -48 VDC power systems. James Robnett provided information on the M&C switch network, the CBE switch, and CBE configuration. Bruce Rowen provided information on CMIB boot sequences. Kerry Shores provided valuable information regarding antenna fiber and I/F mapping to Station Board inputs. And finally, Martin Pokorny provided information on CBE functionality and structure. Hopefully I've put together and annotated their contributions reasonably accurately, and haven't forgotten to mention any direct contributors!

3 Context

The EVLA Correlator System is contained within a dedicated shielded room on the second floor of the Central Electronics Building at the VLA site. A simplified, top-level context diagram, showing all major external interfaces to the correlator is shown in Figure 3-1:

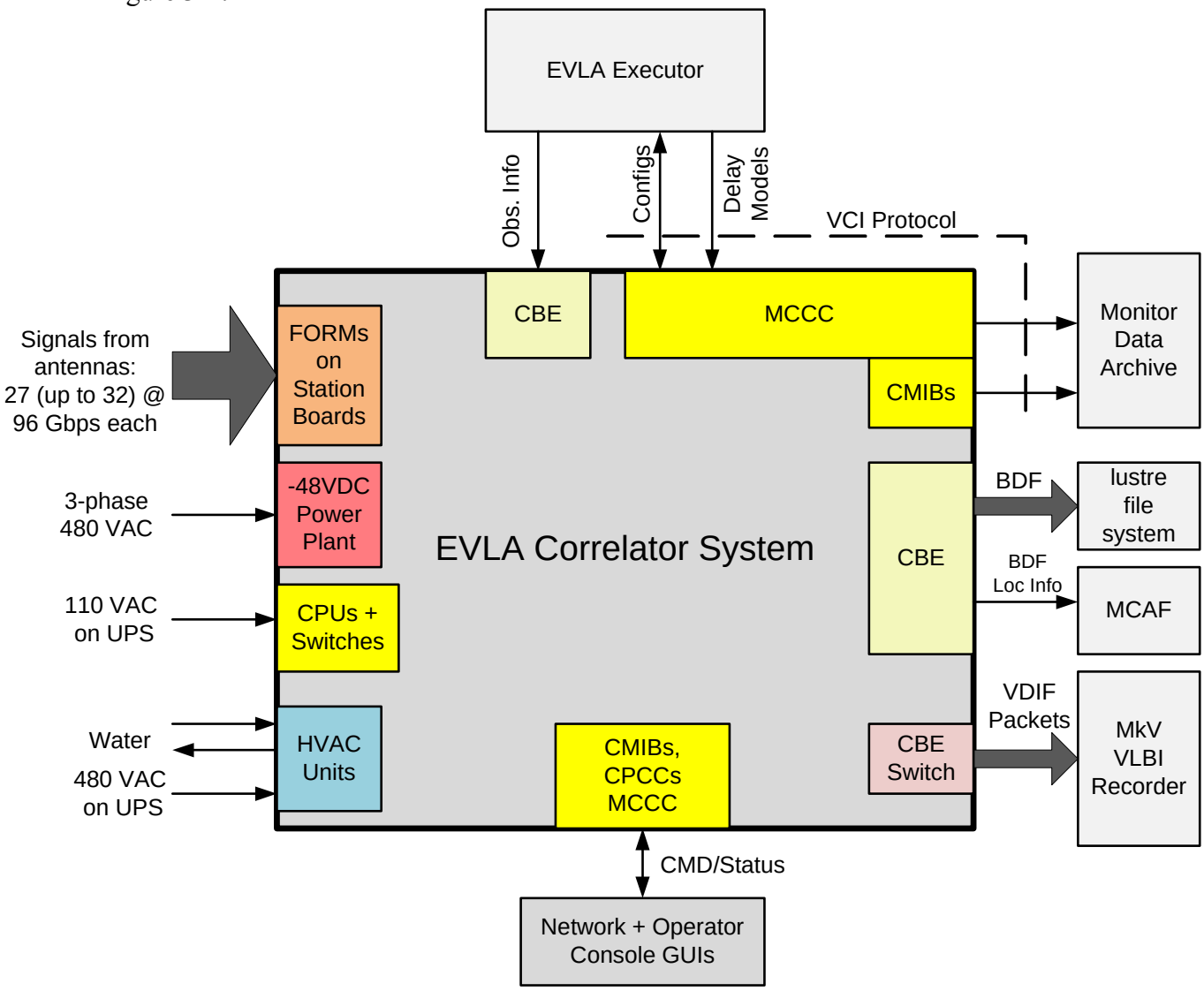

Figure 3-1 EVLA Correlator System top-level context diagram, showing all external-world interfaces, and, within the correlator, the major sub-systems directly interfaced.

The MCCC is the Master Correlator Control Computer, and primarily contains the Configuration Mapper, but also contains tasks to handle routing of Delay Models to Station Boards, and (not shown) the Correlator Resource Monitor (CRM).

CMIBs are Correlator Monitor Interface Boards, which are embedded PC/104+ CPU modules, each one running a real-time Linux operating system. There is one of these on

each Station Board and Baseline Board in the system (and one on each FORM/DTS receiver mezzanine card, although the FORM is not formally part of the correlator). Thus, there are 256 + 128 = 384 networked CMIBs in the correlator.

The CBE (Correlator Back End), is a compute cluster which gathers and formats data products from the correlator, and outputs them to the Science Data Archive as BDF (Binary Data Format) data products.

The CBE Switch is a monolithic (i.e. switching between any ports) Ethernet switch, which also facilitates routing of real-time phased-array VDIF (VLBI Data Interchange Format) packets to one or more MkVc VLBI data recorders.

The CPCCs are Correlator Power Control Computers, responsible for real-time monitoring of correlator status (temperatures, voltages, fan speeds, -48 VDC power plant), and facilitating and controlling graceful correlator startup and shutdown.

4 Overview

A simplified block/signal flow diagram of the correlator system is shown in Figure 4-1:

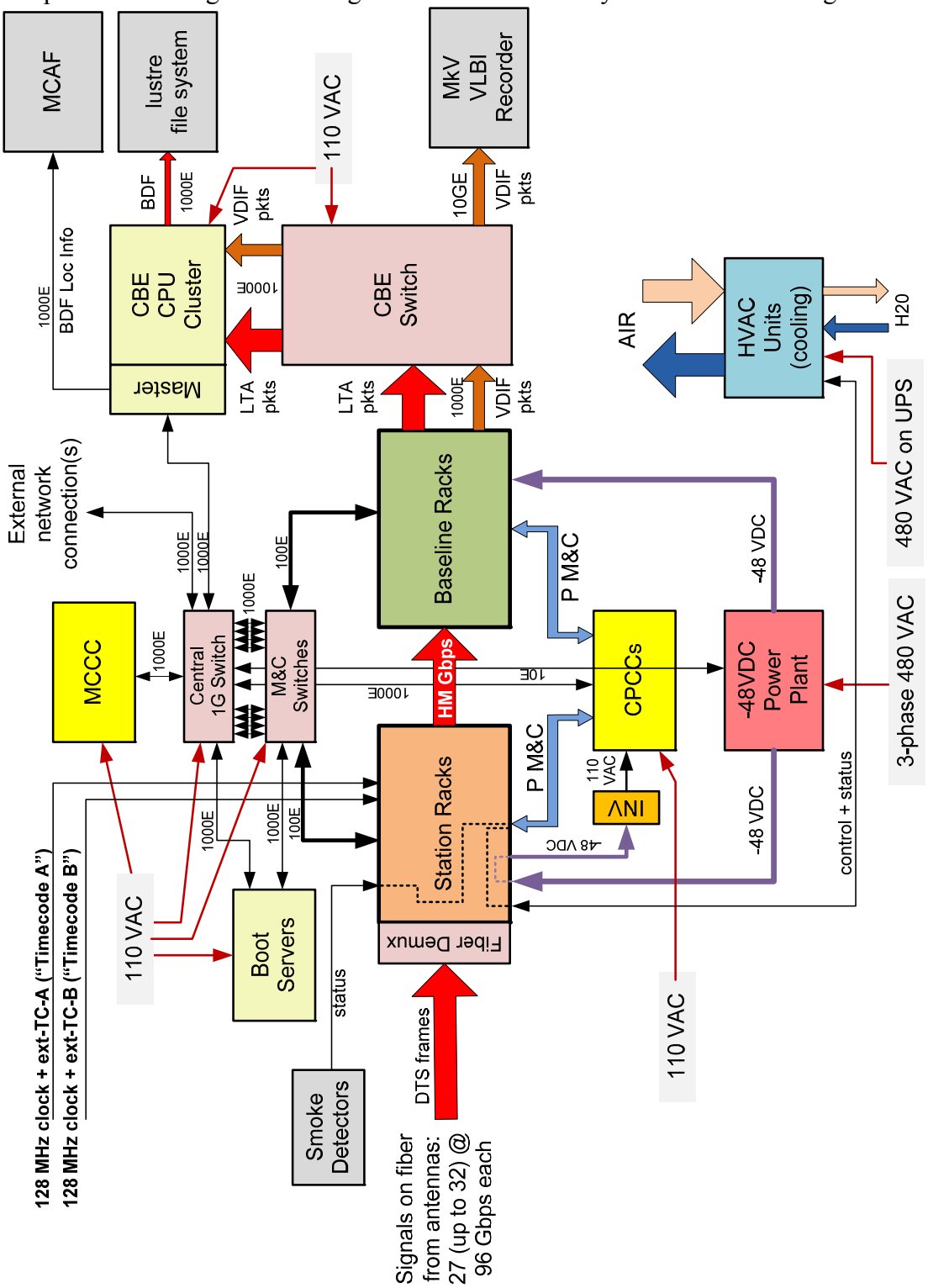

Figure 4-1 Simplified block diagram of the EVLA Correlator System.

Major astronomical data signal flow is as follows:

1. Antennas receive the signal, down-convert it, sample it, and package it into "DTS (Digital Transmission System) Frames", which are transported via fiber to the correlator. The data rate from each antenna to the correlator is 96 Gbps. In 8-bit initial sampler mode, there are 4, 1 GHz signals, sampled at 2.048 Gs/s each, with a single (i.e. single polarization) 1 GHz sampled signal routed to each Station Board. In 3-bit sampler mode, there are 8, 2 GHz signals, sampled at 4.096 Gs/s each, with dual 2 GHz signals (representing a polarization pair), routed to each Station Board. Refer to section 5.4.1 for more information on I/F routing to the correlator.

2. Station Boards in Station racks perform geometrical delay correction, filter the wideband data into sub-bands for correlation, and include integration and phase information for downstream processing. There is a distributed cross-bar switch within the Station racks, and finally data out of Station racks is in "HM Gbps" protocol format [A25022N0041], for transmission to Baseline racks.

3. Baseline racks perform correlations, as well as optionally producing real-time phased-array (a.k.a. "tied-array" or "summed-array") data in the form of VDIF packets [VDIF] [A25093N0000]. Correlated data, in the form of LTA packets or "lag frames" [A25091N0000] [A25092N0001] are routed via the CBE Switch to the CBE CPU cluster. VDIF packets are routed by the CBE switch to a MkVc VLBI data recorder, or optionally to the CBE for data capture and processing.

4. The CBE CPU Cluster performs further processing on LTA (lag frame) data (data gathering/organization, data normalization, Fourier Transform, optional RFI excision and integration, formatting), and writes BDF (Binary Data Format) data to the "lustre file system", ultimately destined for the Science Data Archive. The CBE also writes BDF location information to MCAF, and MCAF ultimately writes SDM (Science Data Model—all auxiliary science "meta-data") data also to the Science Data Archive.

A brief description of each block in Figure 4-1 is as follows:

Boot Servers – This block consists of 2 server CPUs, each with 4 x 1-Gigabit Ethernet ("1000E" in the diagram) interfaces, which route to the "M&C Switches'" 1000Base-T ports (one 1000Base-T port to one port in each of the 8 switches). Station Board and Baseline Board CMIBs boot and obtain FPGA binaries from these servers. There is a 1000Base-T management connection from each Boot Server CPU into the Central 1G Switch.

Smoke Detectors – There are 3 levels of smoke detection. The first level (CPCC-Stage 1), is "supervisory", and is triggered by events in the alarm monitoring system itself such as the alarm box being opened. It is also triggered by high-sensitivity "sniffer" detectors. The second level (CPCC-Stage 2) is triggered when smoke is detected in a single zone of the room. The third level (CPCC-Stage 3) is triggered when smoke is detected in two or

more zones of the room. Each level is a separate wire, routed into spare RPMIB ports in Station rack S002, allowing the CPCC to directly detect when these events have been triggered. Refer to sections 6.1.1 and 7.1.1.2 for further details.

HVAC Units – These are the system cooling units, providing enough cooling capacity for the correlator and all associated systems in the correlator room. Total cooling capacity is 180 tons. There are chilled-water heat exchangers, known as "CW1" and "CW2", and two air conditioning units, known as "DX1" and "DX2". The two 60 ton chilled water units cool a ~1000 gallon water loop to ~45 F. These units are self controlled and staged in a lead/lag configuration with one unit sufficient to handle the entire heat load. The heat is ejected via a hot water loop and external cooling tower. The cold water is circulated around the building to provide temperature control of the building, but primarily feeds the CW1 and CW2 heat exchangers. These units are automatically valved to provide 65 F supply air to the subfloor space. The DX1 and DX2 air conditioning units have a 30 ton cooling capacity each that can be used to cool the subfloor space in the event that additional cooling is necessary or the chilled-water system fails. In the event of a power failure, the chilled-water plant shuts down. However, the cold water loop has a thermal mass such that at full correlator load, the water temperature rises at approximately 0.9 F/min. The cold water pumps and CW units are on a large building UPS system. Therefore the cold water loop can cool the correlator for ~16 minutes at full load without power to the building.

-48 VDC Power Plant – This is a telecom central-office standard DC supply system. It consists of two racks, containing the 480 VAC to -48 VDC PCUs (Power Conversion Units), and Absolyte XL2000 battery banks. It is capable of providing full power to the correlator for 5 minutes on AC fail, and reduced power for a much longer period of time. Refer to section 5.10 for details on system power routing and grounding.

M&C Switches – These switches, located in one rack in the correlator room, consist of 8 units, each unit with 48, 100Base-T ("100E" in the diagram) ports and dual 1000Base-T ("1000E" in the diagram) ports. Each unit is carved into 3 sets of 16 100Base-T ports. The first and second set feed 16 Station Board CMIBs and 16 FORM (DTS receiver module) CMIBs in each Station rack; the third set feeds 16 Baseline Board CMIBs in a Baseline rack. The first switch feeds S001 and B101, the second switch feeds S002 and B102 etc. One 1000Base-T port from each unit ties into the "Central 1G Switch", and the other ties into the Boot Servers (for a total of 8 connections to the Boot Servers).

Central 1G Switch – This is a 48-port 1000Base-T switch, tying together all computers and M&C Switches as shown in the diagram, and providing the gateway to the external world. In addition to the diagram, 4 ports are used for PDUs (Power Distribution Units) in each 19" rack (i.e. racks containing equipment not in Station racks or Baseline racks) for remote power control, 1 port is used for a humidity sensor, 1 port is for in-room laptop use, 2 fiber ports connect to the site switch, and 1 port is used to connect back to the main EVLA site switch.

MCCC – Master Correlator Control Computer. The MCCC is the computer that contains the Configuration Mapper, allowing the EVLA Executor to configure the correlator in a

high-level fashion using the VCI XML protocol. The MCCC also channels Delay Models from the Executor to Station Board CMIBs, and it generates monitor messages destined for the Monitor Data Archive. Refer to sections 5.13 and 7.2 for further details.

CPCCs – Correlator Power Control Computers. These (known as "CPCC-1" and "CPCC-2") are dual hot-running 19" rack-mount computers. Each one contains 16, National Instruments 6509 Digital I/O cards, and it is through these cards, 100-pin SCSI-type connectors and cables, and rack rear-mount RPMIBs (Remote Power Monitor Interface Boards) that the CPCCs control and monitor power lines for each Station Board, Cross-Bar Board, and Baseline Board in the system. Lines on these interfaces are also used for rack fan speed control, and fan speed monitoring. The CPCCs also have connectivity to allow for in-system programming of the Cross-Bar Board FPGA EEPROMs, although there are some limitations as noted in following sections. Additionally, spare ports on RPMIBs in Station racks S001 and S002 allow the CPCCs to monitor smoke detector and HVAC status. Refer to sections 5.11 and 7.1 for further details.

INV – This is a -48 VDC to 110 VAC voltage conversion box, providing power to CPCC-2. The purpose here is to provide a secondary independent source of power, in case the 110 VAC UPS feed fails. In this case, CPCC-2 would still keep the correlator from shutting down instantaneously, as it runs from -48 VDC battery power.

Fiber Demux – Bolted to the inside top front of each Station rack, is a fiber wavelength de-mux panel. This panel contains 4, 1 to 12 WDM de-multiplexers, 1 for each antenna. The 12 fibers out of each de-multiplexer route to 4 FORM/DTS receiver boards mounted in 4 Station Boards. Thus, there are 3 fibers plugged into the front of each Station Board sourcing from this panel, and since there are 4 Station Boards for each antenna, a total of 12 fibers from each of these de-multiplexers is required. Refer to section 5.4.1 for details on I/F mapping to each Station Board.

Station Racks – There are 8 Station racks, each of which contains 16 Station Boards, which process DTS frames from antennas. On each Station Board is mounted a CMIB embedded CPU module, and a FORM board with its own CMIB mezzanine card. Each CMIB has a 100Base-T connection to the M&C Switches. Since there are 8 racks, a total of 32 antennas can be processed. Station racks also contain Cross-bar Boards, which implement a distributed Station rack-to-Baseline rack switch. Wiring from Station Boards to Cross-bar Boards, and on to Baseline Boards in Baseline racks enables much of the flexibility in the correlator. Station racks also accept and distribute the reference 128 MHz clock and "ext-TC" ("external Timecode") signal within the Station racks in a redundant ("A" and "B") daisy-chained ring fashion. As indicated in Figure 4-1, spare RPMIB inputs are used to monitor HVAC and Smoke Detector status information, and route it to CPCCs for appropriate action.

Baseline Racks – There are 8 Baseline racks, each of which contains 16 Baseline Boards. Each Baseline Board contains a CMIB, connected to the M&C Switches by 100Base-T Ethernet. Each adjacent pair of Baseline Boards is able to perform all cross-correlations for a sub-band polarization pair, for 32 antennas, or be used to cross-correlate multiple

sub-arrays, or be used as a smaller part of a sub-band pair correlation, in the case where more spectral channels are to be assigned to a sub-band pair than can be obtained with just one Baseline Board pair (BlB-pair).

Station racks are centrally located, and Baseline racks are located peripherally around Station racks. This is done to facilitate "star" routing from Station racks to Baseline racks, keeping cable lengths within 1 Gbps transmission range. Baseline racks are arranged in quadrants, each quadrant (numbered Q1-Q4) containing 2 racks, and able to correlate 16 sub-band pairs, normally from one I/F pair, but able to be assigned to any of the I/F pairs with Cross-Bar Board switching in Station racks (each BlB-pair can correlate sub-band from any I/F pair, and so the quadrant is not a "rigid" concept). There are 2, 1000Base-T Ethernet ports on each Baseline Board. One port, "SFP1" is for LTA frames encapsulated in UDP/IP packets, and the other port, "SFP2" is for VDIF frames encapsulated in UDP/IP packets. All of these ports route to the CBE Switch, although only a selected subset of SFP2 ports actually connect into the CBE Switch.

CBE Switch – This is a 384-port Gigabit Ethernet switch with 20, 10 Gigabit Ethernet ports, 16 of which are consumed for switch interconnects. Its purpose is to facilitate LTA packet routing to the CBE CPU Cluster, and to facilitate routing of VDIF packets on 1000Base-T sourcing from Baseline Board SFP2, to a MkVc VLBI data recorder with a 10G Ethernet port. VDIF packets may also be routed to CBE CPUs through this switch.

CBE CPU Cluster – This is a cluster of 32 CPU blades, connected to the CBE Switch. These CPUs perform all CBE processing, and write BDF files to the lustre file system for eventual inclusion in the Science Data Archive. There is a Master CBE node, known as "CBE Master", which connects to the Central 1G Switch. CBE Master also writes BDF file location information to MCAF.

The remainder of this User Manual will describe system-level signaling and connectivity within the core of the correlator, which comprises the Station racks, Baseline racks, Station rack-to-Baseline rack connectivity, and CPCCs, in particular CPCC connectivity to the correlator and auxiliary status information routed through the correlator.

5 Functional Description

This section contains a functional description of the correlator core, borrowing diagrams from other documents and with screen shots of GUI panes to illustrate functionality and connectivity.

5.1 Overview of Capabilities

This sub-section summarizes primary overall correlator system capabilities. For further detailed information on processing capabilities, refer to the EVLA Correlator Project Book, Chapter 8—Correlator.

1. 32 antennas, 8.192 GHz per polarization per antenna (3-bit mode, 2.048 GHz/baseband), or 2.048 GHz per polarization per antenna (8-bit mode, 1.024 GHz/baseband).

2. Digital filtering and correlation for 64 sub-band polarization pairs per antenna. Sub-band bandwidths from 128 MHz to 31.25 kHz in binary steps. Flexible sub-band tuning with sub-band slot restrictions. No un-filtered wideband cross-correlation capability.

3. "WIDAR" mechanism for sub-band transition band aliasing suppression, in which a small different LO-offset is introduced in each antenna, and removed in the correlator with a 3-level phase rotator. This mechanism can be optionally by-passed for sub-bands ≤ 64 MHz.

4. All digital sub-sample delay correction to +/-1/16th (baseline) of a sample (16 sub-band filtering). Final residual sub-sample delay correction in software in the Correlator Back End (CBE).

5. Each of the 1-64 sub-bands can be on a different delay center on the sky, within the primary beam of the antenna. This allows a flexible tradeoff between field-of-view, and bandwidth.

6. 4-bit or 7-bit lag cross-correlation. In 4-bit mode, 16,384 to 4,194,304 channels per baseline, depending on bandwidth and sensitivity requirements. 16,384 channels distributed flexibly across 1-64 sub-bands, any bandwidth. Factor of 2 increase in number of channels with every binary decrease in sub-band bandwidth (to maximum 262,144 channels per cross-correlation product). In 7-bit mode, ¼ the spectral channels are available.

7. Flexible integration times, up to 16 independent integration times synchronized to system timing or a model such as a pulsar ephemeris, referenced and updated

w.r.t. system timing. Minimum 10 millisecond[3] integration time at full bandwidth and spectral channel capability (depending on CBE switch fabric and computing capability). Reduced integration times with reduced bandwidth and number of spectral channels. Maximum 1 second integration—longer with CBE integration.

8. Pulsar phase binning: dual banks of 2000 phase bins, with minimum 200 μsec bin width (all channels, full bandwidth) to 15 μsec bin width (reduced channels, reduced bin width). Maximum bin width, 1 second.

9. Phased-array (a.k.a. "tied-array") output on all sub-bands, for the same delay center as the sub-band cross-correlation. Direct output to correlator hardware for autocorrelations on all sub-bands, and output in VDIF (VLBI Data Interchange Format) in 1, 2, 4, or 8-bits per sample on all sub-bands, subject to network connectivity, data capture, and processing capacity. Each sub-band can choose a different sub-array for phasing, independent of cross-correlation sub-array configuration.

10. Sub-array capability with (optimum) 4-antenna granularity.

11. RFI mitigation. Fast RFI blanking, triggering on sub-band voltage level, with programmable blanking dwell time. Post-correlation temporal/spectral RFI excision in the CBE.

5.2 Simplified Signal Processing Fundamentals

This sub-section discusses fundamental WIDAR signal processing, as implemented in the EVLA correlator. For further details refer to the Programmer's Guide [A25290N0000].

Figure 5-1 is a greatly simplified signal processing flow diagram for the correlator, showing two antenna elements, and the basic steps the signal follows through to the correlator output to the CBE.

The received, amplified, and down-converted signal from the sky undergoes an additional shift in frequency by some small LO offset, before being sampled and transmitted to the correlator. At the correlator, "Bulk Wideband Delay", to +/- 0.5 samples *at the wideband sample rate* occurs. Then, in each digital filter, additional *wideband* ("Offset") delay occurs if the delay center on the sky for the particular sub-band is to be different than the for the entire wideband signal. This sub-band specific wideband delay buffer is much smaller than the bulk delay buffer, and so only a small offset from the main delay beam can be affected (see [A25290N0000] for calculations on limitations.

[3] With as-delivered 1G Ethernet capability. ~1 millisecond integration time at full bandwidth with 10G Ethernet field upgrade is possible see [A25092N0001].

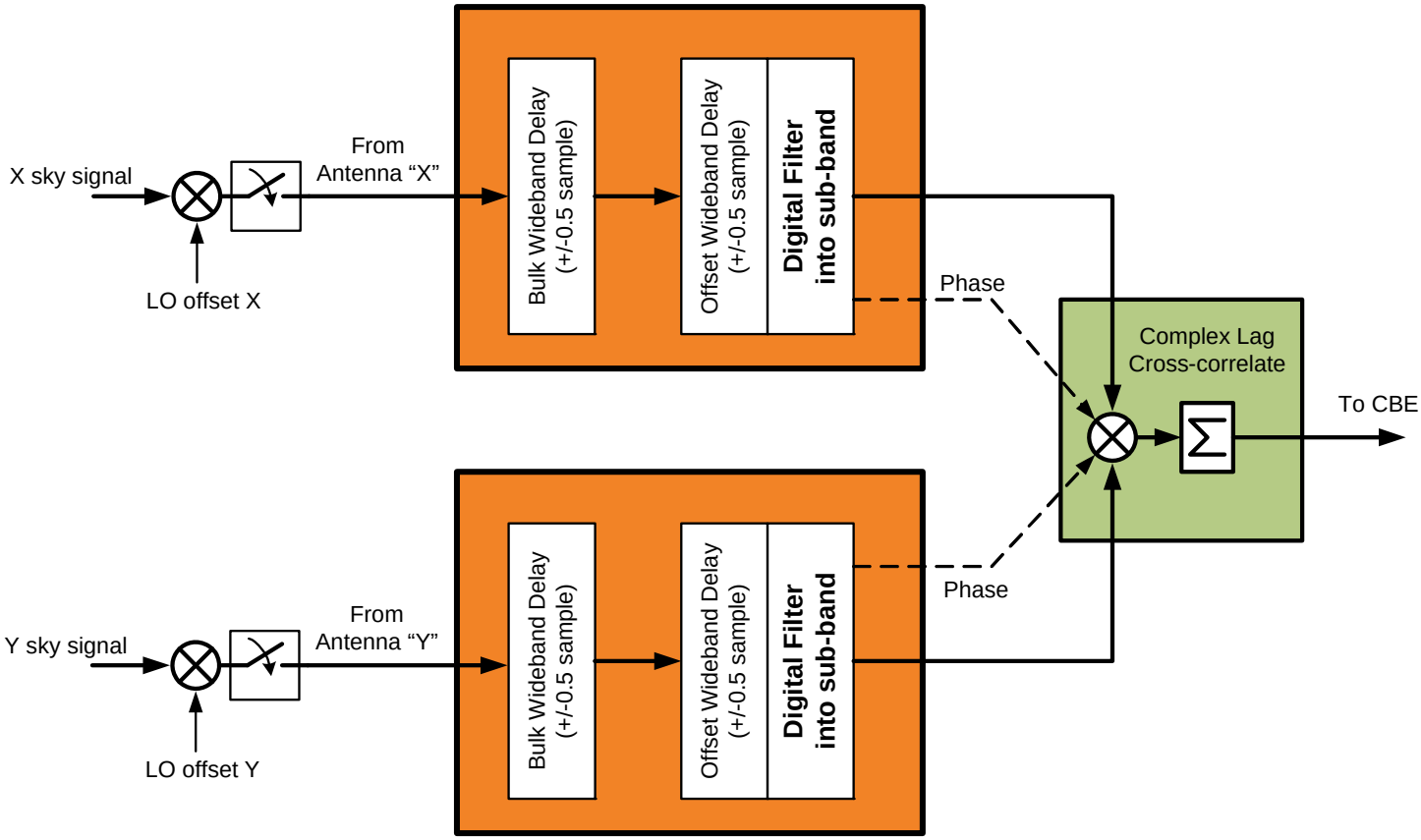

Figure 5-1 Simplified WIDAR signal processing flow.

After wideband delay, the signal is digitally filtered into a sub-band and decimated to a new lower sample rate, which must be ≤ 256 Ms/s, in binary steps. This process selects a certain integer "slot"[4] and bandpass width, and down-converts it to baseband at the new sample rate. The basic steps, showing 4 sub-band slots for clarity, are shown in Figure 5-2 and Figure 5-3.

The signal is then re-quantized to 4 bits or 7 bits, and transmitted to the complex-lag cross-correlator, along with phase, which includes earth-rotation phase, LO-offset phase, and phase ("PHASERR") required for achieving sub-sample delay correction. Cross-correlation and integration occurs, and the results are transmitted to the CBE for further processing.

[4] Stage 2 of the digital filter on the Station Board can overcome this limitation for sub-bands ≤64 MHz, as it contains a digital single-sideband mixer. Thus, any sub-band within the first selected 128 MHz sub-and, can be in any location, but still with binary bandwidth and sample rate restrictions. Note in this case, though, that adjacent sub-bands can't be seamlessly stitched together due to band-edge phase destruction by the SSB mixer, and so in this case, for seamless stitching of sub-bands, sub-band overlap is required.

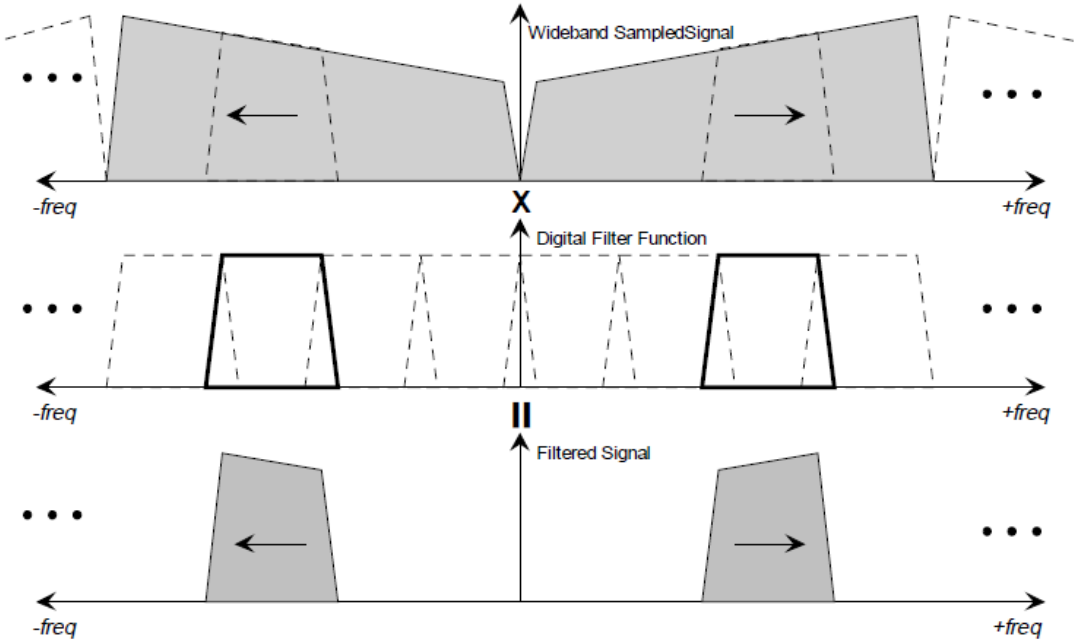

Figure 5-2 Wideband signal, and filtering before decimation. LO offset direction is shown with arrows. 4 sub-band slots are shown for clarity, but many more are available in practise.

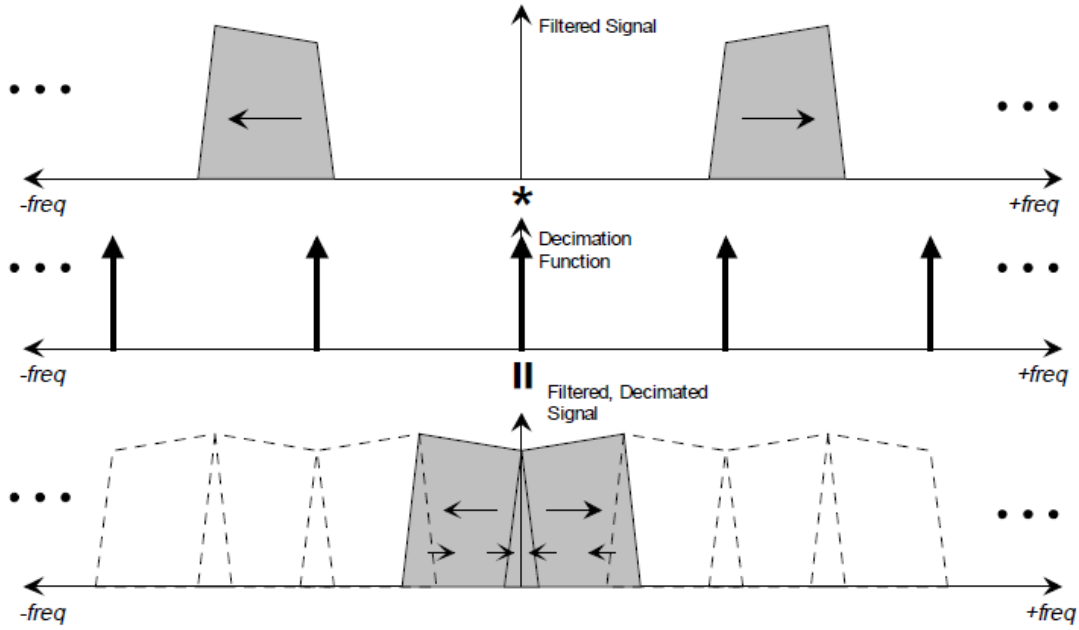

Figure 5-3 Filtered and decimated signal; aliased transition bands have opposite frequency shift, and will de-correlate in the complex correlator.

By introducing the LO offset in the signal before sampling, and removing after digital filtering, aliased sub-band transition bands are highly attenuated, allowing for virtually seamless “stitching” of adjacent sub-bands.

All-digital sub-sample delay tracking is implemented by recognizing that the wideband delay error introduces a phase slope across the wideband that changes with time. When the wideband signal is filtered into narrower sub-bands, the changing delay error results in a changing phase in the sub-band, which is removed with a compensating phase shift in the signal before cross-correlation. The basic process is shown in Figure 5-4.

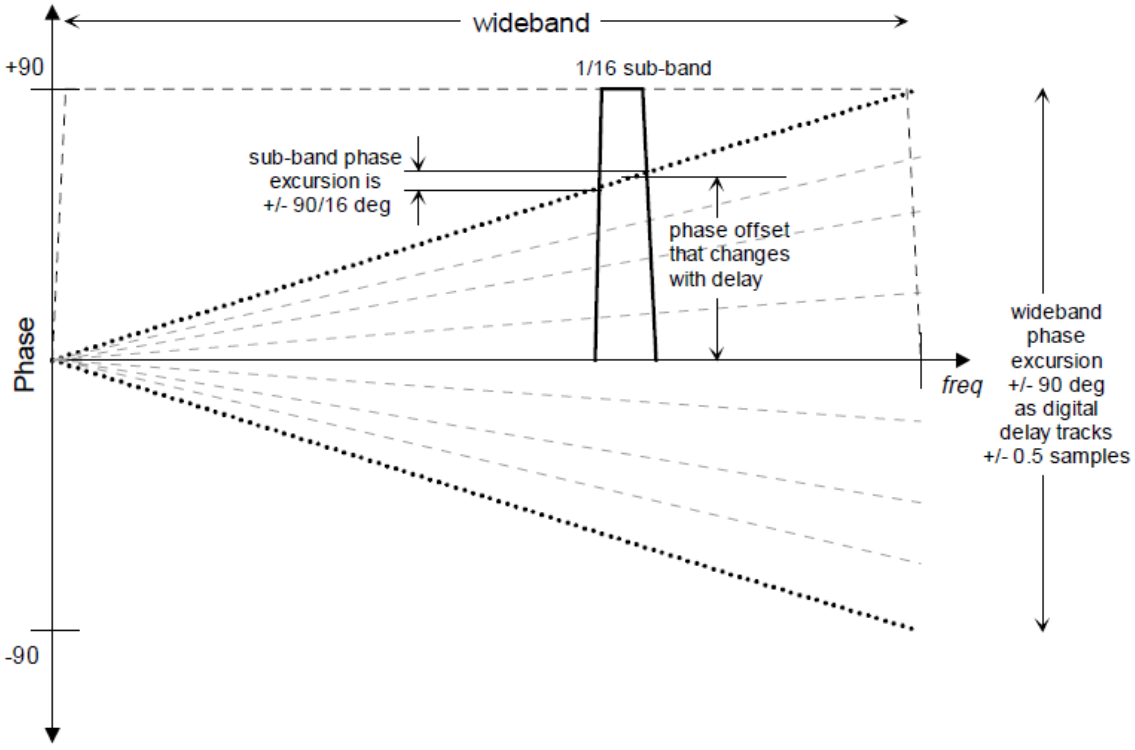

Figure 5-4 All-digital sub-sample delay correction implemented by compensating for the changing phase at the center of the sub-band, as the wideband delay error changes.

There are several "NRC-EVLA Memos" written on the subject of fundamental signal processing in the correlator. Primarily these are **#001**, **#002**, #003, #007, #008, #009, #010, #011, and **#032** (Memo #032 investigates anti-aliasing in detail and discusses additional effects of coarse phase rotation, and mitigation strategies). Also, [A25290N0000] contains details on implementation algorithms in the correlator.

5.3 CPCC Top-Level GUI Description

Figure 5-5 is an annotated screen-shot of the CPCC top-level GUI, reflecting the basic correlator rack layout in the room. From this GUI it is possible to see the power, temperature, and CPU status of all boards in the correlator core (Station Board (**StB**), Cross-Bar Boards (**XBB**), Baseline Boards (**BlB**)), as well as rack fan status, Timecode status, smoke detector status, and HVAC system status. With proper permissions, it is also possible to reboot, shutdown, and power up the entire correlator.

A description of noted elements in the figure is as follows:

A – These are the 8 centrally-located Station racks, numbered S001-S008. Each Station rack processes the data from 4 antennas. Assignment to antennas is determined by fiber routing and is according to Table 5-1. "ea" in the table refers to "EVLA Antenna". The "Antenna I/Fs" are defined in Figure 5-6. There are only 28 antennas, and so inputs to Station rack S008 are not defined, or in some cases, are duplicates of other antennas' signals. Actual mapping of "ea" antennas to physical locations in the Y-array is dynamic and depends on the array configuration and fiber patch panel routing outside the correlator room, and the scope of this document. In practice, MCCC is told via a configuration file, what these mappings are.

B –These are 8 peripherally-located Baseline racks, numbered B101-B108. They are arranged in quadrants (Q1=B101+B102; Q2=B103+B104; Q3=B105+B106; Q4=B107+B108). Each quadrant contains 16 Baseline Board pairs (BlB-pair), and each pair correlates all baselines for a sub-band polarization pair. Nominally each quadrant is assigned to correlation of an I/F pair, however, because of cross-bar switching in the Station racks, assignment of BlB-pairs to sub-bands and I/Fs is flexible.

C – These gauges indicate rack fan RPM, for the selected rack (S001 in the case of Figure 5-5).

D – These up and down arrows and accompanying numerical displays allow setting of fan speeds in each rack (all fans in a rack are set to the same speed, enforced by the design of the RPMIB). There are 32 fan speed steps, however, air movement in the HVAC system will normally not allow the fans to be stopped, so this is only a rough setting/indication of RPM. Fan speed control is normally automatically performed by the CPCC, with signaling via a resistor-to-opto-coupler DAC configuration on the RPMIB.

E – This array of check boxes and LEDs allows for manual power on/off control of each board, and a reading as to whether all the board's power supplies are good, all via the RPMIB board mounted at the back of the rack. "Top" 0-7 is for the 8 slots in the top crate of the rack. "6U" 0-7 is for the 8 slots in the center 6U-height crate of the rack (containing XBBs in Station racks, but empty in Baseline racks); 8-9 are spare control and monitor points and are not wired to 6U slots. "Bottom" 0-7 is for the 8 slots in the bottom crate of the rack.

There are also additional Spare monitor points (0-5), and control points (0-3, as well as 2 relays-SSR1 and SSR2—broken out on an RPMIB terminal block). In Station racks S001 and S002, some I/Os are used for monitoring and controlling the HVAC and smoke detectors. Refer to section 6.1 for these assignments. RPMIBs are identical in Station racks and Baseline racks, although usage of some I/Os are different.

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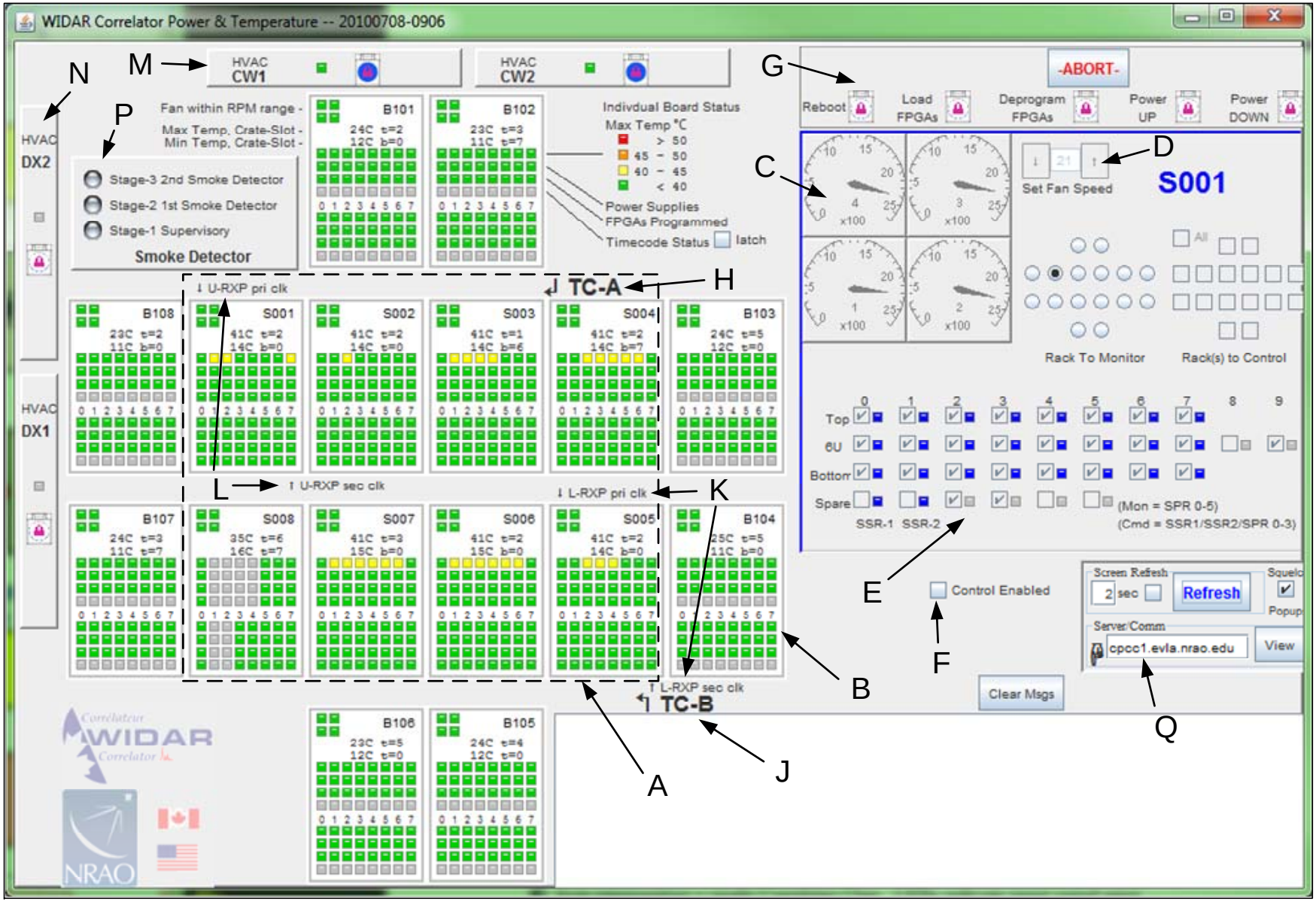

Figure 5-5 Top-level CPCC GUI. This GUI reflects the basic rack layout in the correlator room as well.

B. Carlson, August 25, 2011

	Antenna I/Fs (refer to Figure 5-6)			
Antenna	**A0, A1, C1**	**B0, B1, D1**	**C0, A2, C2**	**D0, B2, D2**
ea01	S001-t-0	S001-b-0	S001-t-4	S001-b-4
ea02	S001-t-1	S001-b-1	S001-t-5	S001-b-5
ea03	S001-t-2	S001-b-2	S001-t-6	S001-b-6
ea04	S001-t-3	S001-b-3	S001-t-7	S001-b-7
ea05	S002-t-0	S002-b-0	S002-t-4	S002-b-4
ea06	S002-t-1	S002-b-1	S002-t-5	S002-b-5
ea07	S002-t-2	S002-b-2	S002-t-6	S002-b-6
ea08	S002-t-3	S002-b-3	S002-t-7	S002-b-7
ea09	S003-t-0	S003-b-0	S003-t-4	S003-b-4
ea10	S003-t-1	S003-b-1	S003-t-5	S003-b-5
ea11	S003-t-2	S003-b-2	S003-t-6	S003-b-6
ea12	S003-t-3	S003-b-3	S003-t-7	S003-b-7
ea13	S004-t-0	S004-b-0	S004-t-4	S004-b-4
ea14	S004-t-1	S004-b-1	S004-t-5	S004-b-5
ea15	S004-t-2	S004-b-2	S004-t-6	S004-b-6
ea16	S004-t-3	S004-b-3	S004-t-7	S004-b-7
ea17	S005-t-0	S005-b-0	S005-t-4	S005-b-4
ea18	S005-t-1	S005-b-1	S005-t-5	S005-b-5
ea19	S005-t-2	S005-b-2	S005-t-6	S005-b-6
ea20	S005-t-3	S005-b-3	S005-t-7	S005-b-7
ea21	S006-t-0	S006-b-0	S006-t-4	S006-b-4
ea22	S006-t-1	S006-b-1	S006-t-5	S006-b-5
ea23	S006-t-2	S006-b-2	S006-t-6	S006-b-6
ea24	S006-t-3	S006-b-3	S006-t-7	S006-b-7
ea25	S007-t-0	S007-b-0	S007-t-4	S007-b-4
ea26	S007-t-1	S007-b-1	S007-t-5	S007-b-5
ea27	S007-t-2	S007-b-2	S007-t-6	S007-b-6
ea28	S007-t-3	S007-b-3	S007-t-7	S007-b-7
ea29*	S008-t-0	S008-b-0	S008-t-4	S008-b-4
ea30*	S008-t-1	S008-b-1	S008-t-5	S008-b-5
ea31*	S008-t-2	S008-b-2	S008-t-6	S008-b-6
ea32*	S008-t-3	S008-b-3	S008-t-7	S008-b-7

Table 5-1 Antenna to Station Board input mapping.

F – This "Control Enabled" box, if checked, enables the GUI user to affect any of the controls available via this GUI. Checking this box requires knowledge of a password, and so it is reasonably protected from indiscriminate use.

G – This section contains several locked switches which allow a qualified user, if the "Control Enabled" box is checked on, to power up or down the correlator, deprogram FPGAs, load FPGAs, or reboot all boards in the system.

H – This text indicates the entry port for the external EVLA system-provided "Timecode-A" signal. More precisely, Timecode-A includes a 0 dBm (-6 to +9 dBm) 128 MHz clock, locked to the system H-maser fed into the "128 MHz In" SMA connector of Station rack S004, slot 0 XBB (S004-x-0), and an "ext-TC" fiber signal, fed into the fiber port of the same board. Timecode-A propagates to the rest of the racks in a counter-clockwise (looking at Figure 5-5, and refer to Figure 5-14) daisy-chain fashion, entering and exiting each of the other racks' slot-0 XBB's Timecode wafer input and output. Each slot-0 board then distributes Timecode-A to all the Station Boards in its rack in a similar daisy-chain fashion (see Figure 5-15).

If the SMA-input 128 MHz clock disappears, no output clock is generated from this board for Timecode-A. The ripple effect of this is two-fold:

1. The immediate downstream XBB (S003-slot-0) will lose its wafer clock input, causing it to select the SMA-IN clock source as a backup, and to generate errored Timecodes (i.e. st-TCs on its wafer outputs with the CRC code inverted) to indicate a problem to downstream hardware. This is why, for slots 0 (and 7) XBBs in every rack[5], an SMA-out to SMA-in short-loop cable is required to provide this backup clock source[6].

2. Any subsequent XBB in the daisy-chain, receiving errored Timecodes on its wafer input, and with no active fiber input, will generate its own locally-sourced errored Timecode.

3. Any Station Boards in this rack which use "Timecode-A" as their clock source will completely lose it, immediately causing them to select "Timecode-B" as their st-TC and 128 MHz clock source, thereby providing a backup.

Thus, if "Timecode-B" (ext-TC fiber and 128 MHz SMA) is still ok it will allow the correlator to run, as Station Boards receiving an errored Timecode (A), will switch to B.

[5] In every rack, because if at any point the Timecode wafer input clock gets interrupted, the SMA-out-to-SMA-in clock provides backup.

[6] Not the designer's choice to do this, but necessary due to FPGA clock source selection and routing limitations.

Note that this new Timecode's tick relative to the tick coming from the antenna, may have shifted in time, and this could cause the fringe peak (delay residual) to have changed by the same amount. To factor out this effect, Station Board CMIB software must know/save the antenna tick to Timecode tick delay during a sky calibration run, and take compensatory action on the Station Board if the Timecode source changes, and the antenna tick-to-Timecode tick delay has changed.

In the case where both A and B external 128 MHz clocks are lost, all racks and boards still have a clock, although they are not synchronized to array timing, and Station Boards will all receive errored Timecodes. In this case S004 will get its clock and errored Timecode (B) daisy-chained sourcing back to S006, and S005 will get its clock and errored Timecode (A) daisy-chained sourcing back to S003.

Keeping clocks active in a synchronous system is important so as not to induce a major power step function, although such a step function is unlikely to be damaging given transient protection provided on each board. Nevertheless, it is generally something to be avoided if possible.

J – This text indicates the entry port for the external EVLA system-provided "Timecode-B" signal. It is a hot-redundant Timecode signal backup and distributes to the correlator in a similar fashion as Timecode-A, except operating in a clock-wise fashion, into and out of slot-7 XBBs.

By distributing Timecodes redundantly in different directions, it makes the system immune[7] to the failure of a single Timecode source, board, or Station rack[8].

K – This text indicates the 128 MHz clock source for the Lower RXP input FPGA on every odd-slot Baseline Board in the system (even-slot Baseline Boards have their Upper RXP clocks ultimately sourced from here as well). The primary clock source is S005-t-0 (Station rack S005, top crate, slot 0), and the secondary clock source is S005-b-7, thus providing fault-tolerant redundancy.

Clocks exiting these Station Boards (i.e. S005-t-0, S005-b-7) enter wafer-0 and wafer-15 inputs of every XBB in Station rack S005; the XBBs are built to automatically switch clock sources if one of the clocks on these wafers which is currently being selected disappears.

When a new clock source is selected, there will be a hiccup[9] in the clock going to Baseline Board Lower RXPs, momentarily throwing all receivers out of sync, and

[7] i.e. provided correct handling by Station Board hardware and software is in place.

[8] Not quite true regarding Station racks, as S001 and S005 provide essential clocks needed by downstream Baseline Boards. If either one of these racks completely loses power, the entire system is effectively unusable. More redundancy is not possible because of clock selection/routing restrictions in the Baseline Board RXP FPGAs.

interrupting clocks to the rest of the board. It can take up to 5 minutes to recover from this hiccup. Once a new clock source has been selected, switching to a new clock source does not occur unless the currently selected source disappears. This avoids unnecessary clock source switching, but does mean that the exact source of the clock (i.e. whether from S005-t-0 or S005-b-7) is indeterminate at any given time.

If both clock sources are inactive, the XBBs generate output 128 MHz clocks derived from their own 128 MHz LO as keep-alive clocks, however, no signal synchronization is possible in this state. Once either a wafer-0 or a wafer-15 input clock comes alive, it is selected, and signal synchronization will be possible.

L – This text indicates the 128 MHz clock source for the Upper RXP input FPGA on every odd-slot Baseline Board in the system (even-slot Baseline Boards have their Lower RXP clock ultimately sourced from here). The description is identical to that for item K.

Note: within a Station rack, top crate-slot-0 (which feeds wafer-0 input of each XBB) is fed "Timecode-A" and its clock comes directly from a XBB, whereas, bottom-slot-7 (which feeds wafer-15 input of each XBB) is fed "Timecode-A" indirectly through a daisy-chain of all Station Boards in a crate, but is fed directly from "Timecode-B". There is no real consequence of this, but could explain oddities depending on which boards in a Station rack fail or lose power.

M – These two boxes are for HVAC CW1 and CW2 status and control. CW1 and CW2 (chilled water 1 and 2) units form the primary cooling system for the correlator room. The status LEDs are GREEN if there is NO ALARM condition, RED if there is an ALARM condition, and GREY if powered off. The status LED does not actually indicate everything is "OK", just alarm and power status. Each CW unit can be powered off or on through these buttons (right-click opens a little door, and left click switches its state[10]). When a CW unit is powered off, its blowers stop. Normally, the CPCC controls these units automatically. Refer to section 6.1.2 for information on how CW unit status signals are wired into the correlator and communicated to the CPCCs.

N – These two boxes are for HVAC DX1 and DX2 status and control. DX1 and DX2 are "direct exchange" HVAC units with their own compressors, and provide secondary cooling for the room. The function and operation of the LEDs and power control switches is identical to the CW units above.

P – This box contains smoke detector status indicators. "Stage-1 Supervisory" is triggered in the alarm monitoring system itself such as alarm box doors open. It is also

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[9] In spite of somewhat Herculean efforts in the design phase, it was not possible to provide a seamless clock switchover.

[10] Kevin Ryan and his "GUI games".

triggered by the super-sensitive smoke "sniffer" system in the room. "Stage-2 1st Smoke Detector" is triggered when smoke is detected in a single zone of the room. "Stage-3 2nd Smoke Detector" is triggered when smoke is detected in a second zone of the room. Stage-1 and Stage-2 result in alerts to the operator, but if Stage-3 is triggered, the CPCC immediately commences a staged shutdown of the correlator, to be completed within ~60 seconds, at which point all power to the room is removed. Refer to section 6.1.1 for information on how smoke detector signals are wired into the correlator, and communicated to the CPCCs.

Q – This box indicates the network name of the CPCC computer which is providing data for the GUI display. Valid names are "cpcc1.evla.nrao.edu" and "cpcc2.evla.nrao.edu".

The -48 VDC power plant is not shown in this GUI. It operates autonomously, and will respond accordingly to loss of AC power etc. Any control of the power plant must be done within the correlator room via the power plant control panel, except that if power to the room is purposefully cut by hitting an emergency red mushroom switch, it causes an immediate battery disconnect and power plant shutdown so that all -48 VDC lines to the correlator racks are de-energized. The CPCC monitors only the AC fail condition of the power plant, communicated to the CPCC via a 10Base-T Ethernet connection to the EVLA network (as shown in Figure 4-1), and takes appropriate action as described in section 7.1. The CPCC does not control the power plant.

5.4 Signal Flow

To understand the operation of the correlator system in more detail, it is useful to understand basic signal flow from entry via the FORM/DTS receiver modules embedded in Station Boards, to the CBE, through to output of the CBE and on to the Lustre file system. Much of this is covered in detail in other User Manuals or RFS documents, so this description is a simplified overview only.

5.4.1 Antenna I/F to Station Board Mapping

A simplified diagram showing antenna signal to sampler and I/F assignment mapping is shown in Figure 5-6. This diagram, coupled with Table 5-1 indicates exactly which signals route into which Station Boards from which antennas.

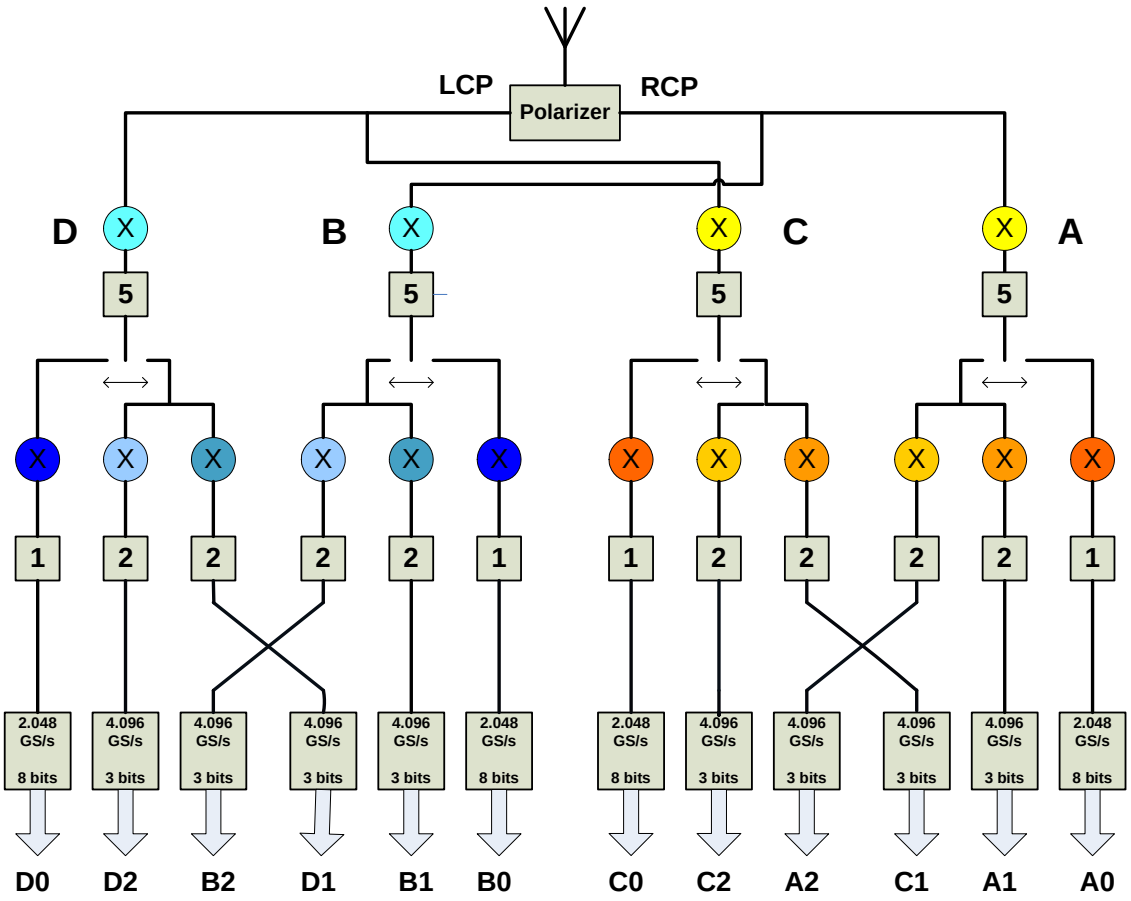

Figure 5-6 Simplified EVLA antenna I/F block diagram (Perley) for I/Fs A, B, C, and D. Identical colours signify identical tunings.

There are 3 fiber inputs to each FORM board, accessed via the front panel of the Station Board. These 3 fiber inputs are labeled "A", "B", and "C" (or in long form "**FORM OPT IN A**" etc.). A, B, and C inputs have no direct mapping to I/F labels.

5.4.2 Station Board to Baseline Board Signal Flow

The FORM mezzanine card embedded in each Station Board decodes the fiber signals, and presents the resulting sample and bit-aligned signals in parallel electrical form to the Station Board via the mezzanine card connector. Digital signals travel and are processed through the Station Board and exit as a number of delay-corrected and filtered digital sub-bands, which route to Station-rack mounted XBBs via a cable-interconnect matrix, which is identically wired in each Station rack.

Outputs of XBBs then route to peripherally-location Baseline Boards in Baseline racks in a point-to-point star configuration, such that each (odd-slot) Baseline Board receives data from all antennas for a single sub-band polarization pair. This sub-band can source from any filter on Station Boards (via the Station Board's "Output Chip" cross-bar switch), and from any antenna I/F pair via a combination of Station Board to XBB cabling and the XBB's switching capabilities.

A simplified diagram of astronomical signal flow is shown in Figure 5-7.

In Figure 5-7, "**StB**" is a Station Board, "**DM**" is a Delay Module (for wideband delay tracking to +/-0.5 samples of delay), "**FB**" is a filter bank comprised of 18 digital Filter Chips, and "**BlB**" is a Baseline Board. Quadrant and rack assignments are as indicated. In each Station rack there are 8 XBBs, each one consisting of two independent cross-bar switches—each implemented in an FPGA, with each switch handling one sub-band pair (refer to Figure 5-18 for sub-band number assignments to XBB switches).

A diagram which illustrates most of the system's primary cross-bar switching capabilities is shown in Figure 5-8. In the diagram, "planes" are nodes (lowest to highest in the diagram: StB filter outputs, StB Output Chip outputs, XBB outputs), and the space between planes is where cross-bar switching occurs.

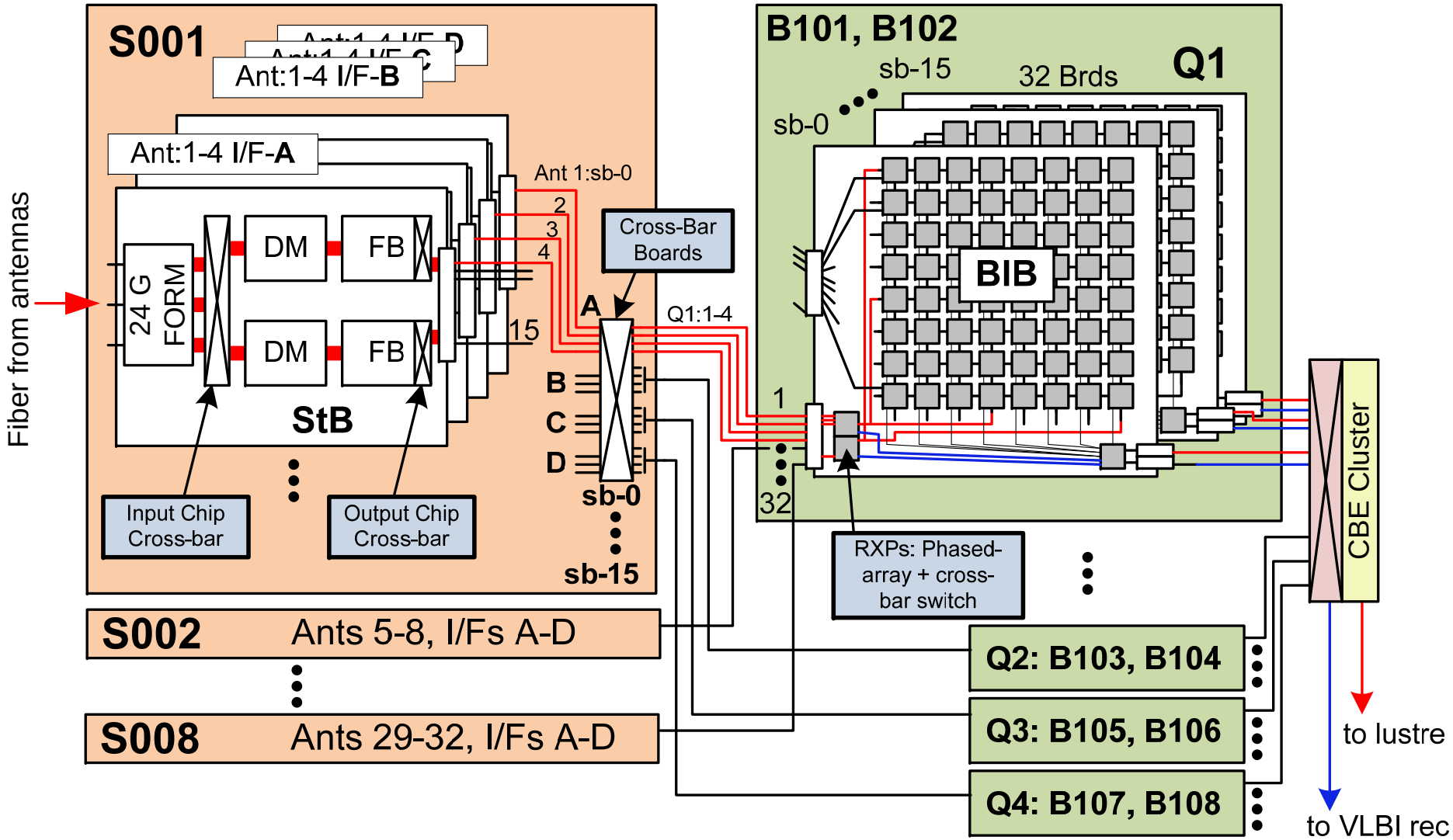

Figure 5-7 Simplified astronomical signal flow (RED) through boards in the system. I/Fs "A, B, C, D" are short-form for the actual I/F nomenclature listed in Table 5-1 and shown in Figure 5-6. DM=Delay Module; FB=FilterBank. Antennas, Station rack numbers, Baseline rack numbers, and Quadrants are shown.

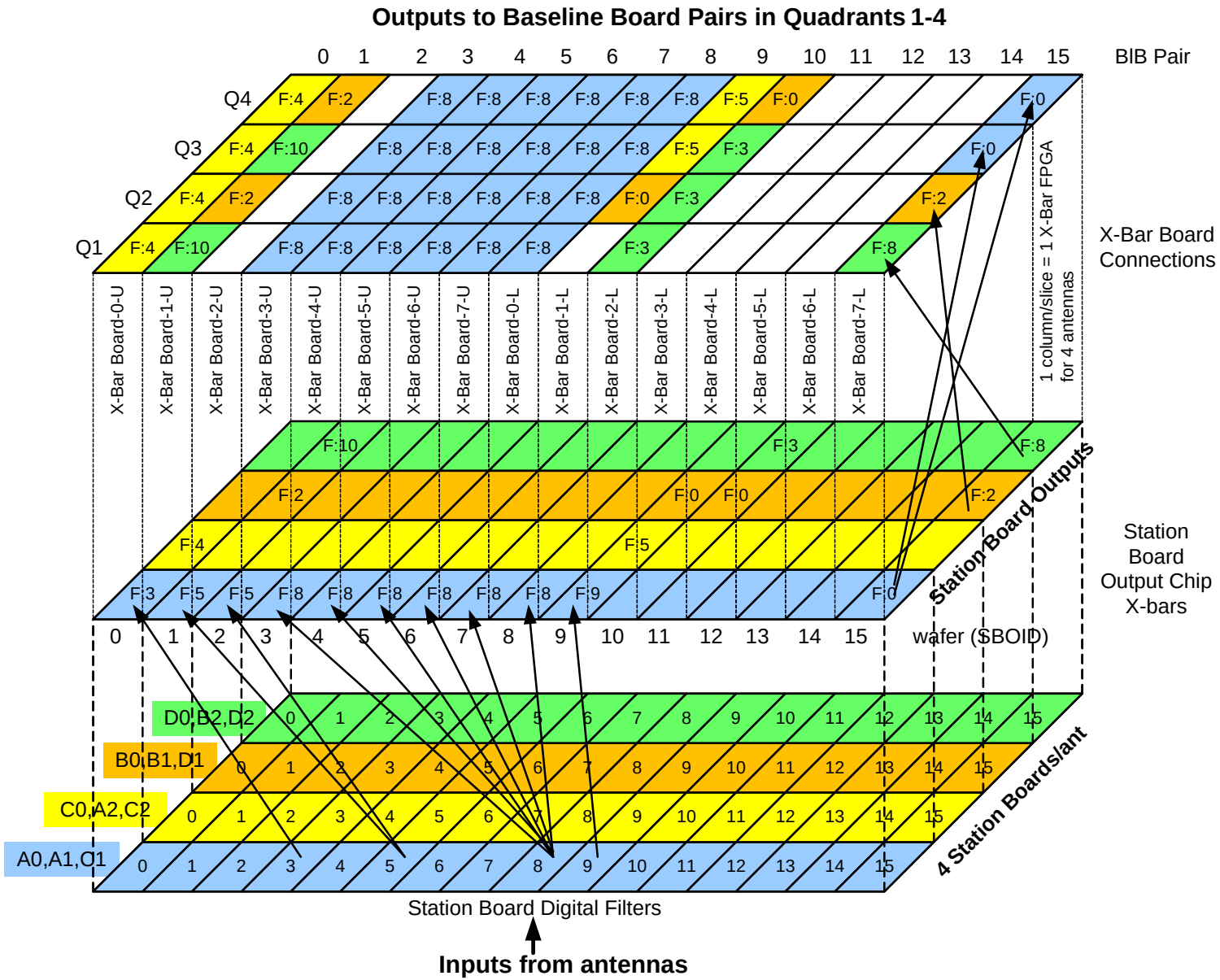

Figure 5-8 Matrix indicating Station Board filter output to XBB output switching capability. The diagram shows example connectivity.

5.4.3 Cross-Bar Board GUI Description

A Cross-Bar Board GUI, shown in Figure 5-9, has been developed which allows a user to see and optionally set (although normally settings are under automatic program control via the Configuration Mapper in the MCCC) distributed XBB configurations in an intuitive manner, closely following the matrix diagram of Figure 5-8 (the specific switch settings in the two figures are different, but I/F colour assignments are matched).

The GUI also indirectly shows Station Board Output Chip settings—see description for "E". This GUI is accessed via the link "Cross-Bar Board GUI" at the asg/widar web site at "http://www.aoc.nrao.edu/asg/widar/"

The XBB GUI is shown below, with a brief description of key parts following.

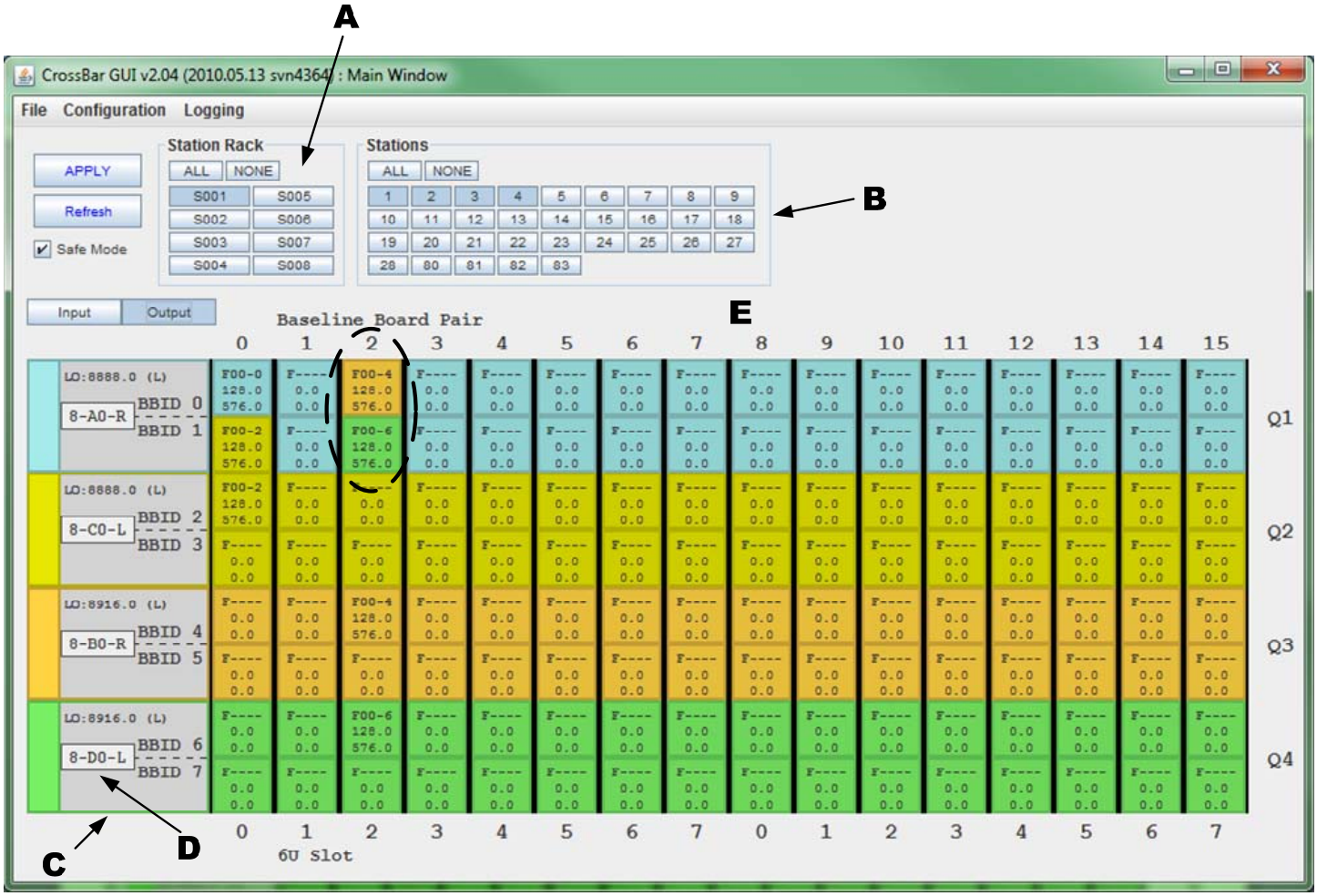

Figure 5-9 Top-level Cross-Bar Board (XBB) GUI.

A – This box allows the user to select for which Station racks to display settings. **B** shows which stations/antennas (referring to Table 5-1) are currently selected, and it is always the case that **A** and **B** are in sync. This feature allows the GUI to show

configurations for individual sub-arrays, provided the user knows which antennas comprise which sub-arrays. (A future enhancement is to allow selection of one or more sub-arrays in the same manner.)

B – Shows which particular stations/antennas are selected, and in-sync with A at all times. Also, individual stations/antennas can be more finely selected here than in A.

C – This box indicates the four antenna I/Fs. Each I/F is marked with a different colour, and when the "Output" button is selected, it quickly allows the user to see which quadrants are processing which I/Fs. Within this box, the "**BBID**s" are the "BaseBand IDs" assigned and embedded in DATA streams travelling to Baseline Boards. This box also indicates the net LO (Local Oscillator) or sky frequency used by the antennas at the current time. In the example, the LOs are tuned to X-band (~8 GHz).

D – Within each I/F colour, this box quickly allows the user to see exactly what signal is being fed to the Station Board. In the example GUI, "**8-D0-L**" indicates **8**-bit initial sampling, "**D0**" sampler (see Figure 5-6), and **L**eft-hand circular polarization. It should be noted that in 8-bit sampling mode, only one wideband sampled data stream (polarization) is fed to each Station Board—a rule imposed by the antenna electronics configuration, not by the correlator.

E – This matrix represents the 64 Baseline Board Pairs ("BlB-P") contained within the 4 quadrants of the correlator, and the assignment of each pair to an I/F and a sub-band. In the circled example of the figure (Baseline Board Pair 2, Q1), the BlB-P is correlating data from I/F **B0** and **D0** (8916.0 MHz, L and R), using digital filter[11] "F00" (assigned/from BBIDs 4 and 6) on the associated Station Boards. The sub-band bandwidth is given, and is 128.0 MHz, with a center frequency within the 0-1024 MHz baseband sampled signal of 576.0 MHz.

Double-clicking on a column within this matrix opens up a more detailed, lower-level GUI, which shows connectivity (and allows connectivity to be established) through the XBBs, shown in Figure 5-10. To establish a connection, left-click-hold on a box to the left, and drag it to the right. If any part of the BlB-P matrix (Figure 5-9 or Figure 5-10) is highlighted RED, it indicates that for at least one selected antenna, there is different XBB connectivity than other selected antennas, which may or may not indicate a problem depending on sub-arrays and current desired correlator configuration.

Note that XBBs do not themselves contain any controlling networked CPUs. ***XBB connections are established by writing XML to appropriate Station Boards, and the Station Boards in turn send commands to downstream XBBs using the HM Gbps COMMAND protocol embedded in the wafer CTRL stream.*** *For a particular XBB,*

[11] Which digital filter is used is determined by the Output Chip cross-bar setting.

COMMANDs coming in on any input wafer (i.e. from every Station Board in the rack), can establish any switch connection. Refer to section 7.3 for more information on the mechanism for configuring XBB switch configurations. A consequence of this is that the XBB GUI only learns about XBB connections by knowing how IDs are set in Station Boards, and reading Baseline Board RXP-received IDs.

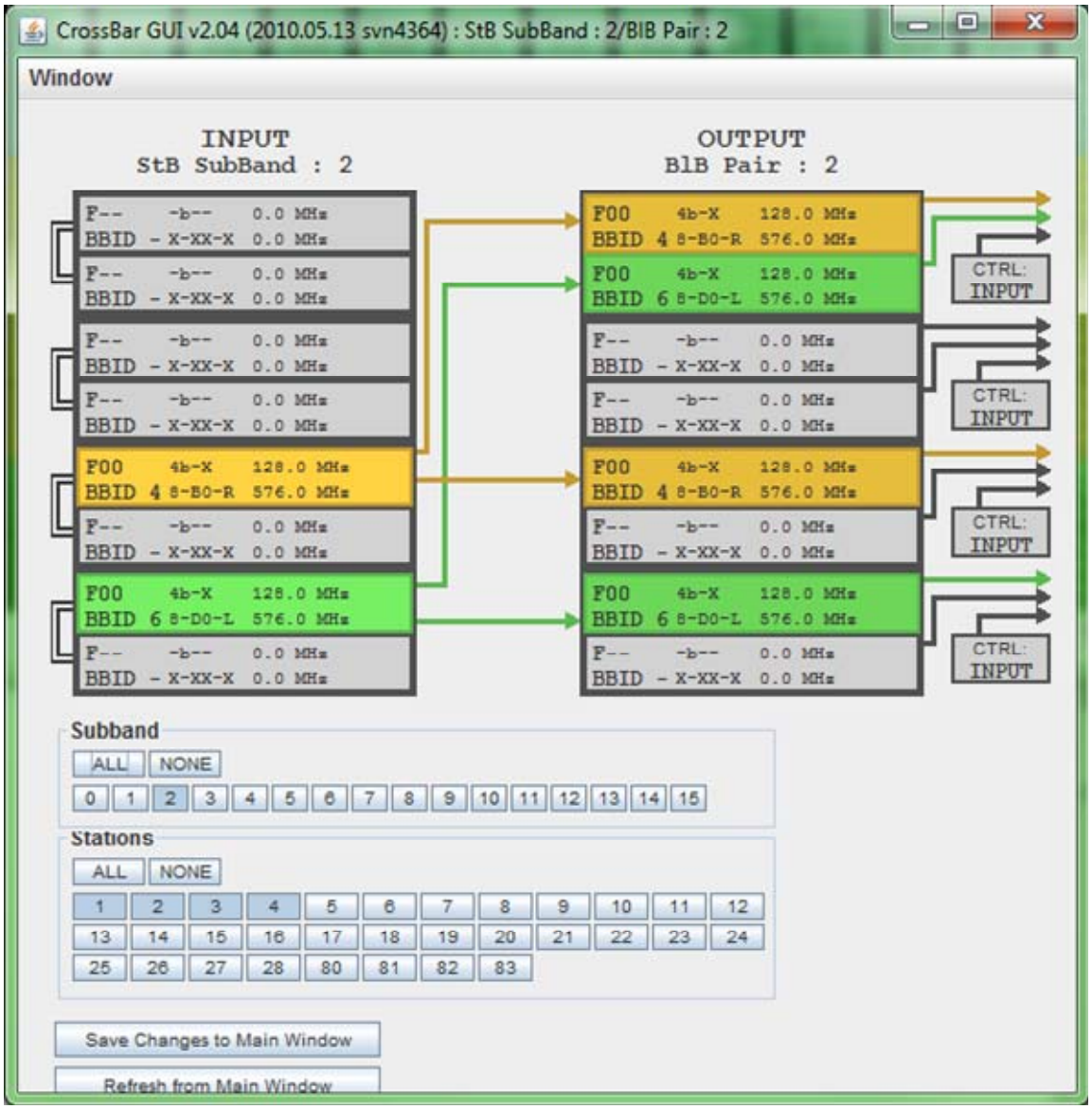

Figure 5-10 Sub-band specific XBBs' detailed connectivity GUI opened via the XBB-GUI.

5.4.4 Cross-Bar Board Switching Limitations and Rules.

The XBB is a circuit-switched device, rather than a packet switched device. This sometimes causes problems as some of the signaling in the HM Gbps protocol is quasi-packetized in nature. To handle these conditions, the following rules apply when establishing XBB connections (refer to section 5.6 for more information on HM Gbps protocol):

- DATA streams are the primary circuit switched elements.
- When a DATA stream switch path is set, the corresponding PHASERR signal (embedded in the CTRL stream in the same incoming wafer), is switched with it, and properly embedded in the outgoing CTRL stream's PHASERR channel on the output wafer. Sometimes this means that the PHASERR channel, w.r.t. TIMECODE, is sooner or later than it originally was on the input to the board.
- When a DATA stream's switch path is set, the corresponding PHASEMOD signal, embedded in the associated incoming CTRL stream, is switched as well, and *merged* with any other switched DATA stream's PHASEMOD signal embedded in the outgoing CTRL stream. This leaves open the possibility of PHASEMOD packet collisions, and so the Configuration Mapper in the MCCC tells each Station Board to generate PHASEMOD "early" or "late", so as to avoid this collision.
- DUMPTRIG is not switched with DATA stream switching. There is an explicit COMMAND required to switch the CTRL stream, and when this is done, DUMPTRIG is switched (PHASEMOD and PHASERR switching are not affected and always follow the above rules; TIMECODE is switched, but is the same everywhere) to the selected output wafer.
- DATA stream switch changes occur in the CRC-4 calculation dead time, and so do not generate downstream CRC errors. However, CTRL stream switch configuration changes occur right away, and so there is some probability of a TIMECODE or DUMPTRIG CRC error being generated, if the switch occurs in the middle of a frame.
- The incoming COMMAND stream does not get transferred to the output CTRL stream.
- The XBB generates output STATUS packets, so that downstream RXPs can detect XBB front-panel LED status.

Since XBB switch settings cannot be directly determined, DATA path connections are indirectly determined by knowing how the embedded IDs are set at the transmit end (Station Board Output Chips), and reading these at the receive end (Baseline Board RXP FPGAs).

5.4.5 DUMPTRIG Source ID

For DUMPTRIG, a mechanism[12] is provided to insert a source ID at the transmit end, to be read at the final destination (Recirculation FPGA on the Baseline Board) receive end. This mechanism is such that when the DUMPTRIG command is "RRC" (110), the 16-bit PB field in the DUMPTRIG frame contains the source identifier. In this case, PB[7:0] is the antenna/station ID (SID), PB[15:13] is the source baseband ID, and PB[12:8] is the source DUMPTRIG ID (there are 16 DUMPTRIG generators on each Station Board, and

[12] Albeit at kludge added after the fact, as the system, and software "knowledge" requirements changed.

the DUMPTRIG ID indicates which one generated the signal). RRC DUMPTRIG frames have no other effect when not in recirculation mode, and when in recirculation mode, they are generated on a regular basis for proper recirculation operation, with the PB field still free for DUMPTRIG ID use.

5.5 Timecode Content and Distribution

"Timecode" is the general term for a time reference signal distributed throughout the system. Each board gets a Timecode signal, and uses it as a foundational reference for all synchronization and processing.

Timecode is a digital signal, and is distributed throughout the system at a clock rate of 128 MHz, and with an accompanying 128 MHz synchronous clock. It contains a 1 Hz and in one case a 100 Hz time tick. Low-level hardware operations synchronize or operate on a precise clock edge, and higher-level software operations (such as CPU interrupt service routines or tasks) synchronize to a 10 millisecond interval or 1 second interval as required.

"Timecode" is the general term for this signal, but it has different forms in the system. These forms, in the direction of signal flow, are as follows:

- **ext-TC** – This designation specifically refers to the externally-provide Timecode signal consisting of a 1 Hz time tick, a 6-bit count incremented on each time tick, and a CRC-4 check code. The entrance of this signal into the system is indicated in the upper left of Figure 4-1. The signal enters specific XBBs (Figure 5-14), and thereafter propagates as the "st-TC" variant. "ext-TC-A" and "ext-TC-B" have identical content, and are inserted into the system for fault-tolerant redundancy. The phase of the ext-TC signal relative to the accompanying 128 MHz clock is unknown, but must be stable (the XBB has a mechanism for settling on a "good" clock phase). The ext-TC frame is shown in Figure 5-11. Refer to [A25022N0090] for more information.

- **st-TC** – This designation specifically refers to the Timecode signal distributed by select XBBs and Station Boards, in a daisy-chain fashion, to all Station Boards in the system. It has the same reference timing content as ext-TC, but contains an additional "hop count", which is incremented on each repeat of the signal. The hop count allows the Station Boards to compensate for repeater (hop) delays, such that the Timecode signal (more precisely, "TIMECODE") exiting Station Boards and destined for Baseline Boards are roughly synchronized in time. The st-TC frame is shown in Figure 5-12. Refer to [A25022N0043] for more information.

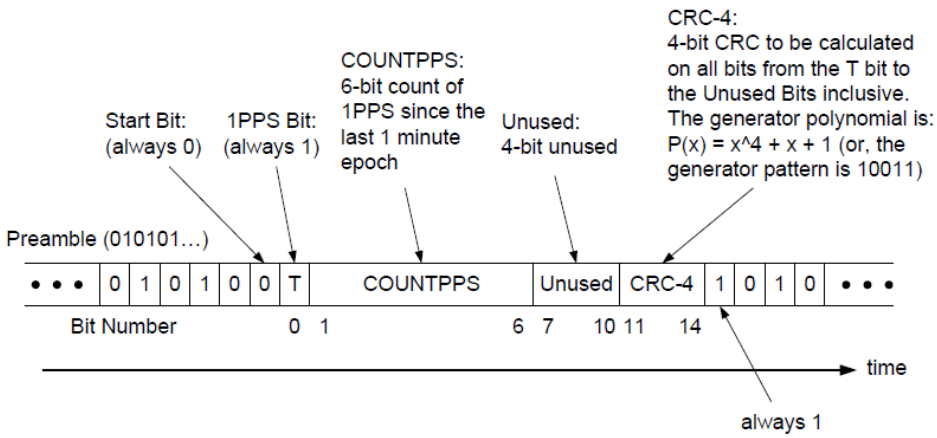

Figure 5-11 The "ext-TC" frame, sourcing from the external EVLA system.

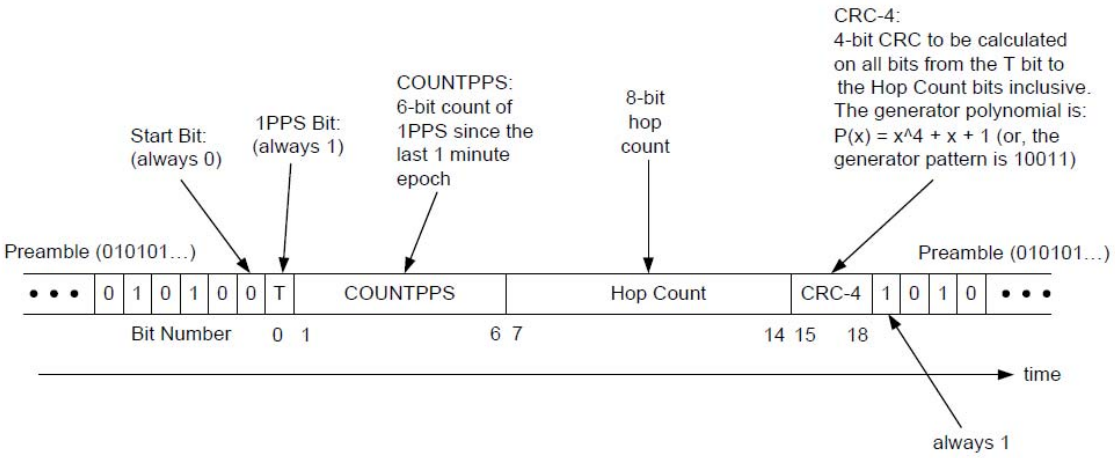

Figure 5-12 The "st-TC" frame, generated and distributed by Cross-Bar Boards and Station Boards.

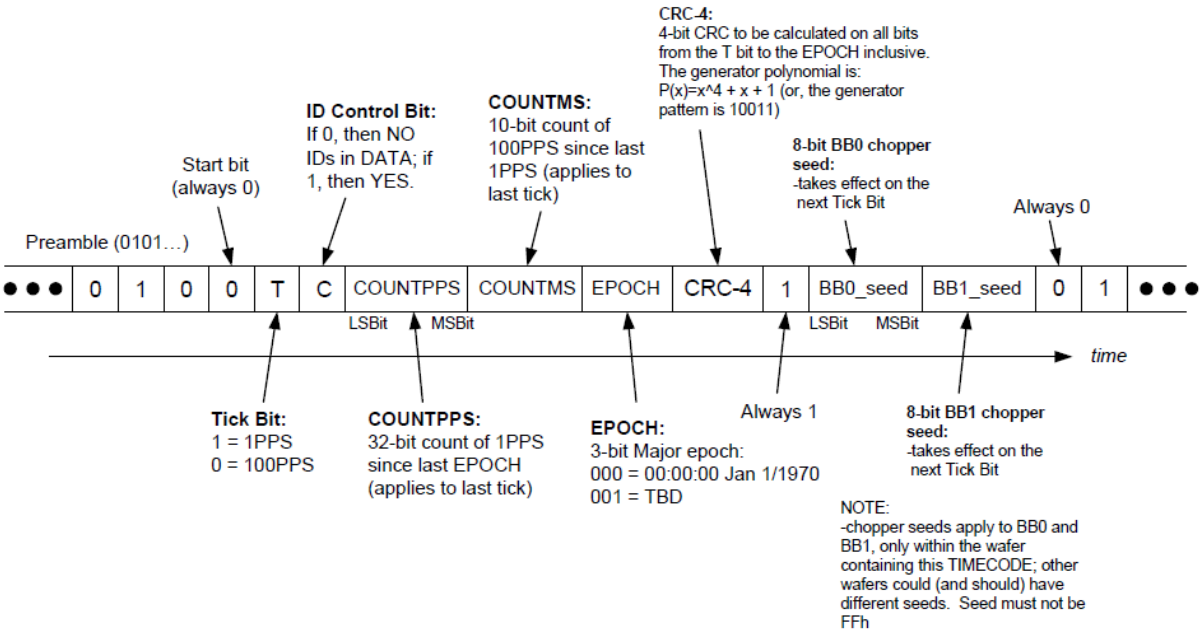

Figure 5-13 TIMECODE frame, generated by Station Boards and flowing to Baseline Boards via Cross-Bar Boards.

- **TIMECODE** – Each Station Board selects and decodes one of the incoming st-TC (-A OR -B) signals, and generates the TIMECODE signal destined for Baseline Boards. This Timecode variant contains an encoded version of the actual observation time, such that the Baseline Board can use it directly to timestamp output correlated and phased (summed-array) data. The observation time is set in software, and synchronized to the 1 second counter in st-TC, sourcing from ext-TC.

  This Timecode signal contains a 1 Hz and a 100 Hz tick, and all other signaling flowing from Station Boards is synchronized to it. If some hiccup occurs which causes a sustained shift or error in the tick position, then all associated receivers will lose synchronization, and will have to go through a re-synchronization process. The TIMECODE frame is shown in Figure 5-13 and described in detail in [A25022N0041]. TIMECODE also contains "chopper" seed numbers, used in the "HM Gbps" protocol to randomize DATA streams such that bit transition density is always sufficient for receivers to maintain lock. Refer to [A25022N0041] for chopper implementation details.

Note that due to the fact that ext-TC (and subsequently st-TC) are roughly coincident with the antenna 1 PPS signal, and the fact that the antenna signal goes through a large delay buffer on the Station Board (the Delay Module memory, with depth ~0.25 sec), the Station Board output TIMECODE signal is delayed by ~0.125 sec w.r.t. st-TC so as to roughly center the Delay Module buffer. Refer to [A25040N0001] and [A25290N0000] for further details, on how this is set and used.

5.5.1 ext-TC Insertion and st-TC Signal Distribution

As previously mentioned, the st-TC Timecode signal is distributed to Station Boards in a fault-tolerant redundant daisy-chain fashion. Distribution is accomplished by a combination of XBBs (known as "Function-1" capability in the XBB User Manual) and Station Boards. XBBs distribute st-TC to other racks and to upper and lower crates (sub-racks) within a rack. Station Boards distribute it to each other in a bi-directional daisy-chained fashion within a particular crate.

Figure 5-14 shows the entry points and routing of the ext-TC-A and B signals. Note that the first time the signal is repeated by a XBB, it is converted to st-TC with a hop count of 0. Subsequent repeats increment the hop count by 1 each time. Slot numbers in the figure are XBB slots.

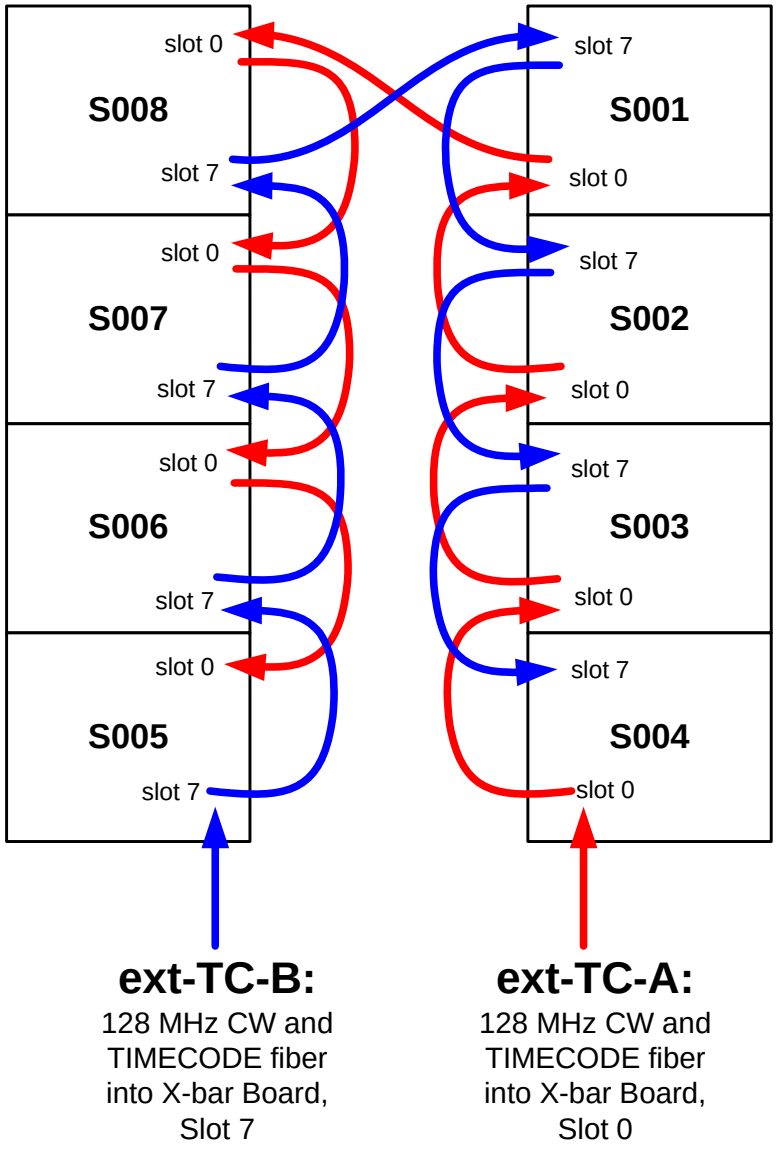

Figure 5-14 ext-TC-A and B entry points and distribution in the correlator.

Figure 5-15 shows st-TC distribution within a particular Station rack [A25005N0004], as seen looking into the back of the rack.

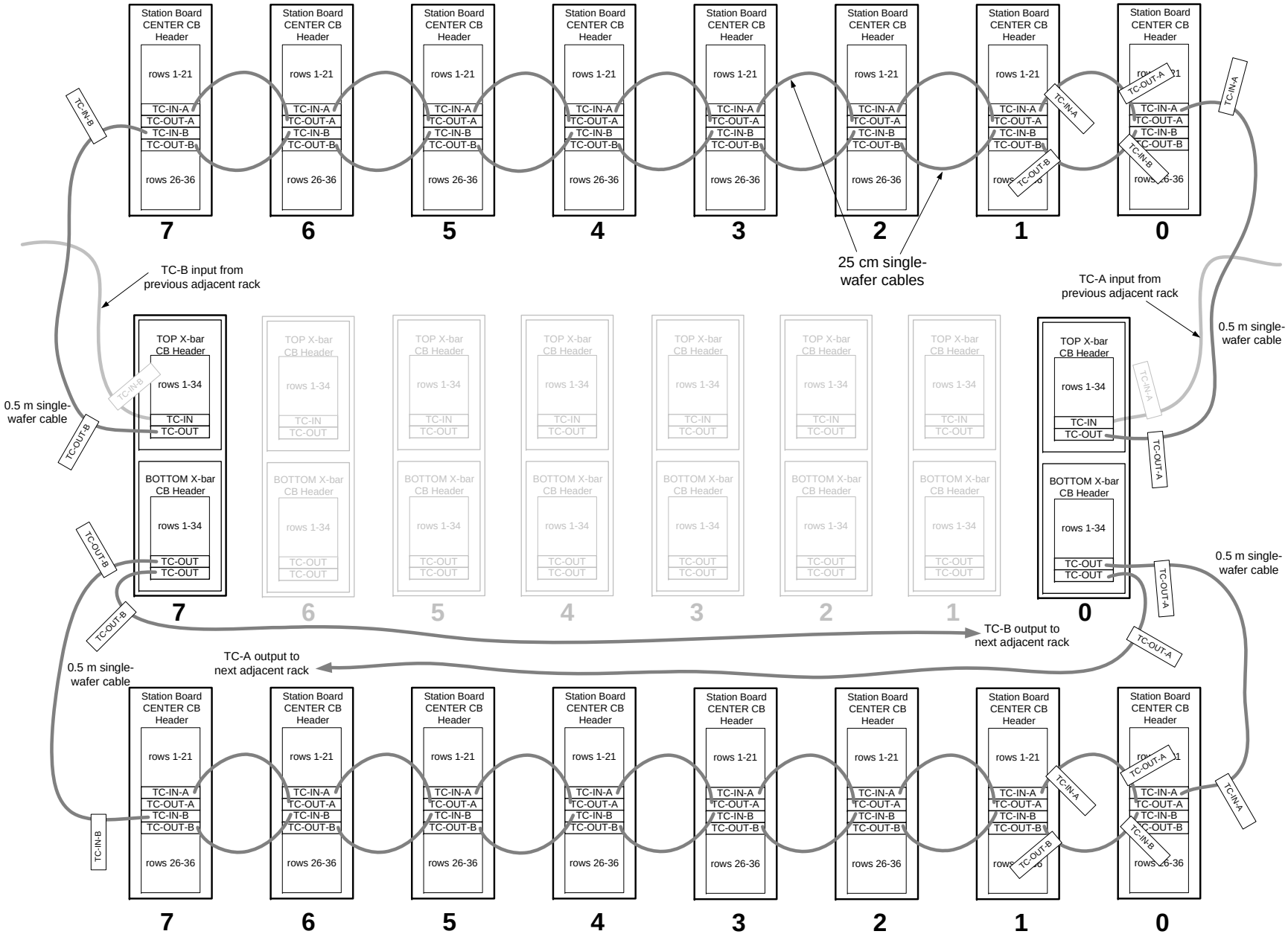

Figure 5-15 st-TC cabling connections within each Station rack.

B. Carlson, August 25, 2011

In Figure 5-15, the large numbers indicate slot numbers, and the diagram, from top to bottom indicates the top crate of Station Boards, the middle ("6U") crate of XBBs, and the bottom crate of Station Boards. Specific board header rows used for Timecode for Station Boards and XBBs are defined in sections 6.6.5 and 6.7.2 (also shown in Figure 5-18). Note that only XBBs in slots 0 and 7 participate in this process.

Refer to [A25005N0004] for the complete Timecode distribution cable installation plan.

5.5.2 st-TC Hop Count Delay Compensation

Each st-TC "hop", whether in an XBB or a Station Board, incurs on average ~135 nsec of delay (including some allocation for cable delay). Thus, the delay in the Station Board "Timing Chip" FPGA [A25052N0000], which determines the input "st-TC" tick to output "TIMECODE" tick delay *portion due to hop count*, must be set for:

*StB_TC_delay ~= (worst_case_hop_count – hop_count) * 17.2*

Where, "*17.2*" is ~135 nsec (minimum 133 nsec, maximum 136.3 nsec) expressed in 128 MHz clock cycles, and the *worst_case_hop_count* is some number which is greater than any *hop_count* in the system.

Thus, the StBs with the lowest *hop_count* will have their Timing Chips set to have the greatest delay, allowing ticks exiting all StBs across the system to be roughly matched. As the worst-case XBB-to-BlB cable delay differential in the system is ~2 m (12 nsec), and the cumulative *hop_count* uncertainty (because a hop delay is not precisely defined) is ~53 nsec (16 hops x 3.3 nsec), the BlB RXP buffers' capability of +/-125 nsec is more than capable of handling this residual delay uncertainty, with plenty of headroom.

5.6 Inter-Correlator Signaling and Synchronization—the "HM Gbps" Protocol and "wafers"

As depicted in Figure 4-1, the "**HM Gbps**" (Hard Metric Giga bit per second) protocol [A25022N0041] is used for data transport and signaling from Station racks to Baseline racks. This protocol is, more precisely, used on all paths from Station Board outputs to Recirculation FPGA inputs on Baseline Boards.

The HM Gbps protocol is a custom-defined protocol built for source-synchronous clocking using 1 Gbps transceiver technology. In source-synchronous clocking, a (low) frequency-synchronous clock is sent along with but separate from the data signal such that a CDR (Clock Data-Recovery) receiver is not required. This technology (for the vintage of the time, ~Y2005) allows a much higher density of transceivers—and therefore I/O bandwidth—to be used on a chip than CDR-SERDES transceivers, and is the enabling technology for data transport in the correlator. The receivers contain DPA (Dynamic Phase Alignment[13]) hard logic, which automatically aligns the 128 MHz

[13] An Altera FPGA term and implementation.

reference clock (multiplied up to 1024 MHz) with the incoming signal, and presents the 1:8 byte-wide[14] de-serialized signal, at 128 MHz, to the FPGA fabric for bit/byte and embedded code alignment/sync.

HM Gbps signaling and data transport within the correlator is defined within the granularity of a "wafer". A wafer is defined as 4 differential pairs of wires contained within a single "2 mm Hardmetric" 2 mm x ~17 mm connector or cable header. Wafer headers and cables are manufactured by Meritec, and the pin header is manufactured by ERNI (ERNI type F and E, part numbers 933142 and 933141). In this protocol a wafer contains the following signals:

- A 128 MHz clock, frequency synchronous and stable w.r.t. the associated DATA and CTRL streams. For hardware efficiency, not all wafers contain this clock—refer to Figure 5-18 and Figure 5-24 for connector diagrams of StBs, XBBs, and BlBs indicating which wafers do and do not have this clock, and which wafer inputs require a clock.

- A 1 Gbps CTRL ("control") pair, which contains several multiplexed signaling channels: TIMECODE, DUMPTRIG, PHASEMOD, PHASERR, COMMAND, STATUS. TIMECODE (Figure 5-13) forms the primary reference tick against which DATA stream synchronization occurs. DUMPTRIG contains real-time correlator dump control signaling, flexible enough to allow for the plethora of dump modes possible limited only by software algorithms. PHASEMOD contains 32-bit phase synthesizer coefficients updated as much as every 10 milliseconds. PHASERR contains real-time phase coefficients required for sub-sample delay tracking (see Figure 5-4). COMMAND contains XBB switch setting commands (section 5.4 of [A25022N0041], and section 5.2.2 of [A25121N0001]). Finally, STATUS contains XBB front-panel LED status sent continuously from XBBs to BlBs.

- Dual 1 Gbps DATA streams, referred to as "BB0" (sourcing from Station Board Data Path 0) and "BB1" (sourcing from Station Board Data Path 1). Each stream can contain 4-bit sampled data up to 256 Msamples/sec, or 7-bit sampled data up to 128 Msamples/sec; the protocol defines precise rules for each of these sample word sizes and data rates. Each DATA stream contains embedded IDs (SID, BBID, SBID) and a CRC-4 check code, to allow downstream receivers to achieve and maintain signal lock. The DATA stream protocol is shown in Figure 5-16:

[14] The DATA streams are defined as 4-bits wide at 256 MHz, and so further FPGA-fabric multiplexing is performed to get the byte-wide signal into this form.

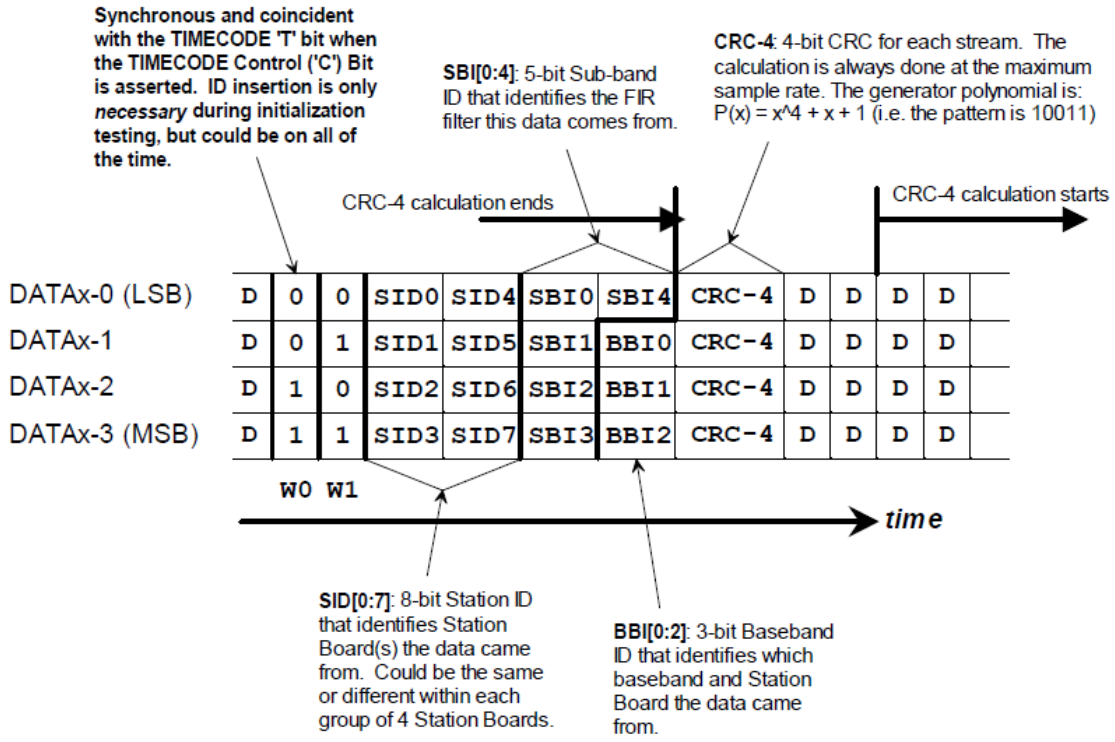

Figure 5-16 HM Gbps DATA stream protocol.

In general, receivers go through the following procedures when acquiring HM Gbps signal lock/synchronization:

1. Lock to the TIMECODE signal. Lock is achieved when enough error-free TIMECODE signals (Figure 5-13) are detected, usually taking less than 1 second. The TIMECODE T-bit is then the reference against which DATA streams are synchronized. Once TIMECODE lock is established, generally all other CTRL streams are acquired and error-free, although signaling-specific receivers do report errors detected in any of these. If the position of the TIMECODE T-bit w.r.t. the DATA stream changes, for whatever reason, the receiver will immediately lose DATA sync.

2. Lock to the DATA signals. Receiver circuitry must search in bit/byte alignment, and also in position (+/-4 256 MHz clock cycles) relative to the TIMECODE T-bit. This can take quite some time; up to a few minutes depending on the conditions under which the receiver lost lock. The FPGA hard-logic DPA receivers are not perfectly autonomous, and can get into a "flutter" condition where lock is achieved, but errors are being detected at a low level (few per minute), requiring a DPA receiver hard-logic reset, and corresponding signal sync search, increasing the signal lock time.

After the receivers, the synchronized signals go through a FIFO buffer, independently written for each wafer, and then synchronously read from all buffers for all wafers such that all wafer's signals are now lined up to a single TIMECODE T-bit. Thus, if the

TIMECODE T-bits from some wafers are delayed or advanced more than the buffer depth (+/-32 256 MHz clock cycles— +/-125 nsec), there will be hiccups on the output of the buffer for the offending signal, and downstream receivers will not be able to achieve signal lock on this hiccupped signal.

5.6.1 Additional RXP and XBB Synchronization Issues

The HM Gbps receiver and synchronization sections of the Cross-Bar Board (XBB) and RXP FPGA on the Baseline Board are essentially the same. Each individual wafer input has a receiver which establishes synchronization/lock to the TIMECODE and DATA signals, and then all same-wafer signals pass through a 64-deep FIFO buffer, clocked at 256 MHz, whose write address for each wafer is independently driven by its *own* TIMECODE, but whose read address is common to all other wafers. The common read address is developed, using *one* of the wafers' TIMECODE signals as the reference. By doing this, all of the signals on the output of the FIFO buffers will be aligned in time and to one TIMECODE reference, it is then possible to perform cross-bar switching (and in the RXP, phased-array summing) and eventual multiplexing to 1.024 Gbps for transmission to the next step of processing.

Logic in the XBB and RXP FPGAs selects one of 4 wafers as the potential TIMECODE reference, and does it in an iterative majority fashion. That is, it uses one TIMECODE as a reference, and checks to see if the majority of the TIMECODE ticks coming out of the FIFO are synchronized; if not, it chooses another TIMECODE as a reference, etc.

In the XBB, if a reference tick can be found, but the outputs of the FIFO buffers for one or more wafers are not synchronized, the front-panel LEDs for the offending wafers will be GREEN but quickly flashing RED, and no downstream receivers will synchronize on these wafers. This is indicative of the Station Board TIMECODE output ticks being out of skew, and the remedy is proper use and compensation for the hop count, as noted in section 5.5.2

For the XBB, wafer inputs 0, 4, 8, and 12 (for either the top or bottom connector—each connector routes to its own FPGA) are the potential TIMECODE references the FPGA has to choose from, and so if there isn't a good TIMECODE on at least one of these inputs, no signals from any wafers will get through the chip to the output.

For the Upper RXP FPGA on the Baseline Board, these special wafer inputs are 0, 4, 8, and 12, and for the Lower RXP FPGA, these special wafer inputs are 16, 20, 24, and 28 (these possible reference ticks are indicated by asterisks (*) in the RXP GUI). As both FPGAs exchange data, and route signals to the X and Y Recirculation FPGAs, at least one of these select inputs must have a good TIMECODE on both Upper and Lower RXPs for proper synchronization and operation.

Additionally, as noted in section 5.3, bullets K and L, XBB wafer inputs 0 and 15 (both connectors, each to its respective FPGA) are the primary and secondary clock inputs. One of these input clocks must be present for the XBB FPGA to function and produce good output. Cascading from this is the fact that for every odd-slot Baseline Board in the

system, the Upper RXP FPGA, wafer 0 is the master reference clock input, and for the Lower RXP FPGA, wafer 16 is the master reference clock input.

What this means for the system is that if:

S001-t-0(FAIL) AND S001-b-7(FAIL) OR S005-t-0(FAIL) AND S005-b-7(FAIL)

is TRUE, all Baseline Boards in the system will not be operational.

The implemented mechanism provides fault-tolerant operation, however it does not mean that any arbitrary collection of Station Boards can be down, and the system will still function. A way around this is to feed a separate but phase-stable 128 MHz clock to every Baseline Board via the external clock connector, but this clock source ultimately has a single source and is therefore itself not fault tolerant.

Full details of the HM Gbps protocol can be found in [A25022N0041]. Further details on receiver behavior can be found in XBB [A25121N0001], RXP [A25093N0000], and Recirc FPGA [A25090N0000] User Manuals and RFS documents.

5.7 Intra-Correlator HM Gbps Cabling

There are two main sections of cabling in the correlator. The first section is within each Station rack, and connects Station Board outputs to Cross-Bar Board (XBB) inputs. Cabling in this section provides in itself signal grouping such that each cross-bar switch of an XBB, handles one sub-band, from all I/Fs, from all 4 antennas in the rack. Cabling within each rack for this section is identical.

The second section of cabling is point-to-point between Station racks and Baseline racks, and connects XBB outputs to Baseline Board inputs. This is a star configuration of 512 quad-wafer cables, running 8 quad-wafer cables from each Station rack to each Baseline rack.

For all of these interfaces, the following rules are followed:

- PCB-mount 100 nF DC-blocking capacitors are in-line with signal pairs at the **transmit** end.
- The receive end re-establishes proper DC bias into the receiver with a resistor.

5.7.1 Station Board to Cross-Bar Board Intra-Rack Cabling

The Station rack cable installation plan [A25005N0003], contains detailed wiring diagrams for the entire intra-Station rack cabling installation. One example, showing the installation of 4 cables installed for sub-band 0, is shown in Figure 5-17. From this figure it is clear that sub-band 0 wafer output from *each* Station Board in the rack routes into a single Cross-Bar Board cross-bar switch (each switch, implemented in an FPGA, is accessed via a separate cable header at the rear of the board).

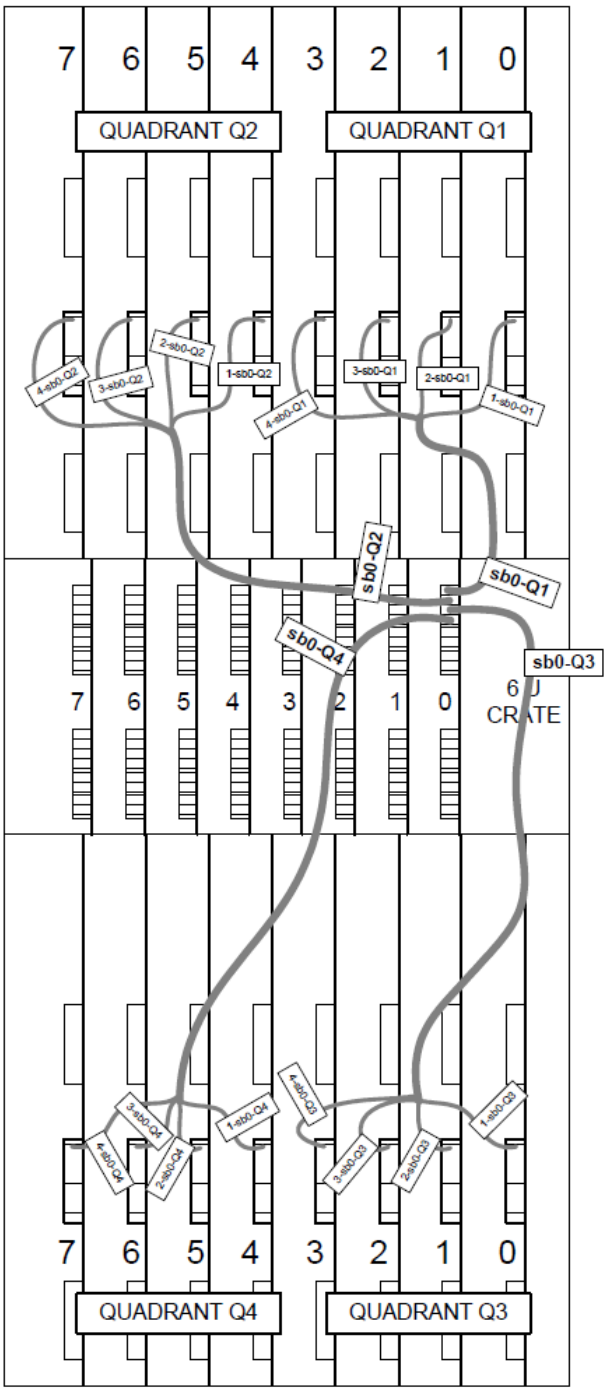

Figure 5-17 Portion of intra-Station rack cabling plan, for sub-band 0 cable routing. Quadrant numbers indicate which Station Board slots are for each I/F, which if routed straight-through the XBBs, map to Baseline Board quadrants.

A better overall concept of this section of cable routing within a Station rack is shown in Figure 5-18. This figure does not show actual cables being routed (as it quickly becomes too complicated in a single diagram), but does show cable header pin assignments, cable header source and destination assignments, and sub-band number assignments to Cross-

Bar Board cable headers. This figure is printed on a decal, and pasted to the inside back door of each Station rack.

All of these intra-rack cables are 1 m in length, and there are 64 in each Station rack, leading to a very "busy" cable layout. Figure 5-19 shows cable entry into Cross-Bar Board headers. Figure 5-20 shows both intra-rack (grey) and inter-rack (black) cables in the back of a Station rack.

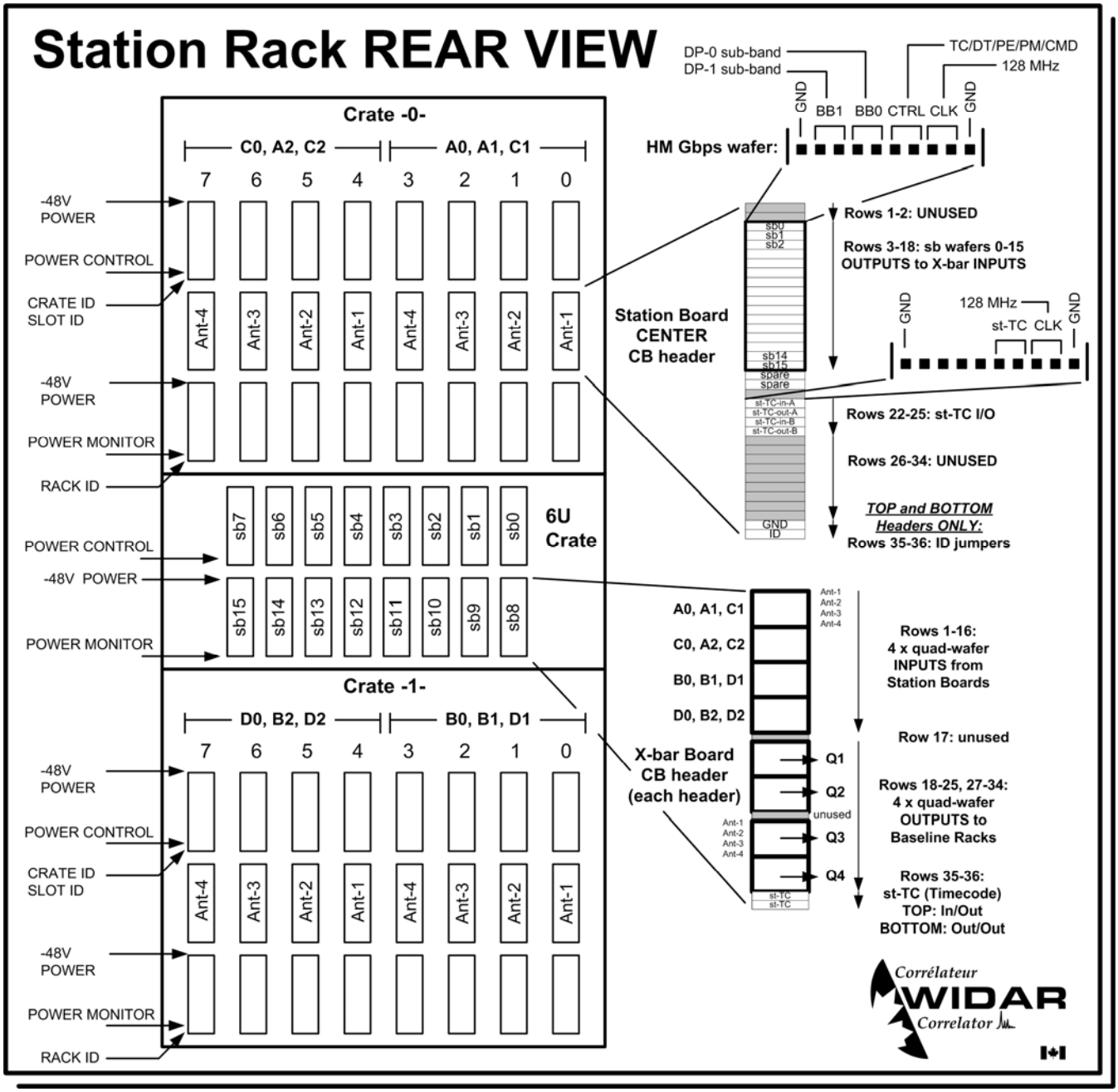

Figure 5-18 Station rack decal, showing cable header pin assignments, sources, destinations, and XBB sub-band cable header assignments. This decal is pasted on the back inside door of each Station rack. Note that every Station Board center ERNI connector wafer output contains a 128 MHz clock, however for XBB outputs, only every other wafer (explicitly, rows 18, 20, 22, 24, and 27, 29, 31, 33) contains a 128 MHz clock.

Figure 5-19 View looking into the back of a Station rack showing intra-rack Meritec cabling entering the top Cross-Bar Board cable headers. Cables are held in place with standard ERNI plastic latches, but additional custom-built padded-metal strain-relief is provided as the ERNI header plastic is quite fragile.

Note: removal and replacement of these cables must be performed with extreme care as the ERNI connector plastic headers and ERNI latches (shown on the right side of the cable headers in the above picture) are very fragile, and cable header insertion into the connector is a tricky and precise business. Refer to section 11.2.6 for details on repair/replacement procedures.

Figure 5-20 View into the back of a Station rack showing intra-rack cabling (grey), and inter-rack (Station rack to Baseline rack) cabling (black).

5.7.2 Cross-Bar Board to Baseline Board Inter-Rack Cabling

There are 8 quad-wafer cables routing from each Station rack to *each* Baseline rack in the system. Each Baseline rack correlates 8 sub-band pairs from one I/F, and so each of these 8 cables carries one sub-band from one I/F, for all 4 antennas in a Station rack. Quadrant destinations for these cables are shown in the "X-bar Board CB Header" connector diagram, in the lower right corner of Figure 5-18. The "Station Rack-to-Baseline Rack High-Speed Cable Installation Plan" [A25005N0001] contains detailed diagrams indicating where all of the cables are installed, and exactly how cables are numbered. Furthermore, groups of 4 quad-wafer cables are bundled together, as they have the same approximate source and destination locations. Figure 5-21 is a cable layout and labeling plan for 8 such 4 quad-wafer cable bundles, sourcing from Station rack S001, and going to all 8 Baseline racks.

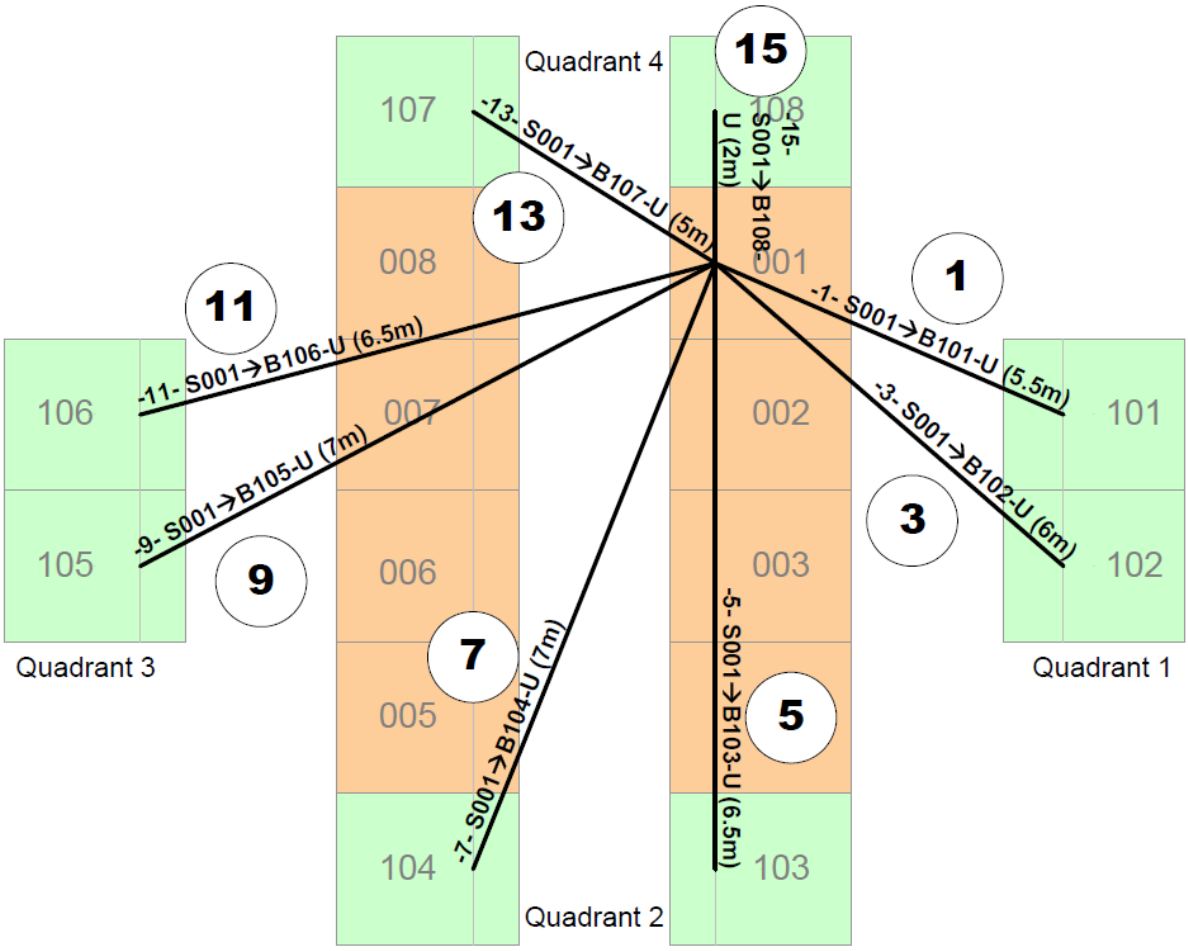

Figure 5-21 One diagram of the [A25005N0001] cable installation plan showing 8, 4 quad-wafer cable bundles, and their labelling.

The Station rack end of this cabling plan shows details on where in Cross-Bar Board headers these cables are installed. One example from the plan is shown in Figure 5-22. Figure 5-23 shows one Baseline rack-end cable installation diagram.

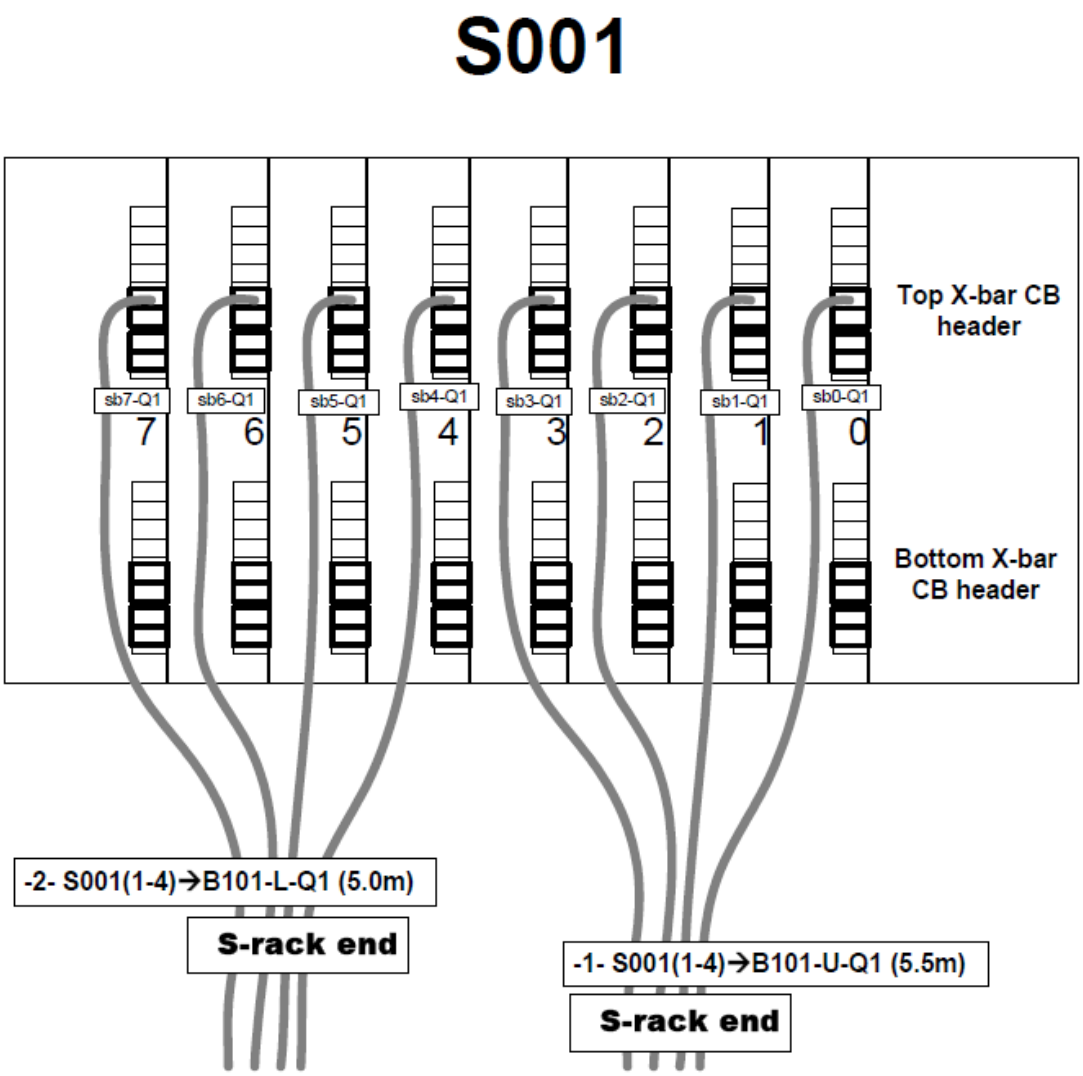

Figure 5-22 Station rack end, inter-rack cable installation plan detail, with cable labels shown.

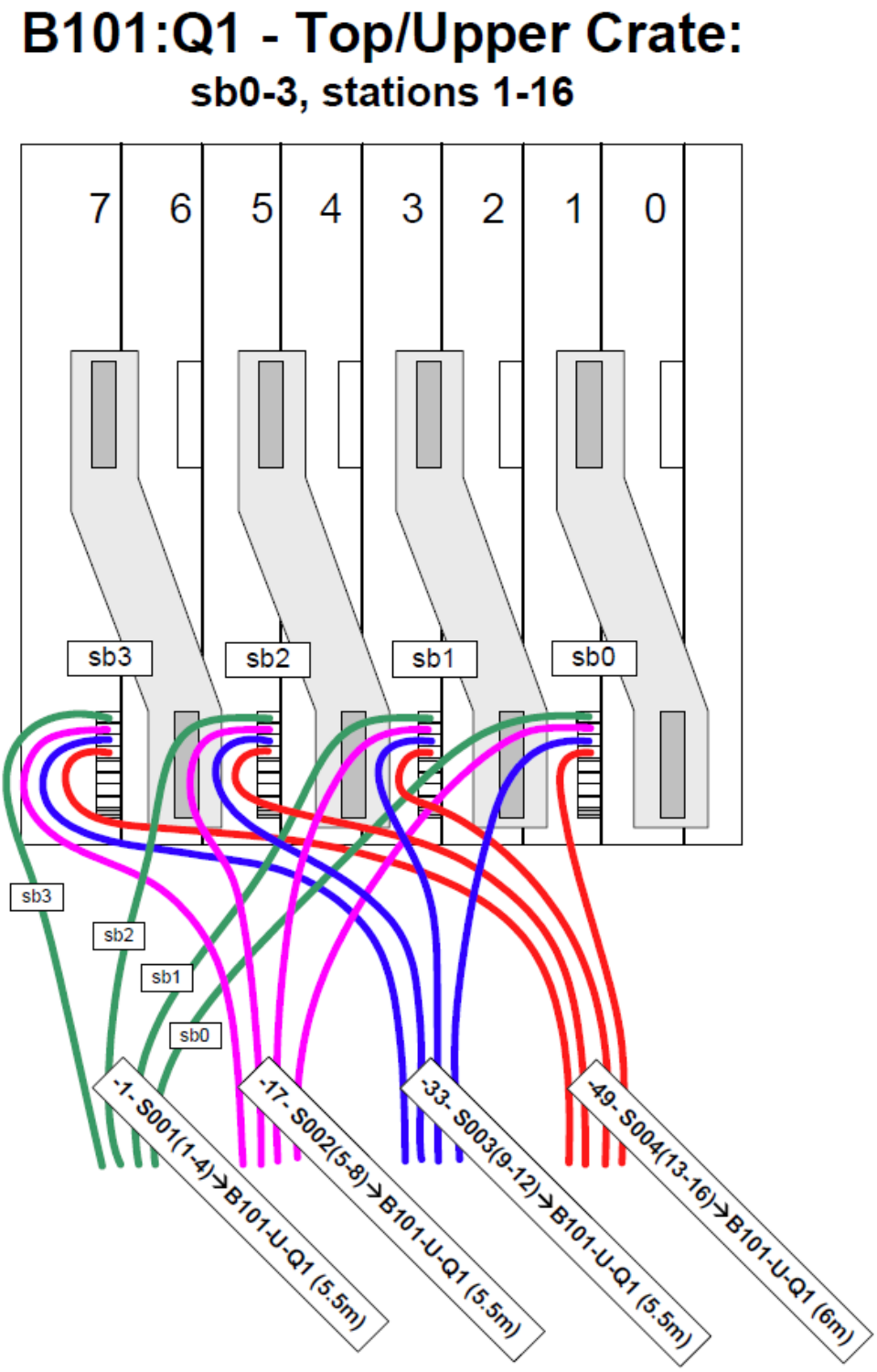

Figure 5-23 Baseline rack-end cable installation diagram, with cable labels shown. Each wire is a quad-wafer cable, and wires of the same colour are bundled together with a split cable wrap/shell as they come from the same Station rack.

Figure 5-19 shows this inter-rack cable (black) at the rear of a Station rack.

Figure 5-24 is a rear-view decal for the Baseline rack. The decal is pasted inside the back door of each rack. The decal shows wafer header row assignments and pinouts, the sub-band-to-Baseline Board pair assignment for each rack, and Patch Board locations/connections, as well as power, monitor and control, and ID settings locations.

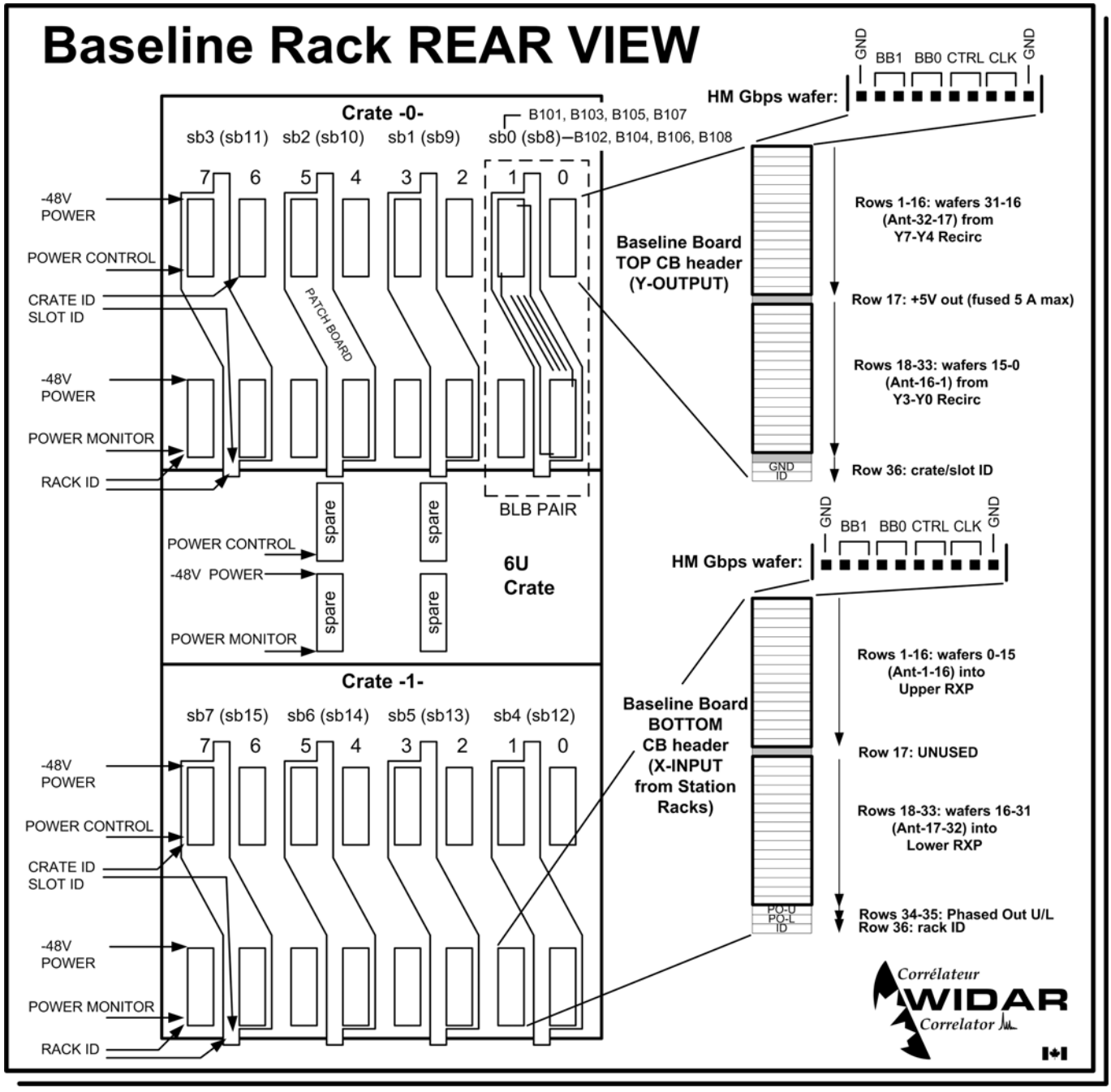

Figure 5-24 Baseline rack decal, showing cable header pin assignments and antenna sources for odd-slot lower ERNI connector inputs, and outputs for the upper ERNI connector. Note that due to Patch Board routing requirements, antennas into RXP chips on the Baseline Board are shifted and mirrored into *even* slots (i.e. Upper RXP gets antennas 32-17, Lower RXP gets antennas 16-1) This decal is pasted on the back inside door of each Baseline rack. "Phased Out U/L" are auxiliary phased-data outputs on wafers (see [A25093N0000] for details).

Figure 5-25 shows inter-rack cabling at the rear of a Baseline rack.

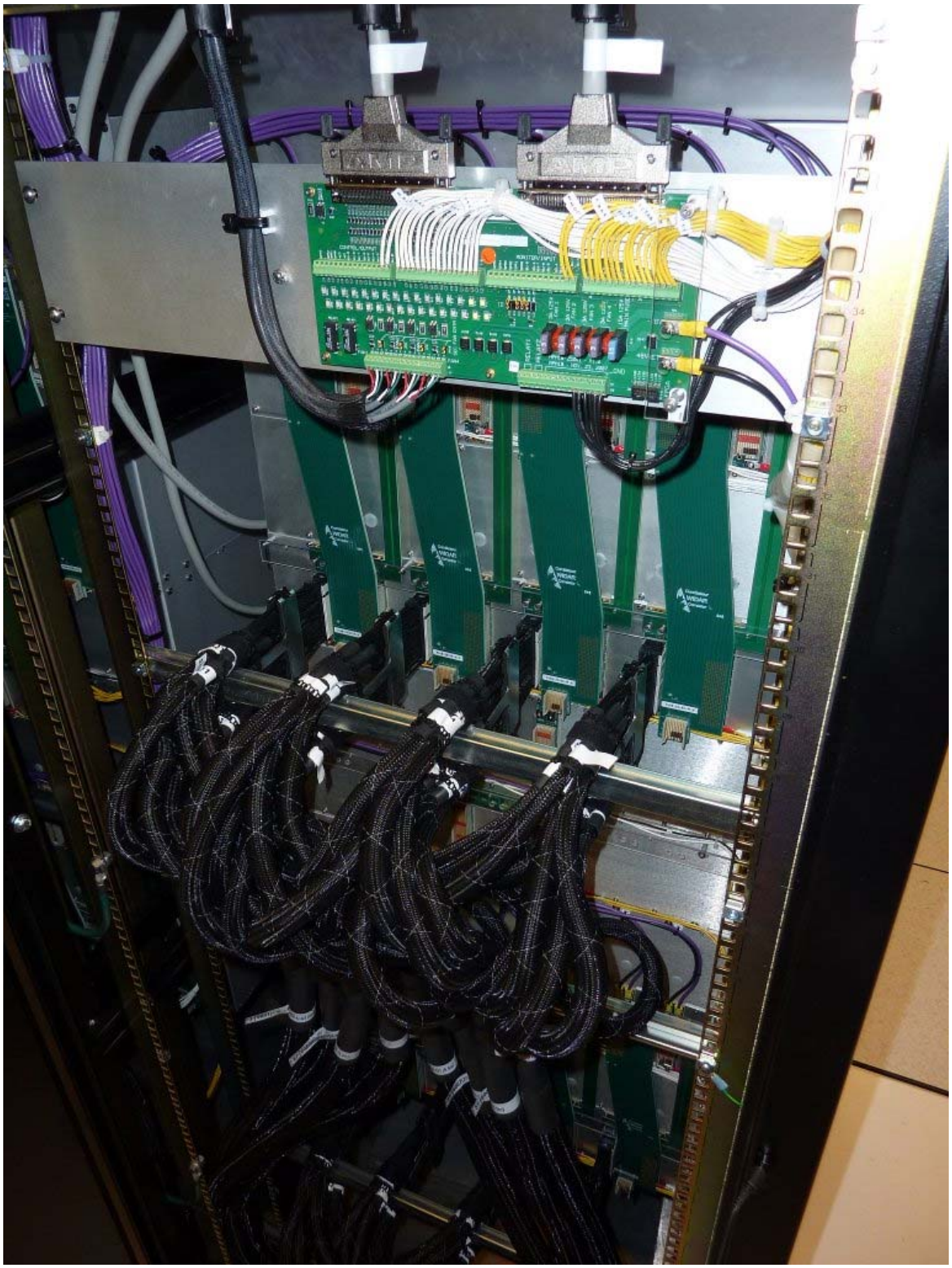

Figure 5-25 Inter-rack cabling looking into the rear of a Baseline rack. The top two (100-pin SCSI) cables/headers plugging into the RPMIB are from the redundant CPCCs, CPCC-1 and CPCC-2.

5.8 Station Rack Layout

Each Station rack in the system has an identical design. Each one consists of:

- The 24" rack frame. This is a COTS rack frame purchased from Hammond, and consisting of the frame, side panels (may or may not be installed, depending on rack location), solid rear door, smoked plexi-glass front door, and front and back adjustable vertical rails.
- Dual 12U-height 8-slot sub-racks (Top and Bottom, sometimes referred to as Upper and Lower). These sub-racks have been reinforced to handle the boards laden with heavy heatsinks.
- One 6U-height 8-slot sub-rack sandwiched between the 12U sub-racks. These are as deep as the 12U sub-racks, but with horizontal rails positioned so as to accommodate the much shallower Cross-Bar Boards.
- An airflow duct, mounted at the top of the rack, to facilitate the transition from the sub-rack "duct" geometry, to the wider quad fan tray geometry at the top of the rack.
- A fan-tray "carriage" assembly, mounted on the outside top of the rack, custom-built to facilitate hot-swapping of individual fans, each one contained within a fan housing.
- At the rear of the rack, there is a mounting plate for the RPMIB, in the upper 2/3rds of the rack.
- At the rear of the rack, the -48 VDC breaker panel.
- At the rear of the rack, DIN "U" rails mounted on vertical rack rails, and used to fasten cable holders and cable strain-relievers.

A simplified cartoon side-view of the Station rack is shown in Figure 5-26. A view looking into the rear of an actual Station rack is shown in Figure 5-19.

Sub-rack slot numbering looking into the *front* of a Station rack is 0-7 left-to-right for both the 12U and 6U sub-racks. Slot numbering looking into the rear is opposite of course, and is shown in the rear-door decal of Figure 5-18.

Rack fans are removed via the front and rear of each rack; loosen the captive spring-loaded screw, and pull on the handle. Insertion is the reverse.

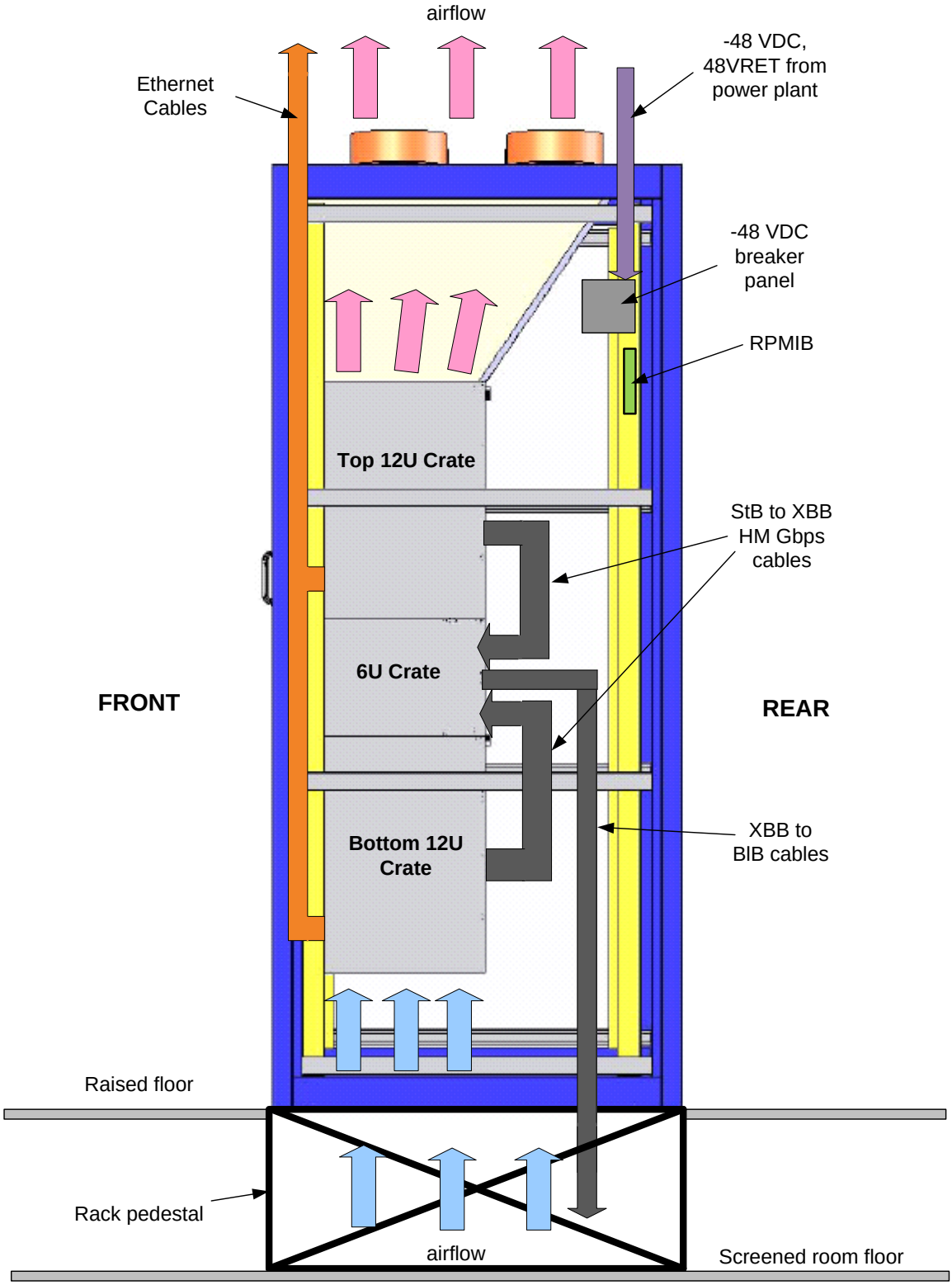

Figure 5-26 Simplified side-view of a Station rack. StB to XBB cable routing is more complex than shown; just the basic direction is indicated.

5.9 Baseline Rack Layout

Baseline rack layout is virtually identical to Station rack layout. The only difference is that the 6U sub-rack (crate) is not used in the Baseline rack (but is still present, with two slots populated with Common Backplane headers), and HM Gbps wiring enters lower-connector odd slots in the 12U sub-racks.

Refer to Figure 5-25 for a view looking into the back of a Baseline rack, and Figure 5-24 for the Baseline rack rear-door decal showing slot numbering, connector pinouts, power, and monitor and control connections.

5.10 -48 VDC Power Distribution and System Grounding

The -48 VDC power plant, located in the correlator room, supplies -48 VDC power to all correlator boards in correlator racks in the system. Correlator racks (S001-S008; B101-B108) *exclusively* use -48 VDC, and so there is no shock hazard when working in the racks[15].

Dual-circuit, two-wire -48 VDC and Return (48VR) is supplied to each rack, and both these wires are completely isolated from earth/shield room ground and signal ground. It is only at the power plant distribution panel where 48VR is connected to earth/shield room ground. This ensures deterministic high-current DC return paths.

A simplified/representative wiring diagram of the -48 VDC distribution system, from the power plant distribution panel on out, illustrating all critical protection and wiring elements, is shown in Figure 5-27. Some points to note from the figure:

- There are dual 200 A breakers for each rack, located in the power plant cabinets, with wiring to the rack, through the rack breaker panel, and on to the boards, isolated between each leg.

- The rack breaker panel is a standard household dual 200 A panel, base manufactured by Square-D, P/N: QON124L2001. Breakers are standard household 20 A, AC or DC also manufactured by Square-D, P/N QO120.

- In the diagram, PURPLE/VIOLET wiring is -48 VDC hot, and black is return. This colour convention is used throughout the correlator, except the power plant to rack 2/0 wires are black, and labelled at each end as to what they are.

- The power indicator lamps, mounted to the side of the breaker panel, are **NOT FUSED**, so as to provide a true indication that the panel is live.

[15] Although there is shorting/high current hazard, and so appropriate care and caution must be used when working inside live racks, in particular when it comes to metal jewellery, watches, screwdrivers etc. All -48 VDC and 48VR contacts in racks are covered with clear lexan shields, however, there is still a shorting hazard.

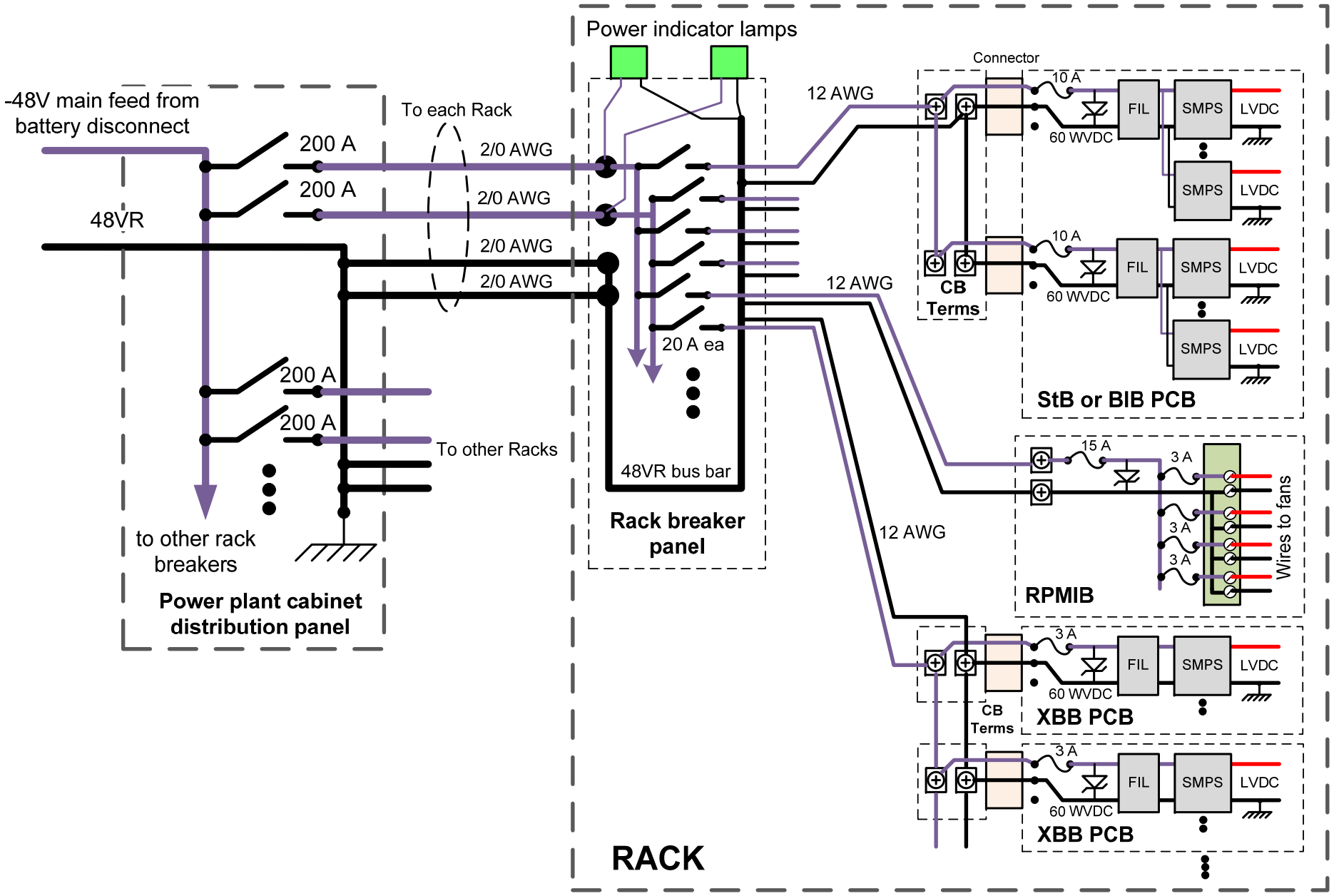

Figure 5-27 End-to-end (-48 VDC battery disconnect onward) -48 VDC power and ground connections, breakers, fusing, and transient protection.

- Fuses on StB, BlB, and XBB PCBs are solder-in, surface mount type. After the fuses, the power supplies on the board are protected with 1500 W 60 WVDC transorbs (Mfg: Bourns, P/N CD214C-T60ALF). This same transorb is used on the RPMIB. Refer to respective board User Manuals for more detailed information.

- Fuses shipped with the racks and installed in the RPMIB for fan power are not rated for 48 VDC. Fuses of that type, and that rating were virtually impossible to acquire. Nevertheless, the entire RPMIB circuit is additionally protected with a 20 A breaker in the breaker panel. The RPMIB contains a 60 WVDC transorb after the main 15 A fuse (as shown in the figure), but also the same type transorb after each individual 3 A fan fuse (not shown in the figure).

- The "FIL" elements on the StB, BlB, and XBB PCBs are active common-mode EMI filters. They are there to prevent SMPS (Switch-Mode Power Supply) common-mode conducted EMI (generated in the SMPS by switching elements coupling through leakage capacitance from the -48 VDC side to the LVDC side) from coupling into the -48 VDC system, and finding ground loops via 48VR grounding at the power plant distribution panel, into rack-to-rack communications lines.

- PCB signal ground is ultimately grounded to the screened room floor as indicated in the figure. This grounding is established through the ERNI (HM Gbps) connector grounds, to CB (Common Backplane) ground, to chassis, to rack pedestal, and finally to screened room floor. Additionally, there are ground straps connecting adjacent rack front and rear vertical rails together, and to the rack pedestal (not shown in the diagram).

- Station and Baseline Boards have dual-leg -48 VDC power entry, via dedicated ERNI 3-terminal power connectors (the 3rd terminal is used for power control or monitor). These are tied together at the CB header studs with a short piece of 2-wire PCB, but the -48 VDC legs on the boards themselves are separate. Each Station Board and Baseline Board has its own breaker.

- Cross-Bar Boards (XBBs), have only one leg, and all XBBs in a (Station) rack have their CB header studs connected together with a single bussing PCB. All of the XBBs in a rack are run off one breaker.

A view looking into the power plant cabinet, showing the 200 A breakers for each rack is shown in Figure 5-28.

A view looking into the rack breaker panel, with the front cover removed is shown in Figure 5-29. The front cover, once installed, clearly indicates what each breaker location is for. All breakers in this panel are "household type", 20 A.

Figure 5-28 View looking into the front of the power plant cabinet, showing 200 A rack breakers. Breaker assignments to racks are labelled here. PCUs (480 VAC to -48 VDC converters) can be seen at the bottom of this figure, and are drawer-like modules for removal /replacement.

Figure 5-29 View of rack breaker panel with the front cover removed. -48 VDC leg un-fused indicator lamps are to the far right. The breaker panel housing is custom built.

Further background information on correlator room specifications and infrastructure can be found in [A25012N0000].

5.11 Correlator Power Control Computers (CPCCs)

There are two hot-running redundant CPCCs in the system. Each one can operate independently, although they talk to each other on a regular basis so as to determine if the other one is alive, and to coordinate taking action. Each CPCC is a 19" rack-mount industrial PC, manufactured by "SuperLogics" (P/N: SL-4U-SBC-CL-865G-BA), although any PC with enough PCI-bus slots to hold the 16 NI6509 digital I/O cards could be used. Refer to the CPCC User Manual for further detailed information.

The primary purpose of the CPCCs is to provide a redundant mechanism for controlling power on/off for each Station Board, Cross-Bar Board, and Baseline Board in the system.

CPCCs additionally monitor board temperatures via network connections, and control fan speeds to maintain temperatures. CPCCs run autonomously to protect the correlator from exception conditions, and allow for manual override via the CPCC GUI (refer to Figure 5-5 for manual override capabilities). There is also a path, from CPCC-1, to in-system programming of the Cross-Bar Boards in the system (refer to section 7.1.2).

Figure 5-31 is a simplified CPCC interconnectivity diagram. NI6509 (National Instruments) digital I/O cards, installed in 16 slots of each 18-slot 19" rack-mount computer, provide TTL control and monitor of each rack, via interconnecting 100-pin SCSI cables. These are long cables, but all signal levels are DC, except for rack fan speed monitor lines, which can run up to 1 kHz. CPCC slot assignment to correlator racks is sequential; slot0—S001, slot1—S002, … slot8—B101, … slot15—B108.

Each CPCC is connected to the "Central 1G Switch" (refer to Figure 4-1), providing network connectivity to each other, all CMIBs in the system, the -48 VDC power plant, and the outside world. CPCC-1 is powered by building 110 VAC on UPS, and CPCC-2 is powered from the system -48 VDC supply, via a -48 VDC to 110 VAC inverter. These alternate power sources provide additional assurance that both CPCCs are unlikely to simultaneously lose power, resulting in the instantaneous shutdown of all correlator boards. Each CPCC computer requires approximately 240 W of power.

100-pin SCSI cables connect the NI6509 cards to RPMIBs (Remote Power Monitor Interface Boards), one inside each rack. Figure 5-30 shows all CPCC 100-pin SCSI cable connections at the rear of both CPCCs. Each cable plugs into a dedicated NI6509 card. The top computer is CPCC-1 (with cables labeled with a "P" for "Primary") and the bottom is CPCC-2 (with cables labeled with an "S" for "Secondary"). Cable lengths vary from 9 m to 13 m. If necessary, any cable could be replaced with a 13 m cable, but length assignments to racks are as follows:

Rack	SCSI Cable Length (m)	Rack	SCSI Cable Length (m)
S001	12	B101	13
S002	11	B102	12
S003	11	B103	9
S004	10	B104	9
S005	10	B105	12
S006	11	B106	13
S007	12	B107	13
S008	12	B108	13

Table 5-2 100-pin SCSCI cable lengths from CPCCs to racks.

Diode-OR connections on each RPMIB are such that either CPCC could fail, and control and monitor of the correlator would still function. However, both CPCCs need to be operational for rack fan speed control—if one CPCC fails, rack fans run at full speed (the safest condition as far as the boards are concerned; to override this setting refer to section 8.7). RPMIBs are designed for reliability, and contain no power supplies or complex communications devices. The RPMIB consists of diodes, opto-coupler isolators (for fan speed control and monitor), resistors, fuses, terminal blocks, and status LEDs. CPCC-1

can also in-system program the XBB FPGA boot EEPROMs via the RPMIB "FPGA Prog Header". Refer to section 7.1.2 for information on how this is done.

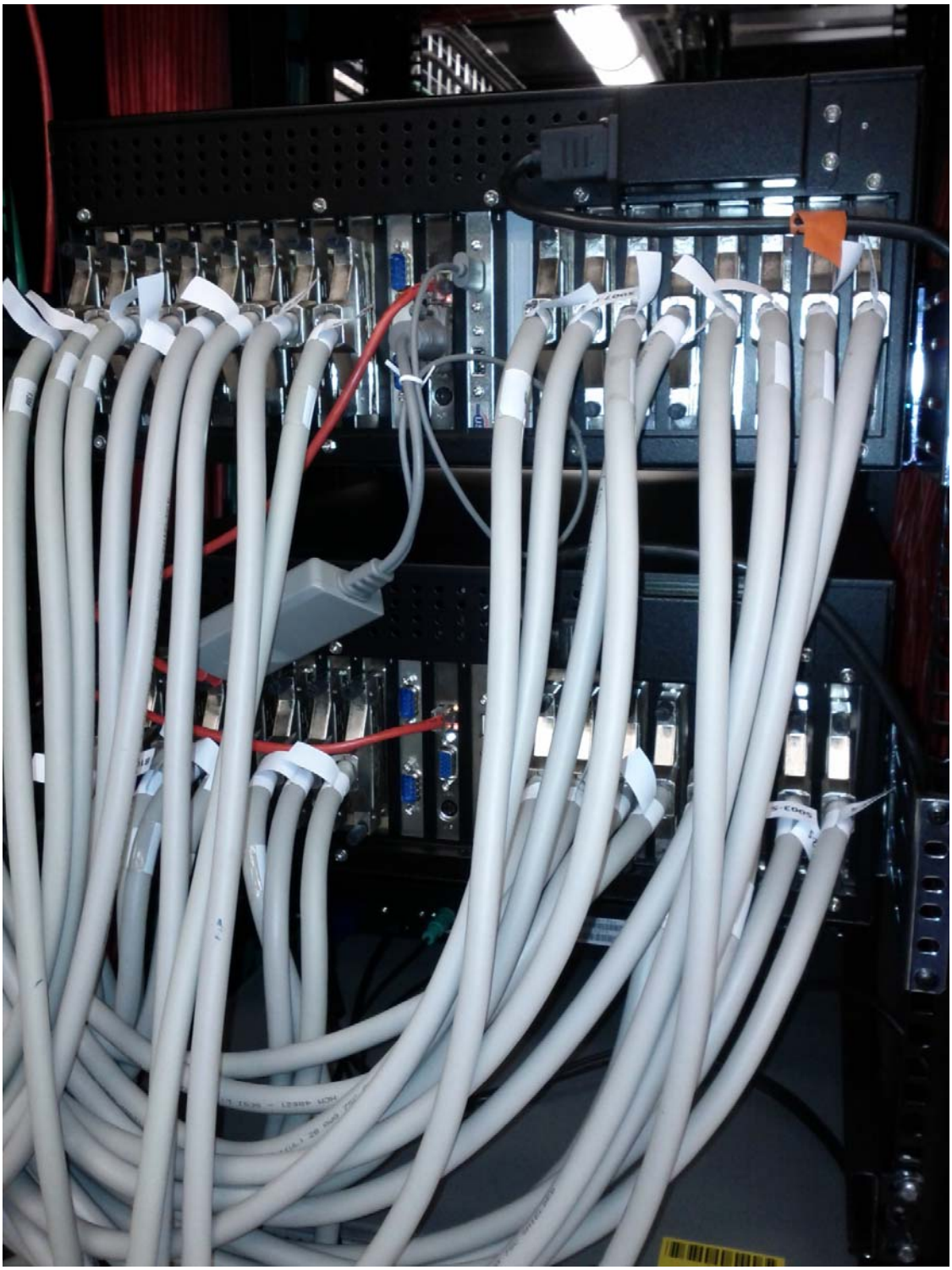

Figure 5-30 A view looking at the back of the CPCCs, with the 100-pin SCSI cables connected to NI6509 boards, and routing to each rack. The top computer is CPCC-1, and the bottom is CPCC-2.

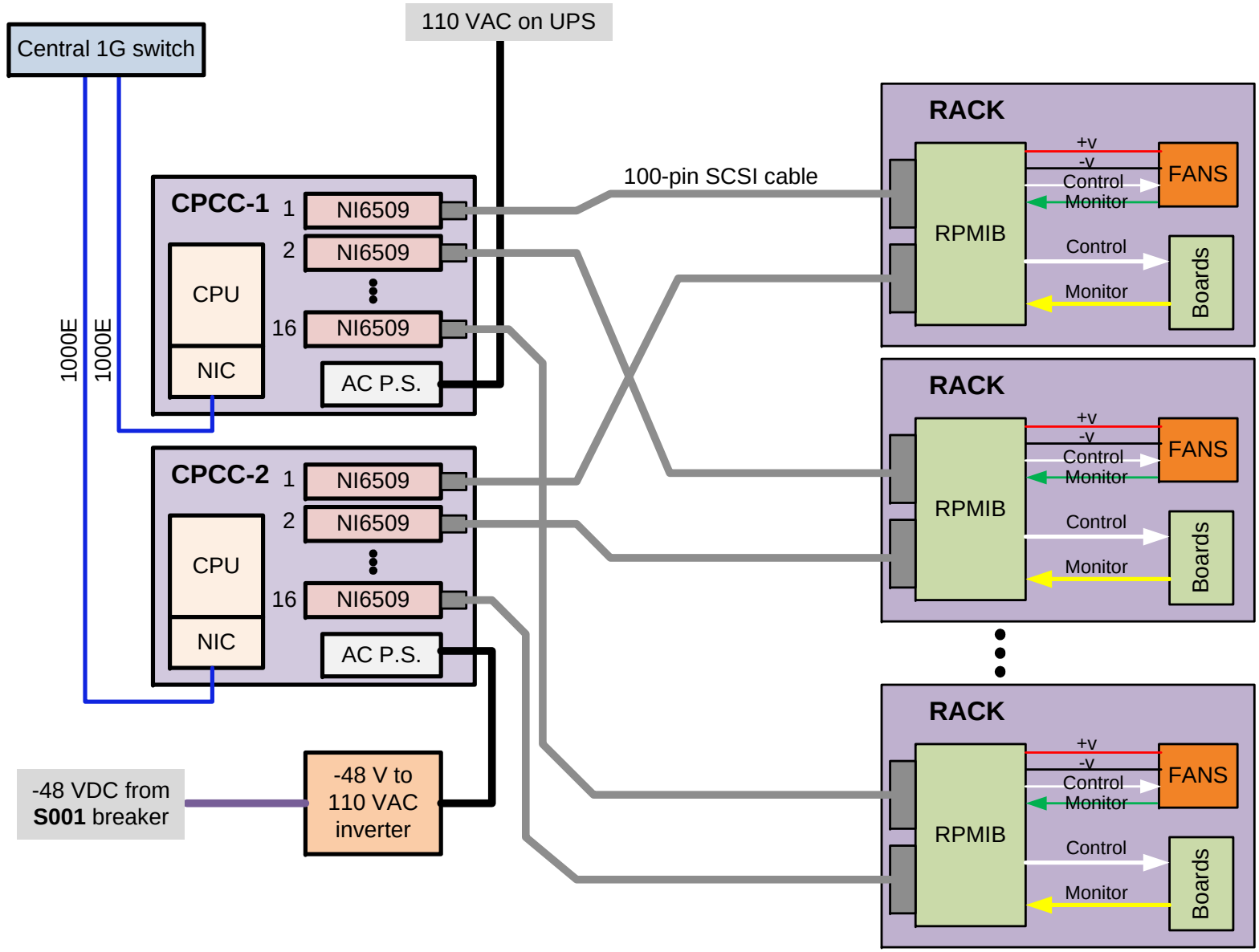

Figure 5-31 Simplified CPCC connectivity diagram. RPMIB wiring colours to "FANS" and "Boards" are as indicated.

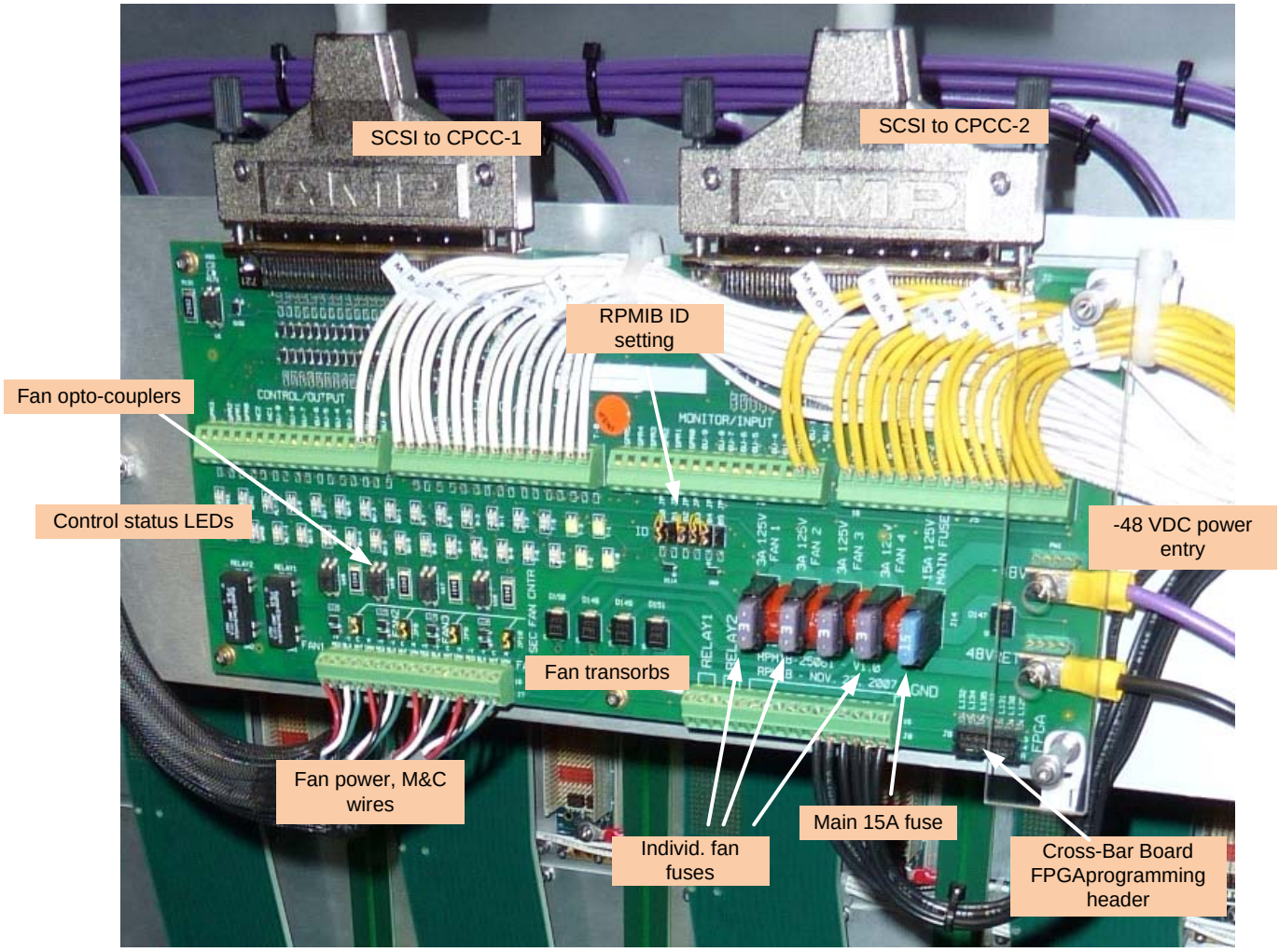

Figure 5-32 View of RPMIB at the back of a Baseline rack.

Wire colours from the RPMIB to the FANs and Boards in Figure 5-31, are as actually wired in the system. The RPMIB PCB consists of a number of terminal blocks, and each port of each terminal block is clearly labeled on the PCB. Other contact points are also clearly labeled. All of the SCSI TTL lines are bead-isolated/filtered. A picture of one RPMIB in a Baseline rack is shown in Figure 5-32. Refer to the RPMIB User Manual for more detailed information on the RPMIB.

A simplified functional schematic of the RPMIB, showing how simple hot-running redundancy is achieved with dual CPCCs, is shown in Figure 5-33 below:

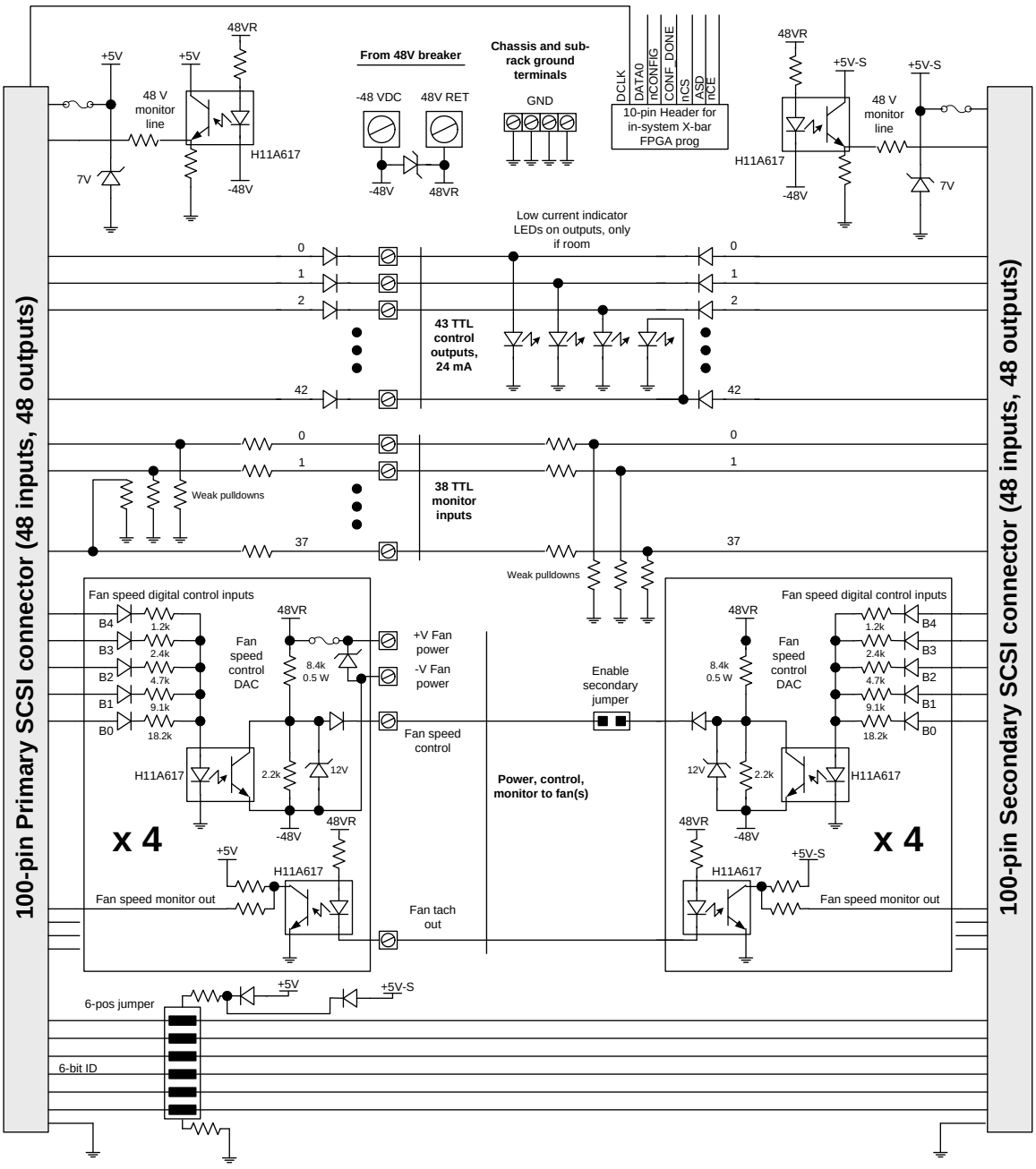

Figure 5-33 Simplified functional schematic of the RPMIB.

Select ports of select RPMIBs are used for smoke detector status monitoring, as well as HVAC system alarm status, and control. Refer to section 6.1 for more information on exactly where these lines are tied into RPMIBs, and therefore into the CPCCs.

The CPCCs are currently running Redhat 5.6 Linux OS, and the main tasks that are running are, “SmokeDetector”, “AC Power Monitor”, “Board Temperature Monitor”, and “Web Server”.

Further background information on system power monitor and control design can be found in [A25026N0000]. Refer to the CPCC User Manual for more details on CPCC design, implementation, and operation.

5.12 Correlator Resource Monitor (CRM)

This section provides a brief description of CRM functionality. Further details will be available in the CRM User Manual when CRM implementation is complete. As of this writing, CRM implementation includes connectivity tests (CRM-CSD: CRM-Connection Self-Discovery), and Baseline Board processing functionality (i.e. standalone) tests (BlB-HST: Baseline Board Hardware Self Test).

The Correlator Resource Monitor is a task running on some computer on the network (nominally the MCCC, however there is no particular reason why it *must* be on it), which facilitates testing of the correctness of Station Board to Baseline Board connectivity, and testing of Station Board and Baseline Board processing functionality. The CRM also builds and maintains a database of bad connections and faulty boards, and makes this information available to a user via a GUI and to the MCCC Configuration Mapper so as to prevent use of malfunctioning hardware (which might have blatant or subtle effects on the data) for observing.

Station Board to Baseline Board connectivity is continually tested on-line, as all HM Gbps signaling contains embedded CRC-4 code checks. However, there are two things that CRM connectivity testing facilitates which may be difficult to track down manually. The first is simply incorrect wiring; all Baseline Board RXP receivers might be happy, but if some wafer pairs are swapped somewhere, it might not be immediately obvious, and it can be very difficult or impossible for the Configuration Mapper to work around the issue. The second is automatically helping to nail down likely faulty communications paths, when there are one or more connectivity problems.

Boards in the system have some startup BIST (Built-In Self-Test), and have continuous on-line connectivity checks (both inter-board and intra-board), however, testing of the *correctness of processing functionality* requires taking boards off-line (i.e. not used for observing, but still in the system and active), and running specific tests. There are many tests that can be envisioned to test processing functionality such as running known patterns and comparing with so-called “golden files”, however the simplest implementation is just to run patterns through a board, have the board perform redundant calculations, and then compare data products that should be identical. This basic strategy was used for all board production functional testing, it is simple and effective, and is what the CRM implements.

5.12.1 CRM Connection Self-Discovery (CSD) Test

This section provides a brief description of the CRM GUI for Connection Self-Discovery (CSD) test, only inasmuch as to illustrate what is being tested, and how it is tested, rather than exhaustively describing the CRM and its implementation.

Referring to Figure 5-34, to start the test, choose the "CSD" tab, click on "Settings" and remove "Safe Mode". Hit the "Execute" button. The test takes about 5 minutes to complete.

The CSD test, when run, takes over the ***entire correlator*** for the purpose of testing *all* HM Gbps wiring from Station Board outputs to Baseline Board inputs. The CSD test goes thru the following basic procedure:

1. Set all Station Board Output Chips to known HM Gbps DATA (refer to Figure 5-16) embedded ID values.

2. Set all XBBs to "straight-thru" connections. Check HM Gbps receiver lock status and embedded IDs on all odd-slot Baseline Board RXPs. Note problems.

3. Set all XBBs so that Station Board I/F "A" (Figure 5-7) route to all XBB outputs, check receiver lock status and embedded IDs on all odd-slot Baseline Board RXPs. Note problems. Repeat for I/Fs "B", "C", and "D". Note problems.

Once complete, the CSD then analyses noted problems, using the following simple algorithm:

- If there were *any* XBB settings where a particular RXP input was good, then the data path from the XBB to the Baseline Board for that wafer is OK.

- If a particular RXP wafer input was bad for *all* XBB settings, then there is likely an XBB to Baseline Board data path problem.

- If there were any XBB settings where a particular RXP input was bad, but at least one setting where it was good, then there is likely a Station Board to XBB data path problem, on the paths/settings where the RXP input was bad.

- If there are data path problems for a particular Station Board on all wafers, then it is likely the Station Board that is at fault, rather than any particular wiring.

A screen capture of the CRM-CSD GUI, and with a "View" of the "Connect Tool" diagnostic "COMPLETE-FLAGGED" is shown in Figure 5-34. The CSD tool has indicated there is a problem with S008-b-3 (Station Board in Station rack S008, bottom 12U crate, slot 3). The selector in the "Connect Tool" screen allows selection of each exception (one at a time), and display of a graphic indicating the problem.

If there had been a problem with just *one* wafer connection from the Station Board to the XBB, the graphical display indicates exactly which wafer is likely bad. If there is a mis-wiring, the graphical display will show it as well.

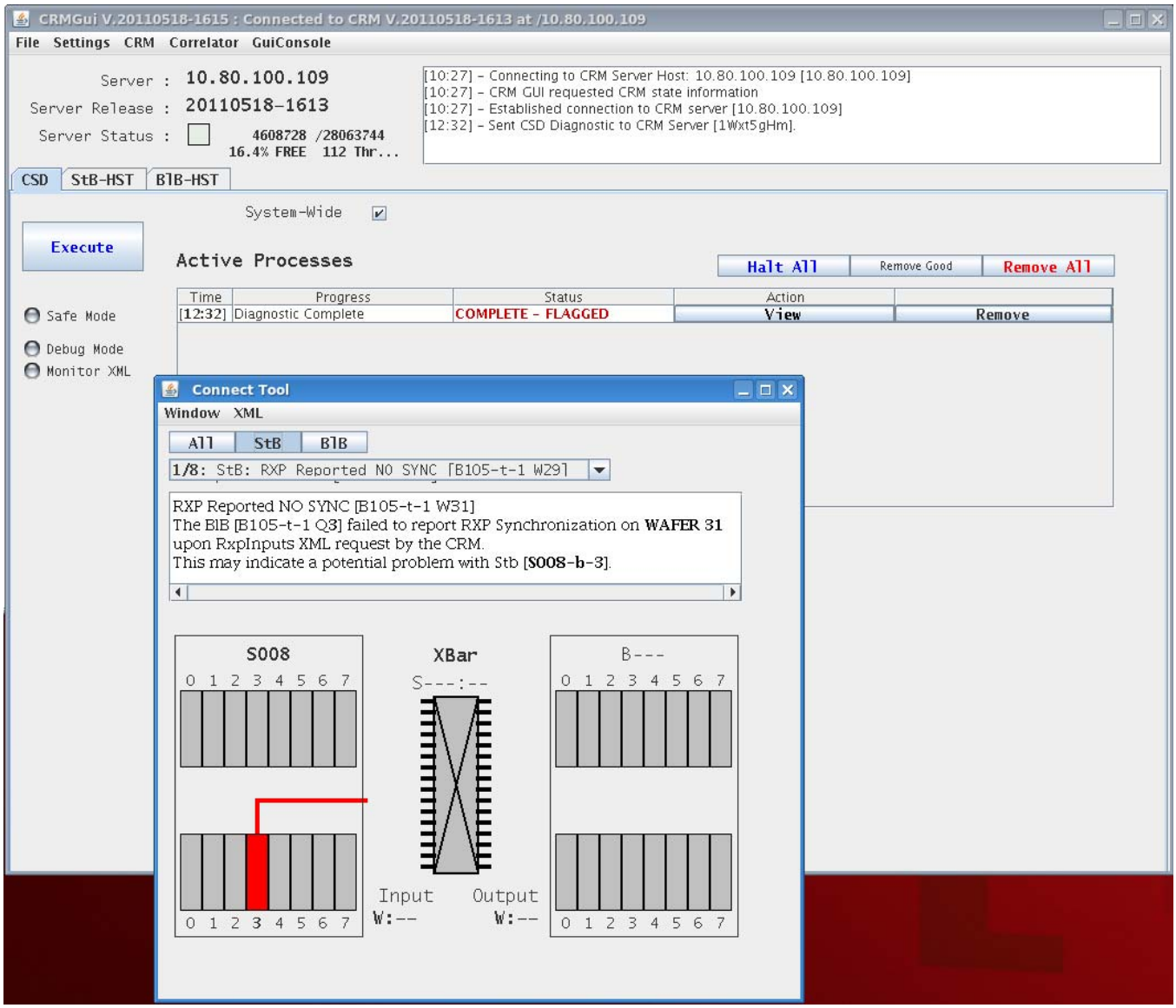

Figure 5-34 CRM-CSD screenshot, with graphical display of a detected problem with a Station Board. Clicking on the "View" button beside "COMPLETE-FLAGGED" brings up the "Connect Tool", allowing selection and graphical display of discovered bad connections.

5.12.2 CRM Baseline Board Hardware Self-Test

This section provides a brief description of the CRM GUI for Baseline Board processing functionality test (a.k.a. "self-test", although the test can be run standalone in test pattern mode, or using wafer inputs as stimuli), only inasmuch as to illustrate how it is tested, rather than exhaustively describing the CRM and its implementation.

To test one or more Baseline Boards in the system, launch the CRM GUI, and select the "BlB-HST" (Baseline Board Hardware Self-Test) tab. This GUI is shown in Figure 5-35, with a test already running. A simplified description of key points in the GUI follows.

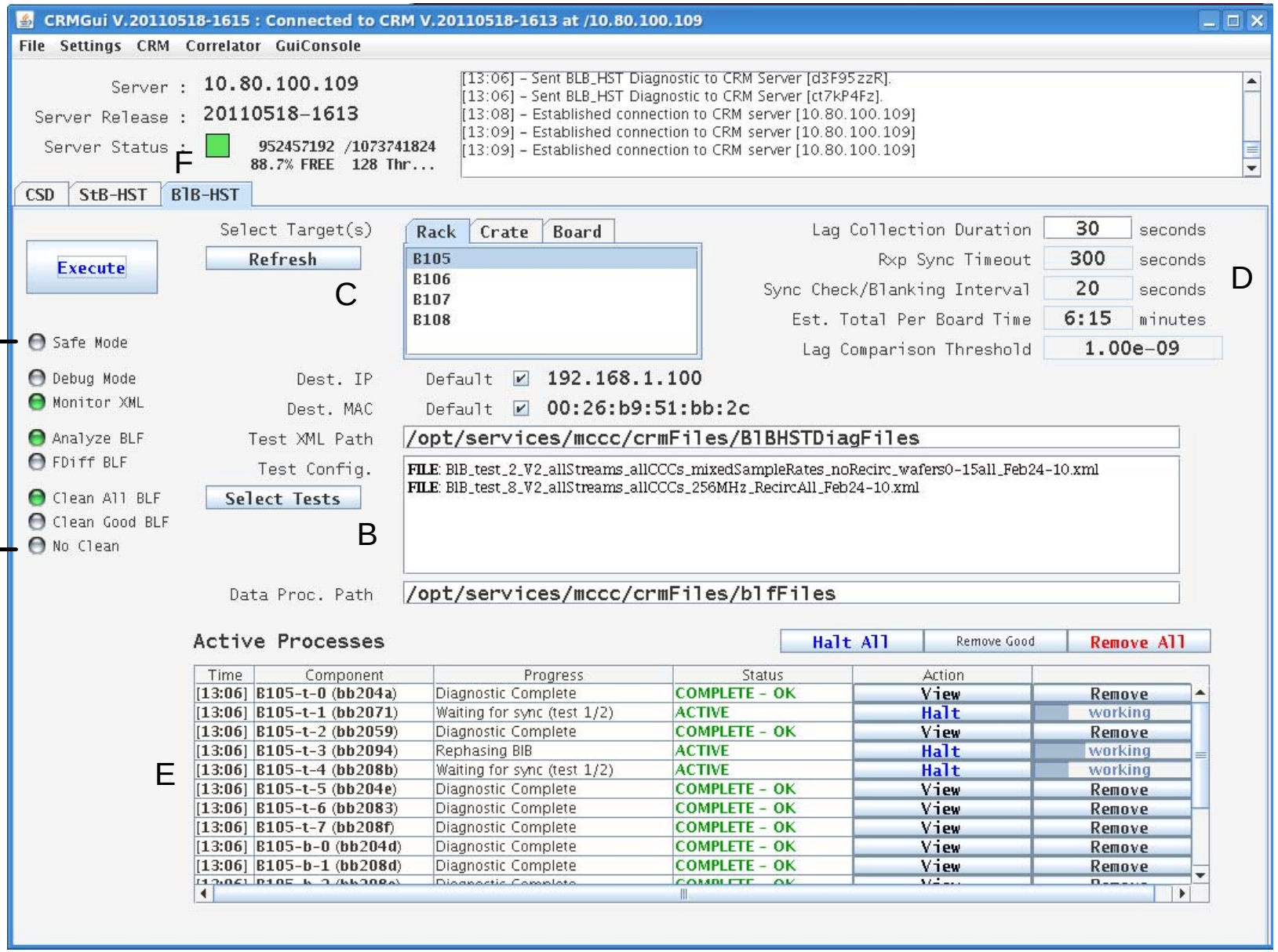

Figure 5-35 CRM Baseline Board Hardware Self-Test (BlB-HST) GUI, highlighting major sections.

A – These LEDs indicate major settings for the test. They are coloured such that if anything other than GREY (OFF) or GREEN (ON/selected) is visible, the test will not run properly when the "Execute" button is pressed. A brief description of each one is as follows:

- **Safe Mode** – YELLOW if safe mode is on. When in safe mode, no actual tests are run. This must be GREY to actually run a test.
- **Debug Mode, Monitor XML** – For debugging and XML message monitoring only. Refer to the CRM User Manual for more information.
- **Analyze BLF** – If GREEN, then the resulting .blf files (containing lag frames produced by Baseline Boards) are analyzed for comparison errors. If GREY, no analysis is performed.
- **FDiff BLF** – If GREEN, then lag frame correlation coefficients are normalized to produce floating-point coefficients before comparisons are performed. When this is the case, it allows the user to determine the relative magnitude of a processing fault, rather than just the fact that a processing fault has occurred. If GREY, then straight bit-exact comparisons are performed.
- **Clean All BLF** – If GREEN, then all .blf files produced are removed after being analyzed. If GREY, they are not removed, allowing for further post-test analysis (for example using the "lagfan" program—see section 13 of [A25080N0001]) to be performed. If GREY, .blf files are not removed, or only .blf files for tests that pass are removed, depending on the next LED.
- **Clean Good BLF** – If GREEN, then only .blf files where there were no errors are removed, leaving ones with errors for further post-test analysis.
- **No Clean** – If GREEN, no .blf files are removed.

B – The "**Select Tests**" button, when pressed, brings up a secondary GUI, allowing selection of any number of "*test*.xml" files, located in the "Test XML Path".

Each file is a particular Baseline Board configuration, set so that there are redundant correlations for the analysis to operate on to find problems. The de-facto nomenclature for these files is such that any "*test_N_*.xml" ("N" is the test number) files put the RXP FPGAs in "Test Pattern" test vector mode, thus completely ignoring wafer signal inputs, and any "*test_Nw*.xml" files keep boards in normal wafer inputs for testing, using only antennas 1-27 (i.e. not using S008 boards, which normally are not populated with antenna signals and subsequently produce bad wafer outputs). Any number of tests can be defined and run at any time.

Important Note: When running Test Pattern vectors for a test (i.e. "*test_N_*.xml" files), it can take up to 5 minutes for each board to re-synchronize to Test Pattern vectors, from wafer inputs, for the first test in the lot of tests. When going back to wafers (after the test is complete, or running a subsequent "*test_Nw*.xml" file), it can take up to another 5 minutes for the receivers to sync. Thus, *test_N_*.xml and *test_Nw*.xml files should not be mixed in an actual test suite run, as it will take the longest to execute.

Note that the "Dest. IP" and "Dest. MAC" is the address of the computer where lag frames will be sent for CRM analysis. .blf files will show up in "Data Proc. Path".

C – Clicking on the "Rack" tab will show all racks in the system there are to test. Clicking on the "Crate" tab will show all crates (sub-racks) there are to test. Clicking on the "Board" tab will show all boards there are to test. Thus, tests can be run on one or more selected individual boards, all the way to the entire system. Within the window, click (CNTRL-click for multiple selections, SHIFT-click for selection range) to select which boards, crates, or racks are to be tested. The "Settings" drop-down window allows the user to select how many boards are concurrently tested at any one time so as to limit network traffic and load on the test computer. The default is 16.

D – These are "test timing" parameters, as the text indicates, set mostly via the "Settings" drop-down window. "RXP Sync Timeout" is how long the CRM will wait for RXP sync before proceeding with the test. When running *test_Nw*.xml tests, when S008 is generating bad signal, this should be set to ~30 seconds so as not to wait for any excessive period of time for RXP wafer sync on signals that are continuously bad. "Sync Check/Blanking Interval" is how often the CRM checks for RXP sync, and also sets the blanking time between tests. As soon as RXP sync is achieved, testing begins.

E – This is the progress and results window. The "Component" is the Baseline Board being tested, and up to 16 boards can be running tests simultaneously (the number of boards can be changed in the "Settings" drop-down dialog, but should not be greater than 16 otherwise the number of CRM-spawned threads, and network traffic could become excessive). The "Progress" window indicates what is happening for that particular Component. The "Status" window indicates, well, status. If "COMPLETE-FLAGGED", then a problem was found with a Component. The "Action" window allows one to "View" results (which pops up a separate window[16] showing the results of the test, the intelligent human analysis of which can help to pinpoint where the problem on the board is), or "Halt" an existing test for a particular Component. Components can also be removed individually, or en-masse with the buttons in the GUI. Refer to the CRM User Manual for further detailed information.

[16] The contents of this window is similar to that produced by the "lagfan –a –diff" program, but enhanced to indicate which test failed to further pinpoint the problem.

F – This large square LED should be on and off GREEN, indicating the GUI is communicating with the CRM server running on the "Server" CPU (in the example at IP address "10.80.100.109"). If this turns RED, then it indicates the GUI has (temporarily, or permanently, depending on how long it is RED) lost contact with the CRM server.

Note that for BlB-HST (and StB-HST), multiple CRM GUIs can be running concurrently, and each one can be running tests—same or different tests, started at the same time or at different times—on the same board; the CRM server will just queue these tests up, and then run them within the 16-board limit, as space becomes available. This is because there is only one CRM server orchestrating all of the tests. Every CRM GUI will see exactly the same tests and results. Care should be exercised, as one GUI could "Remove" results that another person on another GUI produced and wants to subsequently view.

Refer to the CRM User Manual for further detailed information on the CRM GUI, "View" results window, and CRM server functionality.

5.12.3 CRM Station Board Self-Test

TBD.

5.12.4 CRM Database

TBD.

5.13 MCCC – Configuration Mapper, and VCI Protocol

The MCCC (Master Correlator Control Computer) is the principle automatic monitor and control interface to the correlator. It primarily contains the Configuration Mapper process, which translates high-level configuration requests from the EVLA Executor, and a monitor process, which monitors the status of all correlator components, maintains overall system status, and reports it over the VCI. Secondarily, it contains a Delay Model task which receives antenna-based geometric delay models from the Executor, re-labels, and routes them to appropriate Station Board CMIBs for execution (delay tracking).

The VCI (Virtual Correlator Interface) [A25201N0000] is the XML protocol that defines messaging mechanisms, message content, and message protocol for communication with the correlator. Primarily it is with the EVLA Executor, but it is also with the Monitor Data Archive (refer to Figure 3-1).

Other computers on the network, and external to the EVLA network (with permissions), can talk to and configure correlator hardware independent of the Configuration Mapper. To prevent clobbering of configurations, an informal system of access permissions has been developed using the "widar-wg" exploder email (widar-wg@aoc.nrao.edu). In all cases of course, communications with operations personnel via this exploder is required before taking any action to interrupt automatic configurations.

The MCCC and EVLA Executor are VCI peers. The client is the Executor, and the server is the Configuration Mapper. The client originates actions, and the server responds. The MCCC monitor process is the client which writes monitor messages to the Monitor Database. StB or BlB CMIBs monitor messages are always funneled through the MCCC monitor process.

The following classes of messages between VCI peers may be exchanged:

1. Configuration requests, used by the Executor to change part or all of the correlator's configuration.

2. Configuration query, used by the Executor to check whether a particular configuration can be activated at the specified time. A configuration query does not result in a configuration change.

3. Real-time control messages, used by the Executor to specify delay models for currently-in-progress observations.

4. Log and alarm messages, sent by the MCCC to the Monitor Database to report significant events.

5. Status report messages, sent by the MCCC to the Monitor Database to report correlator status.

The format of all VCI messages are encoded as XML documents with schema that is part of the VCI protocol specification.

5.13.1 MCCC Configuration Mapper

The Configuration Mapper (CM) forms the bulk of the MCCC's functionality, and heavily determines the extent to which the flexibility present in the correlator's hardware design can be utilized for science. As seen in previous sections, there are multiple layers of cross-bar switching available, multiple sub-band bandwidths and locations that can be used, multiple stages of filtering, multiple correlation configurations, and multiple ways of doing the same thing. The CM must translate Executor requests into detailed correlator configurations, and send those configurations as XML to 256 embedded CMIBs (real-time Linux CPUs), and also to the CBE.

The details of exactly how the Configuration Mapper performs all of this mapping is well beyond the scope of this document. Refer to the VCI protocol specification [A25201N0000], the MCCC RFS document [A25202N0001] the CM RFS document, and the MCCC Configuration Mapper RFS document [A25202N0000] for further detailed information. A summary of the kinds of configurations the CM can handle is as follows:

- Station Board input bandwidth and initial sampling configuration (i.e. 8-bit or 3-bit). "Input Chip" cross-bar configuration.

- Station Board wideband autocorrelator, and wideband state counts configuration.

- Station Board Filter FPGA configurations. This is probably the single most complex chip to configure, each Station Board contains 36 of them, there are multiple stages, and each chip can be set for a different delay center on the sky. Refer to the Station Board User Manual [A25040N0001] and the Filter Chip RFS document [A25044N0000] for further detailed information.

- Station Board Output Chip cross-bar configurations. This switch determines the mapping of Station Board Filters to outputs, which ultimately route to BlB pairs in quadrants. For example, if 4 BlB pairs are to be used for one sub-band within one I/F pair, to obtain 4X spectral-line resolution, the output of one Filter will be routed to 4 output wafers using this cross-bar functionality (see Figure 5-8).

- Station Board dump control (DUMPTRIG) configuration. The Station Board is capable of generating 16 independent DUMPTRIG sequences, allowing for the possibility of each of the 64 sub-band pairs, across all I/F pairs of being different, for example each one using a different pulsar ephemeris or synchronized to system timing.

- Cross-Bar Board cross-bar configurations. For each particular sub-band, these configurations allow data to be replicated across correlator quadrants to allow a tradeoff between number of I/Fs correlated, and spectral resolution per product. Settings can be different for each sub-array and each I/F pair. Note that the MCCC does not talk to Cross-Bar Boards directly, as they don't contain CMIBs. Rather, connections are established by sending messages to Station Board CMIBs, which send HM Gbps COMMAND messages to downstream Cross-Bar Boards to establish connections. Each Cross-Bar Board FPGA (i.e. switch) can accept COMMAND messages on any of its inputs to affect any switch setting.

- Baseline Board RXP cross-bar configurations. The dual-RXP FPGAs on the Baseline Board act together as a complete cross-bar switch, allowing any of the 32 input antennas for the particular sub-band to be routed to the 8x8 correlator matrix on the board. Each of these 32 inputs could be from a different I/F pair, but normally are all from the same I/F pair for each sub-array. The second Baseline Board in the BlB pair gets only the data exiting the RXP FPGA on the first board, and it is mirror-imaged on its input due to Patch Board and signal integrity constraints.

- Baseline Board RXP phased-array configurations including defining which antennas are phased, what phasing parameters are used, and whether the output is strictly to the GigE FPGA for VDIF packet generation, and/or to the Correlator Chip array for auto-correlation or cross-correlation.

- Baseline Board Recirculation FPGA cross-bar, sample rate, recirculation, and correlator configurations. If dynamic recirculation (whereby a super-set of lags are acquired by time-multiplexing data acquisition on a smaller physical set of lags) is active, the Recirculation FPGA parameters must be set concomitant with DUMPTRIG settings to achieve the desired result. Dynamic recirculation cannot

operate without the cooperation of DUMPTRIG signaling. The Recirculation FPGA can be set on a per-stream basis for normal cross-correlation, or auto-correlation, used in conjunction with the Correlator Chip to obtain 2048 channels in one chip, rather than just 1024 channels. Additionally, there can be a mix of recirculation and non-recirculation streams, with some restrictions (although this is not a supported configuration in the CM).

- Baseline Board Correlator Chip multi-level switch configurations, to allow lag cells (CCCs) to be chained, or separate, depending on how many correlation products are to be obtained.

- Baseline Board LTA FPGA configurations, primarily CBE node destination MAC and IP addresses. These addresses are set in the LTA to allow the output of each Correlator Chip to be directed to a different CBE node, to facilitate deterministic scheduling of packets through the CBE switch as noted in section 5.14.2, bullet 2, and to facilitate CBE node load sharing.

- Baseline Board Gigabit Ethernet FPGA configurations, primarily setting source addresses and ports for LTA lag frames, and source and destination addresses and ports for VDIF phased-array packets.

Additional general Configuration Mapper configurations, with settings in various places include 7-bit correlation (i.e. 7-bit re-quantization after FIR filtering), requiring distribution of partial products within a Correlator Chip, or across BlB pairs, and then assembly of partial products in the CBE. 7-bit correlation could be used with or without recirculation, noting that in the Recirculation FPGA, 7-bits requires two internal data paths, and so recirculation can be performed on only 4 data streams rather than the normal 8.

Regarding recirculation, there are memory restrictions such that if recirculation is performed on 8 streams, the maximum number of spectral channels that can be obtained is 16,384. If it is performed on 4 streams, then the maximum number of spectral channels that can be obtained per correlation product is 262,144. If the desired number of channels lies somewhere in between this range, the CM must decide how many products are produced per Correlator Chip, in the extreme, the answer is 1 (i.e. 256 recirc factor x 1024 channels = 262,144 channels).

There is also the issue of load balancing and trading off spectral resolution for integration time or pulsar time bin dwell time. For shorter integration times, fewer Correlator Chip Cells (CCCs) must be used, so as not to overwhelm the output data rate or the data rate from the Correlator Chip to the LTA, and so the CM spreads cross-correlations across more BlB pairs than otherwise might be required. The concept of “Maximum Packing” (fit configuration into the least amount of hardware) and “Minimum Packing” (spread out configuration amongst a defined limit of hardware) has been developed to deal with this issue.

5.14 Correlator Back End (CBE)

The purpose of the Correlator Back End (CBE) is to gather "lag frames" produced by all Baseline Boards, process the frames, and write them to the Lustre file system as BDF (Binary Data Format) files [BDF-2009] for archiving and image processing.

Each Correlator Chip on each Baseline Board contains 16, 128-complex-lag correlator cells (CCCs—Cross-Correlator Cells), and *independently* of how a cell is used (i.e. whether it is a standalone cross-correlation product or one part of a larger cross-correlation product), its contents is output on the Baseline Board's SFP1 1 Gigabit Ethernet port, as a "lag frame" encapsulated within its own UDP/IP Ethernet packet. (Refer to the Baseline Board User Manual, LTA FPGA RFS, and GigE FPGA RFS for more information on how Correlator Chip data gets to the GigE FPGA, and for the exact contents of the packet.)

The lag frame itself contains identification information, timestamp, status bits etc., however it does not contain all of the additional "meta"-data required to write a BDF file. The Configuration Mapper on the MCCC provides the CBE Master information it needs to know to assemble lag frames, and observation information such as integration time, scan time, etc. The EVLA M&C system (Executor) provides the CBE Master node with information it needs to fill in meta-data in the output BDF files. The Master node distributes all of this information to slave nodes so that they have all information they need for processing.

The CBE therefore gathers together lag frames that "go together" (in lag-space, and temporally), performs data valid normalization (divide raw lag frame coefficients in 2's complement representation by the data valid count in the lag frame), FFTs to the frequency domain, integrates if required[17], formats the data for output including any meta-data required, and writes out BDF files to the Lustre file system.

Referring to Figure 4-1, the CBE switch is configured to allow packets from any Baseline Board to be routed to any CBE compute node, and to allow phased-array VDIF packets on any Baseline Board SFP2 module, (tied into the switch via a patch panel), to be routed to any CBE compute node, the MkVc VLBI data recorder, or any combination thereof[18].

Lag frame packets from any Baseline Board can also be routed to any computer on the network, in particular the MCCC, where the CRM server runs (for BlB-HST—refer to section 5.12.2).

[17] Whether to integrate first and then FFT or FFT and integrate depends on processing requirements. Normally integrate first and then FFT is used for lowest computing requirements, however, for temporal-spectral interference excision, FFT and then integrate is optimal.

[18] Except lag frame packets can't be written to the MkVc VLBI data recorder since it won't recognize them.

Note that the source of lag frame packets is the Gigabit Ethernet (GigE) FPGA [A25092N0001] on the Baseline Board. The design of the FPGA is simple and data flow is uni-directional. The GigE FPGA (and the LTA FPGAs) must be explicitly told all source and destination address and port information that is to be included in output IEEE 802.3 Ethernet packets using the UDP/IP protocol. The GigE FPGA in no way listens to packets on its receive port to set or determine transmit packet addresses. The only receive functionality the GigE FPGA has is that it detects if the receiver is detecting good PCS (Physical Coding Sub-layer) codes[19], and it has the ability to capture receive packets (normally via the GigE GUI, but any host can query such information from the Baseline Board CMIB using the XML protocol).

There are (will be) 32 CBE compute nodes plugged into this switch, plus the Master CBE node. Output BDF-formatted data from the CBE compute nodes are written to the Lustre file system via a separate 48-port switch. The Master CBE compute node also writes BDF file location information to MCAF.

5.14.1 CBE Switch

The CBE switch uses a two-tiered fabric. The first tier is a 20-port 10G switch (Cisco Nexus 5010), and the second tier consists of 8, 48-port 1G + 4 10G port switches (Cisco Nexus 2148), each with two 10G uplinks connected into the first tier. The entire package is an integrated Cisco solution. A simplified diagram of switching blocks and connections is shown in Figure 5-36.

Each of the 8 48-port switches uses 16 ports connected to SFP1 (lag frames) on all Baseline Boards in a particular rack, 16 ports connected to SFP2 (VDIF phased data) on all Baseline Boards of the same rack, and 16 ports to 4 CBE nodes, each node with 4 1G ports, dedicated for data transport, and 2 1G ports for control and output to the Lustre file system.

Two additional 48-port 1G switches (right side of the figure) are used to route CBE output traffic from the CBE nodes to the Lustre system, allow all CBE nodes to talk to each other and CBE Master, and connect to the Central 1G Switch for access by MCCC, CPCCs, and the outside world.

The details of connectivity shown in the figure is subject to change over time as requirements change etc., but in any case, the same basic switching connectivity between the various elements should be maintained as shown.

[19] i.e. indicating a good connection to the far-end switch.

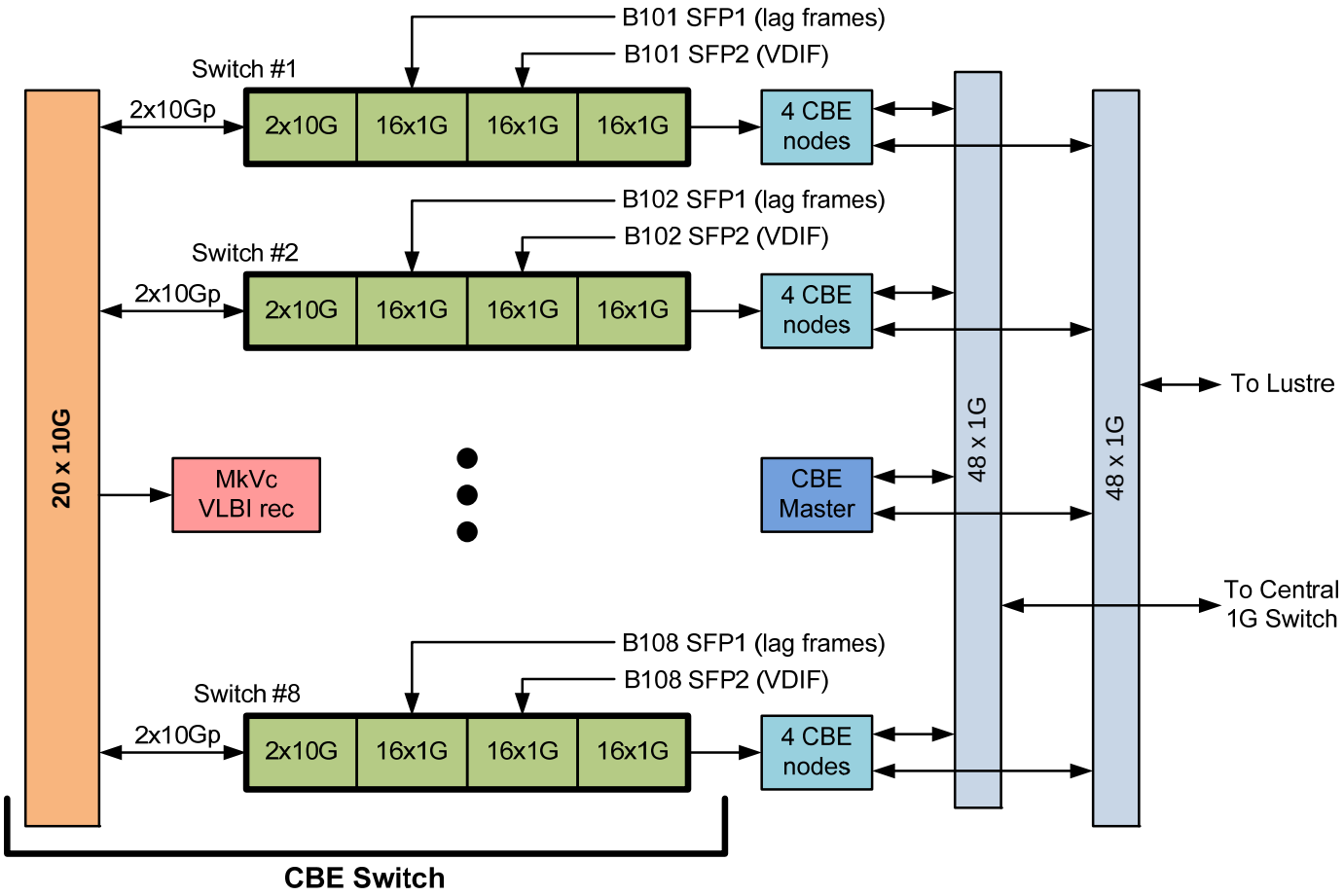

Figure 5-36 Simplified CBE switch configuration. "10Gp" are proprietary Cisco 10G links. Additional 48-port 1G switches provide CBE node connectivity to the outside world.

5.14.2 Packet Traffic Scheduling Through the CBE Switch

With the correlator capable of producing full-capacity packets on every Gigabit Ethernet output, including on SFP2 VDIF phased-array outputs, it can quickly and easily overwhelm the capacity of the CBE switch to handle traffic without dropping packets. Even at low overall packet rates it is possible to have packet collisions in the switch, since when a data dump occurs, all results are available at virtually the same time, and suddenly the network is flooded with a burst of packets.

To deal with this problem, there are 2 methods for LTA lag frame packet transmission scheduling built into the correlator, which might be used:

1. The GigE FPGA on the Baseline Board has a programmable, optionally uniformly randomized, inter-frame delay, with 1 microsecond resolution (4 microsecond resolution over 1.024 millisecond when the randomizer is on), which can be set so that the GigE FPGA uniformly in time spreads out transmission of lag frames ready and waiting in LTAs. In this case, the mean inter-frame delay is set, and the randomizer, for each frame transmission, chooses a wait time or delay before transmission between 0 and 2X the set inter-frame delay. The GigE FPGA

randomizer is built so as to not, under any circumstances, be deterministic. Thus, there a very small probability (determined by the inter-frame delay time resolution, and the inter-frame delay[20]) that more than one board is transmitting at the same time to the same destination CBE node. This method therefore relies on statistics to minimize the probability of a packet collision in the switch. As the integration time decreases, packet traffic density increases and so this method likely only works when the traffic load is low, perhaps < 10%, compared to what wire speed can support, and depending on the capabilities of the switch.

2. The LTA contains a programmable timer (implemented in LTH_COUNT registers) with 31 microsecond resolution, and 65 second duration, which can be set to delay any output data transmission, after the most recent data dump from the Correlator Chip, by a set amount. By strategically setting these timers, and knowing the CBE switch and CPU cluster configuration, it is possible to deterministically schedule packets through the switch so as to avoid collisions (refer to Figure 5-5 of the LTA RFS [A25091N0000] for details on how this might be accomplished).

   If, however, the correlator is dumping data synchronized, for example to multiple pulsars and/or on different sub-arrays, general deterministic scheduling may be difficult to achieve. In this case end-destination CBE CPU nodes should be carefully chosen so that there is a low probability of two packets destined for the same CBE node at the same time, something that can be achieved by exclusively assigning CBE nodes to independent "integration domains", and within each integration domain using deterministic scheduling (assuming that an LTA is exclusively in one integration domain).

For phased-array VDIF packet transmission, there is less flexibility. This is because there isn't the kind of packet buffering capability in the GigE or RXP FPGAs as there is for LTA lag frame packets (in the LTA). For these packets, they will be dropped at the GigE FPGA, if the previous packet isn't on its way out of the transmit packet buffer, before another one comes along (from the RXP). The GigE FPGA provides the ability to delay VDIF packet transmission (i.e. delay from when it is received from the RXP FPGA—where phasing occurs—until it is transmitted), with 1 microsecond resolution. This delay should always be less than a packet transmission time, which is calculated as, packet_length_in_bytes / 125 MHz. It is also possible to route VDIF packets to SFP2 (set in the GigE FPGA), and therefore the above inter-frame delay mechanism can be used, with applicable maximum delay precautions as noted.

A third mechanism to control packet traffic is provided for SFP1 (only) port in the GigE FPGA. The FPGA is built to respond to PAUSE frames (IEEE 802.1D), as per the PAUSE frame protocol, to allow for XON/XOFF flow control. Although normally PAUSE frame flow control is not used in Ethernet networks (due to the domino effect

[20] Noting that the inter-frame delay is an 8-bit register and that when randomization is turned on, the resolution is set to 4 microseconds, so as to allow a greater range in inter-frame delay.

through the network of such action), it could be appropriate here if the CBE switch is so capable and enabled.

5.15 MITR Database

The MITR (Module Instance Tracking and Reporting—pronounced "meter") database is not formally part of the system, but was developed for the correlator project to allow for easy and exhaustive tracking of every module's complete history from cradle to grave.

MITR is implemented in JAVA, with a mySQL database backend. It is accessible anywhere with a web browser, and was designed for, and runs best using Mozilla Firefox.

MITR is intuitive, easy-to-use, user-extensible, and powerful, with features such as the ability to define module types, status, and module location information, which subsequently can be applied to module instances. A module can be anything that has a number to allow it to be tracked, and for the EVLA correlator, modules range from circuit board assemblies, to racks, to the entire correlator system. Documents and images of any kind can be attached to each instance of any module, for record keeping of test results, documenting damage etc.

MITR allows module hierarchy to be defined, useful for the EVLA as each board contains mezzanine cards, each with their own serial number and boards get installed in racks, each with its own serial number etc. MITR contains facilities for component failure recording and reporting, to allow displays of failures versus time to be generated, for example. Each instance of a module can be assigned a particular set of "Procedures", which can be any set of instructions that must be executed during any process phase. Each module instance (and Procedure instance for that matter) has a "History" section, and any number of Histories can be entered, and automatically time-stamped and user-assigned by the software. History entries contain user-entered textual descriptions of problems, observations etc. MITR allows exhaustive searching of Histories using any defined keywords. MITR can search and display on module names and serial numbers in various ways. MITR contains shipping and receiving tracking for each module so its current ship state, waybill number, whether it has been received at the other end etc. can be tracked. ECOs (Engineering Change Orders) can be defined (in text, or as an attached document, or combinations thereof) and entered for a particular module type and Revision range, and then every instance of every module matching those criteria will show the applicable ECOs to it.

MITR contains part number tracking and inventory management as well, so all spare parts for the correlator could be entered[21] and maintained in MITR, along with part ordering, and part shipping and receiving information.. Searching on part keywords is also very powerful allowing the user to quickly find a part if only some small part of text is known.

[21] And indeed are entered for all spare parts at DRAO Penticton.

Reports can be generated by MITR, one of which is failure-rate curves, and History and Procedure entries can be formatted nicely for printing. Any attached document or image can be printed as well. MITR contains on-line help, and this on-line help can be dynamically updated by Administrators.

MITR is also multi-independent project, and multi-user. Administrators can add or delete users, and allow certain users to only see select projects. Thus, for example, the entire EVLA could be tracked with MITR, and each major section could be a separate project, with users assigned only to those projects for which they need to be assigned. The WIDAR correlator is only one such project in MITR.

Of course, MITR is only as powerful as the data that users choose to enter into it. If modules are modified, moved around, or shipped, and the small amount of time required to note what is happening in MITR is not dutifully taken, then, of course, the database will not accurately reflect what is actually happening, and its usefulness diminishes.

MITR resides on a backed-up server at DRAO at: https://mitr.drao.nrc.ca/mitr/index.php, but will be copied and transferred to NRAO in its entirety on hardware acceptance of the system.

5.15.1 Brief MITR Description

A full description of every MITR feature is beyond the scope of this document, but a brief description of key GUI screens is provided to familiarize potential users with its look-and-feel and its capabilities.

Go to the MITR site above, and login. If you don't have a login, contact an Adminstrator to get added as a user and defined a password (at DRAO the administrators are Dave Del Rizzo (the software developer), and Brent Carlson). On user-level login the first screen you will see is as shown in Figure 5-37 below. The upper-left of the screen shows the PROJECT that is currently being viewed—it can be changed by clicking on it, and selecting a different project. User-level users can see only those projects they have permission to see.

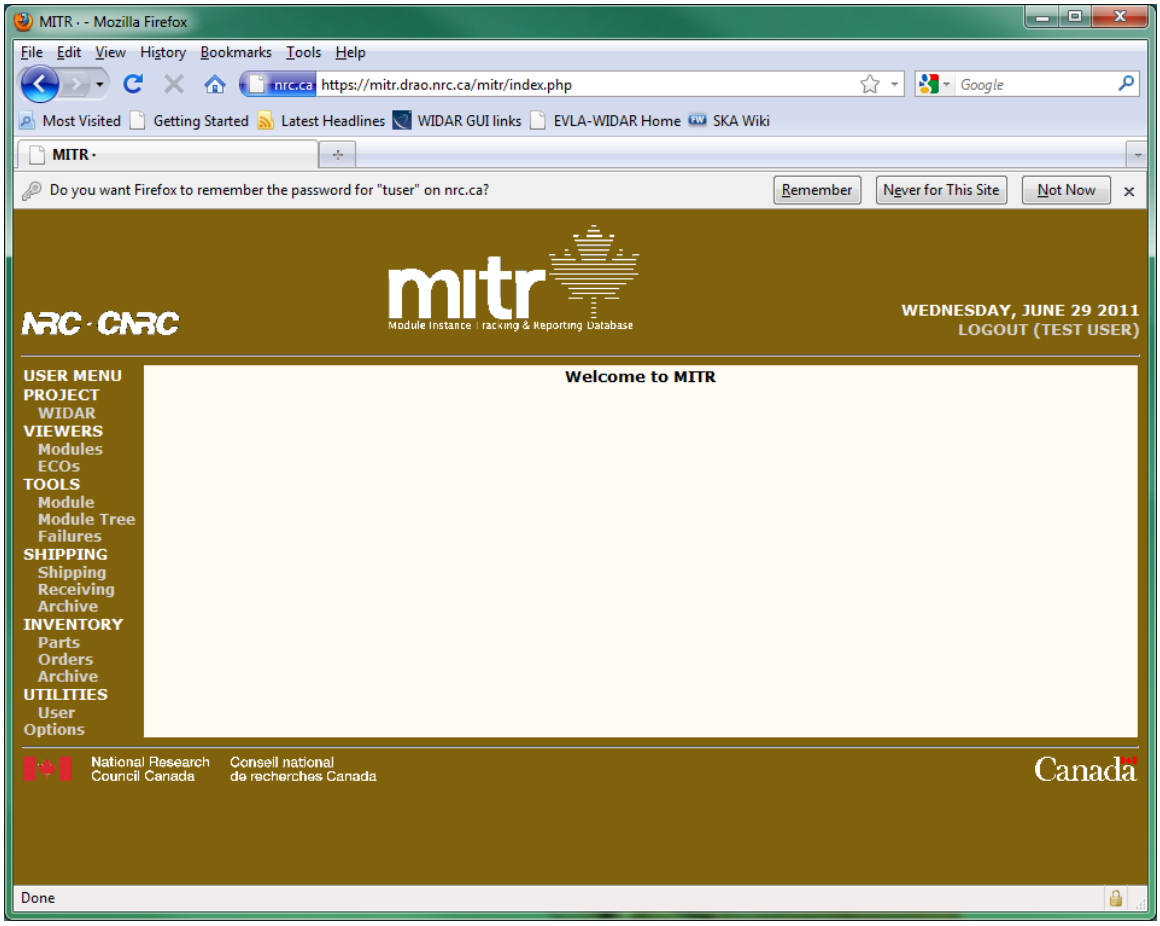

Figure 5-37 MITR user-level screen after first logging in.

Clicking in "VIEWERS—Modules" brings up the main Module display screen and is shown in Figure 5-38.

There is one line per module, showing the module Type, S/N (serial number), M/N (Model Number), Revision, Location, Status, Parent S/N, and three buttons TREE, VIEW, and UPDATE. Clicking on any of these three buttons drills down to other screens to see all attached child modules, View status, History etc., or Update module information. Module Location and Status information can be updated in this main modules screen without drilling down via UPDATE. Clicking on one of the headings (TYPE, S/N, etc.) causes modules to be sorted and displayed alpha-numerically by that column entry. Each page shows only a sub-set of modules (since there can be hundreds or thousands of modules in a project), and the "<< < 1 2 3 …> >>" bar allows one to quickly scroll thru or jump to pages. If only one module type is desired to be displayed, the drop-down box in FILTER allows selection of module type to show (important to remember that module types, locations etc. are all Administrator-defined for any project so there is no limit on the number of modules/types etc. that can be tracked). A general SEARCH (for a specific module S/N) or HISTORY SEARCH can be done.

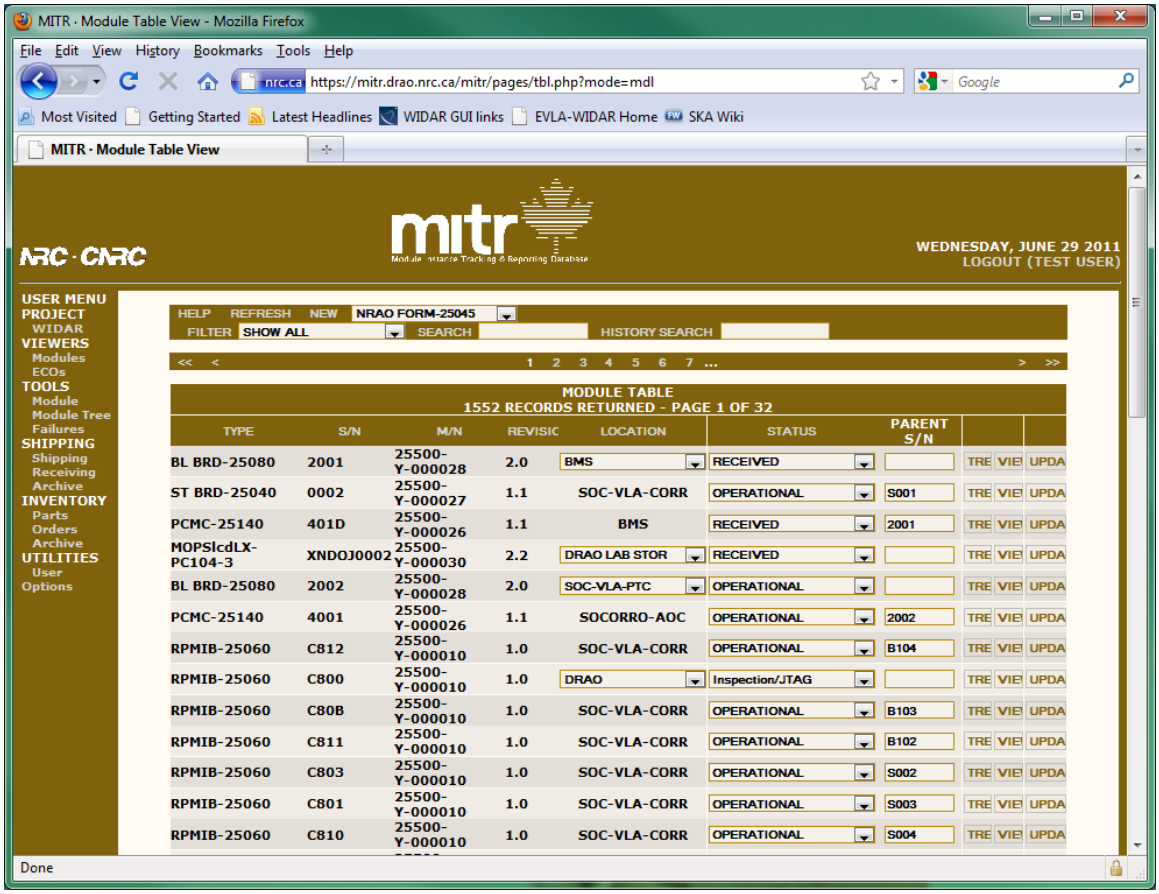

Figure 5-38 MITR main screen obtained by clicking on "VIEWERS—Modules". "CTRL+" increases the font size in the display, and "CTRL-" decreases font size.

Clicking UPDATE on one particular module, brings up the main module instance information/data entry screen (it is long so it must normally be scrolled through), partially shown in several figures on the next couple of pages (Figure 5-39 and Figure 5-40). In the Procedures section is listed a non-modifiable list of all Procedures defined for the module type, and then a section where one or more instances of each Procedure can be instantiated and tracked. These were primarily used for production testing and assembly, but additional procedures could be defined for other purposes for the duration of the module's lifetime. For example, if a module has a regular maintenance requirement, a new Procedure could be instantiated for each maintenance cycle, and any notes or images or documents resulting from any actions taken could be attached to the Procedure.

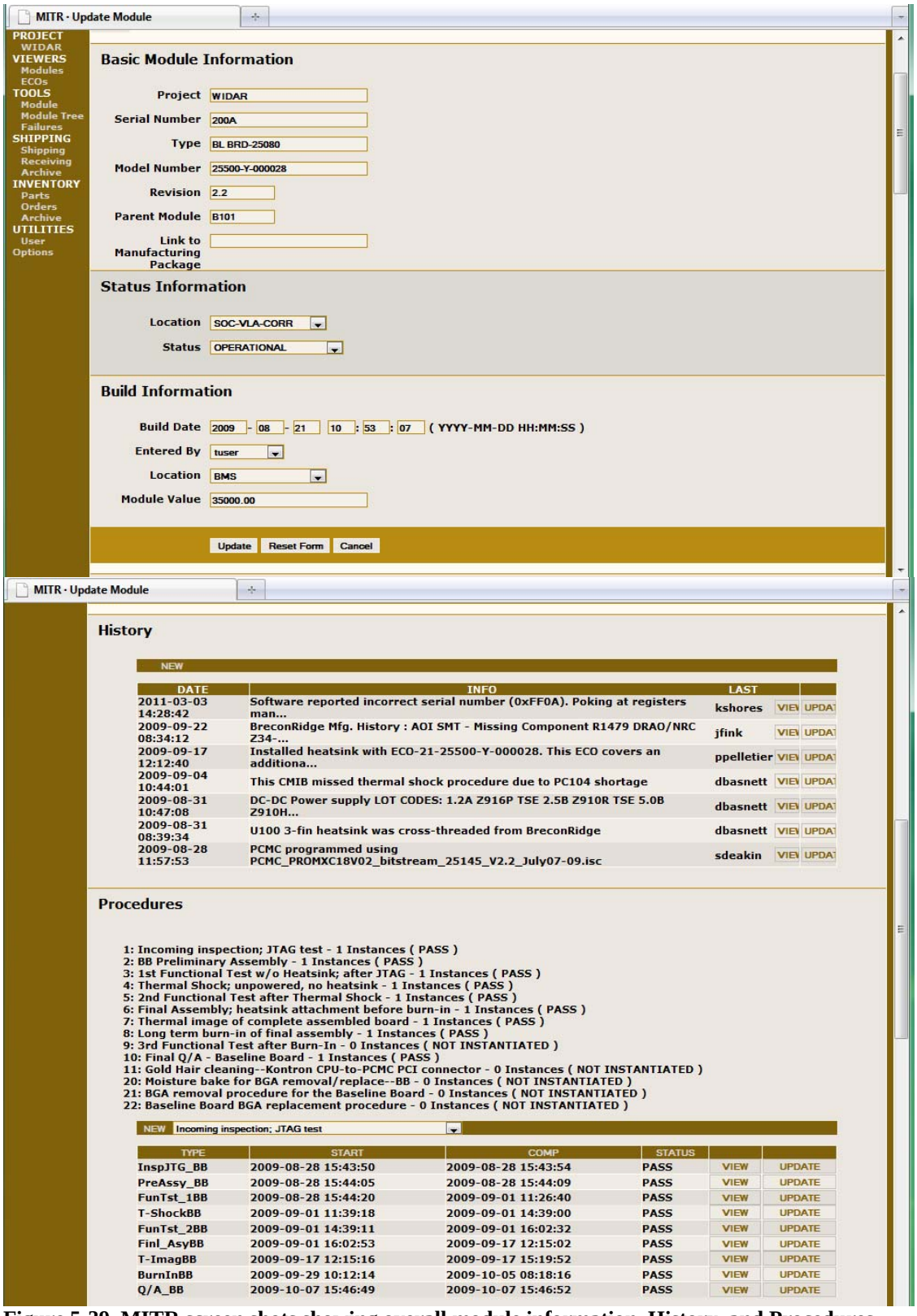

Figure 5-39 MITR screen shots showing overall module information, History, and Procedures. Status can be changed, History entries updated or added, and Procedures can be instantiated and executed.

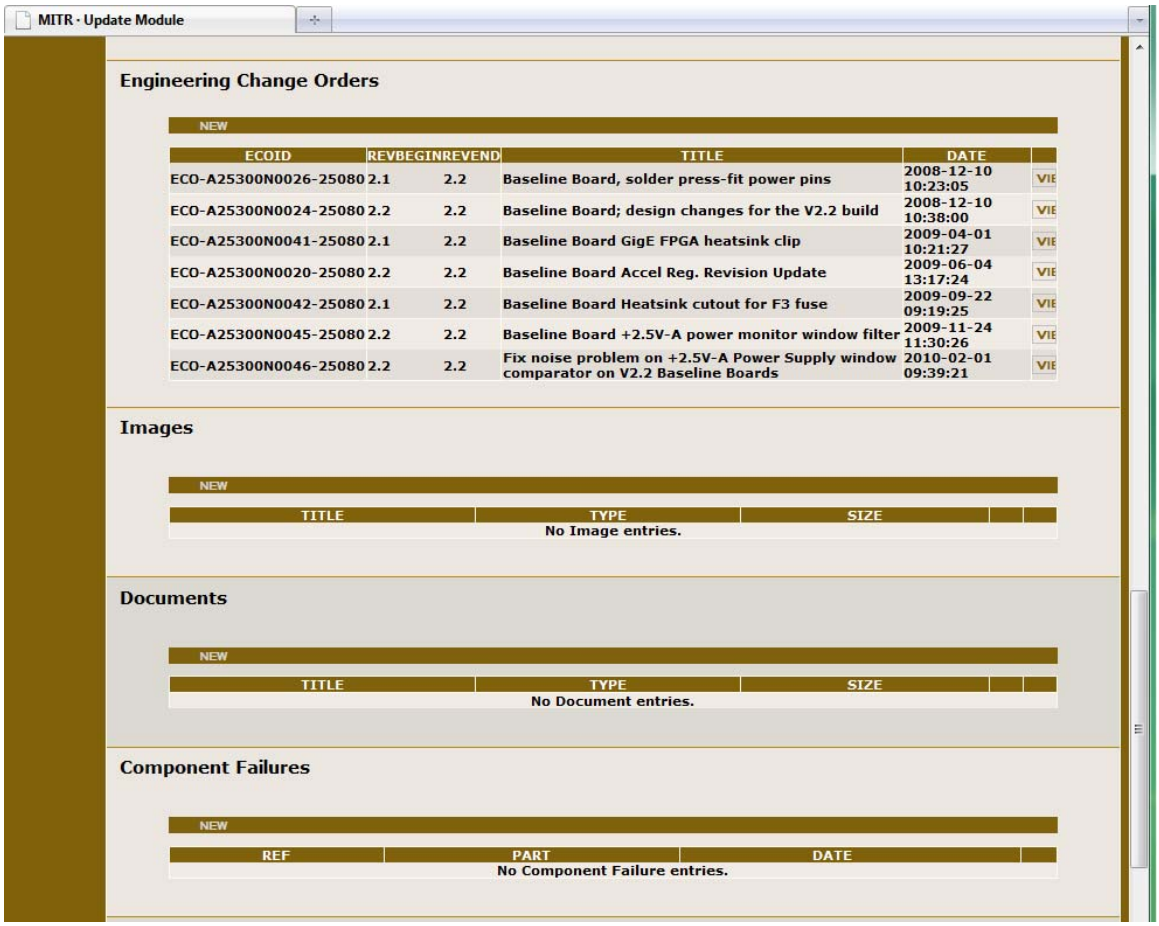

Figure 5-40 Section of Module page showing ECOs, and places where Images, Documents, and Component Failures can be added.

As mentioned, MITR can track and plot component failures vs time in various ways. A component is some widget with a part number, but normally not a serial number. One such plot, obtained by clicking on "Failures" in Figure 5-38, and filling in some drop boxes to select the part, lot number, time calculation bin etc. is shown in Figure 5-41.

Interested or potential users can explore MITRs features by obtaining a login account and working in the "SANDBOX" project, before going "live" on real modules in the WIDAR project.

Finally, to facilitate tracking of correlator system-level History (etc.) a module type called "**EVLA-CORR-SYSTEM**" has been created. Within this module type are Histories associated with the system, as well as attached Documents containing copies of all packing slips for all shipments to the VLA for the EVLA, and to Jodrell Bank Observatory for e-MERLIN. The WIDAR PROJECT (from the main screen click on "WIDAR" under "PROJECT") has major project-level documents attached, primarily having to do with shipping documentation templates etc. This (or the EVLA-CORR-SYSTEM) could be (but isn't, yet), a repository for correlator system documents which currently reside on the DRAO/EVLA web page.

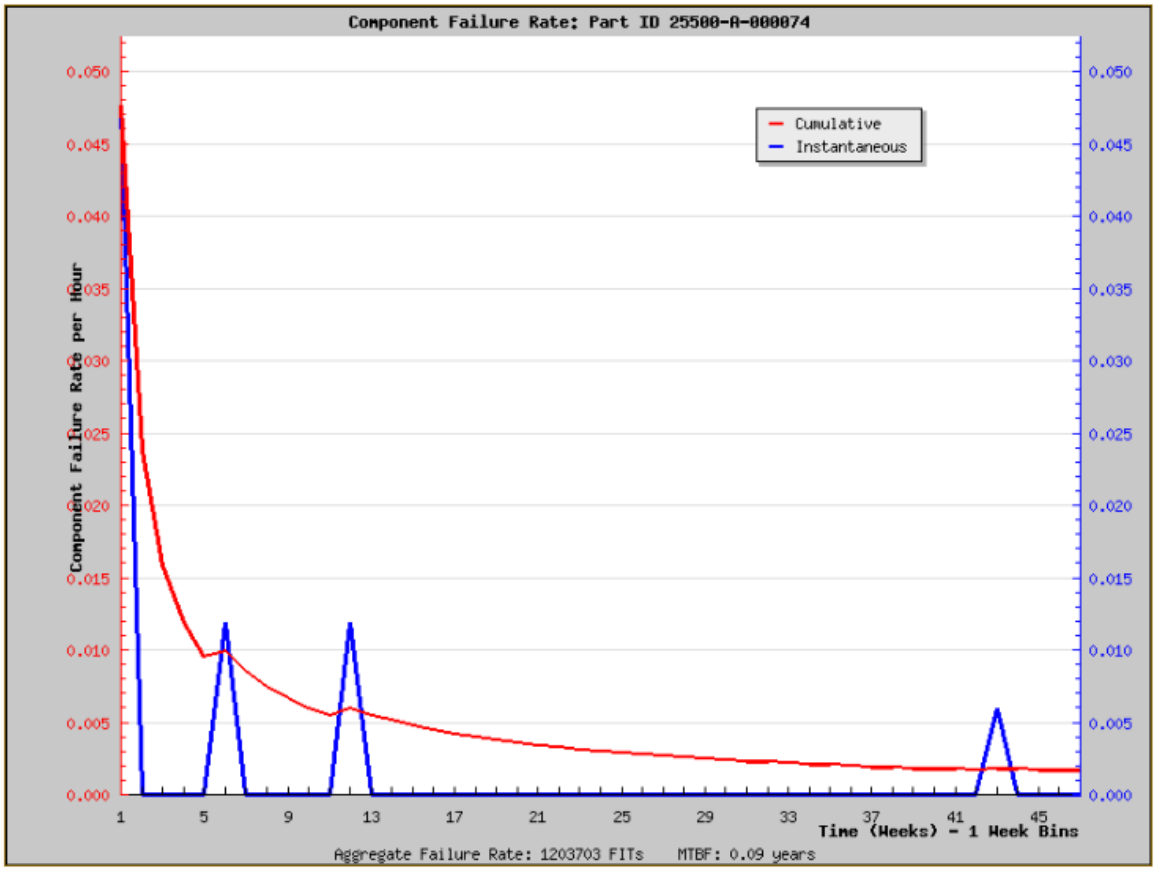

Figure 5-41 Example of MITR failure rate plot.

6 Interfaces

This section contains details of important intra-correlator interfaces. Interfaces to the outside world are primarily 1000Base-T Ethernet connections, with the exception of fiber connections from the antennas, and 10G fiber connections to the MkVc VLBI recorder from the CBE switch.

6.1 CPCC External Connections via Station rack RPMIBs

Spare capacity in Station rack RPMIBs is used to allow the CPCCs access to monitor and control of room-critical systems, including the smoke detectors and the HVAC systems. This section defines exactly where these M&C lines tie into RPMIBs in the system.

6.1.1 Smoke Alarm Connections

Stage-1 alert is wired into terminal "**SPR0**" (In-26) of the RPMIB in Station rack **S002**.

Stage-2 alert is wired into terminal "**SPR1**" (In-27) of the RPMIB in Station rack **S002**.

Stage-3 alert is wired into terminal "**SPR2**" (In-28) of the RPMIB in Station rack **S002**.

Refer to Table 6-2 for detailed RPMIB SCSI 100-pin cable mapping to NI6509 card I/Os, and RPMIB terminal blocks. Refer to Figure 5-32 for a close-up view of an RPMIB.

Each RPMIB PCB has all terminal block pins clearly labeled. Additionally, smoke alarm monitor outputs are open-collector, and so a pull-up resistor is routed from control output "**6U-9**" to each of the above inputs, and that output is turned ON so as to provide pullup capability. The CPCC GUI is built to not allow the user to inadvertently turn off this output, which would trigger a Stage-3 smoke alarm condition, leading to the immediate shutdown of the correlator (section 7.1.1.2). As both CPCC-1 and CPCC-2 drive this line, it is tolerant to a single CPCC or NI6509 failure. If both CPCCs go down, well, the system is down anyway.

It is important to note that -48 VDC power to S002 can completely fail, and these monitor connections and pull-ups would remain active and in effect, as they are driven by the CPCC NI6509 cards.

6.1.2 HVAC M&C Connections

HVAC M&C connections are tied into the CPCCs via Station rack **S001** RPMIB. Connections are according to the following table. Monitor lines are similarly open-collector, and the same "**6U-9**" output of the RPMIB, tied to the 4 monitor inputs via pull-up resistors, provides the necessary pull-up. The user is similarly prevented from fiddling with this output.

Signal	S001 RPMIB Terminal
DX-1 Power ON/OFF (active high)	Control output "**SPR0**" (Out-28)
DX-2 Power ON/OFF	Control output "**SPR1**" (Out-29)
CW-1 Power ON/OFF	Control output "**SPR2**" (Out-30)
CW-2 Power ON/OFF	Control output "**SPR3**" (Out-31)
DX-1 Alarm (active high=Alarm condition)	Monitor input "**SPR0**" (In-26)
DX-2 Alarm	Monitor input "**SPR1**" (In-27)
CW-1 Alarm (active high=Alarm condition)	Monitor input "**SPR2**" (In-28)
CW-2 Alarm	Monitor input "**SPR3**" (In-29)

Table 6-1 HVAC system M&C lines tied into Station rack S001 RPMIB.

6.2 CPCC to -48 VDC Power Plant Communications

As indicated in Figure 4-1, a 100Base-T Ethernet (RJ-45 UTP) connection is made between the -48 VDC Power Plant, and the "Central 1G Switch" in the correlator room. Each CPCC connects into this switch with 1000Base-T Ethernet. It is only the AC fail condition that the CPCC triggers on, and interactions between the CPCCs and the Power Plant are described in more detail in section 7.1.1.

CPCCs monitor the power plant via SNMP (Simple Network Management Protocol) and HTTP. The IP addresses of the two CPCCs are registered with the power plant to receive SNMP Traps via UDP when an alarm condition is detected.

6.3 RPMIB SCSI-100 Pin Connector Pinout

Table 6-2 contains details of SCSI-100 pin connector pinouts at the RPMIB, and how these map to terminal block contacts and NI6509 cards installed in the CPCCs. The RPMIB terminal block contacts are labeled with text representing the "Rack connection", rather than the "RPMIB screw terminal", as might be assumed from the table. In some cases in documentation, these are used inter-changeably, but they all reference this table.

6.4 ext-TC Fiber and 128 MHz Reference Clock Interface

As indicated in Figure 5-14, the external EVLA-system-supplied ext-TC fiber and 128 MHz reference clock enter the system at two locations, S004-x-slot 0 ("Timecode A"), and S005-x-slot 7 ("Timecode B"). As the XBB entry ports are via their front panels, each Station rack is equipped with a bulkhead PCB which these signals can "feedthru" connect through. The ext-TC fiber is a "MT-RJ" connector, and the receiver module on the XBB is an Avago AFBR-5903Z FDDI/Fast Ethernet optical transceiver module. The 128 MHz input is an SMA socket connector, terminated on the XBB, with nominal input level of 0 dBm (range is -6 dBm to +9 dBm).

Outputs/Control					Inputs/Monitor			
Pin #	**NI 6509 Port**	**RPMIB terminal**	**Rack connection**		**Pin #**	**NI 6509 Port**	**RPMIB terminal**	**Rack connection**
47	P0.0	Out-0	Crate 0, Slot 0		97	P6.0	In-0	Crate 0, Slot 0
45	P0.1	Out-1	Crate 0, Slot 1		95	P6.1	In-1	Crate 0, Slot 1
43	P0.2	Out-2	Crate 0, Slot 2		93	P6.2	In-2	Crate 0, Slot 2
41	P0.3	Out-3	Crate 0, Slot 3		91	P6.3	In-3	Crate 0, Slot 3
39	P0.4	Out-4	Crate 0, Slot 4		89	P6.4	In-4	Crate 0, Slot 4
37	P0.5	Out-5	Crate 0, Slot 5		87	P6.5	In-5	Crate 0, Slot 5
35	P0.6	Out-6	Crate 0, Slot 6		85	P6.6	In-6	Crate 0, Slot 6
33	P0.7	Out-7	Crate 0, Slot 7		83	P6.7	In-7	Crate 0, Slot 7
31	P1.0	Out-8	Crate 1, Slot 0		81	P7.0	In-8	Crate 1, Slot 0
29	P1.1	Out-9	Crate 1, Slot 1		79	P7.1	In-9	Crate 1, Slot 1
27	P1.2	Out-10	Crate 1, Slot 2		77	P7.2	In-10	Crate 1, Slot 2
25	P1.3	Out-11	Crate 1, Slot 3		75	P7.3	In-11	Crate 1, Slot 3
23	P1.4	Out-12	Crate 1, Slot 4		73	P7.4	In-12	Crate 1, Slot 4
21	P1.5	Out-13	Crate 1, Slot 5		71	P7.5	In-13	Crate 1, Slot 5
19	P1.6	Out-14	Crate 1, Slot 6		69	P7.6	In-14	Crate 1, Slot 6
17	P1.7	Out-15	Crate 1, Slot 7		67	P7.7	In-15	Crate 1, Slot 7
15	P2.0	Out-16	6U Crate Slot 0		65	P8.0	In-16	6U Crate Slot 0
13	P2.1	Out-17	6U Crate Slot 1		63	P8.1	In-17	6U Crate Slot 1
11	P2.2	Out-18	6U Crate Slot 2		61	P8.2	In-18	6U Crate Slot 2
9	P2.3	Out-19	6U Crate Slot 3		59	P8.3	In-19	6U Crate Slot 3
7	P2.4	Out-20	6U Crate Slot 4		57	P8.4	In-20	6U Crate Slot 4
5	P2.5	Out-21	6U Crate Slot 5		55	P8.5	In-21	6U Crate Slot 5
3	P2.6	Out-22	6U Crate Slot 6		53	P8.6	In-22	6U Crate Slot 6
1	P2.7	Out-23	6U Crate Slot 7		51	P8.7	In-23	6U Crate Slot 7
48	P3.0	Out-24	6U Crate Slot 8		98	P9.0	In-24	6U Crate Slot 8
46	P3.1	Out-25	6U Crate Slot 9		96	P9.1	In-25	6U Crate Slot 9
44	P3.2	Out-26	DC SSR 1		94	P9.2	In-26	Spare-0
42	P3.3	Out-27	DC SSR 2		92	P9.3	In-27	Spare-1
40	P3.4	Out-28	Spare-0		90	P9.4	In-28	Spare-2
38	P3.5	Out-29	Spare-1		88	P9.5	In-29	Spare-3
36	P3.6	Out-30	Spare-2		86	P9.6	In-30	Spare-4
34	P3.7	Out-31	Spare-3		84	P9.7	In-31	Spare-5
32	P4.0	FPGA hdr	DCLK		82	P10.0	FPGA hdr	CONF_DONE
30	P4.1	FPGA hdr	DATA0		80	P10.1	N/A	ID B0
28	P4.2	FPGA hdr	ASD		78	P10.2	N/A	ID B1
26	P4.3	FPGA hdr	nCS		76	P10.3	N/A	ID B2
24	P4.4	FPGA hdr	nCE		74	P10.4	N/A	ID B3
22	P4.5	FPGA hdr	nCONFIG		72	P10.5	N/A	ID B4
18	P4.6		unused		70	P10.6	N/A	ID B5
18	P4.7		unused		68	P10.7	N/A	unused
16	P5.0	N/A	Fan speed B0		66	P11.0	N/A	-48 V mon
14	P5.1	N/A	Fan speed B1		64	P11.1	N/A	Fan-1 mon
12	P5.2	N/A	Fan speed B2		62	P11.2	N/A	Fan-2 mon
10	P5.3	N/A	Fan speed B3		60	P11.3	N/A	Fan-3 mon
8	P5.4	N/A	Fan speed B4		58	P11.4	N/A	Fan-4 mon
6	P5.5		unused		56	P11.5		unused
4	P5.6		unused		54	P11.6		unused
2	P5.7		unused		52	P11.7		unused

Table 6-2 RPMIB SCSI connector pinouts, and mapping to NI6509 ports and RPMIB terminals.

6.5 Cross-Bar Board FPGA Programming Header Interface

The bulkhead PCB mounted to the far left in each Station rack 6U crate, used for entry of the external 128 MHz and ext-TC fiber signal, also contains a 14-pin, 2 mm header used for routing FPGA programming signals sourcing from CPCCs, and present on the RPMIB 14-pin header. Each Station rack contains a 14-pin ribbon cable routing from the RPMIB header to the bulkhead PCB. This ribbon cable is visible in Figure 5-20.

Looking into the front of a Station rack 6U crate, a ribbon cable, with bussed headers for each Cross-Bar Board, is plugged into this header. When Cross-Bar Board FPGA EEPROMs need to be re-programmed, these headers are plugged into every Cross-Board Board front-panel mating headers, and programming proceeds as defined in section 7.1.2. Once programming is complete, remove connections from Cross-Bar Board headers.

Refer to the Cross-Bar Board User Manual [A25121N0001], section 6.4 for details regarding this programming header.

6.6 Station Board Interfaces

This section provides a brief summary of interfaces on the Station Board.

6.6.1 Station Board PCMC EEPROM Programming Header

There are two 14-pin 2 mm headers accessible via the front-panel of the Station Board. The "JTAG BOARD TEST" header is for test purposes and is NEVER used. The "JTAG CMIB ROM" is a header used to program the PCMC module's FPGA EEPROM, the first time the board is turned on, and should the PCMC EEPROM ever be corrupted[22]. Refer to the Station Board User Manual [A25040N0001] for details on how to program the PCMC EEPROM via this header.

To re-program the PCMC EEPROM via the CMIB, click on the "CPU" icon of the "Main" tab in the top-level Station Board GUI, check "Enable PCMC PROM for Programming", press the "Program PCMC" button, and wait for completion. To enable this capability, there must a link called "pcmc.svf", in the directory where all other board FPGA binary links are, pointing to the .svf file for the PCMC FPGA.

6.6.2 DTS Receiver (a.k.a. FORM) Module Fiber

A DTS Receiver module is installed in each Station Board in the system. There are 3 fiber ports to the module, and they jut out through the front panel of the Station Board. They are connected to antenna fiber signals, with mapping to Station Boards as defined in Table 5-1. The content, format, and physical characteristics of these connections are beyond the scope of this document and further detail can be found in DTS Receiver module documentation.

[22] The PC/104+ CPU can in-system program this EEPROM via the PCMC FPGA itself. If, however, the EEPROM is ever corrupted, it can only be programmed via this interface.

6.6.3 DTS Receiver CMIB 100Base-T Ethernet

Each DTS Receiver module contains a CMIB ("Correlator Monitor Interface Board", a PC/104+ CPU module), and the primary connectivity from this module to the rest of the system is via a Station Board front-panel RJ-45 connection, running 100Base-T Ethernet. Each of these ports connects to the M&C switch, as shown in Figure 4-1. Protocol on this link is XML on TCP/IP.

6.6.4 Station Board CMIB 100Base-T Ethernet

Each Station Board contains its own CMIB, and the primary connectivity from this module to the rest of the system is via a front-panel RJ-45 connection, running 100Base-T Ethernet, and tying into the M&C switch. Protocol on this link is XML on TCP/IP. XML schema is defined in TBD.

6.6.5 Station Board Rear ERNI Connections

There are 3, 36-row x 4 pair ERNI connectors at the rear of each Station rack crate. The Top and Bottom connectors are for future expansion (unused/unpopulated "VSI" interfaces), and the Center connector is used to output data—in "HM Gbps" protocol format—to the Cross-Bar Boards and for "st-TC" Timecode access. Board power control and monitor, as well as -48 VDC is provided by the TOP (control) and BOTTOM (monitor) ERNI power connectors. Refer to the Station Board User Manual [A25040N0001] and Figure 5-18 for more details on connector pin-outs.

6.6.6 Station Board USB Connector

The Station Board front panel contains a USB connector, which is connected to the main Station Board CMIB (PC/104+) USB port via a cable. There have been issues with this cable/connector combination causing noise on the USB lines on the PC/104+ card (and generating CPU interrupts) as there is no provision for grounding the cable at the PC/104+ end. Installing a memory stick seems to resolve these issues. Refer to the Station Board User Manual [A25040N0001] for further details of PC/104+ USB connector locations and pin-outs.

6.7 Cross-Bar Board Interfaces

The Cross-Bar Board (XBB) is a 6U x ~160 mm card, and 8 of these are installed in the 6U crate in every Station rack. This section provides a brief summary of the interfaces on this card.

6.7.1 XBB Front Panel Interfaces

The front panel of the XBB contains two SMA connectors, an "MT-RJ" connector, and a 14-pin 2 mm header. The SMA connectors are for 128 MHz clock in and out; the "out" clock always sources from the board's local 128 MHz oscillator, and is used for testing and keep-alive purposes in the system. The "in" clock is used for fiber (ext-TC) signal clocking and master reference input (and only selected if the fiber signal is active), and in

some cases (i.e. if populated in slots 0 and 7), looping the "out" to the "in" clock provides the XBB with a backup clock source if the wafer clock input fails (see description on page 36). Refer to Figure 5-1, and Table 5-2 of the XBB User Manual [A25121N0001] for further detailed information on "Function-1" clocking.

The MT-RJ connector is used for insertion of the "ext-TC" fiber signal into the correlator. Refer to section 5.5 for further information on Timecode fiber insertion into the correlator.

The 14-pin 2 mm header is for FPGA EEPROM programming, with connections to the 6U crate left-mounted PCB bulkhead board for programming via the CPCC (section 7.1.2). Refer to the XBB User Manual [A25121N0001] for details on header pin-outs, and **important** information on jumper settings required for different programming options.

6.7.2 XBB Rear ERNI Connections

There are 2, 36-row x 4-pair connectors and power connectors at the rear of the board, with physical attributes and critical electrical connectivity[23] identical to Station Board and Baseline Board connectors. Each 36-row connector is for inputs and outputs to a cross-bar FPGA on the board (running the "HM Gbps" protocol), and for st-TC Timecode distribution. Two ERNI power connectors are provided, the bottom connector provides -48 VDC power entry (the top connector power entry pins are not used), but both of these are used for power supply control (TOP) and monitor (BOTTOM). Refer to Figure 5-18, and the XBB User Manual [A25121N0001] for more detailed information on the pin-outs of these connectors.

6.7.3 XBB Front-Panel LEDs and Status Signaling

The front panel LEDs of the XBB provide information on the status of HM Gbps and Timecode receivers. This state of front-panel LEDs is also available as output STATUS messages sent in the CTRL stream of all output wafers. Refer to the XBB User Manual for details on status LED coloring, and STATUS message content.

6.8 Baseline Board Interfaces

This section provides a brief summary of interfaces on the Baseline Board.

6.8.1 Baseline Board PCMC EEPROM Programming Header

There are two 14-pin 2 mm headers accessible via the front-panel of the Baseline Board. The "JTAG BOARD TEST" header is for test purposes and is NEVER used. The "JTAG CMIB ROM" is a header used to program the PCMC module's FPGA EEPROM, the first

[23] i.e. so as to avoid the possibility of a short circuit if boards are plugged arbitrarily into mating connections.

time the board is turned on, and should the EEPROM ever be corrupted[24]. Refer to the Baseline Board User Manual [A25080N0001] for details on how to program the PCMC EEPROM via this header.

To re-program the PCMC EEPROM via the CMIB, click on the "PCMC" icon in the top-level Baseline Board GUI, check "Enable PCMC PROM for Programming", press the "Program PCMC" button, and wait for completion. To enable this capability, there must a link called "pcmc.svf", in the directory where all other board FPGA binary links are, pointing to the .svf file for the PCMC FPGA.

6.8.2 Baseline Board CMIB 100Base-T Ethernet

Each Baseline Board contains its own CMIB, and the primary connectivity from this module to the rest of the system is via a front-panel RJ-45 connection, running 100Base-T Ethernet, and tying into the M&C switch. Protocol on this link is XML on TCP/IP.

6.8.3 Baseline Board Rear ERNI Connections

There are 2, 36-row x 4 pair ERNI connectors at the rear of each Baseline rack crate. The BOTTOM connector is often referred to as the "X" input, and is the primary input for signals (running the "HM Gbps" protocol) sourcing from XBBs, or adjacent Baseline Boards, and is secondarily for real-time streaming phased-array output from the Upper and Lower RXP FPGAs. The TOP connector is often referred to as the "Y" output, and used to daisy-chain distribute (HM Gbps protocol) data to other Baseline Boards' X inputs. (It is possible for the board to be configured to use the Y connector as an input—refer to the Baseline Board User Manual [A25080N0001] for more information on this option.) Board power control and monitor, as well as -48 VDC is provided by the TOP (control) and BOTTOM (monitor) ERNI power connectors. Refer to Figure 5-24 for more details on connector pin-outs.

6.8.4 Baseline Board USB Connector

The Baseline Board front panel contains a USB connector, which is connected to the CMIB (PC/104+) USB port via a cable. There have been issues with this cable/connector combination causing noise on the USB lines on the PC/104+ card (and generating CPU interrupts) as there is no provision for grounding the cable at the PC/104+ end. Installing a memory stick seems to resolve these issues. Refer to the Baseline Board User Manual [A25080N0001] for further details of PC/104+ USB connector locations and pin-outs.

6.8.5 Baseline Board SFP1 1000Base-T Ethernet

This SFP port connects to the GigEthernet FPGA on the board and is strictly for 1000Base-X connectivity and protocol between the SFP module and the FPGA with NO

[24] The PC/104+ CPU can in-system program this EEPROM via the PCMC FPGA itself. If, however, the EEPROM is ever corrupted, it can only be programmed via this interface.

AUTO-NEGOTIATION[25]. Boards come equipped with a 1000Base-T SFP module installed in this port, but a fiber module could be installed if desired. This port exclusively contains "lag frames", sourcing from on-board LTAs, but, depending on GigE FPGA settings, could optionally also contain phased-array VDIF frames. For 1000Base-T, only STP or UTP "cat5e" or better copper cable can be used.

The output lag frame (a.k.a. "LTA frame") format is shown in Figure 6-1. Refer to the LTA FPGA RFS [A25091N0000] for detailed descriptions of each bit field.

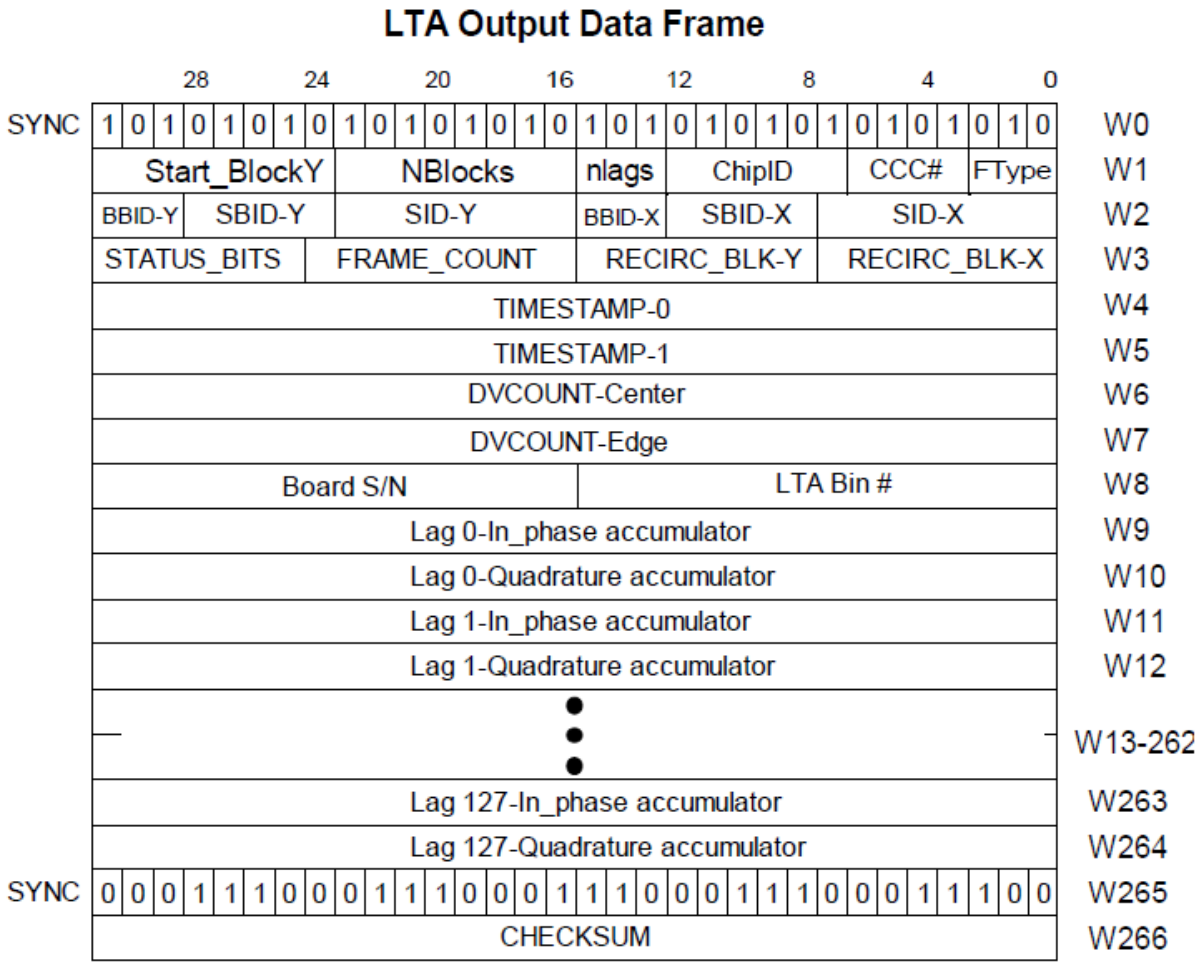

Figure 6-1 LTA "lag frame" format. The first SYNC word is "aaaaaaaa", is Endian independent, and can be used to determine the start of frame in memory or in a file, allowing software to dynamically determine how frame bytes are deposited in memory.

Bytes of the frame are transmitted from left to right, top to bottom of the above figure, in the UDP/IP payload, and are therefore transported "Big Endian".

[25] If a module that requires auto-negotiation is installed in the SFP port, no connectivity is possible, as the FPGA doesn't understand or implement auto-negotiation protocol (1000BASE-X IEEE 802.3-2005, Clause 37).

Note that code in the GigE FPGA is built to respond to PAUSE frames from the switch to implement traffic flow control, although generally such capability seems to never be used in Ethernet networks.

6.8.6 Baseline Board SFP2 1000Base-T Ethernet

This SFP port has identical connectivity and rules as SFP1, except that it is used for VDIF data transport only. The VDIF frame contains an 8-word header, followed by a variable-length frame. All of this is encapsulated in a UDP/IP frame for transport on Ethernet.

The VDIF header is shown in Figure 6-2. The UDP/IP frame within which the VDIF frame is embedded contains VDIF bytes reading from the above figure from right to left, as per the VDIF protocol Little Endian specification requirement. Further details of the VDIF protocol can be found in the RXP FPGA RFS [A25093N0000] and the VDIF protocol specification [VDIF].

VDIF Header

	Bit 31 (MSB) Byte 3		Byte 2	Byte 1	Byte 0 Bit 0 (LSB)
Word 0	I_1	L_1	Seconds from reference epoch$_{30}$		
Word 1	Un-assigned$_2$		Ref Epoch$_6$	Data Frame # within second$_{24}$	
Word 2	V_3		$\log_2$(#chns)$_5$	Data Frame length (units of 8 bytes)$_{24}$	
Word 3	C_1	bits/sample-1$_5$	Thread ID$_{10}$	Station ID$_{16}$	
Word 4	EDV$_8$			Extended User Data$_{24}$	
Word 5	Extended User Data$_{32}$				
Word 6	Extended User Data$_{32}$				
Word 7	Extended User Data$_{32}$				

Figure 6-2 VDIF header. Bytes are transmitted reading right to left in the above figure, as required by the VDIF specification.

6.8.7 Baseline Board XPAK 10G Ethernet Port

A blank XPAK 10G port is provided to allow for field upgrade to 10G Ethernet. Full instructions for performing this conversion are contained in section 8.1 of the GigE FPGA RFS document [A25092N0001].

6.9 RPMIB Rack Fan Connections

The RPMIB (Figure 5-32) contains a terminal block specifically for rack ran wiring connections. Each contact on this terminal block is labeled (on the PCB) to indicate the fan number, function, and the wire color (Red—**V+**, Black—**V-**, White—**C**ontrol,

Green—**M**onitor) that is to be connected to it. At the other end, in the fan carriage assembly and the removable fan trays, these 4 wires are connected into the mating terminal blocks in a specific (color) sequence which must be maintained for any replacement fan trays.

IMPORTANT NOTE: For the EBM-Papst fan itself, White is the tachometer output (monitor), and Yellow is the speed control (control), which is *opposite* to RPMIB wiring colors, and M&C wires exiting the RPMIB for the fan.

6.10 RPMIB Monitor and Control Terminal Blocks; Control Time Constants

Terminal blocks on the RPMIB are connected to rack crate-slots as determined by Table 6-2, and clearly labeled on the RPMIB PCB. The White wires in these terminal blocks are TTL control lines, connecting to crate-slot TOP screw terminals, and the Yellow wires in these terminal blocks are TTL monitor lines, connecting to crate-slot BOTTOM screw terminals.

Each control input of each crate's board contains series resistors and parallel capacitors to filter these TTL control signals to varying extent, as follows.

The Station Board has an RC time constant of 6.5 msec for the main PCB power supplies, but a lesser time constant of 65 μsec for the solid-state relay providing the DTS Receiver mezzanine card with a -48 VDC supply.

The Cross-Bar Board has an RC time constant of 3.7 msec.

The Baseline Board has an RC time constant of 3.7 msec.

The monitor lines source from the AND of voltage window monitors on each board—if any window monitor on the board indicates the voltage is not within acceptable *range*[26], the board's monitor line will go low.

There is sometimes a noise problem with these window monitors, causing these resultant monitor lines to, at times, oscillate. Thus, only if a monitor line is consistently low for some period of time (say, 1 second, sampled every 10 msec interrupt), should it be assumed that the line is actually low.

6.11 Rack -48 VDC Breaker Panel, and -48 VDC Board Connections

The inside of the Station and Baseline rack breaker panel is shown in Figure 5-29, and general details of connectivity, grounding, transient, and over-current protection is shown in Figure 5-27. Details of breaker panel connections (i.e. mapping of breakers to crates and slots) can be determined by referring to labeling on the removable breaker panel cover (not shown in Figure 5-29).

[26] i.e. it does not just indicate if the power supply is dead, but rather if the power supply output is in acceptable range.

Each Station Board and Baseline Board has dual -48 VDC entry contacts in the upper and lower connectors, and these are connected together with short sections of PCB specifically for this purpose. Thus, only two wires (-48 VDC HOT, and -48 VDC RETURN) route from each slot back to the breaker panel.

The entire 6U crate of 8 Cross-Bar Boards have their -48 VDC entry contacts connected together with another special-purpose screw-mount PCB, and there is only one pair of wires for the *entire* 6U crate which routes back to the breaker panel.

7 Monitor and Control

7.1 CPCC Monitor and Control

This section provides some details on CPCC monitor and control. Refer to section 5.8 for a functional description of the CPCCs, and how they connect to the correlator. Refer to the CPCC User Manual for further information on CPCC implementation, configuration, and network interface details.

7.1.1 Autonomous CPCC Operation

The CPCC GUI (section 5.3) allows the operator (or anyone able to access the CPCC GUIs with appropriate permissions) to monitor and control each board in the system, correlator rack fans, and HVAC systems in the correlator room. To provide for 24/7 operation and protection, however, the CPCCs are programmed to take automatic action when exception conditions occur. These exceptions include loss of AC mains to the -48 VDC power plant, board over-temperature, and smoke detector alarms.

7.1.1.1 AC Mains Failure

AC mains to the -48 VDC power plant is monitored via the network, through the Central 1G Switch. CPCCs are tied into this switch, as is a 10Base-T connection to the -48 VDC power plant. The CPCCs monitor the power plant via SNMP (Simple Network Management Protocol). The IP addresses of the CPCCs are registered with the power plant to receive SNMP Traps via UDP when alarm conditions are detected. AC power fail is one such alarm that is sent to registered users, and it is the only condition to which CPCCs autonomously take action.

When an AC fail condition is detected, the following actions are taken:

1. An alert is sent to the operator, and timers are start for further action (on timeout) if power is not restored in time. Nothing is done to affect operation of the correlator immediately. If power is restored within the first 5 minutes, all timers are stopped/reset, and the operator is alerted that the system is still operational.

2. After 5 minutes of AC fail, the CPCCs commence staged deprogramming of all FPGAs on Station Boards and Baseline Boards, except PCMC FPGAs to facilitate monitoring of board temperatures. This reduces the power load to about 1/3rd of its normal operating value to increase battery life, while maintaining power to the boards. During this time, fan speeds are adjusted down to try to maintain current board temperatures.

3. If power is restored after FPGA de-programming takes place, but while the boards are still powered up, the CPCCs automatically reboot the CMIBs and the operator is informed of this event.

4. After 15 minutes of AC fail (normally only occurring if there will be a prolonged power failure), staged power shut down of the correlator boards commences, and finishes within 60 seconds.

5. When the power plant indicates the AC fail condition is cleared (i.e. AC is restored), the operator is informed, and it is up to the operator to bring the system back up manually via the CPCC GUI. This ensures that the system is only brought back up when it is believed that it will be stable for an extended period, so as to minimize system power cycles throughout its lifetime.

During this entire time, the -48 VDC power plant operates autonomously, and the CPCC acts only on AC fail/restore messages. If, at any time, the power plant output voltage drops below a certain point (as set via the power plant front-panel control panel, and currently set to -40 V), the power plant will automatically disconnect batteries and shutdown to protect from excessive battery drain and an under-voltage condition.

7.1.1.2 Smoke Detection

The correlator room fire detection system consists of three stages of alert notification:

- Supervisory (CPCC 'Stage 1') is triggered by events in the alarm monitoring system itself such as alarm box doors being opened. It is also triggered by the super sensitive 'sniffer' system.
- Smoke Detection Stage 1 (CPCC 'Stage 2') is triggered when smoke is detected in a single zone of the room.
- Smoke Detection Stage 2 (CPCC 'Stage 3') is triggered when smoke is detected in a second zone of the room.

CPCC Stage 1 alert is wired into pin IN-26 (Spare-0) on the RPMIB in Station Rack S002, CPCC Stage 2 alert is wired into S002 pin IN-27 (Spare-1), and Stage 3 is wired into S002 pin IN-28 (Spare-2). Refer to section 6.1.1 for RPMIB further wiring details.

When CPCCs detect either of the first two stages, the operator is notified but nothing is done to affect operation of the correlator. When Stage-3 is detected, staged shutdown of the correlator boards commences to be completed within the 60-seconds before all power is removed from the room.

Board shutdown sequence is: Baseline Boards first, top crate, all 8 racks, slots 0 – 7, 1.5 seconds between boards then bottom crate in the same fashion; Station Boards next (same sequence) then Crossbar Boards.

7.1.1.3 HVAC Alarm Status and Control

The CPCCs do not provide autonomous action when it comes to monitor and control of the HVAC units. Rather, the CPCCs monitor alarm status, and provide status indicator LEDs on the CPCC GUI (Figure 5-5), and allow for HVAC systems to be powered on or

off via the same GUI. Refer to 6.1.2 for details on how HVAC alarm and power control lines are wired into Station rack RPMIB ports.

7.1.1.4 CPCC Automatic Rack Fan Speed Monitor and Control via RPMIB

CPCCs control the speed of rack fans using a 5-bit control word on the SCSI-100 cable sourcing from the NI6509 digital I/O cards installed in the CPCCs. These are the "Fan Speed B0-B4" signals shown in Table 6-2. The larger the binary setting of these lines, the slower the fans rotate. The maximum fan speed is ~2500 RPM, and so there is approximately a (after binary code inversion) 1:1 ratio between the fan speed setting and the speed of the fan. For example, a setting (in the CPCC top-level GUI—Figure 5-5) of 13 (binary 01101, inverted to 10010 to go to the RPMIB), results in a fan speed of ~1100 RPM.

In the EVLA system, however, forced air from the HVAC system normally keeps the fans spinning at least half-speed, independent of any speed setting.

CPCCs actively control fan speeds to maintain board heatsink temperatures (read and monitored via the CMIBs' reading of heatsink-mounted temperature sensors) below 40 ^{o}C, with a minimum fan speed setting of "20" (or 10100 binary; inverted is an actual setting of NI6509 output lines of "01011"). The minimum speed setting and selection of 40 ^{o}C is a tradeoff between keeping the boards cool, and longevity of fans. It is not possible to control individual fan speeds in a rack—they are all set the same.

Fan speeds are monitored by the CPCC, by counting pulses from the fan speed tachometer outputs, one for each fan ("Fan-1 mon", "Fan-2 mon" etc. of Table 6-2). The tachometer outputs are such that on these lines, there is a square-wave with 3 pulses (cycles) per revolution. Pulse width is inversely proportional to speed, with minimum waveform *period* approximately 7.5 milliseconds (1/8 msec x 60/3 ~=2500 RPM).

Due to HVAC blowers, a failed fan will never stop (unless there is a bearing seizure), and so the CPCC recognizes a failed fan when it is not running near the same speed as other fans in the rack. If a fan fails, airflow is decreased a bit, but the rack can continue to operate until such time as the fan is replaced.

7.1.1.5 Board Over Temperature Automatic Shutdown

For Station and Baseline Boards, there are two levels of automatic over-temperature shutdown. The first level is CPCC determined. The CPCC continuously reads board temperatures, and if the readings are consistent (i.e. not due to a failed or malfunctioning temperature sensor), and if a temperature of 55 ^{o}C[27] is reached, the CPCC shuts down the board using the control line via the RPMIB. The CPCC does not automatically bring up the board—it is up to a human (operator) to choose to do so.

[27] This number, the 40 ^{o}C number, and the minimum fan speed setting of "20" mentioned in the previous section are set in CPCC software, and can be changed.

The second level of over-temperature shutdown is provided by dual redundant thermostats mounted on board heatsinks, each with a trip temperature of ~65 ^{o}C. If either one trips, the power supplies on the board are shutdown. Thus, in the worst case if all network communications is lost and the CPCCs can't talk to or control the boards, the boards automatically protect themselves from thermal runaway using this "deadman" mechanism.

Cross-Bar Boards have only the second level of over-temperature shutdown, with a trip temperature of 50 ^{o}C. This trip temperature was chosen as it is the point where the output cable driver chips would start to see significantly reduced lifetimes if it were sustained. The CPCC has no access to Cross-Bar Board temperature sensors, since such sensors do not exist.

7.1.2 Cross-Bar Board In-system FPGA Programming via CPCC1

The RPMIB contains a 14-pin 2mm header, which provides an access port for in-system programming of Cross-Bar Boards' (XBBs) FPGA boot EEPROM in Station racks (a null function in Baseline racks). This header is indicated in Figure 5-32.

A 14-pin ribbon cable runs from the header to a bulkhead board mounted in the 6U crate in each Station rack. Another cable bus-connects this bulkhead board header to all 8 headers accessed at the front of every XBB, within the 6U crate. Due to undesirable interactions between XBBs with this cable plugged in (refer to the XBB User Manual [A25121N0001] for details), the cable is sitting in each Station rack's 6U crate, but is not normally plugged into XBBs.

To in-system program XBBs, one Station rack at a time, plug the cable into the front-panel-accessed header for all 8 boards for the particular Station rack, open the "FPGA-cpcc1 GUI" (Figure 7-1) (accessed at the asg/widar web site: http://www.aoc.nrao.edu/asg/widar/), select the most recent Cross-Bar Board .rpd file, click on the "Erase" check box, select the Station rack to be programmed, right-click, and then left-click the "Start" button. Programming takes up to 5 minutes.

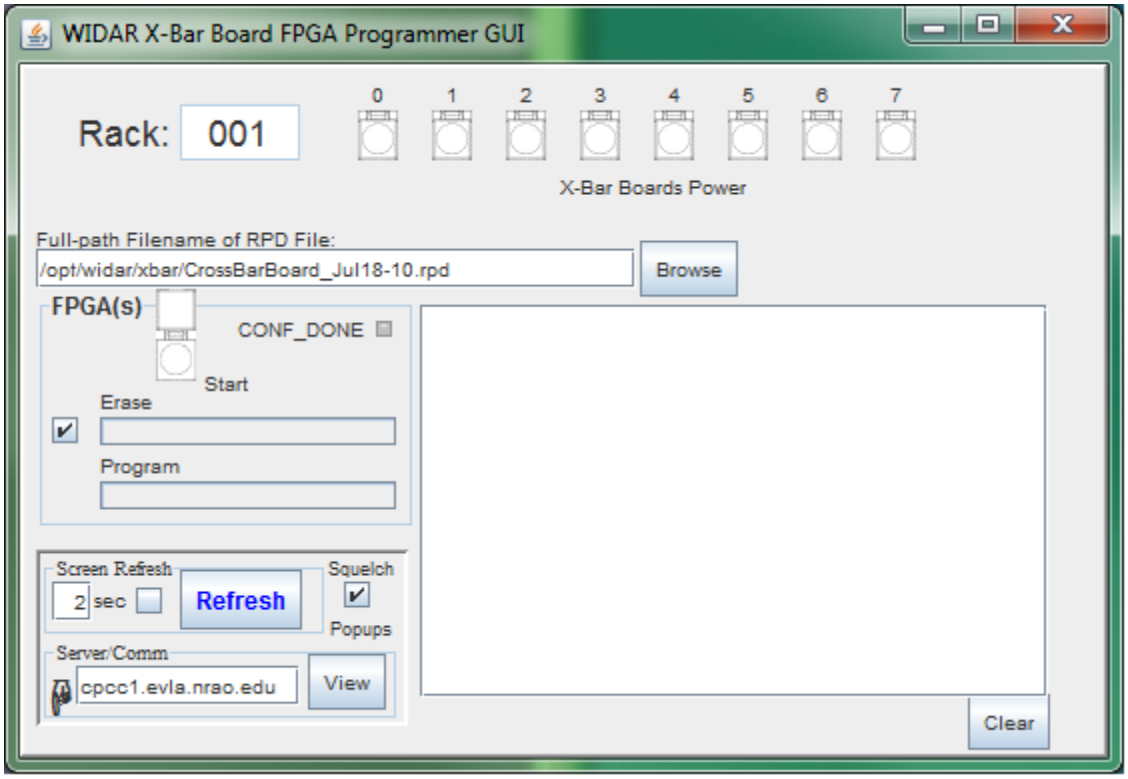

Figure 7-1 In-system XBB FPGA EEPROM programming GUI, ready to left-click the "Start" button.

When programming is complete and successful, the "CONF_DONE" LED in the GUI should be GREEN, although this is not always the case (for some strange reason). To determine if programming for the boards in that rack is successful, remove the programming cable from all the boards—this should cause them to re-load the new FPGA binary from the EEPROM and operate (LEDs flashing). If a board's EEPROM has not been successfully programmed, all LEDs except the power LEDs will be dark. Power cycle the board to try to boot, and if not successful, re-program using the above procedure any particular boards if necessary.

Programming can be performed only via CPCC1 (and the CPCC1 cable), as the RPMIB programming header is connected only to the CPCC1 cable.

Repeat for all 8 Station racks in the system until all Cross-Bar Boards are complete and active. Alternatively, each XBB can be individually programmed using the Altera "Byte-Blaster" cable, and controlling laptop computer. Refer to the XBB User Manual [A25121N0001] for information on XBB jumper settings for this option.

Note that re-programming XBBs in this way completely disrupts Timecode distribution to Station Boards, and clock and signal distribution to Baseline Boards. Thus, before executing this procedure, all Station Boards and Baseline Boards in the system should be set to "FPGAs de-programmed" to avoid unnecessary power bump, and confusing operation.

7.2 MCCC Monitor and Control

Details of MCCC M&C are beyond the scope of this document. For basic information, refer to section 5.13. For further detailed information, refer to the VCI Protocol Specification A25201N0000 and the Configuration Mapper RFS A25202N0000.

7.3 Setting Cross-Bar Board Switch Configurations

A particular XBB switch configurations is set by sending an appropriate XML message to a particular Station Board CMIB, which decodes the request and encodes a COMMAND message in the Timing FPGA to send to downstream XBBs on the COMMAND channel embedded in the desired sub-band wafer CTRL stream (see section 5.6).

From the XBB's cross-bar switch (i.e. FPGA) perspective, a COMMAND coming in on *any* of its 16 input wafers can affect any switch connection, and any Station Board has at least 1 wafer connection to each cross-bar switch in the rack (see Figure 5-17). What this means is that to establish any switch setting on any XBB within a rack, XML messages need only be sent to one Station Board in the rack. Furthermore, since switching is performed on a sub-band basis, and the XML message contains the sub-band number, all of the information is available to tell the software driver in that one Station Board, on which output wafer to send the switch COMMAND to affect the switch setting.

Refer to section 5.4.4 and the XBB User Manual [A25121N0001] for further details and rules regarding XBB switch settings.

7.4 CMIB CPU Booting, and Board Startup

The Station Board and Baseline Board CMIB PC/104+ CPU module (Kontron MOPSlcdLX-PC104-3 or MOPSlcdLX-PC104-5) uses "pxeboot", an Intel/DHCP protocol that allows a computer to request a boot image from the boot server. See:

http://www.pix.net/software/pxeboot/archive/pxespec.pdf

for more information.

When the board powers up, is soft-re-booted, or is reset by pressing the front-panel reset switch, the boot request goes out to the network, and provided a boot host is listening (Figure 4-1 "Boot Servers"), the host returns a boot image to the board. This boot image gets the board booted to a point where it can mount a root file system (RFS). This mounted file system (Linux), contains the required startup files so the board can finish its booting and configuration onto the network.

For all of this to work, the CPU's BIOS (accessed by using the video and keyboard ports of the PC/104+ module—refer to the MITR database "CMIB_setup" Procedure for further details on BIOS settings), must be set to enable "lanboot" or "pxeboot" as the first device tried for booting.

After the board is booted and has its core OS services running, the user software (all of the software task that monitor and control the board), is loaded and run. This also involves loading the MCB bus device driver for the PCMC (refer to the PCMC RFS document [A25145N0000] for information on PCMC devices).

After the PCMC MCB bus device driver is loaded, the board type (determined by reading 3 bits on the PCMC to motherboard 4 x 32 pin connector—see [A25080N0001]), and appropriate device driver software is loaded for that board type. On-board MCB interface FPGAs are then programmed, allowing the CPU to determine its rack-crate-slot (i.e. location), which is used to set its location-based IP address (see section 8.3).

A network lookup is then used to translate any other logical IP addresses to the location-based IP address. Typically a board is addressed logically as "rack-crate-slot.evla.nrao.edu" (e.g. b101-t-0.evla.nrao.edu is the board in the top crate, slot 0, of rack 101), but can also be accessed by its serial number (e.g. bb2006.evla.nrao.edu").

Once the CPU is booted and all device drivers are loaded, it proceeds to boot (startup) the motherboard, a step-by-step process which consists of programming the on-board FPGAs, and setting configurations. Startup is different for the Station Board and the Baseline Board. Refer to the Station Board [A25040N0001], and Baseline Board [A25080N0001] User Manuals for further details. Startup can be run by hand using the board GUIs, but is normally performed using an "auto-start" facility, pointing to an auto-start file, controlled by CMIB software. As there are 256 boards in the system, this is a very handy feature indeed. The top-level board GUIs have facilities for enabling auto-start capability.

Refer to CMIB software documentation for further details regarding CPU booting and board startup.

7.5 -48 VDC Power Plant

The -48 VDC power plant is a complete standalone system that does not require any external monitor and control capability. The only tie-in to the correlator is that there is a 10Base-T connection through the Central 1G Switch to the CPCCs (see Figure 4-1), to allow the CPCCs to be informed of an AC fail condition, and then to take appropriate action as described in section 7.1.1.1. For further details on -48 VDC power plant M&C, refer to appropriate Liebert and Emerson documentation.

8 System Settings and Configurations

This section contains details of system settings and configurations required for operation of the correlator. Primarily this means definition of how individual slot IDs are defined and set, and various RPMIB jumper settings, which also affect the system's ability to function.

8.1 Station Board Rack-Crate-Slot ID Settings

Looking into the rear of the Station rack, the top and bottom ERNI headers of the top and bottom 12U crates are where the RACK, CRATE, and SLOT ID jumpers are set. These jumpers are used to uniquely set the "rack-crate-slot" for each Station Board slot in the system. The Station Board CMIB reads these jumper values, and thereafter knows where it is located. The M&C Ethernet system is also set to logically refer to boards in terms of "rack-crate-slot" for easy logical addressing of boards. To avoid confusion, numerical rack-crate-slot IDs read by the CMIBs are translated logically into more human readable/understandable form. For example rack-crate-slot="1-0-6" translates to "s001-t-6".

Referring to Figure 5-18, far left-hand-side (and header breakout diagram), the top ERNI connector (in each 12 U crate), rows 35 and 36 (i.e. bottom 2 rows) pins are where the "CRATE ID" and "SLOT ID" are set. Settings are according to the following figure, extracted from the EVLA Correlator System Number Plan [A25010N0002]:

Jumper Installed? (X=YES)									
Unused		CID			SLOTID				
B7	B6	B5	B4	CPU read value	B3	B2	B1	B0	CPU read value
		X	X	0	X	X	X	X	0x0
		X		1	X	X	X		0x1
			X	2	X	X		X	0x2
				3	X	X			0x3
					X		X	X	0x4
					X		X		0x5
					X			X	0x6
					X				0x7

Figure 8-1 Station Board top ERNI connector jumper settings. An "X" indicates the jumper is installed. Identical settings are used for Baseline Boards.

Jumpers are installed between rows 35 and 36, in the same column, with bits starting at 0 reading from *right to left* as in the above diagram. If a jumper is installed, the CPU reads that bit as a zero. Thus, bits [B3:B0] are for the slot number (with slot numbering as shown in Figure 5-18, 0-7 reading right to left). The TOP 12U crate is set as crate "0" (both jumpers installed in bits B5, B4), and the BOTTOM 12U crate is set as crate "1" (B5=installed, B4=not installed) (referring to Figure 3-3 of [A25010N0002]). Crate IDs 2 and 3 are normally never used.

The Station Board rack ID is set using the bottom ERNI connector (refer to Figure 5-18), same rows 35 and 36, according to the top half of the following table:

		Jumper Installed? (X=YES)								
RID	**Rack Type**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**CPU/register read value**
S001	**Station**	X	X	X	X	X	X	X		0x01
S002	**Station**	X	X	X	X	X	X		X	0x02
S003	**Station**	X	X	X	X	X	X			0x03
S004	**Station**	X	X	X	X	X		X	X	0x04
S005	**Station**	X	X	X	X	X		X		0x05
S006	**Station**	X	X	X	X	X			X	0x06
S007	**Station**	X	X	X	X	X				0x07
S008	**Station**	X	X	X	X		X	X	X	0x08
B101	**Baseline**									0xFF
B102	**Baseline**								X	0xFE
B103	**Baseline**							X		0xFD
B104	**Baseline**						X			0xFB
B105	**Baseline**					X				0xF7
B106	**Baseline**				X					0xEF
B107	**Baseline**			X						0xDF
B108	**Baseline**		X							0xBF

Figure 8-2 Jumper settings of the Rack ID in the Station and Baseline racks. Settings are different for Station and Baseline racks due to the availability of only 1 row in the bottom connector in Baseline Board slots Baseline racks.

By definition, each slot in a particular Station rack has identical jumper settings.

8.2 Baseline Board Rack-Crate-Slot ID Settings

The same basic scheme is used for setting the unique "rack-crate-slot" in each Baseline rack for each slot. The top ERNI connector (referring to Figure 5-24) sets the slot and crate ID, and the bottom ERNI connector sets the rack ID.

Slight complications result, though, since there is a Patch Board connecting adjacent boards together (which plugs into and uses rows used for settings), and since there is only 1 row available in the bottom connector to set the rack ID.

For the top connector, rows 35 and 36 are still used to set the slot ID and crate ID, and settings are still according to Figure 8-1. In cases where the Patch Board is plugged into the top connector, these rows are broken-out near the bottom of the Patch Board to a Patch Board PCB pin header, using rows labeled "U" on the PCB, indicating it is the break-out for the top (upper) connector. The "U" rows are therefore where jumper settings for slot ID and crate ID are set for the slot to the left (i.e. the top connector where the Patch Board plugs into).

What this means is that when a Patch Board is replaced or moved, the jumpers on the replacement Patch Board must be properly set before installing it in the system.

For top connectors where there is no Patch Board installed, use rows 35 and 36 to set jumpers for slot ID and crate ID as previously described.

For the bottom ERNI connector, only the bottom row of pins is available to set the rack ID. For ODD-numbered slots, jumpers are not used, but rather a short piece of wire-wrap wire is connected from the row pin, to the outer GND pin of the row, according to the bottom half of Figure 8-2.

For EVEN-numbered slots, the Patch Board is installed in that bottom connector, and jumpers are used to set the rack ID using the "L" PCB-labeled rows of the Patch Board PCB pin header, again according to the bottom half of Figure 8-2.

8.3 Rack-Crate-Slot M&C Ethernet Address Mappings

The rack-crate-slot read by the CMIB is translated to an Ethernet IP address for the M&C network as follows.

The first two octets of the address are fixed at "10.80".

The next octet is the rack ID. For Station racks it is 201-208 (i.e. 201==S001, 202==S002 etc.). For Baseline racks it is 211-218 (i.e. 211==B101, 212==B102 etc.).

The final octet is ((crate ID + 1) x 100) + slot ID. For example "t-3" (top crate(0), slot 3) maps to an octet value of 103.

Example: what is the IP address of S006-b-5? Answer: 10.80.206.205.

8.4 Cross-Bar Board Rack-Dependent Jumper Settings

For the Cross-Bar Board, there are no rack-crate-slot jumpers since the board does not contain a CPU. The sub-band(s) that a Cross-Bar Board switches are purely a function of the slot into which the board is installed, according to the layout of Figure 5-18.

However, to satisfy switching requirements for the HM Gbps protocol, there are jumpers on the Cross-Bar Board that should be set according to which Station rack the board is installed in. The "ID Jumpers" (labeled on the XBB PCB as "ID 7 6 5 4 3 2 1 0", and designated in the schematic and XBB User Manual [A25121N0001] as "JP9…JP2"),

should be set to the Station rack ID number – 1, in binary. For example, for S005, these should be set to JP2(b0)=Not installed; JP3(b1)=Not installed; JP4(b2)=Installed.

These jumpers set the randomizer seeds for all outputs such that signals arriving at any RXP in the system will have different switching patterns, to improve clock jitter out of the RXP[28]. Not installing jumpers according to this requirement could see increased clock jitter and errors in downstream Baseline Boards under some conditions (i.e. DC or near DC coming out of Station Board Filter Chips), but otherwise causes no functional problems.

8.5 Cross-Bar Board Backup Clock Settings

To provide a keep-alive clock to the correlator in the event of loss of the external 128 MHz clock source, it is necessary to connect a short loopback SMA cable from "128 MHz out" to "128 MHz in" for every Cross-Bar Board in Station racks in slots 0 and 7 in the system (except S004-x-0 and S005-x-7, as these are where the external 128 MHz clock enters the system). The reasoning for this is described in section 5.3 bullet H on page 36.

8.6 RPMIB ID Jumper Settings

Each RPMIB in the system is set with a unique ID, so the reading CPCCs can determine which rack they are talking to. There are 6 jumpers (B0…B5, reading left to right, and marked on the RPMIB PCB) on the board (indicated in Figure 5-32). If a jumper is installed, the CPCC (for the ID bits of Table 6-2) reads a "0", if it is not installed, the CPCC reads a "1".

Jumpers are installed as follows.

B5 – If installed, it is a Station rack (CMIB reads 0). If not installed, it is a Baseline rack (CMIB reads 1).

[B4:B0] – Binary value of the rack number (a "1" is not installed), ignoring the left-most rack number digit. For example, S001 has B4…B1 jumpers installed and B0 not installed, as does B101. B105 has B4=Installed, B3=Installed, B2=Not installed, B1=Installed, B0=Not installed. Same for S005.

To avoid the possibility of intermittent contacts, RPMIBs use wire-wrap connections on these jumper posts, instead of jumpers.

8.7 RPMIB Fan Single CPCC or Dual CPCC Control Jumper Settings

The delivered default configuration of the RPMIB is that both CPCCs must be actively controlling fan speeds, otherwise fans run at full speed. This configuration is set by installation of wires on jumper posts on the RPMIB, just above the fan wire terminal

[28] To minimize then number of signals switching simultaneously on the 1.024 Gbps inputs.

block (referring to Figure 5-32, just above the “Fan power, M&C wires”). If these wires are not installed across these posts, then only CPCC1 controls the fans, and nothing CPCC2 does has any effect.

What this alternative configuration means is that fans will only run at full speed if CPCC1 is not actively controlling fans (e.g. has failed).

9 DC and Switching Characteristics

This section contains applicable system-level DC and switching characteristics. Timing and action-triggers specified here are mostly set in the -48 VDC power plant and the CPCCs, and therefore are subject to change.

9.1 Power Supply, Control, and Shutdown

Parameter	Min	Typical	Max
-48 VDC supply voltage from power plant, *measured at power plant*.	-40 V[29]	-54 V	-56 V
-48 VDC supply voltage from power plant, measured at power plant, under AC FAIL condition, and at Typical load, for 5 minutes.	-44 V		
-48 VDC supply current	700 A[30]	2300 A[31]	2800 A[32]
Total correlator system -48 VDC power[33]	34 kW[34]	124 kW	151.5 kW[35]
-48 VDC power plant total output current capacity (all 20 PCU modules installed)			4000 A
-48 VDC power plant backup time at Typical correlator load, -44 VDC.[36]		8 min	
Time from AC fail, until power plant reports AC FAIL condition		15 seconds	
Time from AC good, until power plant reports AC OK.		25 seconds	
Time from AC fail, until CPCC de-programs all FPGAs in the system.		5 minutes[37]	
Time from AC fail, until CPCC executes a staged shutdown of all boards.		15 minutes	
Board temperature rise after prolonged AC fail (HVAC AC fail as well), maximum power.			5 ^{o}C
CPCC staged power down of correlator.			60 seconds

[29] This minimum shutdown voltage can be set in the power plant, and must not be too high as it was found that on AC fail under full load conditions, the battery voltage dips down to -44 V. Once this voltage is reached, the power plant performs a battery disconnect.
[30] At minimum power, and measured at –48 VDC (battery voltage under AC fail, at this load).
[31] At -54 V, based on full system load test, October 20, 2010.
[32] At -54 V, calculated at maximum power of 151.5 kW.
[33] Not including HVAC or AC systems.
[34] Achieved when all FPGAs in the system are de-programmed. Measured October 20, 2010.
[35] Calculated based on 625 W per Station Board, 480 W per Baseline Board, 100 W per fan, and 57 W per Cross-Bar Board.
[36] Based on dual strings in parallel, each one rated for 2200 A for 5 minutes.
[37] These, and other CPCC controlled parameters are determined by CPCC software.

Parameter	Min	Typical	Max
CPCC staged power up of correlator (all CMIBs booted, board FPGAs booted, everything synchronized).			15 minutes[38]
Station+Baseline Board CPCC-controlled thermal protection trip temperature.			55 ^{o}C
Station, Baseline Board deadman thermal protection trip temperature.		65 ^{o}C	70 ^{o}C
Cross-Bar Board deadman thermal protection trip temperature.		50 ^{o}C	55 ^{o}C

9.2 System Timing

Parameter	Min	Typical	Max
External 128 MHz clock reference frequency[39] (into S004 and S005—see Figure 5-14).	100 MHz	128 MHz	130 MHz
128 MHz input levels (sine wave)	-6 dBm	0 dBm	+9 dBm
128 MHz input levels (square wave, pk-pk)	200 mV	600 mV	2400 mV
128 MHz input cycle-cycle jitter tolerance (pk-pk)			1 nsec
128 MHz input impedance		50 ohm	
Station+Baseline Board M&C CMIB Ethernet			100 Mbps
Baseline Board SFP1			1000 Mbps
Baseline Board SFP2			1000 Mbps
Baseline Board SFP1 128-lag LTA frame rate			110 k/sec
Baseline Board SFP2 aggregate VDIF payload data rate (@ maximum VDIF frame size).			988 Mbps

"ext-TC" fiber interface: 1300 nm multi-mode fiber with optical performance compliant with FDDI PMD standard. The FDDI PMD standard is ISO/IEC 9314-3 1990, and ANSI X3.166-1990. Refer to Avago AFBR-5903Z data sheet for more information.

[38] Not including any DTS receiver complications, and assuming surrounding systems are operational.

[39] The correlator itself can handle clocks within this range, however, to get fringes, and be properly synchronized to the EVLA antennas, this frequency must be locked to the same frequency source.

Note: *The 128 MHz reference clock must be phase stable w.r.t. the "ext-TC" fiber input signal. What this means is the total pk-pk jitter of this clock w.r.t. ext-TC, measured within a 30 second integration time can be as high as the above 1 nsec pk-pk clock jitter requirement. For >30 second integration, phase stability must be much better, likely <50 psec. This is because the receiver circuit uses a ~40 second integration window to settle on selection of a clock edge, and assumes that if there is a jitter problem, it will show up within that time. Therefore, if long-term phase stability exceeds ~50 psec, it could keep searching for a stable clock edge, and if the conditions are right, never find one, as it will not change clock edges within the 40 second integration window, unless an error is detected.*

Refer to relevant board User Manuals for further information regarding board-specific timing and other parameters. Also, refer to the correlator room RFS document [A25012N0000] for further specific parameters regarding correlator room infrastructure.

10 Physical, Environmental, and Reliability Specifications

This section provides some useful numbers for various components in the system, according to the following table.

Description	Min	Typical	Max
Humidity (relative, non-condensing)	20 %	35 %	65 %
Rack inlet temperature[40]	10 °C	15 °C	30 °C
CPCC rack fan speed auto-setting[41].	20 (~2200 RPM)		32 (~2500 RPM)
Rack fan MTBF		TBD[42]	
Station Board calculated MTBF		72,000 hrs	
Baseline Board calculated MTBF		56,000 hrs	
Cross-Bar Board estimated MTBF		300,000 hrs	
On-board ¼ brick power supply MTBF (mfg data)		3.9 Mhrs	
Power Plant batteries (GNB Absolyte XL2000), float condition, expected lifetime.		20 years	
Power Plant batteries (GNB Absolyte XL2000), cycles to 80% discharge.		1200	
Power Plant 200 A PCU		(not avail)	
Station Rack weight, fully populated			1100 lbs
Baseline Rack weight, fully populated			1100 lbs

[40] All boards were tested over the range of 0 °C to +40 °C during burn-in, but for reliability purposes, the Max temperature should never be maintained over long periods of time.

[41] The rack fan speed should never go lower than this, as board power supplies, which rely on airflow in particular, could overheat and internally shutdown, even if the ambient temperature is still low.

[42] 56,800 hours from the correlator reliability study; however this number is still trying to be verified with the manufacturer.

11 Maintenance, Removal, and Replacement Guide

11.1 Regular Physical Maintenance

There are no regular physical maintenance requirements for the correlator core itself. In fact, the less the boards can be disturbed the better, as each extraction/insertion cycle wears down the socket ERNI connectors on the boards and has the potential to bend backplane connectors.

When a board is removed, it is recommended to use a clean, slightly damp cloth to clean the bottom board edge, where most of the aluminum oxide buildup (from contact with the rail) resides due to the mass of the board. When removed, it should be inspected/repaired for damage, and cleaned/blown-out to remove any dust buildup, although dust buildup should not be an issue in the clean room environment of the correlator.

System HVAC systems should be regularly serviced so as to maintain the air quality in the room to the ISO Class 8 specification.

Other correlator room systems maintenance requirements are beyond the scope of this document.

11.2 Removal/Replacement

11.2.1 Rack Fans

Each rack fan is a hot-swap replaceable unit. The LED on the front of the unit is connected to the tachometer output, and when a fan fails (or, fails to rotate), it will go dark.

To remove a rack fan module, loosen the spring-loaded captured slot screw on the side, and pull with the handle. Replacement is the reverse operation.

11.2.2 Station Board and Baseline Board

These boards may be removed and replaced without powering down the rack. However, due to lack of inrush current protection, when a unit is removed or replaced, the corresponding breaker for that slot should be turned off (breaker is at the back of the rack), and turned on only once the new unit has been fully installed.

Remove all front-panel cables, and move cables out of the way of the board face. To remove the board, engage the ejector handles with the front rail, and leverage the board out of seating position. Pull on the handle to remove the board. As noted above, use a slightly damp clean cloth to wipe aluminum oxide residue off the bottom edge of the board.

CAUTION: THE BOARD IS HEAVY DUE TO THE ATTACHED HEATSINK. IF THE BOARD IS DROPPED, IT COULD BE PERMANENTLY DAMAGED.

Installation is the reverse, taking care to line up the board with the railings and not short to adjacent boards. Turn on the breaker for that slot when installation is complete.

11.2.3 Cross-Bar Board

Cross-Bar Boards are contained within 6U crates of Station racks. To maintain proper airflow, this crate has a transparent cover which must be removed before the board is removed.

There is only one breaker for all boards in a crate. Ideally, this breaker should be turned off before the board is removed/replaced, however no significant damage will occur if it is not, provided there are not too many remove/replacement cycles for a particular board or slot.

To remove the board, engage the ejector handles, and pull out. Once free of the recessed 6U front rail, carefully rotate the board 90 degrees so it can clear the rest of the crate and rack metal.

Replacement is the opposite of removal.

11.2.4 RPMIB

The RPMIB PCB is a central part of a rack, and is designed to be very reliable, as it contains simple semi-conductor devices. Removal/replacement of the RPMIB is an involved process and requires the complete shutdown of the rack. ALL BREAKERS IN THE RACK BREAKER PANEL MUST BE OFF BEFORE REMOVAL AND REPLACEMENT. REMOVE BOTH SCSI-100 PIN CABLES AS WELL.

All wires are either grouped or marked, and so they can be removed and replaced quite easily. The fan wire groups are not particularly assigned to any terminal block section; just ensure that wires for a particular fan are always assigned to contiguous terminals in the terminal block.

11.2.5 Common Backplane (midplane)

Each slot in every rack uses the same Common Backplane (which is really a midplane).

To remove a backplane, FIRST TURN OFF ALL BREAKERS IN THE RACK to fully de-energize the rack. Carefully remove all cables, using extreme care to disengage (but not remove) the plastic latches on the rear header (the rear header plastic is quite fragile) from the cable headers. Move the cables out of the way, and then remove the 4 backplane fastening screws, noting that each one has a washer that is not captive (i.e. try not to drop it as it is conductive and can easily get lost).

It is easiest if the replacement backplane connector header is “pre-loaded” with plastic ERNI latches, in the same positions as the one that was removed. These snap into place in the holes in the header, but care must be used as too much force could cause the header plastic to break. Therefore, it is best to install a dummy wafer in the area(s) where the

latches are being installed to support the header plastic whilst snapping the latches in place. To remove old latches from a header, use a small flat screwdriver to wedge between the two snaps and gently pry apart. Of the cantilevered latch end is simply bent back, it will easily break. Old latches can be re-used in a new header if the snap-in teeth are intact.

To replace the backplane, position it, install the 4 fasteners and washers, and leave slightly loose (i.e. so that the board slides around easily in the X/Y direction, but not Z). Install a dummy non-heatsink-mounted board into the slot from the front until the connectors just start to engage (don't use the ejector handles for force). This positions the backplane relative to the board connectors so they will properly mate. Tighten backplane fastening screws. Install and latch the cables, referring to the rear-door-mounted decal to ensure they are all in the same place.

With these cables, always start at the top row, and work down, and thereafter always install against a reference wafer. If there is a blank row, temporarily install a blank wafer or a single wafer dummy cable in the blank row(s) so it acts as a reference.

NOTE THAT THE BACKPLANE PINS BEND EASILY, SO USE VERY LITTLE FORCE TO INSERT THE CABLE—IF ANYTHING OTHER THAN GENTLE FORCE IS REQUIRED, IT PROBABLY ISN'T PROPERLY LINED UP WITH THE HEADER PINS.

Once all the cables are installed, remove any temporary blank or dummy wafers, ensure all the right-hand-side plastic latches are engaged, and re-attached (with zip ties) the metal backshell for strain relief.

11.2.6 Meritec Cable Removal/Replacement

The Meritec cable connects Station Board outputs to Cross-Bar Boards, and Cross-Bar Boards to Baseline Boards. It is also used for st-TC Timecode distribution.

If a cable must be replaced, it is generally better to remove the cable from the connectors at both ends, tie-off and mark it, but leave it in the system. TRYING TO DRAG THE CABLE OUT COULD CAUSE DAMAGE TO OTHER CABLES. If the cable must be dragged out, be sure to cut the connector off at the far end so that the header can't damage other cables. Normally, the long cables from Cross-Bar Boards to Baseline Boards cannot be removed, as they are bundled together with other cables.

Removal/replacement of a cable is similar to that noted for Common Backplane removal/replacement. Cables are tightly packed and Common Backplane pins bend easily, so extreme care and caution with superior lighting and optics must be used with each cable remove/replacement cycle. Patience during this procedure is a must!

Refer to the correlator cable installation plans [A25005N0003] [A25005N0001], and [A25005N0004] for details on cable routing and labeling (also the brief discussion in sections 5.5.1, 5.7.1, and 5.7.2).

In many cases, 4 or more wafers are fastened together with a short plastic piece with studs in it, as part of the cable header. This must be removed from both sides of the cable header to separate the 4 wafers. Also, a single wafer might have two protruding plastic barrels through the flat metal surface of the wafer header. If this wafer it not to be bundled with 4 or more other wafers, or this is the bottom wafer of a stack and other wafers must slide in place next to it, these barrels must be removed (easily with a sharp knife) so they are flush with the metal surface. These plastic barrels are not essential for the cable wafer header, they just aid in mechanically grouping cable wafer headers together.

11.3 Board Repair Notes (BGA Remove/Replace)

All boards contain multiple BGA (Ball Grid Array) devices. The Baseline Board is the extreme case and contains 183 such devices of various sizes (F256, F672) and functions, mounted on both sides of the board.

Removal and replacement of a BGA device on a board is a non-trivial operation, requiring specialized equipment and training, and should only be attempted by thoroughly trained and knowledgeable personnel.

The general procedure for repairing a board (remove/replace a BGA device) is as follows:

1. "Tear-down" the board. This involves removing the heatsink, removing residual thermal pad material, removing the front panel, removing all socketted ¼ brick or 1/8th brick power supplies[43], and removing the CMIB stack (i.e. PC/104+ CPU module and PCMC module) and associated cables.

   Note: the Baseline Board heatsink has an additional mounting screw under the "+2.5V-C" power supply, which must be removed before the heatsink can be removed.

2. Moisture-bake the bare PCB assembly AND replacement device(s) in an ESD-safe oven for 24 hours at 125 ^{o}C. This is very important, as reflow temperatures can cause plastic devices to "popcorn" if they have absorbed too much moisture, and pre-baking is used to purge moisture from the devices. It is best not to thermally shock the board by installing it in a hot oven, but rather place it in the oven and then heat the oven to 125 ^{o}C from cold.
3. Develop a thermal profile of the device using auto-profiling, during removal, on a BGA rework machine capable of handling the thermal mass and size of the board.

[43] Power supplies must be removed VERY CAREFULLY, ALWAYS with a controlled gentle rocking about the LONG axis of the power supply. If a bin gets bent, it normally breaks, and then the pin or entire power supply must be replaced. This can happen it is removed rocking about the short axis, when one side suddenly gives way.

The replace profile is the same as the remove profile, except that it is important to add a post-reflow cool-down time of about 20 seconds to 150 ^{o}C.

4. Replace the device using the replace profile. Clean and inspect the board (using X-ray and visually). Note in the MITR database for the module the fact that a remove replace cycle has occurred. Each BGA site can withstand only ~3 remove/replace cycles, and then PCB pad attachment can degrade to the point of destruction.
5. Replace all power supplies, the CPU module, front-panel, and cables. Attach any temporary heatsinks required (e.g. the Baseline Board RXPs require temporary heatsinks so as to not overheat).
6. Test the board in a test bed with adequate forced air cooling to ensure the fix worked, before attaching the heatsink with thermal pads.
7. Fully test the board with heatsink attached.

The MITR database contains specific instructions in BGA remove/replace "Procedures" (which can be instantiated for a module in the module entry to be viewed) for BGA device removal and replacement, including examples of thermal profiles that have worked quite well for the VJE Summitt 1100 machine they were developed on.

Note: successful removal of RXP BGA devices has been found to be especially problematic, often resulting in pad damage/removal, even with very good solder wetting and first-time pickup removal. The reason for this is unclear. For these devices, we have made it a policy to send the torn-down board back the manufacturer (Sanmina-SCI, Kanata, Ontario) for repair.

Typical removal and replacement profiles are shown in Figure 11-1 to Figure 11-3 below.

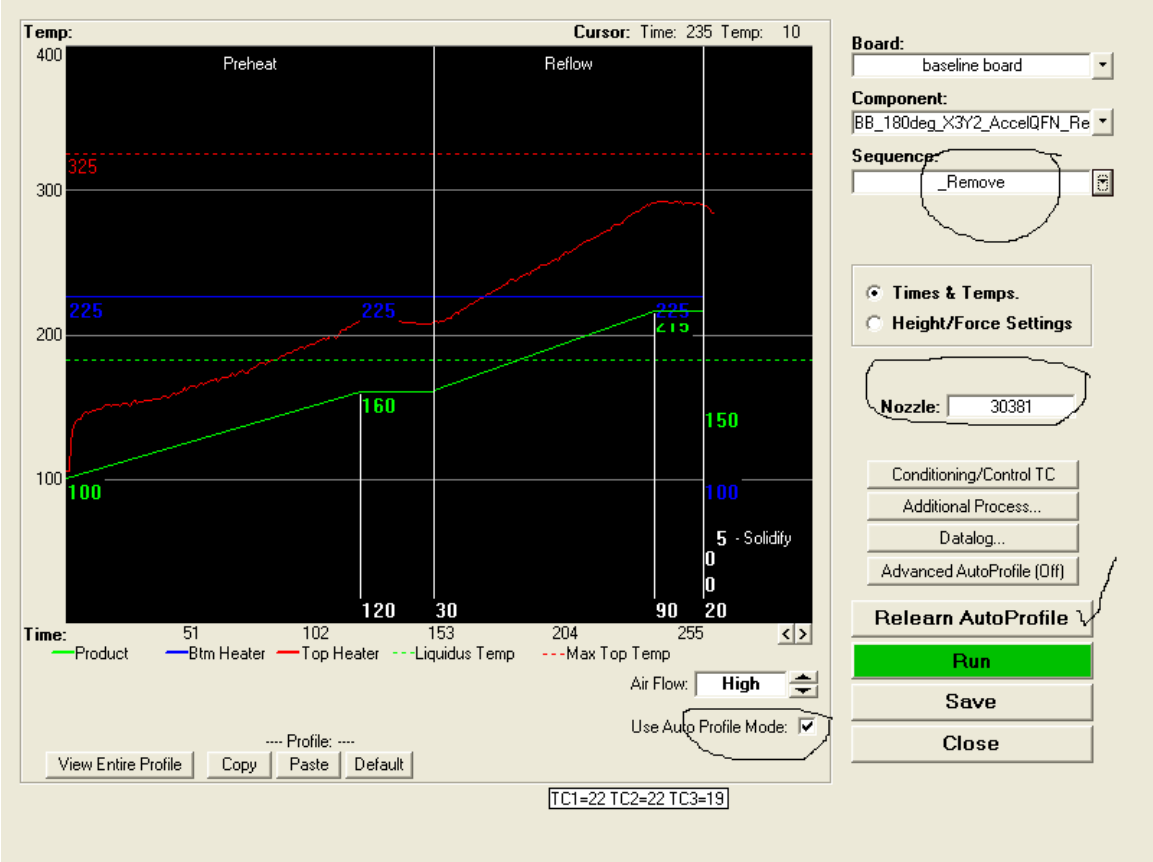

Figure 11-1 Typical remove profile for the VJE Summitt 1100 machine, taken from the MITR database. The GREEN curve is the actual profile that is desired. The RED curve is the top heater (i.e. removal head) temperature required to obtain that profile.

Once the auto-profile run is complete, actual temperature curves are obtained and are shown in the figure below:

Figure 11-2 Typical curves for a complete removal cycle using auto-profiling. The top RED curve is the top heater (removal head) temperature. The middle GREEN curve is the under-chip thermocouple temperature. The bottom curve is the board temperature ~3" away from the device. The BLUE curve is the bottom heater temperature.

The replace profile is the same, except a 20 second (@-5 °C/sec) post-reflow ramp time is manually programmed into the process file (see MITR BGA replacement Procedure instructions for how exactly to do this, as the VJE machine does not normally allow for this operation[44]). The post-reflow ramp time is essential to allow the solder to solidify before the top heater head is retracted; failure to do so could likely result in the device sliding or rotating as the head is retracted. The replace profile is shown in Figure 11-3.

[44] The reason for this is unclear. Our approach has been to auto-profile on the remove cycle for *every* removal procedure, and then use that profile, with the post-reflow ramp time, for the corresponding replacement, rather than maintaining a static database of remove/replace profiles to be used on every board. The reason being that auto-profiling every time tracks machine temperature calibration changes to get more accurate thermal curves, than might be possible with once-obtained profiles. One could, of course, set up and use static curves (i.e. found once with auto-profiling, and used thereafter open-loop).

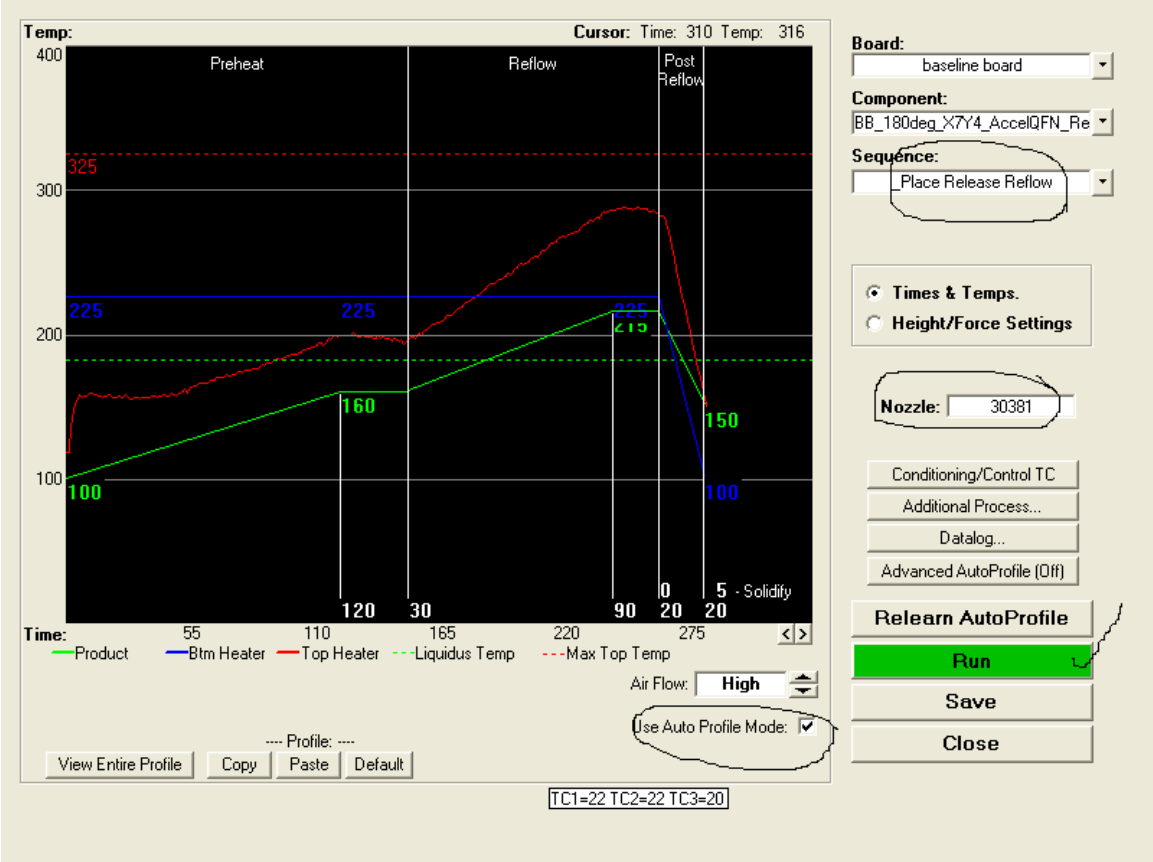

Figure 11-3 Typical BGA replace profile, showing 20 seconds of post-reflow ramp time.

Note that all of these profiles are for leaded solder, and all boards in the system are built with leaded solder, and so LEAD-FREE REWORK SHOULD NEVER BE PERFORMED.

It is important that the differential between the top heater curve (RED), and the under chip temperature curve (GREEN) have approximately the temperature differential shown in these graphs. Smaller differentials can indicate that the thermocouple is not properly placed, and larger differentials causing the top heater temperature to saturate could mean a calibration problem or a thermocouple problem. Also, if the thermocouple metal shorts to the top heater head, it can cause it to malfunction, and so it is important that the thermocouple in the region where the top heater head contacts it be insulated.

Refer to the MITR database BGA remove/replace Procedures for more specific instructions and notes, and for example thermal profiles.

11.4 Important System COTS Part Numbers

This section lists some important part numbers for field replaceable units in the system. For all part number details, refer to the EVLA System Bill of Materials (BOM).

Description	Part Number	Mfg
Rack Fan	R1G225-AF11-52	EBM-Papst
Rack Breaker, 20 A	QO120	Square D
Meritec quad-wafer cable, 1 m	945390-040[45]	Meritec
Meritec quad-wafer cable, 5 m	945391-197EQ	Meritec
Meritec quad-wafer cable, 2 m	945390-079	Meritec
Meritec quad-wafer cable, 5.5 m	945391-217EQ	Meritec
Meritec quad-wafer cable, 6 m	945391-237EQ	Meritec
Meritec quad-wafer cable, 6.5 m	945391-256EQ	Meritec
Meritec quad-wafer cable, 7 m	945391-276EQ	Meritec
-48 VDC power plant 200 A breaker	513775	Emerson
-48 VDC power plant 200 A PCU (3-phase 480 VAC to 48 VDC converter)	486532601 (LPS200E50)	Marconi/Lorain
-48 VDC power plant battery	Absolyte XL2000	GNB
1000Base-T SFP Module (NO AUTONEGOTIATION)	FCMJ-8520[46]	Finisar
CPCC computer (19" rack mount, 18 PCI slots, industrial grade)	SL-R4U-3.0-1024-XP-18PCI	SuperLogics
NI6509 digital I/O PCI card for CPCC	NI-PCI-6509	National Instruments

[45] All of these Meritec cables, while being standard product offerings, are custom-built to length and number of wafers. Obtaining these from the manufacturer most likely would require a special order, and after some time, may not be available.

[46] Or equivalent SFP. The SFP module must not require (1000BaseSX) autonegotiation between the module and the FPGA, as the FPGA does not support autonegotiation.

12 Troubleshooting Guide

System-wide issues are normally due to clock stability, Timecode (ext-TC and st-TC) distribution, and TIMECODE signal synchronization exiting Station Boards. If any of these signals are unstable, or there is interruption in their distribution, the system will be unstable.

Each board in the system operates in its own "reference frame", being driven by a 128 MHz reference clock and Timecode 1 PPS ticks, and containing an embedded Linux CPU connected to the network by 100 Mbps Ethernet. In some cases (Cross-Bar Board, Baseline Board), many Timecode ticks converge in one place and must be within +/-30 256 MHz clock cycles (~+/-118 nsec) of each other for synchronization and normal processing to occur. If proper compensation of st-TC Timecode delay (via hop counts, as described in section 5.5.2) in each Station Board is not performed correctly, then relative tick delays will exceed this limit, downstream signals will get scrambled, and downstream receivers won't be able to synchronize.

The system is synchronous[47] to a 128 MHz reference clock, locked to the array hydrogen maser, and if this reference clock (entering the system via Cross-Bar Boards according to Figure 5-14) or reference tick glitches or is unstable, then the entire system will be unstable. 128 MHz clock distribution within the system uses the Meritec cables for distribution and is fault-tolerant, but there are limitations to this and the system can become completely unusable if a *set* of particular boards are off or malfunctioning (refer to the CPCC top-level GUI, bullets K and L, of section 5.3)

The CPCCs (CPCC-1 and CPCC-2) are the master power controllers for the system, and one of them must be up and operational or the entire correlator is down.

The remainder of this section contains a table to assist with troubleshooting of the system. This table can never be exhaustive as there are many interactions possible, and they can be fluid as embedded software changes, possibly with bugs inadvertently introduced over time, and with enhancements added. Nevertheless, it should cover the majority of problems that could occur, or have been seen from time to time.

For further troubleshooting information on individual boards, refer to troubleshooting sections in their respective User Manuals.

[47] Synchronous in the sense of locked to a phase stable reference. The system is designed such that absolute phase of the data relative to the clock is automatically established where it needs to be established.

Problem	Possible Cause/Solution
All Cross-Bar Board receivers occasionally lose sync.	Either A or B 128 MHz reference clock, or ext-TC is unstable or glitching from time to time. To test the correlator independently of the external reference, do the following: 1. S004-x-0[48] connect the SMA-out to SMA-in clock, and remove the external fibre cable. Put "Test" toggle switch in the "On" position, and power-cycle the board. This causes the board to generate a good ext-TC output signal, synchronized to the on-board LO and its own tick generator, even though all downstream Baseline Boards getting signal from this board will have problems. 2. S005-x-7, remove the 128 MHz SMA reference clock. At this point all Station Boards should be getting a good and stable "Timecode-A", and all Cross-Bar Boards, except S004-x-0 should sync to all Station Board outputs. If the system is still glitching, then it is internal to the correlator (trace down and repair possible cabling problems, Figure 5-14 and Figure 5-15). If it is not glitching, it is external to the correlator. Repeat steps, swapping S004-x-0 and S005-x-7 functions/connections above, to test "Timecode-B" propagation in the system.
All Cross-Bar Board receivers sync, but one or more front-panel LEDs are flashing RED for ~80 msec, every ~640 msec.	This indicates that one or more inputs coming from Station Boards has a TIMECODE 1 PPS tick that is outside the relative time skew of ~+/-118 nsec (~+/-30, 256 MHz clocks). Refer to section 5.5.2 for information on hop count compensation in Station Boards.
All rack fans are running at 100%	This condition will occur if either CPCC-1 or CPCC-2 are down. Rack fan speed control requires both CPCCs active. To override this setting, refer to section 8.7.
Lag frame packets from one or more Baseline Boards are not showing up in the CBE, or are intermittently showing up.	Check the offending board to ensure that outgoing addresses (MAC, IP, UDP port) are as expected. This can be done using the Baseline Board Gigabit Ethernet (GigE) GUI's "Capture Data" facility (set capture source as "Tx", "SFP1", "Framed"=checked on). Ensure the "Discard Tx Frames" in the GigE GUI check box is not checked.

[48] S004 Cross-Bar Board in slot 0.

	DUMPTRIG, sourcing from Station Boards could be inactive or intermittent. Check Baseline Board Recirc GUIs for dump count increments. One or more Correlator Chips on the board(s) could be in an indeterminate state. Try resetting (CC Reset and PLL Reset) via the LTA GUI. If this fixes the problem, then there is a Baseline Board software problem in how it handles loss of 128 MHz clock conditions. If the clock is lost (Recirc PLL bit goes low), the entire board must undergo a "Rephase", after all Correlator Chips have been completely and properly reset ("PLL Reset" released first, then CC Reset). There could be a connection problem from the board to the CBE switch. The "SFP1" LED must be GREEN in the GigE GUI (except V2.1 boards, noted in section 5.6.1, bullet D of the Baseline Board User Manual [A25080N0001]). Even still, if it is GREEN, there could be a transmit wire connection problem—check the switch port at the far end to see if it too is active. Packet collisions (and dropped packets) could be occurring in the switch. Refer to section 5.14.2 for more information on how packets can be scheduled, both statistically and deterministically, to avoid collisions and dropped packets.
Cross-Bar Board front panel LEDs are not all GREEN; they intermittently or consistently are different or flashing different colours.	Refer to section 6.1 of the Cross-Bar Board User Manual for a complete description of front-panel LED colour signaling. This could indicate unstable reference clock source, bad Station Board outputs, or bad interconnects.
One or more boards cannot be remotely power controlled by the CPCCs	Possible bad SCSI-100 pin cable, most likely in the shielded back-shell. Swap cables to determine bad cables. Temporary fix is to disconnect offending cable, and control only with one CPCC. If the SCSI cable is not the problem, check connectivity from the RPMIB to the board slot. Also, the control LED on the RPMIB for the slot should be GREEN. Use volt meter to test for TTL voltage at terminal block, and at board slot. If all else fails, replace RPMIB.
CPCC-2 has no power.	The -48 VDC to 110 VAC inverter providing AC power to CPCC-2 may have died. Check connections, check output, replace as necessary. Could also be the CPU power supply.
Baseline Board Correlator Chip-to-LTA interface	If the "Frame Abort" LED in the "From CC" LEDs in the LTA GUI for the corr chip-to-LTA interface is lit GREEN, it indicates the

"Bit 28" LED in the LTA GUI is RED.	LTA is aborting frames for some reason: -could be due to the LTA being full (maybe the "Enable Data Flow" check box in the GigE GUI is not on). -could mean the corr chip is in indeterminate state. See above steps for proper reset/re-phase.
Station Board or Baseline Board CMIB is unreachable.	This could be a CMIB CPU crash, or network connection problem. Try to resolve by: 1. Power-cycle the particular board using the CPCC top-level GUI (Figure 5-5). 2. Check network connectivity at the "M&C switches" (Figure 4-1) to ensure the switch port LED is active. If these methods don't work or don't indicate the problem, remove/replace the CMIB.
Baseline Board RXP receiver for one or more inputs is not locked.	This could be anything from bad Station Board output (indicating a Station Board putting out bad Hm Gbps protocol codes), to a wiring problem. Use the CRC "CSD" (section 5.12.1) facility to check for system problems if the source Station Board seems to be ok (GUI "Main" screen has all GREEN LEDs). Check the source Cross-Bar Board front-panel LEDs.
One or more LEDs in the Station Board top-level GUI, "Main" tab are RED.	If "Delay" box LEDs are RED, there is a delay tracking problem, probably resulting in output data flagged invalid. If the "Timing" box LED is RED, there is some time tick/Timecode problem that is affecting output time ticks or stability. Refer to the Station Board User Manual [A25040N0001] descriptions for further detailed information.

13 Known Bugs, Workarounds, Anomalies

13.1 No -48 VDC Current In-rush Protection

When removing/replacing boards (Station, Cross-Bar, Baseline) in the system, turn-off power to the individual slot using the rack breaker panel, as there is no -48 VDC current in-rush protection.

13.2 Station Board Timecode-A and B Outputs are DC-coupled

The "st-TC-out-A" and "st-TC-out-B" outputs of the Station Board (Figure 5-18) are DC coupled (i.e. no in-series DC blocking capacitors), and the inputs ("st-TC-in-A", "st-TC-in-B") have no bias resistors. This is fine for Station Board-to-Station Board connections, but means that there is no DC bias in the st-TC differential signal for Cross-Bar Board-to-Station Board connections (i.e. since Cross-Bar Board outputs are AC-coupled). Extensive testing has not revealed this to be a problem, but it is worth noting in case of future issues. The workaround, if it does cause a problem is to solder a 1 k-ohm pullup resistor on st-TC-in-A and st-TC-in-B to 1.2 V, for Station Boards which get their st-TC signal from a Cross-Bar Board.

13.3 CMIB-Stack PC/104+ to PCMC Connector Issues (Black Connector Header only)

There are two issues regarding this connector. The first is gold-hair shedding due to poor plating on the PC/104+ connector pins. On repair, before mating the PC/104+ with the PCMC, inspect (with ~3X magnification) and remove any gold hairs.

The second issue is the press-fit connection in the PC/104+ end for this connector is not reliable. All offending PC/104+ modules that have had this performed should have their serial numbers appended with "**-S**" in the MITR database.

If a PC/104+ module is having problems, ensure the ECO (consult the MITR databased for the module for any applicable ECOs) for this solder operation is complete, if the mating connector header plastic is BLACK.

13.4 CMIB USB Cables Produce Noise

The USB cables running from the PC/104+ CPU module to the front panel can pick up noise and cause CPU interrupts that disrupt CPU activity, probably due to the fact that the cable can't be grounded at the PC/104+ end. Plugging a memory stick into the front panel USB connector seems to settle this down, but the best solution seems to be to disable the USB interface driver in the CPU.

13.5 SCSI-100 Pin Cable Header Soldering Poor Workmanship

After delivery, a couple of SCSI-100 pin cable headers had problems, and disassembly revealed that there was rather poor workmanship on the cable wire to connector header

connections. The solder joints themselves seemed ok, but the wire insulation was burnt in places, and residual solder flux is left in place. This was the case, even though a supposedly reputable cable assembly manufacturer, ("Cablek Ind.") was used. Something to keep an eye on if there are problems (see section 12).

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14.2 Useful Web Links and Addresses

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MITR database home page at DRAO: https://mitr.drao.nrc.ca/mitr/

widar-wg exploder email (for general correlator issues, scheduling time etc.): widar-wg@aoc.nrao.edu

DRAO Penticton website (restricted access):
https://mitr.drao.nrc.ca/widar/private/Private.html

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