INTERFACE CONTROL DOCUMENT

EVLA Correlator System Numbering Plan

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Brent Carlson, August 25, 2008

National Research Council Canada
Herzberg Institute of Astrophysics
Dominion Radio Astrophysical Observatory

P.O. Box 248, 717 White Lake Rd
Penticton, B.C., Canada
V2A 6J9

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List of Abbreviations and Acronyms

EMCS – EVLA Monitor and Control System. This refers to one or more layers of software residing on computers outside of the correlator, but networked to it, that tell the correlator what to do via the VCI.

VCI – Virtual Correlator Interface. This is a communications interface to the correlator across which all high-level configuration and status information flows.

CMIB – Correlator Monitor and control Interface Board. This refers to the embedded processor, a PC/104+ module, installed as a mezzanine card onto each of the Station Boards and Baseline Boards.

VSI – VLBI Standard Interface. This is an interface standard for VLBI transmission/recording/playback interfaces. Refer to the VSI-H standard.

MCCC – Master Correlator Control Computer. This is the host computer that communicates with the hundreds of embedded processors in the system, and is the primary interface to the EVLA Monitor and Control System.

CPCC – Correlator Power Control Computer. This is the host computer that is responsible for power monitor and control of the correlator system.

CBE – Correlator Back End. This refers to the cluster of computers that accepts data out of the correlator, processes it, and formats for output to the archive and image processing system.

IF – Intermediate Frequency. Refers to either ‘A’, ‘B’, ‘C’, or ‘D’ in the EVLA antenna. Refer to Figure 3-4 and Figure 4-1.

BB – BaseBand. Refers to selected 2 GHz or 1 GHz partitions of IFs. Refer to Figure 3-4 and Figure 4-1.

1 Revision History

Revision	Date	Changes/Notes	Author
DRAFT	October 12, 2004	Initial DRAFT release	B. Carlson
1.0	November 9, 2004	Release after peer review.	B. Carlson
1.1	February 25, 2005	Modify Station Board and Station Rack drawings to reflect updated design: the fiber-optic receiver module is mounted on the Station Board.	B. Carlson
1.2	March 12, 2007	Modify Module Serial Number ranges: delete TGB; add Correlator Chip Test Board, RPMIB, Terminator Board, Power Connection Boards (Vertical & Horizontal).	A. Fink
1.3	March 19, 2007	Change maximum Baseline Rack number from 255 to 254. Update Module Location ID to be set on Common Backplane by jumper instead of DIP switch. Update definition of 4th octet of Embedded Processor IP Address. Remove references to the TIMECODE Generator Board and Phasing Board from the following sections: Module Type, Embedded Process IP Address, Module Front Panel Label, Module Location ID.	A. Fink
2.0	November 14, 2007	Extensive changes to reflect new connectivity scheme; Rack ID is on the bottom ERNI connector; nail-down BB/IF associations with Station Boards.	B. Carlson
2.1	August 25, 2008	Correct BB/IF assignments to Station Boards based on new drawing from Rick	B. Carlson

		Perley. Include “S” and “B” prefixes in RIDs (rack IDs) Add RXP blocks and data paths to the Baseline Board logical diagram; inputs are now in terms of wafers. Fix Figure 4-4	

2 Introduction

The EVLA Correlator system consists of a couple of hundred modules distributed across 16 racks, connected by a thousand interconnect cables, and with a couple hundred embedded processors networked together through a hierarchy of switches.

Given the size of the system, it is clear that a coherent numbering plan in terms of physical and electronic identification is needed to ensure that all modules are kept track of. Many project-level numbering assignments—including part numbers and document numbers—have already been made [1] and many elements of the numbering scheme defined in this document are contained in [2]. This document is meant to contain a definition of all fundamental numbering definitions required for the operation of the correlator. In addition, a coherent cable labeling plan is defined in [8].

Any usage of identifiers and numbers defined by this document must use the nomenclature established in this document.

3 Overview

There are many inputs, outputs, and objects that require identification in the correlator system and a formal list of them in alphabetical order is as follows:

- **Antenna ID (AID)**. This is an ID number assigned to a particular antenna. For the purposes of the correlator, this is the identifier associated with a particular SID (Station ID) and is supplied as part of a correlator configuration message. Refer to section 4.1 on page 15.
- **BaseBand ID (BBID)**. This is an ID number associated with a particular antenna IF and is supplied as part of a correlator configuration message. This ID is embedded in sampled data streams, and propagates to downstream modules and the CBE. Refer to section 4.2 on page 16.
- **Correlator Chip ID (CCID)**. This identifies the row (Y) and column (X) location of a Correlator Chip on the Baseline Board. Refer to section 4.3 on page 18.
- **Crate ID (CID)**. This is a number for a particular 12 U crate in a rack. Crate numbering starts at 0 for the top and gets larger moving down the rack. Normally there are only 2 crates in a rack, with IDs 0 and 1. Refer to section 4.4 on page 19.
- **Data Path ID (DPID)**. This is an integer, 0 or 1, that identifies the Data Path on the Station Board. Each Data Path is a 64-bit data highway that contains 1 or more basebands (normally 1 for the EVLA). Refer to section 4.5 on page 20.
- **Embedded Processor IP Address (EPIP)**. This is an IP address that is partly derived from the Module Location ID, and forms the IP address for an embedded processor module (CMIB) that is installed on and controls a piece of correlator hardware. Refer to section 4.6 on page 21.
- **Filter Chip ID (FCID)**. This is an ID number associated with a particular Filter Chip in one Data Path on a Station Board. Refer to section 4.7 on page 22.
- **Module Serial Number (MS_N)**. A physical serial number assigned to a manufactured module. These numbers are kept in a database and are used to track modules throughout their lifetime. For those modules that contain an embedded processor, this number is electronically available (i.e. the CPU can determine the board's serial number) and set in hardware during manufacture. For those modules that do not contain an embedded processor, the serial number is printed on the module in an appropriately allocated place (i.e. blank spot with no solder mask). This is a 4-digit hexadecimal number. Refer to section 4.8 on page 23.
- **Module Location ID (MLID)**. This is an ID that depends on the location of the module in the system. This number is set for each rack slot in the system with jumpers or wires on the Common Backplane and is unique to a particular slot in the system. Refer to section 4.9 on page 24.

- **Module Type ID (MTID)**. This is a number assigned to a particular module type, and is read by the CMIB CPU from the board it is plugged into. This ID allows the CMIB CPU to know what code it is to boot and run. Refer to section 4.10 on page 25.
- **Rack ID (RID)**. This is a unique decimal number assigned to each rack in the system. It forms part of the Module Location ID, and each rack is physically labeled with its Rack ID for easy human identification. This number is never 0. Refer to section 4.11 on page 26.
- **Slot ID (SLOTID)**. This is the number, starting from 0 and left-justified looking into the front of the crate, for the slot number that a particular board is plugged into. Refer to section 4.12 on page 28.
- **Station Board Output ID (SBOID)**. This is an ID number associated with a Station Board output cross-bar switch number a.k.a. "wafer number". Refer to section 4.13 on page 29 and Figure 3-1.
- **Station ID (SID)**. This is an ID number associated with a particular Antenna ID, and is supplied as part of a correlator configuration message (sourcing from the EVLA Monitor and Control System). This ID is embedded in sampled data streams, and propagates to downstream modules and the CBE computers. Refer to section 4.14 on page 30.
- **Quadrant ID**. This is in the range 1-4, and defines the correlator Quadrants associated with antenna IFs. Refer to section 4.15 on page 32.
- **SubBand ID (SBID)**. This is an ID number associated with a particular Station ID (SID) and is supplied as part of a correlator configuration message. Normally, this ID is the same as the Filter Chip ID (FCID). This ID is embedded in sampled data streams, and propagates to downstream modules and the CBE computers. Refer to section 4.15 on page 32.
- **Polarization ID (POLID)**. This is the polarization identifier for a particular Data Path on the Station Board. This is only ever one of "**R**" or "**L**". Refer to section 4.17 on page 34.

The following figures graphically show the location and use of these IDs, as well as numbering and location conventions for boards, racks, and crates. These figures will be referred to throughout the remainder of this document.

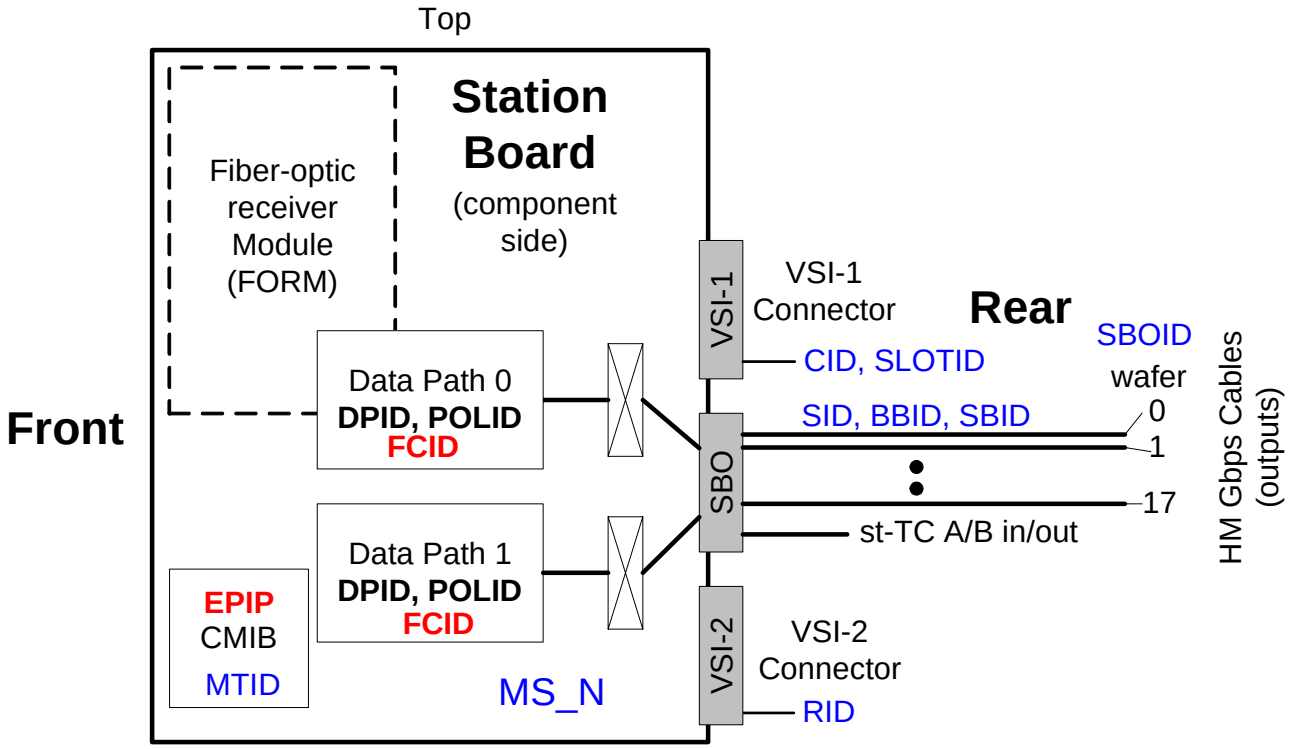

Figure 3-1 Station Board numbering, indicating the two main data paths (or data "highways"), Filter Chip banks and the location and use of ID numbers. Each output with a unique SBOID consists of 1 row of pins or 1 "wafer". Note that the location of modules on the board is conceptual only, and does not reflect the exact hardware configuration.

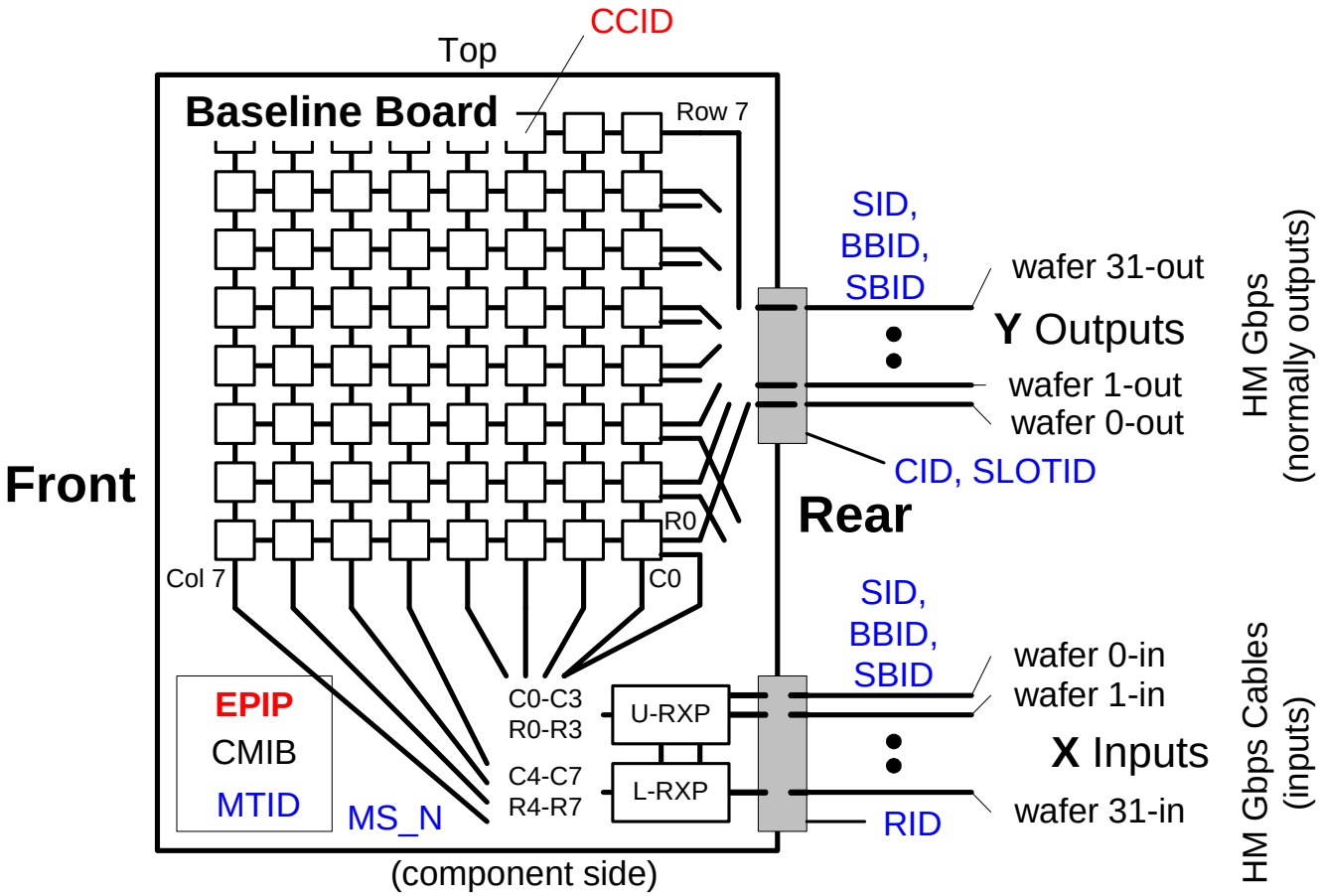

Figure 3-2 Baseline Board numbering including column (X) and row (Y) numbering of the Correlator Chip matrix, and X/Y column/row input numbering to the Upper RXP (U-RXP), and Lower RXP (L-RXP) Receiver, X-bar, and Phasing FPGAs. Each row and column input consists of 4 rows of pins or "wafers"; there are 32 wafer inputs and 32 wafer (normally) outputs.

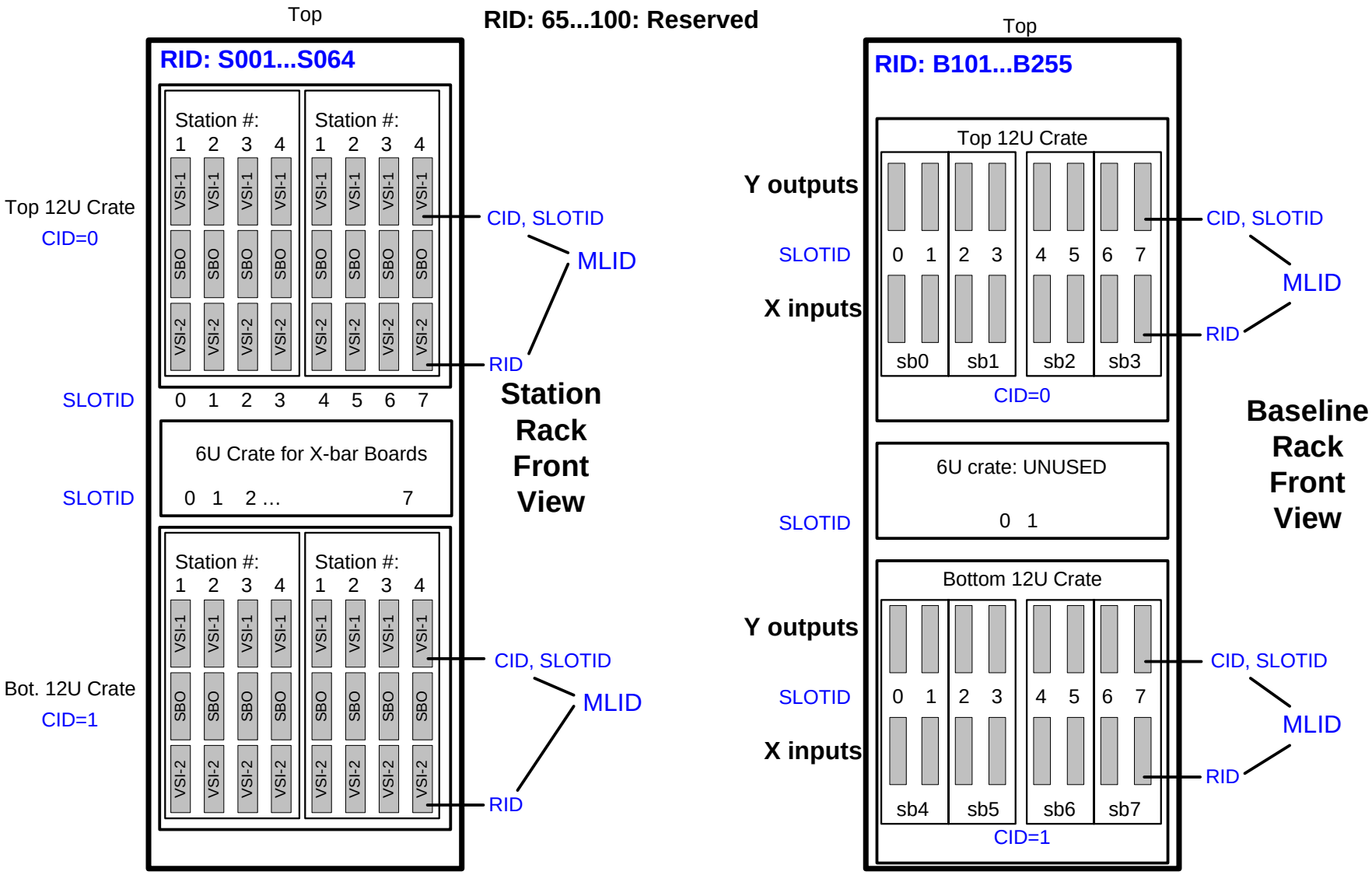

Figure 3-3 Station and Baseline rack crate and slot locations and numbering conventions. Both views are front views (i.e. looking into the front of the racks). Station Racks ("S racks") are decimal numbered, starting from 001 and Baseline Racks ("B racks") are decimal numbered starting from 101. Note that rack 000 is NOT ALLOWED. RID 65…100 are reserved.

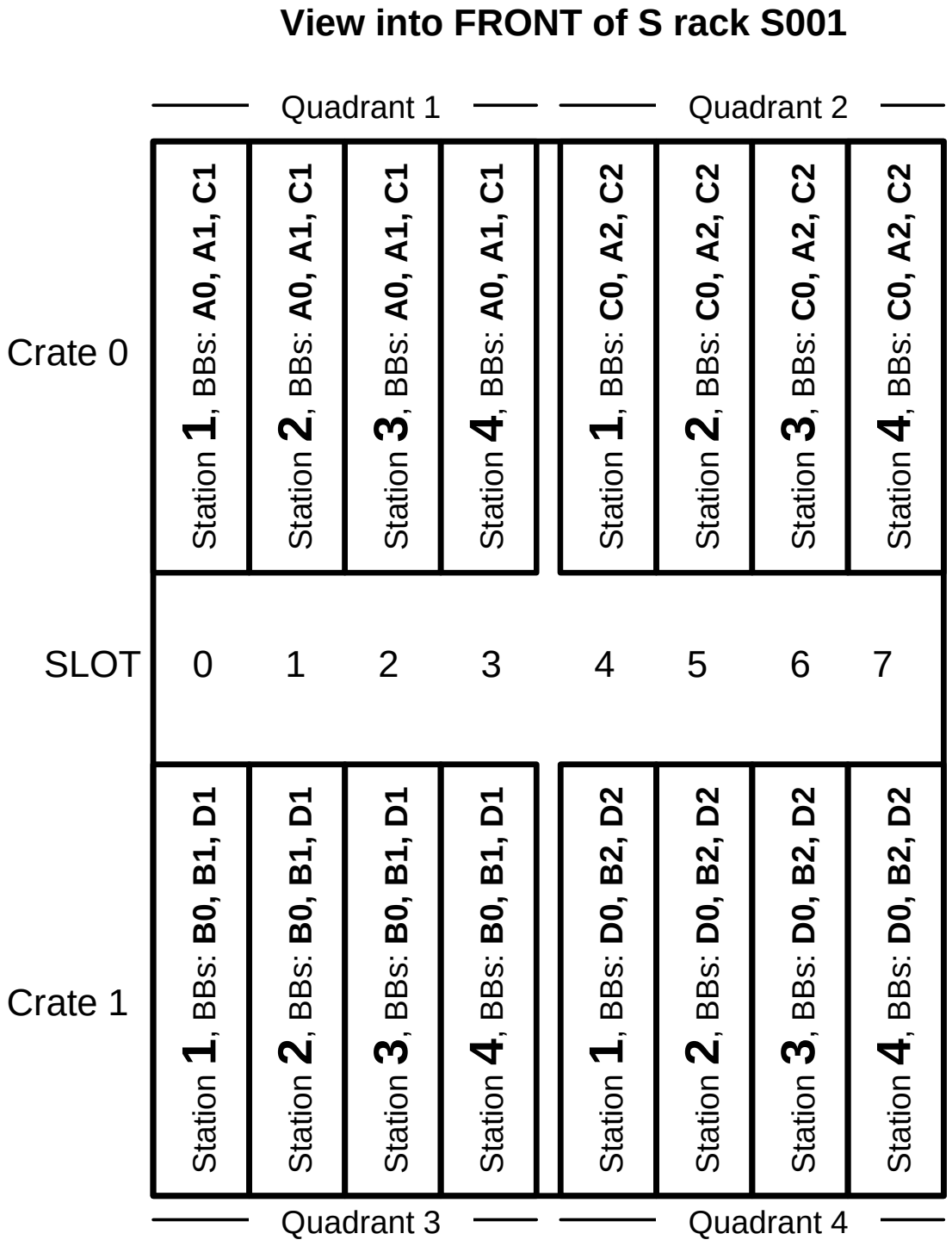

Figure 3-4 IF/BB allocations to Station Boards, looking into the front of the station rack, for logical stations 1-4.

4 Virtual, Physical, and Electronic ID Numbers and Application

4.1 Antenna ID (AID)

The Antenna ID is an identifier that has meaning to the EVLA Monitor and Control System (EMCS), but it is used within the correlator software only as a label, and as such is provided as an ASCII string. The Antenna ID is provided to the correlator during an observation configuration, via a message from the EMCS, and is associated with a particular Station ID (SID). An *example* of an Antenna ID (AID) is as follows:

“Antenna6_on_Pad10”

This example places no restriction or requirement on the Antenna ID content or format, except that it is an ASCII string.

4.2 BaseBand ID (BBID)

This is an ID number associated with a particular antenna IF and is supplied as part of a correlator configuration message. This ID is embedded in sampled data streams leaving the 4 Station Boards assigned to each antenna as a 3-bit number, and propagates to downstream modules and the CBE computers. Referring to Figure 3-1 and Figure 3-4, the normal assignment of the BBID for Station Boards and BBs/IFs is according to the following table:

Receiver BB/IF	Polarization?	Data Path	BBID	Station Board/Quadrant
A1 (A0)	A1=R; A0=R	0	0	1
C1 (A0)	C1=L; A0=R	1	1	1
A2 (C0)	A2=R; C0=L	0	2	2
C2 (C0)	C2=L; C0=L	1	3	2
B1 (B0)	B1=R; B0=R	0	4	3
D1 (B0)	D1=L; B0=R	1	5	3
B2 (D0)	B2=R; D0=L	0	6	4
D2 (D0)	D2=L; D0=L	1	7	4

Table 4-1 Normal BBID assignments to Station Boards for each antenna BB/IF, associated with the Data Path. The BBID is a free parameter, though, and is set by software configuration.

Note that BB nomenclature is according to NRAO standards [5] (with the seminal diagram from that power point document shown in Figure 4-1), and allocation to Station Boards/Quadrants is according to Figure 3-4.

Example: A1 and **C1** refer to both polarizations (R and L) of 3-bit-sampled, 2 GHz BW signals, originating from IFs **A** and **C**. **A0** refers to 1 polarization (R) of an 8-bit-sampled, 1 GHz BW signal, distributed to both Data Paths on the Station Board, allowing all Filter Chips on the board to be applied to the 1 GHz signal. Only **A1** and **C1** are both active, **-OR-**, **A0** is active on a particular board. It is not possible for **A0**, **A1**, and **C1** to all be active simultaneously.

***IMPORTANT RESTRICTION**: Any sampled data streams exiting the Station Board that have the same SID, BBID, and SBID **must** be from the same antenna, have the same sky center frequency, net LO frequency, and bandwidth. If not, indeterminate phase rotation and sub-sample delay tracking will occur on the Baseline Board.*

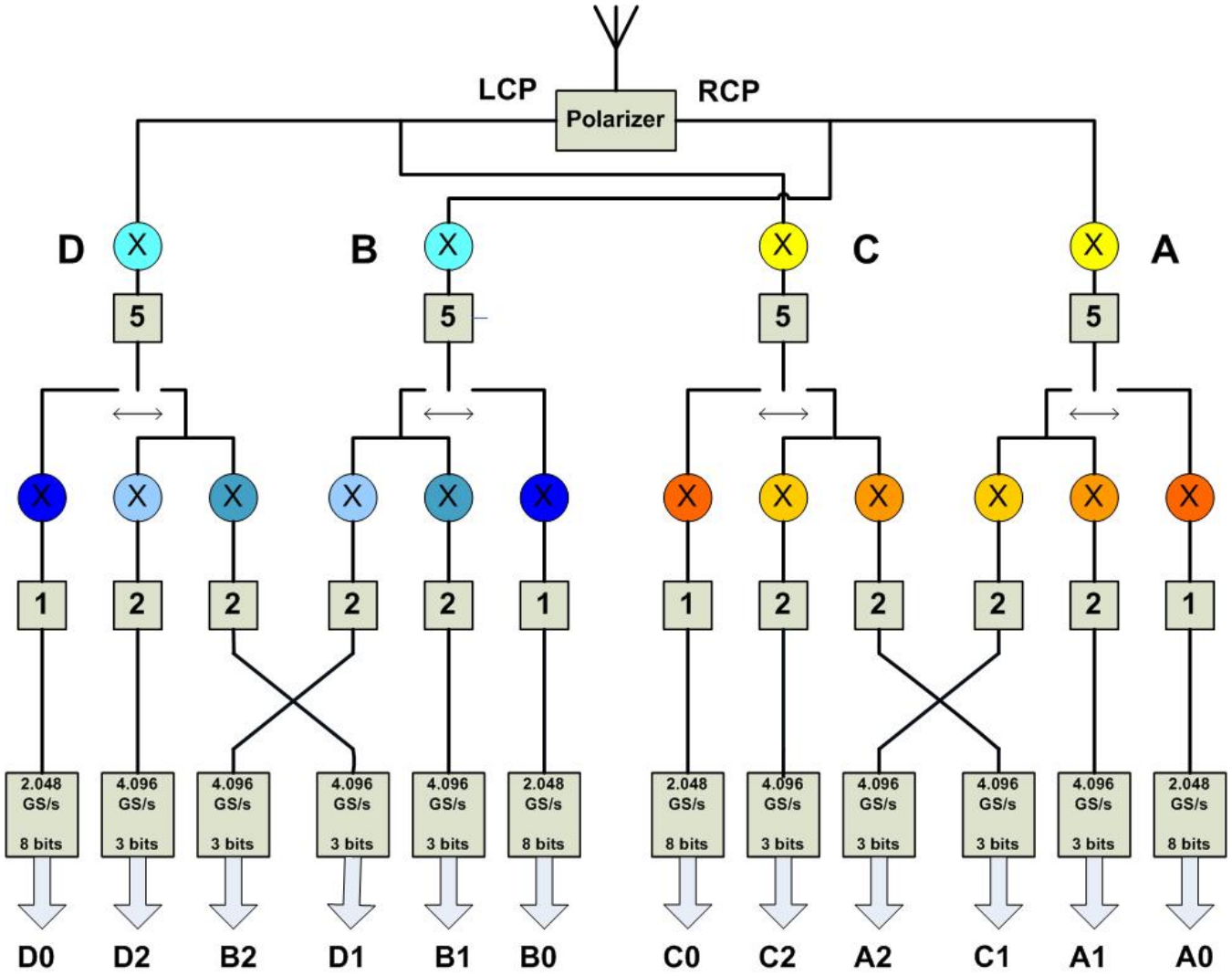

Figure 4-1 Simplified EVLA antenna IF block diagram (Perley) for IFs A, B, C, D. Identical colors signify identical tuning.

4.3 Correlator Chip ID (CCID)

This ID identifies the row (Y) and column (X) location of a Correlator Chip on the Baseline Board according to Figure 3-2. For consistency, this ID must be assigned and used according to Figure 3-2 throughout the system. Lower-level hardware registers require this as a 6-bit number with the lower 3 bits containing the column (X) number and the upper 3 bits containing the row (Y) number.

4.4 Crate ID (CID)

This is a number for a particular **12 U** crate in a rack. Crate numbering starts at 0 for the top and gets ***larger*** moving ***down*** the rack. Normally there are only 2 crates in a rack, with IDs 0 and 1. Any 6 U crates present in a rack are not numbered (e.g. for the X-bar Boards).

The Crate ID forms part of the MLID and is determined from jumper/bit locations **4** and **5** of the upper-most Common Backplane for the board (Figure 3-3). Refer to section 4.12 for CID and SLOTID settings using Common Backplane jumpers.

4.5 Data Path ID (DPID)

This is an integer, one of 0 or 1 that identifies the Data Path on the Station Board. Each Data Path contains a Delay Module and a filter bank comprised of 18 Filter Chips. The upper bank ("bank 0" of filters on the Station Board is Data Path 0, and the lower bank (bank 1) is Data Path 1. Each Data Path is a 64-bit data highway. Refer to Figure 3-1, and section 4.2 for Data Path ID allocations to the Station Board and antenna IFs.

4.6 Embedded Processor IP Address (EPIP)

This is an IP address that is partly derived from the Module Location ID, and forms the IP address for an embedded processor module (CMIB) that is installed on and controls a piece of correlator hardware. This includes the Station Board and the Baseline Board.

The EPIP is comprised of 32 bits—the upper 16 bits are free parameters and set by software configuration. The lower 16 bits are derived from the RID, CID (Crate ID), and SLOTID according to Figure 4-2:

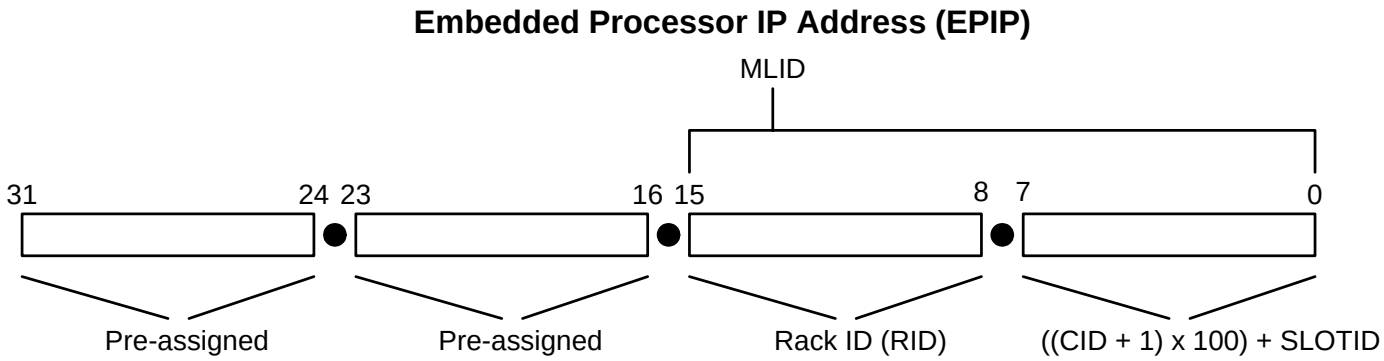

Figure 4-2 Embedded Processor IP Address (EPIP).

Refer to [6] for the exact procedure for obtaining the CMIB IP address, as well as additional CMIB IP mappings/allocations.

4.7 Filter Chip ID (FCID)

This is an ID number associated with a particular physical Filter Chip in one Data Path on a Station Board. It is defined by the location of the FIR filter on the Station Board. There are 18 FIR filters per Data Path, and thus this number is in the range of 0…17.

*Normally, the SBID is the same as the FCID—although the association and assignment of the SBID is a software assignment, noting the **IMPORTANT RESTRICTION** identified in section 4.2*

The FCID is hard-coded in the software system, and always refers to the same physical Filter Chip, for the given Data Path. Refer to the Station Board Memory Map, in the "Programmer's Guide to the EVLA Correlator System Timing, Synchronization, Data Products, and Operation" User Manual for FCID assignments.

4.8 Module Serial Number (MS_N)

This is a 4 digit hexadecimal serial number assigned to a manufactured module and written on the module in a space allocated for the purpose (i.e. blank spot with no solder mask). These numbers are kept in a database and are used to track modules throughout their lifetime. For those modules that contain an embedded processor, this number is also electronically available (i.e. the CPU can determine the board's serial number) and set in hardware during manufacture.

The MS_N is a 16-bit number (4 hexadecimal digits) and uniquely identifies each PCB module assembly ever built (except for Common Backplanes that are not assigned any serial number). These numbers are global in scope, and not associated with any particular correlator installation. The serial number range assignments, by module type and in hexadecimal format, are according to Table 4-2.

Module	MS_N (serial number) range
Station Board	0000…1FFF
Baseline Board	2000…3FFF
PCMC	4000…5FFF
Cross-bar Board	6000…7FFF
Delay Module	8000…9FFF
Correlator Chip Test Board	C000…C7FF
RPMIB	C800…CBFF
Power Connection Board - Vertical	N/A
Power Connection Board - Horizontal	N/A
Reserved	E000…FFFF

Table 4-2 Correlator module serial number ranges.

4.9 Module Location ID (MLID)

This ID is used to uniquely identify each physical location in the system where a Station Board or Baseline Board resides. The MLID is comprised of RID, CID, and SLOTIDs (prefixed with "S" or "B"[1]) derived from jumpers/wires in the bottom row of the upper 2 Common Backplanes within the crate that form the slot (refer to Figure 3-3 for Common Backplane jumper/ID locations).

The jumpers of the **upper-most** Common Backplane of the crate set the CID and SLOTID. Refer to section 4.4 and section 4.12.

The jumpers of the **next-lower** Common Backplane of the crate set the RID (Rack ID). Refer to section 4.11.

The MLID is of the form **"rack-crate-slot"**:

<S|B><RID>-<CID>-<SLOTID>

Example: The MLID for the board plugged into rack 002, crate 1 (bottom), slot 7 is:

S002-1-7

Example: The MLID for the board plugged into rack 104, crate 0 (top), slot 3 is:

B104-0-3

[1] If the first digit of the RID is a "0", then the prefix is "**S**"; if the first digit of the RID is non-zero, then the prefix is "**B**".

4.10 Module Type ID (MTID)

This is a 3-bit number that a particular module supplies to the PC/104 CMIB CPU mezzanine board via the PCMC connector. This lets the CPU know what module it is plugged into, and therefore what software and firmware to boot and run. Assignments are according to the following table:

	MTID		
Module Type	**B2 (pin C32)**	**B1 (pin B32)**	**B0 (pin A32)**
Baseline Board	0	0	0
Station Board	0	0	1

Table 4-3 Module Type ID (MTID)

These bits are available in bits 29-31 (B0-B2) of the Monitor/Control Function Status register (address 0x00 of "Function-2") of the PCMC register set.

4.11 Rack ID (RID)

This is a unique decimal number assigned to each rack in the EVLA system. It is derived from **lowest** Common Backplane jumpers/wires and forms part of the MLID (Module Location ID). RIDs, for the various racks in the system, are defined according to Table 4-4 (also refer to Figure 3-3) and are decimal encoded.

Rack Type	Rack ID (RID) range
NOT ALLOWED	000
Station Rack	001…064
Baseline Rack	101…254
Reserved	65…100

Table 4-4 Rack ID (RID) ranges for the different rack types in the correlator.

The RID is set with jumpers/wires in the lowest 2 pin rows of the lowest Common Backplane location as shown in Figure 3-3. Due to the difficulty in setting wires[2] for Common Backplanes associated Baseline Boards, encoding of the RID is according to Figure 4-3:

[2] Wires are used instead of jumpers for the Baseline Board lower connector, because all pin rows are allocated, leaving only the lowest pin row (36) for this purpose, unfortunately.

		Jumper Installed? (X=YES)								
RID	**Rack Type**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**CPU/register read value**
S001	**Station**	X	X	X	X	X	X	X		0x01
S002	**Station**	X	X	X	X	X	X		X	0x02
S003	**Station**	X	X	X	X	X	X			0x03
S004	**Station**	X	X	X	X	X		X	X	0x04
S005	**Station**	X	X	X	X	X		X		0x05
S006	**Station**	X	X	X	X	X			X	0x06
S007	**Station**	X	X	X	X	X				0x07
S008	**Station**	X	X	X	X		X	X	X	0x08
B101	**Baseline**									0xFF
B102	**Baseline**								X	0xFE
B103	**Baseline**							X		0xFD
B104	**Baseline**						X			0xFB
B105	**Baseline**					X				0xF7
B106	**Baseline**				X					0xEF
B107	**Baseline**			X						0xDF
B108	**Baseline**		X							0xBF

Figure 4-3 EVLA correlator Rack ID (RID) bit encoding using Common Backplane jumpers/wires. The actual RID used by software, jumper settings, and the RID's mapping to the 8-bit value read by the CPU from H/W registers is shown in this table. "S" and "B" prefixes are shown, but are not used as part of the numerical value of the RID (i.e. they are used when labeling racks for human identification).

4.11.1 Station Board and Baseline Board RID CPU Read Instructions

For the **Station Board**, the 8-bit "CPU read value" for the RID (lowest Common Backplane) is read from the LSByte of the MCB Fan Out "SID" register, address 0x00, bits 0-7.

Example: for Station rack S004, the actual value read by the CPU from the Station Board MCB Fan Out FPGA, register address 0x00, bits 0-7, is 0x04.

For the **Baseline Board**, the 8-bit "CPU read value" for the RID (lowest Common Backplane) is read from the LSByte of the "Slot ID" register of the MCB Fan Out FPGA, register address 0x01.

Example: for Baseline rack B106, the actual value read by the CPU from the Baseline Board MCB Fan Out FPGA, register address 0x01 is 0xEF.

4.12 Slot ID (SLOTID)

This is the number, starting from 0 and left-justified looking into the front of the crate, which identifies the slot number that a particular board is plugged into. This ID is encoded in the **upper-most** Common Backplane jumper/wire setting, in bit locations 0-3. Refer to Figure 3-3.

If a jumper is INSTALLED, then the CPU read value for that bit is a 0. If a jumper is NOT INSTALLED, then the CPU read value for that bit is a 1.

SLOTID and CID bit assignments to jumper/wire settings are according to the following table:

Jumper Installed? (X=YES)									
Unused		**CID**			**SLOTID**				
B7	**B6**	**B5**	**B4**	**CPU read value**	**B3**	**B2**	**B1**	**B0**	**CPU read value**
		X	X	0	X	X	X	X	0x0
		X		1	X	X	X		0x1
			X	2	X	X		X	0x2
				3	X	X			0x3
					X		X	X	0x4
					X		X		0x5
					X			X	0x6
					X				0x7

Table 4-5 CID and SLOTID Common Backplane jumper settings.

4.12.1 Station Board and Baseline Board CID and SLOTID CPU Read Instructions

For the **Station Board**, the "CPU read value" for the CID and SLOTID is read from the MSByte of the MCB Fan Out "SID" register, address 0x00, bits 8-15.

For the **Baseline Board**, the "CPU read value" for the CID and SLOTID is read from the MSByte of the "Slot ID" register of the MCB Fan Out FPGA, register address 0x02.

4.13 Station Board Output ID (SBOID)

This is an ID number associated with a "wafer" output from the middle connector—the sub-band output connector—from the Station Board. Wafer outputs are numbered sequentially from 0 through 17, starting with the upper-most output (where each output is a row of pins) of the connector. Refer to Figure 3-1. Refer to [3] and [4] for details on assignment of row pins, and signaling protocol.

Note: *SBOID is a completely physical assignment/concept and is thus not software configurable. The mapping between FCID and SBOID is determined by the Data Path output cross-bar switch on the Station Board.*

Note: *Each "wafer" contains a sub-band output from Data Path 0 (known as "BB0" in wafer terminology [3][4]), a sub-band output from Data Path 1, a control "CTRL" output which contains TIMECODE, DUMPTRIG, PHASEMOD, and PHASERR, and a 128 MHz clock.*

4.14 Station ID (SID)

This is an 8-bit ID number associated[3] with a particular Antenna ID, and is supplied as part of a correlator configuration message (sourcing from the EVLA Monitor and Control System) to address correlator physical hardware in a logical and consistent manner.

This ID is embedded in the sampled data streams and propagates to downstream modules and CBE computers. Refer to Figure 3-1, Figure 3-2, Figure 3-3, and [4].

Normally the SID should be set according to the logical station that the Station Board is part of, numbered 1-32, according to Figure 4-4.

Note: hardware and software must be able to set the SID independently on each Station Board. It is desirable, but not essential, to set the SID independently on each output data stream (i.e. each SBOID).

Note the IMPORTANT RESTRICTION identified in section 4.2.

[3] Antenna ID to SID associations are established by which antennas are on which pads, and by fiber patch panel connections. It is expected, but not guaranteed, that there is a one-to-one association between Antenna ID and SID. E.g. Antenna ID "5" is SID 5 etc.

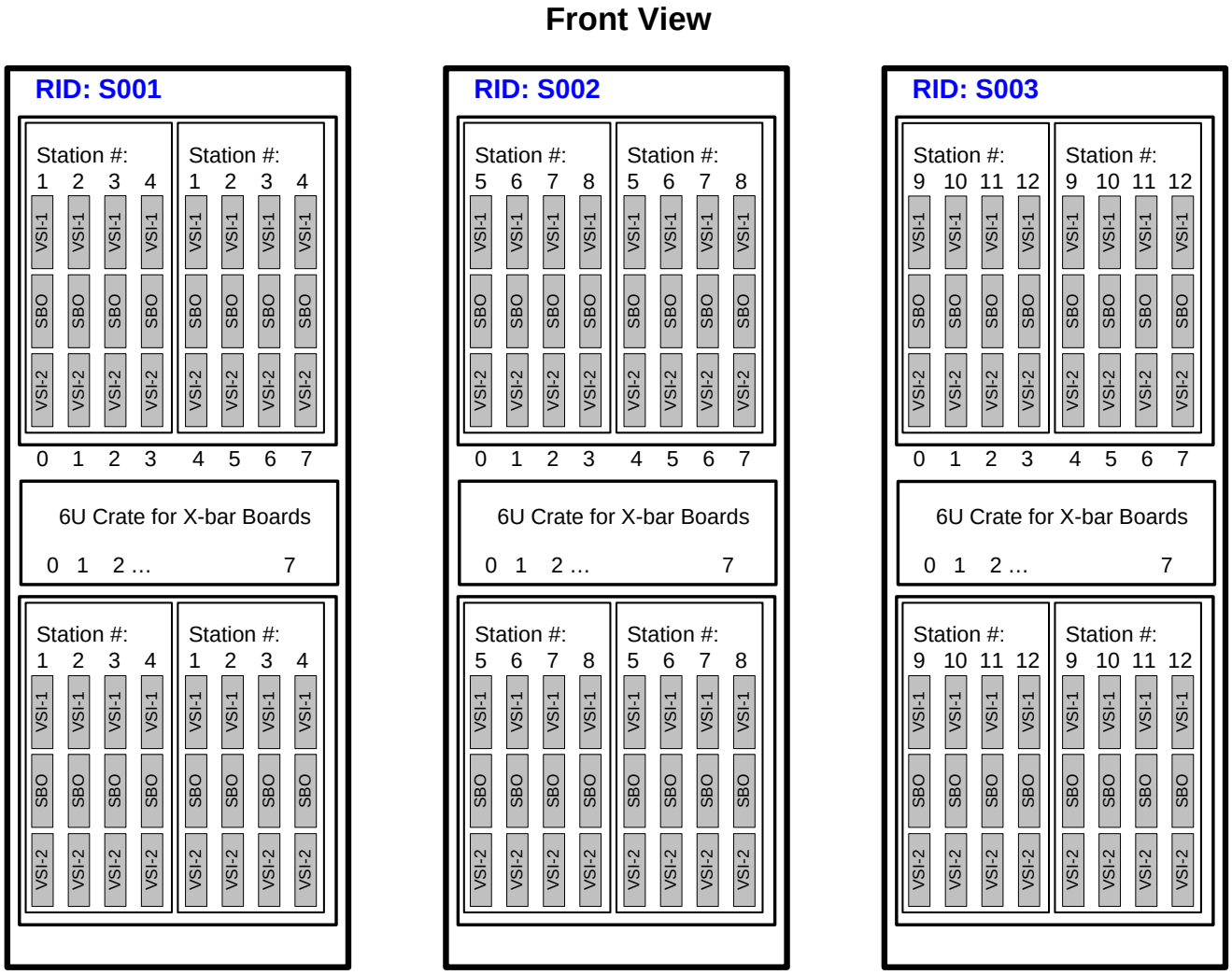

Figure 4-4 Station (SID) numbering for the first 3 Station Racks in the correlator system.

4.15 Quadrant ID

Cross-correlation resources in the correlator are partitioned into 4 "Quadrants" [7]. Each Quadrant is associated with[4] antenna IFs according to Figure 3-4, although, the X-bar Boards in the Station racks allow Quadrant correlation resources to be allocated to BBs/IFs in virtually any manner.

The Quadrant ID simply identifies these quadrants. Quadrant IDs are, by definition, in the range from 1-4. Quadrant 1 is associated with BBs/IFs according to Figure 3-4.

[4] In the sense that if the X-bar Board switch is set for straight-thru, then the Quadrant processes the associated BB/IF signals.

4.16 SubBand ID (SBID)

This is an ID number associated with a particular sub-band and is supplied as part of a correlator configuration message. Normally, this ID is the same as the Filter Chip ID (FCID), and the SBOID if the Station Board Output Chip cross-bar is set to straight-thru. However, this number may be freely assigned by software, noting the IMPORTANT RESTRICTION of section 4.2. This ID is embedded in sampled data streams, and propagates to downstream modules and the CBE computers [4]. This ID number has a range of 0 to 17 inclusive, although signaling protocol and hardware allows it to be in the range 0-31.

4.17 Polarization ID (POLID)

This is a polarization assigned to a Station Board Data Path. This is a logical software assignment and can ONLY be one of "**R**" or "**L**". This identifier is included with a Station Board configuration message from the EVLA Monitor and Control system, and is not encoded in any hardware in the correlator. Refer to Table 4-1 for polarization to BB/IF assignments.

5 References

[1] A25000N0000, EVLA Correlator Document Numbering Plan, Revision: 1.14, December 11, 2006.

[2] A25200N0001, The EVLA Correlator Software Architecture, Revision 1.1, February 17, 2004.

[3] A25022N0040, HM Gbps Cable Physical Specification, Revision Draft, April 13, 2004.

[4] A25022N0041, HM Gbps Cable Signaling Specification, Revision 1.2, August 18, 2005.

[5] Perley, R., Rupen, M., Carlson, B., EVLA Tuning and WIDAR Correlator Setups for the Interested User, PowerPoint presentation.

[6] Ryan, K., Mapping Names, Locations and IP Addresses of Embedded Components in the EVLA WIDAR Correlator, NRC-EVLA Memo# 030, NRAO, May 19, 2007.

[7] Carlson, B., LOGISTICS AND DIRECTIONS: EVLA Correlator Room Station Rack-to-Baseline Rack High-Speed Cable Installation Plan, LAD Document: A25005N0001, Rev. DRAFT3, October 25, 2007.

[8] Carlson, B., LOGISITICS AND DIRECTIONS: EVLA Correlator System Cable Labels and Labeling Plan, LAD Document: A25005N0005, Rev. DRAFT, October 17, 2007.