

# **REPORT on EVLA Correlator Room/Power Plant Tests conducted Oct. 20, 2010**

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## **Summary:**

On October 20, 2010 a number of tests associated with AC fail conditions in the EVLA correlator room were conducted. Bob Broilo, Kevin Ryan, and Brent Carlson were in the correlator room to execute these tests. The purposes of the tests were as follows:

1. Test communications and control software algorithms between the MCCC (eventually the CPCC) and the -48 VDC Power Plant.
2. Determine temperature and Power Plant battery reading under various conditions and failure times.
3. Gather data under realistic conditions to determine the best and simplest automated CPCC power monitoring and shutdown algorithm.

The data gathered during the tests revealed that the originally planned algorithm had some flaws, which would have resulted in unacceptable, although not damaging, behaviour when real power failures occurred. In particular, the battery voltage, when AC failed, and when the correlator was at very high power (~2280 A @ 54 VDC=123 kW; all boards populated and ostensibly set in the highest power configuration), dropped below expected levels.

In addition, left-over cold cooling capacity was available to support desired time out values, with plenty of headroom available until boards would start to shut themselves down.

Based on the tests performed, the following algorithm and settings were determined to be the best, until further experience and data proves otherwise:

1. Set the Power Plant self battery disconnect voltage to -40 VDC. This is based on the fact that under high load (123 kW), the battery voltage dipped to as low as -44 VDC.
2. The CPCCs register with the Power Plant to receive SNMP traps for alarm conditions. The AC fail condition is sent by the Power Plant ~20 seconds after it actually occurs, and is cancelled ~30 seconds after AC is returned. This provides some healthy hysteresis to weather AC fail glitches. Once AC fail is detected, the following actions occur:

- a. Start Timer-1; Timer-1 is set for 5 minutes. Timer-1 is set to be greater than the maximum time it takes for AC power to be restored from mains supply or diesel generators (3 min, 15 sec—Bob Broilo).
- b. Start Timer-2; Timer-2 is set for 15 minutes. If an AC fail condition lasts longer than this, it is likely that diesel generators have failed, and it will last an indefinite period of time.
- c. Until Timer-1 expires, no action is taken—the correlator runs on battery backup power, and the CPCC continues to monitor individual boards for overtemperature conditions and take individual board appropriate action if the threshold of 55 °C is reached.
- d. If AC is returned (determined by receiving a message from the Power Plant) before Timer-1 expires, cancel both timers, and return to normal conditions.
- e. When Timer-1 expires, the CPCC signals all Station Boards' and Baseline Boards' CMIBs to de-program all FPGAs, in a staged fashion. When this occurs, total system power drops by ~75%. The CPCC fan controller continues to control fans to maintain optimum board temperature as normal.
- f. If AC returns before Timer-2 expires, the CPCC issues a reboot command to all CMIBs, which will cause them to reboot CPUs and get the boards into a fully operational state. Originally it was thought that a command to “program FPGAs” and then start up the board would be better, but a reboot is simpler and software mechanisms are already in place for proper startup from reboot. Before Timer-2 expires, the CPCC continues to monitor board temperatures and control fan speeds accordingly.
- g. When Timer-2 expires, the CPCC executes a staged shutdown of the correlator, and shuts off all fans. Power up of the correlator after this point is under manual operator control.

There are a number of exception conditions that could occur, and anticipated ones are noted below:

3. CPCC-2 is on 110 VAC mains backup, and CPCC-1, through an inverter box, is powered by -48 VDC Power Plant battery-backed bvoltage. If both CPCCs are up, then full correlator control is possible. If one CPCC fails, due to loss of power, the other CPCC can control power to the boards, but the rack fans will run at full speed, and will not shutdown until their rack breakers are turned off, or until a -48 VDC battery disconnect is executed.

If both CPCCs lose power, then all boards in the correlator will immediately shut off; this should be a very rare occurrence, and should only happen if the -48 VDC

to 110 VAC inverter powering CPCC-1 fails at the same time as mains AC fails. If this happens a large delta-I occurs, which could result in a large voltage transient; all boards are outfitted with dual (instantaneous) 1500 W transient suppressors and so no damage should occur.

If one or both CPCCs fail due to a CPU crash, which may result in the internal NI-6509 boards still maintaining output control voltage, then the other CPCC is inhibited from powering down the correlator. Thus, in the case where either CPCC can't contact its partner, a warning to the operator should be issued to ensure that the failed/crashed CPCC is indeed powered off, or power-cycled to recover.

Therefore, generally, if either CPCC loses contact with its partner, operator or technician action should be initiated to correct the problem by trying to power-cycle or reset the zombie CPCC, or at least ensure the zombie CPCC is powered off. (Kevin notes: This could be trouble because, if the first CPCC commanded the boards off already, then rebooting the second one will cause all boards to shutdown at once. Not sure what should be done in this case. Perhaps the best we can do is power the boards back ON from the good CPCC, reboot the bad one and then do the shutdown.)

4. It may be possible for either or both CPCCs to lose communications with the Power Plant, as this communication goes through a network switch. In this case, the safest course of action is to immediately execute a staged power down of the correlator. However, this will result in a single point of failure, which could have the undesirable effect of causing a shut down if one contact or one wire goes open. What may be better under this condition is to issue a warning to the operator, and continue to monitor CMIB temperatures and voltages, and only shutdown the correlator if communications to CMIBs is lost or, CMIB -48 VDC voltages show low voltage ~40 VDC readings.

In any case, even if the CMIB does nothing in this case other than issue warnings to the operator, if AC fails at this time, the CPCCs do nothing, cooling is lost, communications is lost etc., eventually the boards will start automatically shutting down by themselves once overtemperatures are reached and/or the Power Plant will trip its low voltage disconnect, and execute a battery disconnect.

5. When AC fails or is disconnected for an extended period of time, and either CPCC loses power, fans will continue to run at full speed as long as -48 VDC is available. Thus, in this condition, a battery disconnect or full room power down should be performed.
6. It is assumed that the power plant contains an internal over-voltage protection and shutdown circuit. All correlator boards have 60 WVDC transient suppressors, and so for safety, the DC voltage should never be allowed to exceed -58 VDC, as severe heating damage could occur if these suppressors start to conduct DC current.

## **TEST Results**

For the following tests, “cut AC” means cutting AC to the 48 VDC Power Plant, and cutting AC to the chiller located in the basement. This was done nearly simultaneously by having another person in the basement in phone contact with Bob in the room to coordinate throwing AC breakers. The correlator room AC continues to be available to network computers, switches, and HVAC blowers (unless otherwise noted) as room AC is on battery backup.

Bob Broilo, Kevin Ryan, and Brent Carlson were present in the correlator room for these tests.

Bob Broilo was responsible for AC control of the room and chillers, and battery voltage monitoring.

Kevin Ryan monitored his software for trigger messages, timer timeouts, and actions.

Brent Carlson monitored the status of the correlator via the CPCC GUIs, room temperature, maximum board temperatures, and set/implemented test timing via stopwatch.

## **TEST #1: Dry Run**

### **Purpose:**

To ensure that the CPCC detection code (running on the MCCC for this test) recognizes AC fail from the Power Plant, and that Timer-1 (set to 2 minutes for this test) is functioning as expected, without the CPCC code taking any automated action.

### **Procedure:**

1. cut AC (to the correlator room only)
2. wait 2 minutes, monitor 48 VDC battery voltage, Power Plant indication and Timer-1. Set Timer-1 to 2 minutes for this test only.
3. restore AC.

### **Initial conditions:**

1. Power Plant current ~1700 A; Power Plant voltage -54.1 VDC.
2. Room Tamb ambient at start ~18 °C.
3. All boards installed in the system, all boards powered up. Some boards (mainly B108) not functional.

### **Expected outcome:**

1. No disturbance to the system, no boards shutdown.
2. CPCC detection code recognizes AC fail, timers work as expected.

### **Actual outcome:**

1. Battery voltage dropped as low as -45 V.
2. AC fail detected ~15 seconds after AC cut.
3. Loss of AC, and Timer-1 timed out successfully.
4. Power Plant indicated AC good ~30 seconds after AC restored. Once AC good was detected, Power Plant voltage reached ~-51 VDC.

### **TEST RESULT: OK**

**TEST #2: 15 second AC fail.****Purpose:**

To check system for behaviour for short duration AC power failure. CPCC code, running on MCCC, was set for automated operation.

**Procedure:**

1. cut AC (to the correlator room only, not the chillers).
2. wait 15 seconds.
3. restore AC.

**Initial conditions:**

1. Power Plant current ~1843 A; Power Plant voltage -54.1 VDC.
2. Room Tamb ambient at start ~18 °C.
3. All boards installed in the system, all boards powered up. Some boards (mainly in B108) not functional.

**Expected outcome:**

1. No disturbance to the system, no boards shutdown.

**Actual outcome:**

As expected outcome.

**TEST RESULT: OK.**

### **TEST #3: 3.5 minute AC fail.**

#### **Purpose:**

To check system behaviour for normal duration of AC fail until diesel generators active.

#### **Procedure:**

1. cut AC, including chiller AC.
2. wait 3.5 minutes, monitor battery voltage, CPCC set to take automatic action.
3. restore AC.

#### **Initial conditions:**

1. Power Plant current ~2273 A; Power Plant voltage -54.1 VDC (123 kW). Power Plant was allowed to re-charge batteries to near full capacity.
2. Room Tamb ambient at ~20 °C, max board temperature ~42 °C. Max rack fan speeds ~2700 RPM.
3. All boards installed in the system, all boards powered up. Some boards (mainly in B108) not functional.

#### **Expected outcome:**

1. No disturbance to the normal functioning of the system, no boards shutdown or FPGAs deprogrammed.

#### **Actual outcome:**

1. DC voltage drops to as low as 44 V. ~15 seconds after AC cut, Power Plant reports loss of AC.
2. After 3.5 minutes, Tamb ~ 20 °C, max board temp ~ 45 °C. After 5 minutes, Tamb rose to ~21.5 °C.
3. Timer-1 did not time out, correlator continued to function normally. Timer-1 reset after AC returned OK.
4. Rack fan speeds drop to ~2100 RPM (fan speeds are proportional to DC voltage) during AC fail.
5. 25 seconds after AC returned, Power Plant reports AC OK, and Power Plant voltage returns to -54 VDC.

**TEST RESULT: OK**

## **TEST #4: 10 minute AC fail.**

### **Purpose:**

To check for system after 10 minute AC failure; normally this length of failure is a very rare condition, resulting from failure of diesel generators.

### **Procedure:**

1. cut AC, including to chiller.
2. wait 10 minutes, monitor battery voltage, CPCC set to take automatic action.
3. restore AC.

### **Initial conditions:**

1. Power Plant allowed to charge batteries to near full charge.
2. Power Plant current set to 2300 A, -54.1 VDC.
3. Room Tamb $\approx$ 22 °C, max board temp  $\approx$ 44 °C, max fan speeds  $\sim$ 2600 RPM. Inlet temperature into racks  $\sim$ 10 °C.

### **Expected outcome:**

1. FPGAs should de-program after Timer-1 timeout of 5 minutes.
2. FPGAs should re-program, and get back to normal config, AC good detected.

### **Actual outcome:**

1. Minimum battery voltage reached -44 VDC.
2. Before Timer-1 timed out, correlator continued to operate normally.
3. Once Timer-1 timed out, and FPGAs deprogrammed, battery voltage climbed to -48 VDC, and DC current dropped to  $\sim$ 700 A.
4. Maximum board temperature reached 48 °C. Max Tamb did not go much over  $\sim$ 20 °C.
5. Fan speed reached minimum of 1500 RPM, due to the current software algorithm. Otherwise, fan speeds dropped to  $\sim$ 2000 RPM.
6. CPCC detected AC good, and voltage climbed to -54 V,  $\sim$ 30 seconds after AC restored.

7. Once AC restored, boards got into running state OK.

## **TEST RESULT: OK**

### **NOTES, Actions, Conclusions:**

1. Kevin: rack fans should always be in control loop, and powered off (set to 0 RPM) only when racks power off.
2. Kevin: rack fan speed LEDs in the CPCC GUI go RED when AC fails. This seems to be due to them slowing down to ~2000 RPM. RED fan LEDs should only occur if fan has failed (stopped) OR is below 1000 RPM (which in most cases would indicate the fan has stopped<sup>1</sup>, or cooling is severely hampered). YELLOW could be used for fan speed >1000 RPM but <2000 RPM, otherwise GREEN.
3. Once FPGAs are deprogrammed, the DC voltage rises significantly, and the Power Plant batteries can therefore sustain a long-duration AC failure. However, due to the dip in DC voltage under full load, it was decided that the CPCC need only trigger on AC fail, and then only operate on the two timers (Timer-1 and Timer-2) to control the correlator. Timer-1 and Timer-2 duration were chosen based on:
  - a. what the Power Plant and batteries can do,
  - b. what the operational/failure requirements and durations are,
  - c. what seems reasonable to ensure long battery life.

Timer-2 was chosen to be 15 minutes, as the maximum duration beyond which it is expected that a prolonged power failure would occur.

4. It was decided, due to the Power Plant voltage dip under full load, to set the Power Plant auto-shutdown voltage to a conservative -40 VDC, knowing that normally load would be disconnected well before this voltage is reached, and this voltage would only be reached under pathological conditions.
5. Kevin: to save even more power (~40 A @ 48 VDC) after Timer-1 times out, all Cross-Bar Boards could be powered down as no timing signals or StB to BIB data path is required. These would then be powered up if AC is restored before Timer-2 expires, or operator initiated power up.

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<sup>1</sup> Even if a fan has failed, it could still auto-rotate, and so some minimum speed must be established to indicate it has effectively stopped.

## **TEST #5: Long duration power failure, resulting in total system shutdown.**

### **Purpose:**

To test system behaviour after  $\geq 15$  minute<sup>2</sup> AC failure, to ensure total system shutdown. Also, to see what system does with one CPCC (CPCC-2) losing power after ~8 minutes into the test.

### **Procedure:**

1. cut AC, including to chiller.
2. After 8 minutes, power off CPCC-2 (AC powered).
3. wait 16 minutes after cut AC, monitor battery voltage, CPCC set to take automatic action.
4. restore AC.
5. Manually initiate system power up via the CPCC GUI.

### **Initial conditions:**

1. Power Plant allowed to charge batteries to near full charge.
2. Power Plant current set to 2500 A, -54.1 VDC.
3. Room Tamb $\approx$ 19 °C, max board temp  $\approx$ 44 °C, max fan speeds ~2600 RPM. Inlet temperature into racks ~10 °C.

### **Expected outcome:**

1. Up until 5 minutes, system operates normally.
2. At 5 minutes, all board FPGAs deprogrammed.
3. At 8 minutes, CPCC-2 powered off, rack fans go to full possible speed of ~2500 RPM.
4. At 15 minutes<sup>2</sup>, staged shutdown of the correlator occurs, fans continue to operate at full speed.
5. Full recovery once AC is back, **human initiated power up via CPCC GUI.**

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<sup>2</sup> Total system shutdown occurred in the actual test after 10 minutes, due to misunderstanding of Timer-2 duration between Kevin and Brent. However, this report is written up as if it was 15 minutes.

**Actual outcome:**

1. As expected outcome: de-program FPGAs after 5 minutes, staged system power down after 15 minutes (actually 10 minutes as noted).
2. AC fail detected ~15 seconds after it occurred. Minimum battery voltage -45.5 VDC.
3. Maximum board temperature reaches 48 °C. Maximum Tamb reaches ~20 °C. Minimum fan speed, until CPCC-2 off, reaches ~1700 RPM. After 8 minutes with CPCC-2 off, fan speed is ~2500 RPM. At the 10 minute mark, the rack inlet temperature is ~20 °C.
4. When FPGAs deprogrammed, 48 VDC load current drops to ~800 A, and DC voltage reaches and sustains ~-48 VDC.
5. After staged power down, AC was restored. CPCC detected AC good ~30 seconds later. Human-initiated power up was mostly successful, with human-initiated power up getting all boards to running state with the exception of S005-b-4, S002-t-1, and S002-b-0, which had to be rebooted to get going ok.

**TEST RESULT: OK**

## **TEST #6: Simulated smoke alarm test**

### **Purpose:**

To simulate smoke alarm detection levels by manually shunting connections to see if the CPCC could detect alarms on the correct lines.

(Kevin, these definitions could be wrong.)

Stage 1 – supervisor trigger, indicating some exception has occurred. Operator warning.

Stage 2 – Single zone detects smoke. Operator warning.

Stage 3 – 2 or more zones detect smoke, power down correlator.

### **Procedure:**

Kevin: We had a little trouble here. The supervisory alarm is not working at all (wiring issue?)  
Bob knows.

Then he tried the 1st smoke alarm (single zone) that turned out actually be the 2nd smoke alarm which caused the system to shutdown.

SO, I was satisfied that CPCCs got SOME signal and worked from the software point of view.

But the outcome was that we still need to get the wiring straightened out and retest.

### **Initial conditions:**

Correlator operating normally, smoke alarm detection only.

### **Expected outcome:**

CPCC detects trigger, no action taken.

### **Actual outcome:**

See above Procedure.