1 Delay Counter

**V1.01 07 May 2002.** Originally written by Joseph Dickerson.

**Purpose:** The delay counter gives a preprogrammed delay from 0.1 μs to 400s in steps of 0.1 μs.

1.1 Function Summary

The Crab pulsar occasionally emits ‘giant pulses’, which are much stronger than the normal pulse profile. During dual frequency observations, the giant pulse is dispersed, or delayed, from one frequency to the next. If we want to efficiently record and store giant pulse data at two frequencies, we need to be able to trigger the computer and oscilloscope at the appropriate times. As an example, the Crab pulsar may have a dispersion delay of \( DM = 56.791 \). The time lag of a giant pulse received at the observatory is

\[
t_2 - t_1 = \frac{DM}{2.41 \times 10^{-16}} \left( \frac{1}{f_1^2} - \frac{1}{f_2^2} \right).
\]

If we are observing in 4 and L bands,

\[
t_2 - t_1 = \frac{56.791}{2.41 \times 10^{-16}} \left( \frac{1}{(1420 \times 10^6)^2} - \frac{1}{(74 \times 10^6)^2} \right)
\]

\[= 42.9 \text{ sec.}
\]

The delay counter must therefore be set to 42.9 seconds. The giant L band pulse will arrive at the observatory first, and trigger the timer. The timer will expire exactly 42.9 seconds later, coincident with the arrival of the 4 band giant pulse.

1.2 Physical Description

The delay counter consists of 26 74LS series logic chips that are wire wrapped on two boards. The boards themselves are labeled **board 1** and **board 2**. Board 1 contains four 8 bit registers and eight 4 bit counters. Board 2 contains a series of D and JK-type flip flops that serve as ‘state machines’, that is, they control the operations that the counter performs. Figures 3 and 4 show where each chip is located on each board, with the circles representing pin 1. At this time, there are sixteen 10 nf bypass capacitors. With one for each logic chip, that leaves 10 capacitors to be attached in the future. All inputs and outputs are properly buffered through a 74LS244 chip.

1.2.1 Headers

The two boards also contain input and output lines soldered onto three headers.

**JP1** is an **8 × 2** header located on board 2 with pin 1 defined to be the ‘Trig 1 In’ input (blue wire). Pin 1 of JP1 is to be connected to Pin 50 of board 2.

**JP2** is an **2 × 1** header located on board 1 with pin 1 defined to be the input of the 10MHz clock which is supplied by the GPS unit. Pin 2 is ground. Pin 1 of JP2 is to be connected to Pin B12 of board 1 and Pin 2 of JP2 is to be connected directly to the grounding pin.

**JP3** is an **8 × 2** header located on board 2. This header only contains one output and no input. That output is ‘Trigger 1 Out’. A coaxial cable is used for this output, so the header is used for extra stability. Pin 1 of JP3 is defined to be the output and is connected to Pin J34 of board 2.

1.3 State Machines

The operations of the delay counter can be broken down into two ‘state machines’, each with a separate design. Figures 1 and 2 are flow charts which describe these state machines. Each state on the flow charts are labelled with the format ‘State BA’ where B and A are the JK flip flops of the state machine. As an example, State 01 indicates that flip flop B is logic false while flip flop A is logic true.

Before the delay counter is triggered by a giant pulse, it should be in the following initial state:

- Time of Day state machine reset to state 00.
- Delay state machine reset to state 00.
- Scope Ready.
- Computer Ready.
- Counter Load, since the delay counter does not automatically load the preprogrammed delay time into the counters.
- Trigger Enable On.
Figure 1: Flow chart for the time of day state machine
Figure 2: Flow chart for the delay state machine
Figure 3: Layout of Board 1
Figure 4: Layout of Board 2