WIDAR Prototype Boards
and Correlator Chip

Test Software Development Plan

Version 2.0.2
Revision History
Version 1.0.0 of this document is taken to be the material contained in “EVLA Monitor and Control Software, Status as of Q2 2005”, Version 1.0.0, by Bill Sahr, 20June2005. This document can be found on: http://www.aoc.nrao.edu/evla/techdocs/computer/workdocs/index.shtml. It is document #43.

<table>
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<tr>
<th>Revision</th>
<th>Date</th>
<th>Author(s)</th>
<th>Description of Changes</th>
</tr>
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<tr>
<td>2.0.0</td>
<td>04Jan2006</td>
<td>Bill Sahr</td>
<td>Original for version 2.0.0</td>
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<tr>
<td>2.0.1</td>
<td>05Jan2006</td>
<td>Bill Sahr</td>
<td>Added references to the WIDAR test plans for the Timecode Generator, Station, and Baseline Boards.</td>
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<tr>
<td>2.0.2</td>
<td>05Jan2006</td>
<td>Bill Sahr</td>
<td>Added information re status of Timecode Generator Board tests.</td>
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1.1 **WIDAR Prototype Board Tests**

### 1.1.1 Relevant Milestones & Target Dates: WIDAR Prototype Board Tests

<table>
<thead>
<tr>
<th>Test</th>
<th>Target Date as of 3/25/2005</th>
<th>Target Date as of 1/04/2006</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gbit Transmission Test</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gbit Test Plan document available</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(A formal test plan will not be written)</td>
<td>Not Applicable</td>
<td></td>
</tr>
<tr>
<td>Hardware testbed ready</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bruce Rowen at Penticton for 2 weeks</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(depends on parts acquisition problem)</td>
<td>mid-May 2005</td>
<td>done</td>
</tr>
<tr>
<td>Software installed on testbed and ready for use</td>
<td>mid-May 2005</td>
<td>done</td>
</tr>
<tr>
<td>Finished assemblies available for testing</td>
<td>awaiting parts</td>
<td>done</td>
</tr>
<tr>
<td>Start of tests</td>
<td>mid-May 2005</td>
<td></td>
</tr>
<tr>
<td>Duration of tests</td>
<td>approx 1 week</td>
<td></td>
</tr>
<tr>
<td>End of tests</td>
<td>end of May 2005</td>
<td>done</td>
</tr>
</tbody>
</table>


<table>
<thead>
<tr>
<th>Test</th>
<th>Target Date as of 3/25/2005</th>
<th>Target Date as of 1/04/2006</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timecode Generator Board (TCGB) Tests</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timecode Generator Board test plan available</td>
<td>Apr 04, 2005</td>
<td></td>
</tr>
<tr>
<td>Hardware testbed ready</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(dependent upon parts deliveries)</td>
<td>mid-May 2005</td>
<td>done</td>
</tr>
<tr>
<td>Software installed on testbed &amp; ready for use</td>
<td>mid-May 2005</td>
<td>done</td>
</tr>
<tr>
<td>Finished assemblies available for testing</td>
<td>mid-May 2005</td>
<td>done</td>
</tr>
<tr>
<td>Start of tests</td>
<td>mid-May 2005</td>
<td></td>
</tr>
<tr>
<td>Duration of tests</td>
<td>a few weeks</td>
<td></td>
</tr>
<tr>
<td>End of tests</td>
<td>May-Jun 2005</td>
<td></td>
</tr>
</tbody>
</table>

Because of a conflict with a higher priority task, as of 1/5/2005, the Timecode Generator Board tests have not yet been done. These tests will begin when the work needed to manufacture a prototype Baseline Board has been completed. A formal report of the test results will probably not be available until the work on the Fanout Board redesign is well in-hand.
**Station Board Prototype Tests**

Station Board Test Plan document available | Apr 6, 2005 | done
1st prototype board available for testing | Aug 31, 2005 | April 2006
Testbed ready, hardware & software | Aug 31, 2005 | basically complete
Start of tests | Sep 01, 2005 | April 2006
Duration of tests | 6 to 9 months | 6 to 9 months
End of test | Feb to May 2006 | Sep to Dec 2006

**Baseline Board Prototype Tests**

Baseline Board Test Plan document available | Mar 17, 2005 | done
Prototype CBE ready, hardware & software | mid-May 2005 | basically complete
Modifications to CBE software | Not Applicable | April 1, 2006
1st prototype board available for testing | Aug 31, 2005 | April 2006
Prototype correlator chips available | Aug 31, 2005 | late March 2006
Testbed ready, hardware & software | Aug 31, 2005 | basically complete
Start of tests | Sep 01, 2005 | April 2006
Duration of test | 6 to 9 months | 6 to 9 months
End of tests | Feb to May 2006 | Sep to Dec 2006

**Target Date as of 3/25/2005**

**Target Date as of 1/04/2006**

### 1.1.2 Discussion: WIDAR Prototype Board Tests

An overview of the test software might list the following components:

- Module Access Handlers (MAHs)
- GUIs
- Data Collection Tasks
- Plotting software
- Correlator Backend (CBE) software
- Numerous infrastructure and utility items

The MAHs consist of a driver for a correlator board module (Input, Delay, Output, Filter, etc) plus a layer that sits above the driver that decodes XML packaged parameters sent to the driver and encodes into XML quantities coming from the driver. Since the correlator boards contain multiple modules, multiple MAHs are needed to fully test a board.

GUIs refer to the test software graphical user interfaces – the means by which a user interacts with the board under test. The GUIs provide both the ability to configure a board and feedback on the test results. Some of the GUIs are quite complex, providing a wide range of board configuration options and test results.

The term "Data Collection Tasks" is meant to designate the software developed to satisfy the requirements for storing a number of data products, other than lags and visibilities, which will be produced by the boards. The most likely approach to these tasks is that the appropriate module
access handlers (MAHs) will stream the data to external processes that will then collect the data and write it to files. The MAHs are hosted by and execute on the CMIBs that reside on the actual prototype boards. The data collection processes are external to the boards and CMIBs. They will likely be hosted by some component of the board test setup, perhaps the machine that serves as an OS and applications server for the CMIBs. The requirement for these data collection tasks is specified in the Requirements and Functional Specification (RFS) document entitled "EVL A Correlator, Software Requirements For the Testing of the Board Prototypes", RFS Document A25204N0001, Rev 1.2, by Sonja Vrcic and Bruce Rowen, October 19, 2005, located on: http://www.drao-ofr.hia-iha.nrc-cnrc.gc.ca/science/widar/private/Software.html. Information on the file format to be used for the data to be collected can be found in NRC-EVLA Memo #026, "EVL A Correlator Output Data Format", Rev. 1.3, 21Nov2005, S. Vrcic, located on: http://www.drao-ofr.hia-iha.nrc-cnrc.gc.ca/science/widar/private/Memos.html.

By Plotting software is meant items such as section 1.1.36.e Graphical Representation of Station Board Output and section 1.1.312 Graphical Representation of CBE Output. The term is pretty much self-explanatory. Please see the specific items cited for further information.

The Correlator Backend (CBE) software is a prototype version of the software that will run on the actual CBE. The CBE software receives frames containing header information and lags from the Baseline board. It will then perform a long-term integration of the lags, will write some intermediate data products for later analysis, and will perform an FFT on the lag data.

Infrastructure and utility items are too numerous to list in detail. This category includes everything from the CMIB servers at Socorro and DRAO to software used to generate test vectors, models, and filter coefficients. Most of the infrastructure and utility items have been omitted from this document. For further information see the aforementioned RFS document "EVL A Correlator, Software Requirements For the Testing of the Board Prototypes", document number A25204N0001, Rev 1.2, Sonja Vrcic, Bruce Rowen, October 19, 2005.

1.1.3 Task Breakdown: WIDAR Prototype Board Tests
This task breakdown does not attempt to be exhaustive. Rather, it attempts to capture the bulk of the tasks that can be considered critical or essential to the testing of the prototype WIDAR correlator boards and the prototype correlator chip. Even for that case, not all of the necessary software tasks are present in this task list. Items such as necessary software capabilities on the fiber optic receiver module (FORM) and software used to generate various test vectors and models have been omitted. For additional information on the requirements and functional specifications for the correlator prototype test software, please see "EVL A Correlator, Software Requirements for the Testing of the Board Prototypes", RFS Document A25204N0001, Rev 1.2, Sonja Vrcic, Bruce Rowen, October 19, 2005, located on: http://www.drao-ofr.hia-iha.nrc-cnrc.gc.ca/science/widar/private/Software.html.

1. CMIB <-> GUI/test apps communications software
   Due: 29Apr2005    Developer(s): Bruce Rowen & Kevin Ryan
   Status: Completed

3
2. Specification of GUI framework technology
   Due: 29Apr2005       Developer(s): Kevin Ryan
   Status: Completed

3. Sample common look & feel for GUIs
   Due: 6May2005        Developer(s): Kevin Ryan
   Status: Completed

4. Gbit Transmission test software

   a. Software to load personality file into FPGA
      Due: late June 2005  Developer(s): Bruce Rowen
      Status: Completed

   b. Raw Register Read/Write GUI
      Due: late June 2005  Developer(s): Kevin Ryan
      Status: Completed

5. Timecode Generator Board test software

   The Test and Verification Plan (TVP) for the Timecode Generator Board is document number A25151N001, Revision 1.0, entitled “Test and Verification Plan, Timecode Generator Board”, by Zhang Heng, April 4, 2005. It can be found on the web page: http://www.drao-ofr.hia-iha.nrc-cnrc.gc.ca/science/widar/private/Other_Boards.html

   a. Module Access Handler (MAH)
      Due: late June 2005  Developer(s): Bruce Rowen
      Status: Completed

   b. GUIs
      Since only 3 GUIs have been specified for the Timecode Generator Board Tests they will be listed.

      1. Board Top-Level GUI
         Due: late June 2005  Developer(s): Kevin Ryan
         Status: This screen is responsible for the loading of the personality file into the FPGA. It has been agreed that this function will be handled by a command line interface (CLI) until the MAH can be enhanced to support this functionality in a GUI. The CLI-based capability is in place & ready.

      2. Timecode Generator FPGA GUI
         Due: late June 2005  Developer(s): Kevin Ryan
         Status: Completed
3. Raw Register Read/Write GUI
   Due: late June 2005  Developer(s): Kevin Ryan
   Status: Will use the same Raw Register Read/Write GUI as the Gbit Transmission Test.

6. Station Board Prototype Test Software
   The TVP for the Station board is document number A25040N0003, Revision 0.0, entitled “Test and Verification Plan, Station Board”, by Dave Fort, 6 April 2005. It can be found on the web page:

   a. Module Access Handlers (MAHs)

      1. Input MAH
         Due: 11/2005  Developer(s): Bruce Rowen
         Status: Completed

      2. Delay MAH
         Due: 11/2005  Developer(s): Bruce Rowen
         Status: Completed

      3. Autocorrelation MAH
         Due: 11/2005  Developer(s): Bruce Rowen
         Status: Completed

      4. FIR Filter MAH
         Due: mid-Jan 2006  Developer(s): Bruce Rowen
         Status: Nearly complete. Expected completion date is 12/30/2005.

      5. Output MAH
         Due: 12/2005  Developer(s): Bruce Rowen
         Status: Completed

      6. Timing MAH
         Due: mid-Jan 2006  Developer(s): Bruce Rowen
         Status: As of 12/19/2005, the work is just beginning. It is expected that this module will be completed on schedule

      7. VSI MAH
         This item is the VLBA interface. It is not actually funded for Phase I of the EVLA. The only planned work on this item for Phase I of the EVLA is to leave a blank footprint on the Station Board. It is unlikely that there will be any hardware or software development on this item during Phase I of the EVLA.
Due: no date set             Developer(s): Bruce Rowen  
Status: no development planned at this time.

8. MCB MAH
Due: end of February 2006     Developer(s): Bruce Rowen  
Status: Not yet started

9. Configuration MAH
Due: mid-February 2006       Developer(s): Bruce Rowen
Status: Not yet started

b. Station Board software for TIMECODE Generator
Basically, this item calls for the development of software that will allow the baseline board to be tested without a station board by using the TIMECODE Generator as a Station board simulator.

Due: mid-February 2006        Developer(s): Bruce Rowen
Status: Not yet started

c. GUIs
Some minimal prioritization of the GUIs has been specified. Of the 30+ screens specified in the Station Board Test and Verification Plan (TVP), those needed soonest will be:

1. The CRC GUIs
   The CRC GUIs are a group of 11 screens that display accumulated CRC errors for the inputs and outputs of the Input Chip, the Delay modules, the Autocorrelation Chip, the Filter Banks, and the inputs of the Output and Timing Chips.

   Due: mid-January 2006 (?)   Developer(s): Sonja Vrcic
   Status: Status assessment done at DRAO

2. A GUI or GUIs to display internal FPGA errors
   Due: mid-January 2006 (?)   Developer(s): Sonja Vrcic
   Status: Status assessment done at DRAO

3. A GUI to display Input Chip state count histograms
   Due: mid-January 2006 (?)   Developer(s): Sonja Vrcic
   Status: Status assessment done at DRAO

4. A GUI to display Filter Chip state count histograms
Due: mid-January 2006 (?)  Developer(s): Sonja Vrcic
Status: Status assessment done at DRAO

d. Station Board Data Collection Tasks
For more information on Data Collection Tasks, see section 1.1.2 of this document, “Discussion: WIDAR Prototype Board Tests”.

Due: March 2006 (?)  Developer(s): Not yet specified
Status: Not yet started

1. Auxiliary data to file(s)
The exact list of auxiliary data that will be saved is TBD.

2. Input and output state counts to a file.

3. Wideband Correlator (WBC) products to a file

4. Raw output data for one filter (radar mode) to a file

e. Graphical Representation of Station Board Output
This software will plot the data saved by the Station Board Data Collection Tasks.

Due: ?  Developer(s): Dave Del Rizzo (DRAO)
Status: Status assessment done at DRAO

1. Input FPGA input state counts (histogram)

2. Input FPGA output state counts (histogram)

3. Filter FPGA output state counts (histogram)

4. WBC FPGA cross power vs. lag

5. WBC FPGA cross power spectrum for a frequency range

6. Filter FPGA pre-quantizer power and noise diode on/off vs. time

7. Filter FPGA post quantizer power vs. time

8. Filter FPGA tone extractor amplitude vs. time

9. Filter FPGA tone extractor phase vs. time

10. Output FPGA spectrum of radar mode output
7. Baseline Board Prototype Test Software


a. Module Access Handlers (MAHs)

Due: Summer, 2005  Developer(s): Bruce Rowen

1. Correlator Chip MAH
   Status: Completed

2. Recirculation Controller MAH
   Status: Completed

3. Ethernet Transmitter MAH
   Status: Completed

4. LTA Controller MAH
   Status: Completed

5. MCB Interface & Clock Selector MAH
   Status: Completed

b. GUIs

1. Baseline Board Top Level GUI
   There are two panes in this GUI – one contains the graphical representation of the baseline board and the other provides a means of loading correlator chip configurations from files.
   
   Due: No date specified  Developer(s): Kevin Ryan
   Status: Overall, ~ 75% complete. The pane for loading chip configurations from a file is approximately 50% complete.

2. The Recirculation Controller GUI
   Due: mid-January 2006  Developer(s): Kevin Ryan
   Status: ~ 80% complete

3. The Correlator Chip GUI
   Due: 15Oct2005  Developer(s): Kevin Ryan
   Status: Completed

4. LTA GUI
5. Gbit Ethernet GUI
   Due: 22Dec2005  Developer(s): Kevin Ryan
   Status: Completed

6. Recirculation Controller Raw Register GUI
   Due: 13Jan2006  Developer(s): Kevin Ryan
   Status: Not yet started

7. Correlator Chip Raw Register GUI
   Due: 13Jan2006  Developer(s): Kevin Ryan
   Status: Not yet started

8. LTA Controller Raw Register GUI
   Due: 13Jan2006  Developer(s): Kevin Ryan
   Status: Not yet started

9. GigE Chip Raw Register GUI
   Due: 13Jan2006  Developer(s): Kevin Ryan
   Status: Not yet started

10. Baseband Configurations GUI Screen
    This GUI has a lower priority. It is wanted more for on-the-sky testing than for lab tests of the prototype boards.
    Due: No date specified  Developer(s): Kevin Ryan
    Status: Not yet started

11. HM Gbps Receiver GUIs
    The term “HM gigabit per second (Gbps) receiver” refers to the high speed Station Board to Baseline Board (and, therefore, rack-to-rack) transmission system.
    Due: end of January 2006  Developer(s): Kevin Ryan
    Status: Not yet started

8. General MAH Tasks
   a. MAH Optimization
      Code cleanup – housekeeping and code optimization for the MAH code base.
      Due: mid-February 2006  Developer(s): Bruce Rowen
      Status: Not yet started
9. General GUI Tasks

a. GUI code optimization
This task will consist of housekeeping and code optimization for the GUI code base as a whole – creation of a rational directory structure for the files, refactoring, repackaging and renaming as necessary, consistency in the methods used, etc.

Due: February 2006  Developer(s): Kevin Ryan
Status: Not yet started

b. Update the basic GUI RFS document – “Prototype Board Test and Verification User Interface Description”, A25220N0000
Due: After GUI code optimization has been complete
Developer(s): Kevin Ryan
Status: Not yet started

10. Single Screen GUI (Station & Baseline Boards) to Configure Entire System Under Test
Due: No date currently specified  Developer(s): Kevin Ryan
Status: Not yet started

11. Correlator Backend (CBE) Software tasks
At this point in the development timelines, the CBE tasks are focused on the need to support testing of the prototype boards at Penticton.

a. Installation of software to produce simulated correlator frames on Penticton server.
Due: Summer 2005  Developer(s): Tom Morgan
Status: Completed

b. Installation of CBE input task (on Penticton server) to receive lag frames from prototype baseline board.
Due: Summer 2005  Developer(s): Tom Morgan
Status: Completed

c. Installation of CBE data processing task on Penticton server.
Due: Summer 2005  Developer(s): Tom Morgan
Status: Completed
d. Installation of command line interface (CLI), control task and monitor task on laptop.
Due: Summer 2005  
Developer(s): Tom Morgan  
Status: Completed

e. Tests of ability of Penticton server and laptop installed tasks to intercommunicate.
Due: Summer 2005  
Developer(s): Tom Morgan  
Status: Completed

f. CBE SW modification to write intermediate data files (for plotting)
Due: Initial set of modifications are due by 28Feb2006  
Developer(s): Tom Morgan, on contract  
Status: Not yet started

1. Installation of modified CBE SW at DRAO
Due: At start of tests of prototype Baseline Board, ~ 01April2006  
Developer(s): Tom Morgan, on contract  
Status: Not yet started

12. Graphical Representation of CBE Output
Due: March or April 2005 (?)  
Developer(s): Dave Del Rizzo (DRAO)  
Status: Status assessment done at DRAO

a. Amplitude vs. lags (real vs. time, imaginary vs. time magnitude vs. time)

b. Amplitude vs. frequency (Fourier transform of lags)

c. 3D graph: magnitude, lag, FFT of time

d. 3D graph: magnitude, frequency (FFT of lag) FFT of time

13. Miscellaneous Items

a. CMIB server at DRAO
   Basically, this item creates a means by which CMIBs on test boards can download the CMIB OS and other files and applications.

   Status: Completed in May-June 2005

b. CMIB server at Socorro
   A crude version was put in place early in 2005. A more fully developed version with enhanced capabilities came online in late September or early October 2005.
c. **PCMC board tests**

The PCMC (PC/104 Monitor/Control Mezzanine Card) board is an interface board that allows the PC/104 Plus CMIB to communicate with modules on the WIDAR Correlator boards.

Status:  (As of early June 2005) CMIB <-> PCMC communication and the ability of the CMIB to read the interface to the monitor/control bus (MCB) that is to be present on all correlator boards has been tested. The tests were successful. Additional hardware is needed to enable testing of CMIB read/write access to modules on the correlator boards.

d. **Access to CMIBs in Penticton B.C. from Socorro, NM**

Status: Completed