EVLA Correlator Prototype and OTS Testing

B. Carlson
Outline

• Initial prototype testing.
  – Test setups.
  – Test equipment.

• Prototype system testing.

• On-the-Sky (OTS) testing.
  – Review of DRAFT test plan.

• Schedule.
Initial Prototype Testing

- Station Board and Baseline Board tested separately.

- Station Board contains its own timing, test vector generators, and has loopback test capability for testing HM Gbps.

- Baseline Board stimulated with a Timecode Board.
  - TGB FPGA special design used to generate HM Gbps signals for testing.
  - Prototype Corr Chips socketed…all sites can be tested…some risk.
  - Formal qualification of Corr Chips before full ASIC production (hopefully in ’06).
TVP: A25040N0003
Baseline Board proto testing

- Description of test vectors, GUI panels, CBE requirements in appendix of Correlator Chip prototype verification matrix document A25082N0005 (in prep, no DRAFT release yet).
B. Carlson, 2006-Apr 3-4

EVLA Correlator S/W F2F - Prototype testing
### Timing and Dump Control

- **Enable TIMECODE**
- **DUMPTRIG Enable**
  - Sync Test Frame
  - Speed dumps
  - Normal dumps

<table>
<thead>
<tr>
<th>DATA str</th>
<th>Period (usec)</th>
<th>Dump Modulo</th>
<th>LTA</th>
<th>Frames/s/CCC/chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATA-0</td>
<td>20</td>
<td>4</td>
<td>100</td>
<td>500</td>
</tr>
<tr>
<td>DATA-1</td>
<td>40</td>
<td>8</td>
<td>200</td>
<td>125</td>
</tr>
<tr>
<td>DATA-2</td>
<td>60</td>
<td>12</td>
<td>300</td>
<td>56</td>
</tr>
<tr>
<td>DATA-3</td>
<td>80</td>
<td>16</td>
<td>400</td>
<td>31</td>
</tr>
<tr>
<td>DATA-4</td>
<td>100</td>
<td>20</td>
<td>500</td>
<td>20</td>
</tr>
<tr>
<td>DATA-5</td>
<td>120</td>
<td>24</td>
<td>600</td>
<td>14</td>
</tr>
<tr>
<td>DATA-6</td>
<td>140</td>
<td>28</td>
<td>700</td>
<td>10</td>
</tr>
<tr>
<td>DATA-7</td>
<td>160</td>
<td>32</td>
<td>800</td>
<td>8</td>
</tr>
</tbody>
</table>

### Data Stream Control

- **Sample rate Ms/s**: 256
- **DATA Stream IDS**
  - SID, SBID, BBID

<table>
<thead>
<tr>
<th>DATA</th>
<th>SID</th>
<th>SBID</th>
<th>BBID</th>
<th>DATA Stream IDS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATA-0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>03026EFB 00259506</td>
</tr>
<tr>
<td>DATA-1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0D416D36 00A58873</td>
</tr>
<tr>
<td>DATA-2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>05B36D0B 0047310D</td>
</tr>
<tr>
<td>DATA-3</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1A060683 0144FA12</td>
</tr>
<tr>
<td>DATA-4</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>08646C1B 0068CD14</td>
</tr>
<tr>
<td>DATA-5</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>26CA9FCF 01E46BB2</td>
</tr>
<tr>
<td>DATA-6</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0B156AAB 008A691B</td>
</tr>
<tr>
<td>DATA-7</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>338F391C 0283DD52</td>
</tr>
</tbody>
</table>

### PHASEMOD Models

- **PHASEMOD coeffs**

<table>
<thead>
<tr>
<th>DATA</th>
<th>x</th>
<th>P0</th>
<th>P1</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATA-0</td>
<td>105</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>DATA-1</td>
<td>115</td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>DATA-2</td>
<td>125</td>
<td>7</td>
<td>2</td>
</tr>
<tr>
<td>DATA-3</td>
<td>135</td>
<td>9</td>
<td>3</td>
</tr>
<tr>
<td>DATA-4</td>
<td>145</td>
<td>11</td>
<td>4</td>
</tr>
<tr>
<td>DATA-5</td>
<td>155</td>
<td>13</td>
<td>5</td>
</tr>
<tr>
<td>DATA-6</td>
<td>165</td>
<td>15</td>
<td>6</td>
</tr>
<tr>
<td>DATA-7</td>
<td>175</td>
<td>17</td>
<td>7</td>
</tr>
</tbody>
</table>

### CRC Error Generation

- **Auto-calculate PHASEMOD coeffs**
- **Re-Calculate PHASEMOD coeffs for current sample rate**

### PHASERR Models

- **TIMECODE**
- **DUMPTRIG**
- **PHASERR0_1**
- **PHASERR2_3**
- **PHASERR4_5**
- **PHASERR6_7**
- **PHASEMOD**
- **DATA-0**
- **DATA-1**
- **DATA-2**
- **DATA-3**
- **DATA-4**
- **DATA-5**
- **DATA-6**
- **DATA-7**
Baseline Board

- Raw frames from CBE inspected for correctness.

- Plots from CBE…cross-correlation of vectors generated by TGB special FPGA (should) produce fringes.

- Vectors support bit-exact comparison of hardware via CBE’s raw floating-point Re/Im lags with S/W reference correlator.
  - Don’t need to use Corr Chip RTL simulation (slow).
  - Not quite bit-exact—within double-precision floating-point numerical error.

- Also, perform redundant correlations…compare with each other.
aaa
W0: START SYNC WORD -- OK
W1: B31=ASIC[1] Yin=1 Xin=1 XSyner=0 XSyner=0 ACC_OV=0 OVR=0 Rsrv=00000000 NUM_CLAGS= 128 CCC=13 Cmd=010
W2: BBID-Y=0 SBID-Y= 7 SID-Y=100 BBID-X=1 SBID-X= 3 SID-X=200
d972e2900 W3: LTA/Phase bin=55666 Recirc_blk-Y=233 Recirc_blk-X= 0
W4: TIMESTAMP=- 222333444
W5: TIMESTAMP=- 555666777
W6: DVCOUNT-Cntr= 2153
W7: DVCOUNT-Edge= 2119

0003a300 W8: DATA_BIAS = 238336
0003a545 Lag 0 = 238917
0003a3e6 Lag 0 = 238566
0003a5f8 Lag 1 = 239096
0003a5d8 Lag 1 = 238552
0003a370 Lag 2 = 238448
0003a1fa Lag 2 = 238074
0003a3a6 Lag 3 = 238502
0003a078 Lag 3 = 237688
0003a2af Lag 4 = 238255
0003a1d2 Lag 4 = 238034
0003a2ce Lag 5 = 238286
0003a268 Lag 5 = 238184
0003a3b6 Lag 6 = 238518
0003a256 Lag 6 = 238166
0003a1fc Lag 7 = 238076
0003a1fa Lag 7 = 238074
0003a20a Lag 125 = 238090
0003a3fe Lag 125 = 238590
0003a6cc Lag 126 = 239080
0003a57c Lag 126 = 238972
0003a550 Lag 127 = 238928
0003a418 Lag 127 = 238616
1c7c71c W265: END SYNC WORD -- OK
b9fa8535 W266: Checksum calculated OK
1.675218060543869e-01   -1.723961005643920e-01
3.732683427398666e-02   -1.918932786044125e-01
-5.438686505900462e-02  -1.096716264751154e-01
1.282709081580298e-03   5.246280143663417e-02
.
.
.

CBE raw floating-point output
Test Equipment

- **Agilent 16900A/16950A logic analyser.**
  - 64 channels, 600 MHz state, 4 GHz timing.
  - Mate with soft-touch probe headers on board.
  - 4 test pins out of FPGAs.

- **Agilent Infineon Digital Storage Oscilloscope.**
  - 4 channels, 20 Gs/s/channel. 7 GHz bandwidth.
  - 2 differential or single-ended probes.
  - Probing...difficult due to speed, signal integrity, routing density...use signal vias...special probing kits.
  - Jitter analysis software.

- **X-ray machine, BGA re-work machine.**
Prototype System Testing

• Connect Station Board outputs to Baseline Board inputs.

• Establish/test HM Gbps connectivity.

• Delay Module test vectors stimulate Station Board and downstream Baseline Board.
  – Compare results with software filter/correlator that processes the same test vectors.
  – Not bit-exact comparison…statistical only.
On-the-Sky Testing (OTS)

- DRAFT Test Plan A25010N0005.

- Prototype correlator test setup.

- 45 tests. Specified in plan in an overview fashion. Details filled in with GUIs/configuration files.

- Digital tone comb generator in DTS Tx or Rx or Station Board Input Chip useful…for detecting timing/delay tracking hiccups with Filter Chip tone extractor.
Fan Tray

Ethernet Switch

12U crate

"External Timecode" (fiber)

128 MHz CW, 0dBm

From NRAO Array Timing Reference

Host Computer

Backend Computer

110 VAC, 15 A

To NRAO network

-48 VDC Breaker Panel

-Timecode Board

Station Board

Station Board

Station Board

Station Board

Baseline Board

Station Board

Station Board

Station Board

Station Board

Timecode Board

1 phase: 170-264 VAC (30 A)
<table>
<thead>
<tr>
<th>TEST</th>
<th>Purpose of Test</th>
<th>Description/Test Setup</th>
<th>Expected Outcome</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Shipping damage check, prototype correlator installation and setup.</td>
<td>Unpack system, check for damage, install boards. Install system in test location.</td>
<td>All components available and undamaged. System installation successful.</td>
<td>Some assembly required.</td>
</tr>
<tr>
<td>1</td>
<td>System power-up and self-check with local 128 MHz oscillator on the Timecode Board.</td>
<td>Connect AC power to -48 VDC power supply. Connect AC power to AC-powered components. Power-up system, use the Timecode local crystal oscillator. Perform Station Board checks. Perform Baseline Board checks. Check connectivity of Station-to-Baseline</td>
<td>All self-checks and functions ok. Backend receives frames. RTDD can display data products.</td>
<td>No antennas are required.</td>
</tr>
<tr>
<td>2</td>
<td>Computer network setup and check.</td>
<td>The Host Computer must be connected to the embedded processors via the switch. The switch is connected to the NRAO network to allow for time setting (or this setting may be manual via a control computer GUI), and for connection to Model Server.</td>
<td>Connected to network. Communications established with NRAO Model Server.</td>
<td>The control computer sets correlator configurations. The only connection to EVLA M&amp;C is the Model Server and, optionally, the time setting.</td>
</tr>
<tr>
<td>3</td>
<td>Run self-checks with connection to NRAO &quot;External Timecode&quot;, and 128 MHz 0 dBm CW.</td>
<td>Same as TEST 1, except use NRAO time reference. Check for timing synchronization of TIMECODE to array UTC.</td>
<td>TIMECODE synchronized to NRAO UTC. Phase-lock achieved on all chips on all boards. All intra-system checks ok.</td>
<td>No antennas required.</td>
</tr>
<tr>
<td></td>
<td><strong>First fringe test</strong></td>
<td><strong>Description</strong></td>
<td><strong>Tests Performed</strong></td>
<td><strong>Notes</strong></td>
</tr>
<tr>
<td>---</td>
<td>----------------------</td>
<td>-----------------</td>
<td>---------------------</td>
<td>----------</td>
</tr>
<tr>
<td>11</td>
<td>First fringe test, single, short baseline, 8-bit, 4-bit re-quantization. One sub-band. One antenna should be &quot;Reference Antenna&quot;, with well-known LO fiber delay.</td>
<td>Set RF to C-band for minimal interference. Set antenna differential frequency shift to 1 kHz. Observe and track strong continuum source. Turn on digital tone comb generator in DTS transmitter. Turn on one sub-band filter at the center of the wideband.</td>
<td>Stable phase-cal ampl and phase vs time, with delay tracking active. State counts, auto-spectra, power measurements within normal regions. Cross-correlation fringes detected, displayed with RTDD. Ampl and phase vs frequency as expected. SNR as expecte</td>
<td>This test requires 2 antennas, possibly for an extended period of time.</td>
</tr>
<tr>
<td>12</td>
<td>First fringe check compared with old correlator, short baseline.</td>
<td>Single baseline fringes with old correlator for comparison with new correlator, TEST 11. Minimal setup change…route analog out of DTS receiver to old correlator. Fshifts turned off.</td>
<td>Check SNR and normalized amplitudes. Check spectrum. Check and compare with AIPS.</td>
<td>This test requires 2 antennas for a short period for the observation. Comparison of old and new correlator can be performed off-line.</td>
</tr>
<tr>
<td>13</td>
<td>Fringe test, single, short baseline, 3-bit, 4-bit re-quantization. One sub-band.</td>
<td>Set RF to X-band for full 2 GHz bandwidth. Set differential frequency shift to 1 kHz. Observe and track strong continuum source. Turn on digital tone comb generator in DTS transmitter. Turn on one sub-band filter at the center of the wideband. Turn o</td>
<td>Stable phase-cal ampl and phase vs time, with delay tracking active. State counts, auto-spectra, power measurements within normal regions. Cross-correlation fringes detected, displayed with RTDD. Ampl and phase vs frequency as expected. SNR as expecte</td>
<td>This test requires 2 antennas, possibly for an extended period of time.</td>
</tr>
<tr>
<td></td>
<td>High SNR solar observation.</td>
<td>Correlator settings as required by astronomy teams, possibly incorporating &quot;wideband recirculation&quot;. Possibly requiring 64 lags per CCC output mode from correlator.</td>
<td>Results as required by astronomy teams.</td>
<td>This test requires 4 antennas for the duration of the experiment.</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>31</td>
<td>Narrowband, high-spectral resolution.</td>
<td>Maximum spectral resolution on desired sub-band bandwidth. Possibly 1 Hz resolution. Correlator settings, number of antennas, set by astronomy team. Try to exercise all stages in the Filter Chip.</td>
<td>Results as required by astronomy teams.</td>
<td>This test requires 4 antennas for the duration of the experiment.</td>
</tr>
<tr>
<td>32</td>
<td>Radar-mode data capture.</td>
<td>Set sub-band for capture to 31.25 kHz. Capture data into NFS files. Use Filter Chip Stage 2 mixer to stop fringes and very-fine delay tracking. Observe spectral-line source with continuum.</td>
<td>Correlate captured data in software. Ensure results are as expected.</td>
<td>This test requires 4 antennas for the duration of the data capture portion of the experiment.</td>
</tr>
<tr>
<td>33-44</td>
<td>Astronomer-driven key science experiments of various kinds: continuum, high dynamic range spectral-line, mixed continuum and spectral-line, pulsar, recirculation, fast dumping, long integrations, radar mode.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
OTS

• Station Board real-time S/W critical for OTS testing.
  – Delay tracking…models from NRAO “Model Server”.
  – Phase model generation.
  – Dump control (DUMPTRIG) generation.
  – Acquisition of state counts, wideband correlation coefficients, etc.

• “Programmer’s Guide” (A25290N0000) contains comprehensive information on many low-level real-time functions that software needs to control.
OTS

• Many tests require science input and work for source selection and image processing/data analysis.

• Last 10 tests are completely astronomer-driven experiments of various kinds.

• OTS testing not used to qualify hardware for Stage 3 production. Used to demonstrate correlator functionality, provide “early”-use correlator, 1st step in total system integration testing.
Schedule

• Many unquantifiable uncertainties/risks. Have paid in $, time, and tools to minimize risks as much as possible.

• Allocated ~6 months for initial prototype testing.

• Another ~6 months for getting proto corrs for OTS ready.

• ~4 months for OTS testing.

• ~Nov. 15/06 deadline for decision on Corr chip production in FY 06/07. Currently $ not in FY 06/07 budget.
**This schedule assumes no re-spins will be necessary.**
**This schedule is the current quasi-optimistic view of the project.**
**Long Term Schedule Modifications (from the previous edition - 06Feb2006):**

--- Task 1: Stage 1 Prototype Hardware in Penticton end date has been pushed out by one month to the end of May 2006.
--- Task 2: Stage 1 Prototype PCB Acceptance Testing is now no longer dependent on Stage 1 Prototype Hardware in Penticton being complete because some testing can begin before all boards are in house. This task has now been set to start mid-May 2006, the current estimate for delivery of the Baseline Board Stage 1 Prototype.
--- Task 15: Prototype Software end date has been pushed out by two months to 25Oct2006.