Correlator
Outline

• Requirements
• Architecture
• Technology
• Software
• Budget
• Schedule
• Installation
Requirements

- 16 GHz bandwidth (8 x 2 GHz bands).
- 16,384 spectral channels/baseline (wideband), 0.25 million (narrower w/recirculation).
- 16 independently tunable digital sub-bands/baseband + N.B. radar filter.
- Flexible: tradeoff B.W. for freq. channels.
- 2 banks of 1000 phase bins/baseline.
- High performance, flexible dumping.
- Very long baseline capable (>10k km baselines).
- 1/16th sample digital delay tracking.
- Baseband and sub-band multi-beaming…on the same data.
- Simultaneous 1 GHz B.W. phased output on multiple sub-arrays.
# Requirements

<table>
<thead>
<tr>
<th>Description</th>
<th>“Dream” Correlator Spec.</th>
<th>Planned deliverable</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>No. of antennas</strong></td>
<td>36</td>
<td>32, expandable</td>
</tr>
<tr>
<td><strong>Bandwidth</strong></td>
<td>4 x 2 x 2 GHz (16 GHz)</td>
<td>4 x 2 x 2 GHz (16 GHz)</td>
</tr>
<tr>
<td><strong>Freq. Resolution</strong></td>
<td>few Hz ... 10’s MHz</td>
<td>1 Hz ... 2 MHz</td>
</tr>
<tr>
<td><strong>No. of independently tunable IF pairs</strong></td>
<td>at least 4, prefer 8</td>
<td>64, with digital sub-bands</td>
</tr>
<tr>
<td><strong>No. of frequency channels</strong></td>
<td>1000 (full polarization per IF pair), 8000 total</td>
<td>1024 W.B. (more w. recirc)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16384 W.B. total (more w. recirc)</td>
</tr>
<tr>
<td><strong>Frequency channel flexibility</strong></td>
<td>split flexibly among IFs, select subset for writing</td>
<td>split flexibly among IFs and sub-bands, select subset for writing</td>
</tr>
<tr>
<td><strong>Flexibility</strong></td>
<td>Frequency resolution: factors of 2 Flexible tradeoffs (#baselines, B.W., #channels, pol’n, time res’n)</td>
<td>Ok</td>
</tr>
<tr>
<td></td>
<td>Interf. sub-arrays: 4 independent Phased sub-arrays: 4 independent</td>
<td>Can’t tradeoff baselines at full bandwidth Interf. sub-array: unlimited. Phased sub-arrays: 5</td>
</tr>
<tr>
<td><strong>Integration times</strong></td>
<td>0.1 sec (less with tradeoffs)</td>
<td>0.011 sec (less with tradeoffs)</td>
</tr>
<tr>
<td><strong>Total data rates</strong></td>
<td>few tens of Mvis/sec</td>
<td>several Gvis/sec</td>
</tr>
<tr>
<td><strong>Autocorrelations</strong></td>
<td>all stokes parameters</td>
<td>W.B. all stokes, SNR loss S.B. all stokes, no SNR loss</td>
</tr>
<tr>
<td><strong>RFI</strong></td>
<td>as many channels as possible 10^6 dynamic range automatic flagging gating</td>
<td>Ok: 16,384...262,144 4-bit sampling standard, up to 8-bit sampling avail (d.r. depends on noise+RFI) post-corr. interference excision + facilitates post-corr. cancellation. from antenna, external signal</td>
</tr>
<tr>
<td><strong>Pulsar phase binning</strong></td>
<td>up to 1000</td>
<td>2 x 1000, min 15 μsec each</td>
</tr>
<tr>
<td><strong>Phase Cal</strong></td>
<td>at least auto-spectra</td>
<td>minimum 1 pCal extractor/IF</td>
</tr>
<tr>
<td><strong>Delay tracking</strong></td>
<td>1/16th sample, 250 km baseline</td>
<td>digital ±1/32nd sample, 10^4 km+ bl</td>
</tr>
</tbody>
</table>
Architecture

• FIR filter banks followed by complex XF correlator:
  – “Stitch” sub-bands together after correlation to yield wideband cross-correlation.
  – Use small LO offsets in antenna to keep fringe rotators “wet”: fringe stopping, anti-aliasing, artifact decorrelation, digital sub-sample delay tracking, VLBI.
  – Each poly-phase FIR independently programmable for flexibility…scientific req’t.

• Three main modules:
  – Station Board (2 x 2 GHz).
  – Baseline Board (64 baselines ea).
  – Phasing Board (48 stations, 2 sub-bands, 5 sub-arrays).

• Plus some 4 small interconnect modules…expandable, flexible.
Architecture
Architecture

Station Board

-48 V DC to 1.8V, 2.5V POWER SUPPLY

FIR Filter Bank

FIR Filter Bank

Switch

Switch

Timing

Wideband Autocorrelator

DELAY

DELAY

Fibre-Optic Receiver Module
Architecture

Baseline Board

- 8 x 8 Correlator Chip and LTA Controller Matrix
- 8 'Y' Recirculation Controllers

- MCB Interface Module
- SERIAL I/F(s)
- -48 VDC to 1.8V, 2.5V POWER SUPPLY

8 'X' Recirculation Controllers
Architecture

Phasing Board

(5) Sub-array 2nd-Stage Adders

4-Station Complex Mixer + 1st Stage Adder

4-Station Complex Mixer + 1st Stage Adder

4-Station Complex Mixer + 1st Stage Adder

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4-Station Complex Mixer + 1st Stage Adder

4-Station Complex Mixer + 1st Stage Adder

FIR Filter Bank

Switch

MCB Interface Module

48 Station Data Entry Connectors

-48 VDC to 1.8V, 2.5V POWER SUPPLY

Brent Carlson
EVLA System PDR (Correlator V2)
December 4-5, 2001
• Future upgrade possibilities:
  – “maxed-out” on bandwidth.
  – replace Baseline Board with “Moore” lags…(more channels and/or more bandwidth in bandwidth/number of antennas tradeoff.)
  – keep existing software and hardware infrastructure…painless upgrade.
Technology

• 256 MHz system clock rate:
  – FPGA and gate array tech. supports this.
  – Development tools (Mentor/Cadence) well-equipped for this speed/complexity.
  – Can de-scope to 128 MHz on PCB (with 256 MHz interconnects) if absolutely necessary.

• FIR filter:
  – Prototype in FPGA (power, $$). Convert to 0.18 µm gate array (AMIS). Should be able to get 1024 taps. ($200k NRE, $50 ea, 10k qty). Claim that they use 1/5th the number of gates for same function as Xilinx.
  • 2048-tap power estimate: 20 nW/MHz/gate * 300k gates * 256 MHz * 1.0 (switching fraction) = 1.5W
Technology

• **Correlator chip:**
  
  – **Original plan:** develop full-custom 0.18 μm standard cell from scratch ($900k NRE + $700k production).
  
  – **Current plan:** prototype with scaled-down (fewer lags) FPGA, convert to gate array or standard cell afterwards. *Pushes back technology freeze to latest possible date to take advantage of improvements...*

• **Power:** 20 nW/MHz/gate * 0.5 million (hi-speed switching) gates * 256 MHz * 0.75 transition fraction = 1.9W (2.5W with 1.0 transition fraction)
Software

• Use hierarchical approach (mirrors AMCS):
  – 1 SCC and 1 BCC (perhaps one platform).
  – Use NRAO MIBs on boards.

• Backend software/configs…
Software

A "station input": shares TIMECODE, DUMPTRIG etc.

Sub-band filters (16)
- copy_control
- physical_SBout
- dataParms
- PCal_Parms
- stats_Parms
- autocorr_Parms
- antenna_coords
- recirc_Parms
- requant_Parms
- num_spec_chans
- num_pol

Indicates what we want the correlator to do with this sub-band, but not how it is done.

Sub-band Control Parameters
- BBstr(a...b)
- BB_width
- slot_factor
- slot_number
- filter_Parms
- SB_LO
- fshift
- SRC_coord
- array_center
- delay_Parms
- binning_Parms
- int_time
- polarization
- gating
- pulsar_Parms
- phasing_Parms
- RFI_control

Physical BaseBand Control Parameters
- antenna_ID
- antenna_coords
- SRC_coord
- array_center
- BBstr[16][a...b]
- BBbits[16]
- BBcoding[16]
- BBLO[16]
- BBsideband[16]
- wb_autocorr_Parms
- wb_stats_Parms
Software

NOTES:

X-input, Y-input: PhBB0...PhBB7, or "adjacent"
start_lag, end_lag: full range of lags this CCC acquires.
X/Y_dump_select: X or Y

Sub-band correlator.
Software

Correlator Station Control Data Flow Diagram
Could shave ~$1.3 million off this budget with cheaper cables and AMIS gate array for FIR (& corr chip).
<table>
<thead>
<tr>
<th>Date</th>
<th>Milestone</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1, 2002</td>
<td>New personnel in place. Design tools in place. Training and design work begins.</td>
</tr>
<tr>
<td>Q1, 2004</td>
<td>Critical User Manuals in place. Device driver code can be written.</td>
</tr>
<tr>
<td>Q1, 2005</td>
<td>Prototype test at the VLA starts.</td>
</tr>
<tr>
<td>Q2, 2005</td>
<td>Prototype test at the VLA complete.</td>
</tr>
<tr>
<td>Q2, 2006</td>
<td>Production model test and burn-in, system integration and test in Penticton, and rack and cable installation begins at the VLA.</td>
</tr>
<tr>
<td>Q4, 2006</td>
<td>Begin full installation at the VLA. Earliest possible start of installed correlator testing.</td>
</tr>
<tr>
<td>Q2, 2007</td>
<td><strong>Earliest possible “beta” science data.</strong> (Middle of full installation schedule.)</td>
</tr>
<tr>
<td>Q1, 2008</td>
<td>Correlator commissioning. Correlator fully on-line for observing. Continuing debug support available.</td>
</tr>
<tr>
<td>Q1, 2009</td>
<td>End of project. End of NRC debug support. Full handover to NRAO complete.</td>
</tr>
</tbody>
</table>
Installation

Station Racks (12)

48 VDC Plant

Baseline Racks (24)

Station Racks (12)

Max cable length=36 ft (11 m)

3 Racks = 2 sub-band correlators

48-Station Rack Layout: 1 Floor; 2 sub-racks per 7 ft rack (Nov. 20/2001)
Summary

• Wideband, high-performance, flexible.
• Expandable, re-configurable.
• Painless upgrade path.
• (0→10k+ km baselines).
• $10 - $12 million (32 stations; another ~$6 million for 48 stations).
• Start installation ~2006.
• First “beta” science ~2007.
• Completion 2008-2009.