EVLA Monitor and Control

Module Interface Board (MIB) Design
MIB Block Diagram
Embedded Controller

- Infineon TRICore TC11IB
  - System On a CHIP
  - 12 MHZ External Clock
  - 1.5 MBytes RAM
  - Hardware, Software & Watchdog Resets
  - Sleep Modes
  - Six Thirty-Two Bit Timers
Embedded Controller

- Infineon TC11IB – Interfaces
  - Media Independent Interface (Ethernet)
  - Two Asynchronous Serial Ports
  - One Synchronous Serial Port (SPI)
  - External Bus Unit (EBU)
Ethernet Interface

- Ethernet Interface – 100 MBits/second
  - Translation Chip – Intel LXT971A
  - Fiber Optic Transceiver – Infineon V23809-C8-C10
Flash Memory

- Flash Memory
  - Serial Flash or Parallel Flash (8MByte)
    - Serial Flash?
    - Parallel Flash – AMD Am30LV0064D
  - All Code Documented
Power & Reset Logic

- Power & Reset Logic
  - Power Regulator & Supervisor
    - Texas Instruments TPS70351PWP
  - Watchdog Protection – TC11IB
  - Devices will get User Reset and MIB Reset
  - Devices Must Reset into Safe Condition
Timing Logic

- Timing Logic
  - 19.2 Hz Timing Signal (Heartbeat)
  - 1 PPS Timing Signal?
  - 10 Second Timing Signal?
  - Devices May Require Precise Timing
    - Hardware Timing
Parallel Interface

- Parallel Interface
  - External Bus Unit
  - Thirty-Two Bits Data Transfer (8, 16 or 32)
  - Address Lines (Twenty-Four Possible)
  - Texas Instruments SNLVTH32(244/245)
  - LVTTL Outputs, TTL Compatible
Control Logic

• Control Logic
  ➢ Peripheral Interface Signals
    ◆ RD*, WR*, ALE, WAIT*, CS* Lines
    ◆ Resets*, SPI, etc.
  ➢ Texas Instruments SNLVTH32244
  ➢ LVTTL Outputs, TTL Compatible
Serial Interfaces

• Serial Interfaces
  ➢ Asynchronous Ports
    ◆ One RS232 Modem Port (Auto Off)
      Maxim MAX3225CAP
    ◆ RS485 Port?
  ➢ Synchronous Ports
    ◆ Serial Peripheral Interface Port – SPI