APPLICATIONS AND DEVICE INTERFACE ISSUES
MIB MASTER RACK

SYSTEM DIAGRAM

- GPS Interface
- RF Interface
- Control Reference Interface #1
- LO Transmitter Interface #1
- Master Offset Interface #1
- Control Reference Interface #2
- LO Transmitter Interface #2
- VLA Site Generators
- Control Building HVAC
- Control Building UPS
- Software Watchdogs
- System Buffer
- Data Tap
- Data Set 0
- Weather Station
- Data Set 1
- MT1 Master Rack
- Data Set 2
- MT2 Master Rack
- Data Set 3
- MT1 Master Rack
- Data Set 4
- VLA/LBA Radios
- Data Set 5
- MC Master Rack
- LBT Clock
- 1Ghz Fiber
- Fiber Optic Switch
- 100MHz Fibers
- Wye Monitor Computer
- Transition Only
- Orphans
SERIAL PERIPHERAL INTERFACE (SPI)

Synchronous Serial Communications

Master

MOSI

MISO

Clock

Slave 1

SS

Slave 2

SS

With select lines, one master can communicate with more than one slave
SERIAL PERIPHERAL INTERFACE (SPI)

- Widely Used to Communicate With Many Devices (A/D & D/A Converters, Memory Chips, Temperature Sensors, Microprocessors, Etc.)
- Clock is Idle When Not Used
MIB TO MIB COMMUNICATION

- Can Be Used As Needed – Control Computer to MIB is Most Common
- Pointing Model Interface
- Front End to Cryo Communications
- Total Power to Down Converter Communications
- Utility Module
• “F14 Like Module” In Rack Away From Receiver (To Reduce RFI) Contains MIB
• Each Module Interfaces to One or More Front Ends
• Single 25 Pin Connector Carries All Analog and Digital Signals to/from Receiver Card Cage
FRONT END M & C

- SPI Used for Digital Signals
- Analog Multiplexers to Select Three Analog Signals at a Time
- RFI Issues Must be Considered
Monitor and Control Induced RFI

- Hardware Design to Conform to RFI Plan
- If Glitches Still Occur, Data Could be Flagged Bad
- We Could Plan Periodic Flagging of Data Throughout the Array (Infrequently) For Transactions That May Cause Glitches