Project Plan
Outline

- Design tools
- Personnel
- Correlator chip
- Prototype construction and testing
- Production
- System integration and test
- Delivery and installation
- Design reviews
- Schedule
- Budget
- De-scoping options
Design Tools

• Budget includes nearly $0.5 million for CAE design tools.

• Mentor Graphics and Cadence are primary candidates.

• Demos/initial evaluation indicate impressive capabilities.

• RFP now out…40 day tendering process.

• Expect to be in-place in early 2002…but, requires CFI funding for full complement of tools.
Design Tools

- Tools of this caliber judged to be essential for design of this speed and complexity.
- Integrated end-to-end design environment.
- Integrated FPGA design/synthesis/simulation.
- Powerful PCB-level design:
  - Nets treated as transmission lines.
  - Define constraints that drive PCB design.
  - Pre-PCB P+R design/investigation facilities (signal integrity, timing).
- “Amazingly powerful” PCB P+R capability.
- Post P+R symbolic timing analysis + signal integrity.
  - Allows a complete analysis of waveforms and timing margins before the board is ever fabricated.
Discovery Series

Solve Your High-Speed Design Problems Throughout the Design Process

With over half of today’s designs depending on high performance circuitry, signal integrity issues are an ever increasing reality. The speed and complexity of today’s integrated circuits are pushing interconnect density and timing problems out onto the printed circuit board. Increasing speeds are causing a rise in design iterations in an attempt to solve the associated effects. Mentor Graphics offers the way to address and resolve these issues throughout the design process—from start to finish. With the Discovery Series for high-speed design, you can implement design solutions as you go from design concept to manufacturing output.
Design Tools Cost

- THIS PAGE CONFIDENTIAL
Personnel

- 2 senior digital/DSP engineers (Carlson + ______).
  - Each responsible for 1/2 the project (Station/Baseline Board split).
- 2 digital engineers.
  - FPGA/PCB-level design under direction of senior engineers.
- Eng. Positions now being advertised. Identified “A+” candidate for senior eng.
- 1 engineering assistant.
  - Component investigation/procurement + project manage assistance + organization.
- 1 secretary.
- 1 PCB design specialist (contract position).
- 2 technologists: production.
- 1 software engineer.
- 1 contract mechanical engineer.
- 1 part-time high-level project manager.
Correlator Chip

• Split development into 3 phases:
  – design.
  – prototype fabrication and test.
  – production.

• Current indication is that a 2048 complex-lag chip @ 256 MHz, in 0.18 μm is feasible using low-power VLSI design techniques.
  – Based on work done by Margala at U Rochester (0.25 μm).
  – Possibly obtain multiply-accumulate block from Margala optimized for low-power, and use as instance in standard-cell design environment.
Correlator Chip Design

• Possible design routes:
  – Complete “turn-key” design (GDSII output) (Qthink: ~$XXXk ROM).
  – Design ourselves within a design house environment. CONFIDENTIAL PRICING.

• Experience? Advice?
Correlator Chip Proto. Fab.

- Have contacted MOSIS, and they quote about $80k for 40 prototypes. Suggested longer run (200 to 500 die) to get better yield estimate (extra ~$40k).

- Design for “right first time”, but mistake requiring a 2nd run is not a disaster.
Correlator Chip Prod. Fab.

- MOSIS suggests a dedicated mask.

- For 11k chips:
  - $430k for the mask.
  - $70k/wafer-run (x 12 wafers/run) x 4 runs = $280k. (50% yield)
  - $64/chip + $4/chip packaging ~ = $70/chip.

- Larger production run would reduce per chip cost because of large mask cost.
Correlator Chip Cost Summary

- Total cost for development + production is probably a minimum of ~$1.6 million.

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Prototype Construction

• Plan to use BGA technology (speed, # of pins, reliability).

Problems:
  – Require an X-ray machine for inspection. Cost ~$185k. Could possibly lease for $x/year. **NOT IN BUDGET**.
  – Require a rework machine. Budget $50k.
  – Long-term maintenance?

• Solutions:
  – Out-source prototype construction.
  – Out-source prototype construction with BGA sockets.
  – Lease machine for ~2 years (depends on cost).
  – Minimize BGA use.
Prototype Testing

• CAE tools analysis.
• Test vectors.
• Accelerated-life/stress testing.
• Correlator chip testing.
  – Plan to build S/W emulator, compare results with actual chip.
• VLA-site on-the-sky testing.
  – Deep integration, phase and amplitude closure tests.
  – Limited correlator chip prototypes a problem?
• FPGAs permit post-installation bug fixes.
• CDR before production.
Production

• Procurement of production components.
  – After CDR (but probably some before because of lead-time).
• Qualification and selection of a production house.
  – Critically important!
• Production, including on-site testing and quality assurance.
  – Go/nogo tests to minimize future rework requirements.
• Production module accelerated-life testing.
  – Thermal cycling (thermal stress).
  – Vibration (mechanical stress to find marginal solder joints).
  – ~200 hr burn-in @ 35-40°C (thermal breakdown).
  – Minimize field infant mortality, maximize reliability.
System Integration and Test

- Starts with prototype testing.

- Penticton-site testing with substantial slice of correlator.
  - Hopefully find bulk of bugs where they are easiest to track down and fix.

- VLA-site installed correlator testing. Run in parallel with old correlator and gradually phase-in full operation.
Delivery and Installation

• Prepare correlator room at VLA starting mid-2005.

• Install racks and cables at VLA mid-2006 concurrently with production module test and system integration tests in Penticton to expedite installation.

• Begin full installation ~late 2006.
Design Reviews

• 3 formal reviews:
  – CoDR (now).
  – PDR (before proto. construction ~mid 2004).
  – CDR (before production ~mid-late 2005).

• Hold informal 1 day internal reviews:
  – internal quality control: consistency of methodology and design.
  – when major milestone on a module’s development is reached.
  – senior engineers and project manager to recommend changes.
### Schedule

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<th>Date</th>
<th>Milestone</th>
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<td>Q1, 2002</td>
<td>New personnel in place. Design tools in place. Training and design work begins.</td>
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<td>Q1, 2004</td>
<td>Critical User Manuals in place. Device driver code can be written.</td>
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<td>Q1, 2005</td>
<td>Prototype test at the VLA starts.</td>
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<td>Q2, 2005</td>
<td>Prototype test at the VLA complete.</td>
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<td>Q2, 2006</td>
<td>Production model test and burn-in, system integration and test in Penticton, and rack and cable installation begins at the VLA.</td>
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<td>Q4, 2006</td>
<td>Begin full installation at the VLA. Earliest possible start of installed correlator testing.</td>
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<td>Q2, 2007</td>
<td><strong>Earliest possible “beta” science data.</strong> (Middle of full installation schedule.)</td>
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<td>Q1, 2008</td>
<td>Correlator commissioning. Correlator fully on-line for observing. Continuing debug support available.</td>
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<tr>
<td>Q1, 2009</td>
<td>End of project. End of NRC debug support. Full handover to NRAO complete.</td>
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<td>Debug support-VLA fully on-line</td>
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B. Carlson, 2001-Nov-02

EVLA Correlator Conceptual Design Review
Budget

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Budget

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De-scoping Options

- Multiple FPGAs with same footprint…use affordable FPGAs at production time.
- Design FIR FPGAs with capability of 2-bit data + 2 filters in one chip. De-scope at production to save ~$300k.
- Cheaper baseline rack cabling. If 1/2 cost, could save ~$370k. (not really de-scoping…). Will seriously investigate.
- One LTA Controller/4 correlator chips: save ~$150k.
- Build/install only 1/2 Station Boards for 8 GHz: save ~$900k.
- 1/2 size correlator chip in 0.25 μm: save ~$400k.
- No recirculation, 1 LTA Controller/4 corr. Chips: save ~$650k.
- Poly-phase FIR/FFT filter bank: save ~$700k.
- Permanent 8 GHz design: save ~$2 million.
Summary

- High performance design tools.
- Sufficient personnel for schedule? (4 HE, 1 SE, 2 sup, …).
- Corr. Chip: fab plan ok, need to investigate design plan more.
- Prototype construction: BGA inspection impossible without X-ray machine $$$.
- Production: out-source, quality control, accelerated-life tests.
- System integration and testing: Proto., Penticton, VLA.
- Budget: CONFIDENTIAL
- De-scoping options to save money…