MOSFET Capacitances

Figure 10 is a graphical representation of the capacitances in a switching MOSFET. An understanding of these capacitances is important for properly driving a class D/E/F PA. Figure 11 shows the nominal values of these parameters for the IRF510.

Input Capacitance, \( C_{iss} \), is the gate-source capacitance, \( C_{gs} \), plus the reverse transfer capacitance, \( C_{rss} \). For the IRF510, \( C_{iss} \) is \( \sim120\,\text{pF} \) when the device is OFF, increasing to \( \sim180\,\text{pF} \) when the device is ON, due to the influence of \( C_{rss} \) and the drop in drain voltage.

Applying a square wave to the gate, \( C_{iss} \) must charge before the voltage appears across the gate-source junction. This is illustrated in Figure 12, where (A) is the input square wave, and (B) is the true gate voltage, that is, the voltage impressed across the internal gate capacitance. The resulting drain current would appear virtually the same as waveform (B).

Once \( C_{iss} \) charges to \( V_{gs(th)} \), about 4V for the IRF510, drain current begins to flow and a portion of the output capacitance, \( C_{oss} \), is reflected back to the gate in the form of the reverse capacitance parameter, \( C_{rss} \). This (and other factors) causes a sudden increase in the gate capacitance at \( V_{gs(th)} \). This is illustrated in Figure 13, with \( V_{gs(th)} \) at 4.0V. The graph is derived from the data sheets, application notes, and measurements I have made on the IRF510.

This rather complex input capacitance graph is not shown in Figure 11, as most data sheets show only the average capacitance over the gate or drain voltage range, not the aberration that occurs when drain current first begins to flow. This is important to realize, as it alters the actual gate voltage waveform. One will observe on an oscilloscope when driving with a square wave.

When the gate drive goes from HI to LO, gate voltage returns to the 3V bias level rather sluggishly, due to \( C_{iss} \) discharging. Note that at \( V_{gs(th)} \), the falling waveform again changes its slope – due to \( C_{iss} \) being altered by the gate junction storage charge effect when gate voltage falls below \( V_{gs(th)} \).

Gate Driver Considerations

Of importance in class D/E/F is the time to reach \( V_{gs(th)} \), the gate threshold voltage, after application of the gate drive going HI. This is described by:

\[
I_g = \frac{C_{iss} \times V_{gs(th)}}{t}
\]

Solving for gate current, \( I_g \):

\[
I_g = \frac{C_{iss} \times V_{gs(th)}}{t}
\]

The above equation indicates that the higher the gate current, provided by the driver stage, the faster \( C_{iss} \) will charge, and the higher the efficiency of the PA.

For class D/E/F, the point of the square wave drive is to get through the linear region as soon as possible. This
means Ciss should be charged as quickly as possible.

I recommend striving for 15–20nS. See Figure 15. This is also consistent with the ~16ns rise time, tr, of the IRF510. "Tr" is theoretically the fastest Ciss can be charged.

The figure shows the input gate drive (A) being a 25% duty cycle, or 90° of the RF cycle. At 10.1 MHz, the gate drive "pulse" would be about 25ns, and to charge Ciss two times faster would indicate 12ns, as shown in (B). From the previous equation, this would indicate a gate current of 50mA is required. This is a bit high for QRP!

I have found a driving current of 25-30mA to be a nice compromise to charge Ciss sufficiently fast for high efficiency. Referring to Fig. 15 (B), if the gate waveform does not flatten out at the 8v level (looks more like a sine wave), the driver is not providing sufficient current to the gate. Driving the gate voltage to saturation quickly, by providing sufficient gate drive current, is paramount in achieving the high efficiency of class D/E/F. The 25mA of drive current will save 200mA or more of PA current at 5W QRP. Observing the oscilloscope drive waveform in Fig. 14, note that Ciss charges in 18-20ns at 10.1 MHz. This 30M transmitter has an overall efficiency of 82%, which includes the 40mA of key-down current due to the TX mixer, comparator and emitter follower driver providing the gate current. This same 18-20ns Ciss charge time will cause a lower efficiency on 20M, as it's approaching the period of the RF. At 40/80M, this 18-20ns rise time will produce higher efficiencies, since it is a smaller percentage of the RF cycle at lower frequencies.

Also note that the input gate square wave in Fig. 14 is about a 30% duty cycle ~ 30% ON and 70% OFF. The output power from the class D/E/F PA is determined by the duty cycle. With the IRF510, a 15% duty cycle produces about 1W output; about 5W at 30%, and 8W at 45%. Efficiency begins to drop above 45% duty cycle.

25mA Emitter Follower Driver

The square wave drive can be developed by some type of CMOS or TTL gate. These alone do not have the current sinking capabilities needed to properly drive the IRF510. Some type of current booster, plus the ability to shift the dc level of the input square wave is required. The emitter follower circuit in Figure 16 is one approach. This works best if you provide a 6V square wave to Q1, such as from a 6–8v CMOS gate, rather than 5V TTL. This is due to the 0.7v drop in the emitter follower, leaving only about 4V from a TTL drive. This may not drive the IRF510 into saturation.

The input square wave is dc shifted by C1 (dc blocking) and the RV1–R1 bias network. Adjust RV1, by monitoring the gate on an oscilloscope, as follows: when the input square wave is LO, the voltage on Q2 gate should be about 3v; when the input goes to +6v HI, the gate voltage should be between 8–9v, depending upon the loading to the circuit. This 3–8v output is developed across R2 and R4. The 3v level is to ensure the IRF510 is OFF, >Vgs(th), and 8v for saturated ON.

Q1 is powered from the +12v TX term to shut down the driver in receive, in the event RV1 is misadjusted to cause mosfet drain current to flow when the mosfet should be OFF.

R3 is 3.9–10W to de-Q the gate and prevent VHF oscillations. The value is not critical. R4 is a resistive load to both the Q1 emitter follower and Q2 gate. The value should be about the Xc of the mosfet Ciss, ~120–180pF, or a few hundred ohms, depending upon the transmit frequency. Initially, you can make R4 a trim pot and adjust for the best possible square wave (Fig. 14) to match to the Ciss of the IRF510. This value will vary from device-to-device. If the rise time is slower than 25-30nS, then more gate current is needed by decreasing the value of R2. In this example, if a 3v-to-8v signal is formed across R2, then the output drive current would be about 33mA on the drive peaks. (I=5V/150W). Ohms law is thus used to determine R2 for the drive current desired.

In the technical literature, the following equation is used to calculate the driver resistance, Rd, needed (R2 in Fig. 16):  
\[ Rd = \frac{-t}{Ciss Ln(1-V2/V1)} \]

Where, t is the desired rise time of the gate signal (usually 15–20ns), V1 is Vg at saturation, V2 is the peak-to-peak gate voltage, or V1 minus Vgs(on), and Ln is the natural logarithm. For the driver in Fig. 16:

\[ Rd = \frac{-20ns}{120pF} = 160W \]

Keep in mind, this value of Rd is based on the ideal current to charge Ciss, about 50mA. Again, I have found 25-30mA to be sufficient. This exercise does show that using Ohms Law for R2 is close enough (and a lot easier!).

The NA5N Mosfet Driver

Another driver scheme developed for my class D/E transmitters is shown in Figure 17. It is similar in some regards to the emitter follower driver in Fig. 16.

The low-level RF output from the TX mixer is applied to a high speed comparator, which converts the RF sinewave into a square wave. The operation of the TX mixer and comparator is beyond the scope of this part of the article, but will be presented in a class D & E transmitter construction project in Part 3. Suffice it to say that the duty cycle of the square wave is variable from about 15–45%. The
Comparator is powered from +12v TX, so that during receive, the output is 0v, disabling the IRF510 drive circuitry.

On transmit, the comparator output is an 8Vpp square wave at the RF frequency, such that the dc output levels are about +1v LO to +9v HI.

This emitter follower is an NPN-PNP pair, commonly called a "totem pole" configuration. Since the base voltage is an 8v square wave, the transistors are driven nearly into saturation and cutoff, acting as switches. When the comparator output goes from LO to +9v HI, both the NPN and PNP are turned on. Q1 emitter voltage is the +9v base voltage, minus the 0.7v junction drop. This 8.3 volts is applied to the emitter of the IRF510, rather than supplied to the IRF510, rather than the gate.

Even though there is only 2.5v drive to the IRF510 gate, the +8v previously on the Q1-Q2 emitters is now discharging. This decaying gate voltage also appears on the Q1-Q2 emitters. The low Q2 emitter-collector resistance, which is in parallel to R2, gives Ciss a lower resistance to discharge into. When Ciss is discharged, Q2 turns off. Thus, the purpose of Q2 is to place a low-Z load across the IRF510 gate to quickly discharge Ciss when the mosfet turns off.

For class D/E/F efficiency, the drain current must be zero before the next square wave LO to HI transition occurs.

**Figure 18** is an oscilloscope display of this circuit driving a class E transmitter. The top trace is the gate voltage at 5v/div. Vgs(th) of this particular device is 3.8v, shown by the dotted line marker on the oscilloscope. Gate voltage rises fairly quickly to saturate at 8v. When the drive signal switches from HI to LO, the action of Q2 discharges Ciss and drops the gate voltage below Vgs(th) faster than the emitter follower version in Fig. 16. In this case, R1=3.9W and R2=220W.

Gate voltage settles out around 2.5v, due to the LED and Q2, keeping the IRF510 turned off. If the gate were allowed to discharge to 0v, it would take longer to charge Ciss when the next gate drive goes HI. This saves 2.5v of Ciss charging. The main purpose of the LED is to provide this gate bias when the mosfet is off. Of course it does make for a nice XMIT indicator as well, indicating RF is being supplied to the IRF510, rather than simply coming off the key line.

The bottom trace is the drain voltage (Vd) at 5v/div. The peak-to-peak voltage is about 25v, the 2Vcc (or 2Vdd) expected. Note that when the gate voltage reaches +3.8v Vgs(th) going HI, the drain voltage is just passing through 12v Vcc – the point when drain current is zero. This is exactly the point you want the gate voltage to reach Vgs(th) to start drain current to flow. Vd drops from 12v down to 0v, indicating drain current is increasing. When the gate voltage reaches 8v drain current should be saturated, evidenced by Vd reaching ~0v. In this case, Vd=0.4v, certainly indicating the IRF510 is in saturation, or the "full-ohmic on" region. This is important, as the closer to 0v at maximum drain current, the smaller the power losses across the drain–source junction. The lower the loss, the higher the efficiency. The drain current is also building up the current field in inductor L1 at this time. If drain voltage does not reach <1v, the mosfet is not in saturation.

When the gate voltage begins it’s HI to LO transition, to turn OFF the mosfet,

**Calculating PA Efficiency**

PA efficiency of class D/E/F can be easily measured on an oscilloscope by measuring the LO to HI gate drive transition to the point the drain current first saturates (when drain voltage hits the lowest value). This accepted method is basically a measure of how long you spend in the linear region. The time to reach saturation is compared to the time of the RF cycle to determine the phase delay, in degrees. The steps to calculate PA efficiency, based on the NA5N driver and PA waveform in Fig. 18, are shown below. Calculating efficiency based on measuring PA currents (input vs. output power) yielded 91%.

![Fig. 18 – Gate/Drain Waveform](image-url)
drain voltage begins to rise, indicating drain current is turning off as desired. Gate voltage drops from +8V to +3.8V Vgs(th) faster than the single emitter follower waveform in Fig. 16, due to the loading effect of Q2. Drain voltage rises above 12v Vdd as the current stored in L1 now jumps into the output network when drain current stops.

In class E, L1 is also part of the output tuned circuit, resonant at the transmit frequency by the shunt capacitor in conjunction with the internal Coss. See "Cv" in Fig. 6, Part 1. When the current stored in L1 is depleted, drain voltage will begin to decrease. However, in class E, the energy stored in the capacitor parallel to L1 will provide voltage when the current in L1 is depleted, causing the familiar "fly-wheel" effect of the resonant circuit. In Fig. 18, the hesitation in drain voltage at 20v is when L1 runs out of current, and the voltage peak to 25v is the voltage being supplied by the shunt capacitor, which has been charged to 2Vdd. Two or three peaks may be seen at the 25v level, depending upon the harmonic power present. With this waveform, the transmitter had a power range of 1W to 9W (by varying the duty cycle from 15% to 45%) with an overall efficiency of 85% and a PA efficiency of 92%.

Class D Drain Output Efficiency

The output capacitance, Coss, lowers efficiency, since it must be charged to 2Vdd, if the current in L1 is depleted. Drain voltage will begin to decrease. However, in class E, the energy stored in the capacitor parallel to L1 will provide voltage when the current in L1 is depleted, causing the familiar "fly-wheel" effect of the resonant circuit. In Fig. 18, the hesitation in drain voltage at 20v is when L1 runs out of current, and the voltage peak to 25v is the voltage being supplied by the shunt capacitor, which has been charged to 2Vdd. Two or three peaks may be seen at the 25v level, depending upon the harmonic power present. With this waveform, the transmitter had a power range of 1W to 9W (by varying the duty cycle from 15% to 45%) with an overall efficiency of 85% and a PA efficiency of 92%.

Class D Drain Output Efficiency

The output capacitance, Coss, lowers efficiency, since it must be charged to 2Vdd by the mosfet. The equations below show how efficiency, η, is based on the switching power, Ps, lost across Coss. The following math only serves to raise the mosfet drain voltage for higher efficiency. Let's see if this is true.

\[ \eta = \frac{P_o}{P_o + P_s} = \frac{5W}{5W + 1.78W} = 74\% \]

\[ P_s \text{ is the switching loss in watts):} \]
In some of the amateur literature, the recommendation is sometimes given to raise the mosfet drain voltage for higher efficiency. Let's see if this is true.

\[ V_{eff} = 18v - 0.5v = 17.5v \]
\[ Ps = 120pF(2*17.5) \times 2(14MHz) = 4.1W \]
\[ \eta = \frac{5W}{5W + 4.1W} = 55\% \]

At Vdd=18v, to produce 5W output power:

Increasing Vdd to 18v does produce 5W with less drain current. However, charging Coss to 36v (2Vdd) greatly increases the switching power loss, lowering efficiency from 74 to 55%. This should dispell the rumor that increased voltage lowers efficiency – and that the +12v customarily used by homebrewers is actually quite ideal for switching mosfet QRP PAs.

The second point with the above equations is how the switching losses are frequency dependent, due to the term "2fo." The lower the frequency, the lower the losses, and hence higher efficiency. Therefore, a Class D/E/F PA will be much more efficient on 80M than 20M. This is why most Class E circuits on the internet are only for 160M or 20M. This is why most Class E circuits on the internet are only for 160M or 20M, as even a sloppy job of designing the circuit and using a sinewave drive

\[ V_{eff} = 12v - 0.5v = 11.5v \]
\[ Ps = 120pF(2*11.5) \times 2(1.8MHz) = .23W \]
\[ \eta = \frac{5W}{5W + .23W} = 96\% !!! \]

will still yield high efficiency. Recalculating the 20M 12v QRP example to 160M yields an astounding 96%. This is also why those scaling these amplifiers for 20M have had disappointing results, as the switching power losses double as you double the operating frequency.

A few loose ends ...

IRF510 vs. IRL520

The IRL520 is a logic family mosfet, meaning it is designed to saturate with only 5V (TTL logic HI) on the gate. It would therefore seem the IRL520 would be ideal for a class D/E/F PA for QRP, since it can be turned on with only a 2v swing on the gate. However, the input capacitance, Ciss, for the logic drive devices is very high – in the order of 300-400pF. This is tolerable for their intended purposes in 50-100 KHz switching power supplies, but virtually impossible to drive at HF frequencies. I have built some fairly successful Class C PAs with IRL520's, but efficiencies at Class D/E/F never much more than 50%. Theoretically, one can drive the gate with a parallel inductance to cancel out this huge capacitance through resonance, but I have not tried this. There are some SMC SOT-23 logic mosfets with a lower Ciss worth experimenting with.

Other switching MOSFETs

Just look through the Mouser or Digi-Key catalog and you will see listings for legions of cheap, switching mosfets. Many can be used in lieu of the IRF510. In order to use them for Class D/E/F, you need to know primarily the Vgs(th), Vgs(sat), and output capacitance, Coss or Cds. Maximum drain current is important, as this is about the maximum allowed Id for smooth power stress why controlling output power is important. For QRP power levels, you want a device with a Id(max) of 1-2A for smooth power control with a 50% duty cycle, since you are forcing maximum Id for some period of time. The IRF510 Id(max) is about 4A. Such a high Id(max) actually makes the IRF510 a bit difficult to control in the 5W or less range.

Surface Mount MOSFETs

Some of the switching mosfets that meet the above requirements are only available in surface mount packages, such as SOT-23's with Id(max) around 1.5–2A. I have built a class D and E PA with these devices with good success, and surprisingly, the high efficiency causes little heating of these very small packages. However, operating them Class C causes excessive heating above about 2W. There is just very little room for error with a SOT-23 due to the low power dissipation of such small physical packages.

Other available literature

There is plenty of available information on Class D/E/F transmitters on various websites, engineering magazine articles and the application notes in National and Motorola data books. However, this information needs to be used with caution for QRP, as most are based on RF type switching mosfets, deal with power ranges in the hundres of watts, push-pull circuits, or frequencies below HF, such as for AM broadcasting or ultrasonic use. Still, these articles are worth further study for those wishing to learn more, keeping the application of the article in mind.

Interpreting the IRF510 Data Sheet

The data sheet for the International-Rectifier IRF510 is in Appendix B. This is extracted from their complete data sheet.

Maximum Ratings. Continuous drain current is important, as this is about the drain current for the period of time the IRF510 is in saturation. This should stress why controlling output power with a small duty cycle is important. Maximum gate-to-source voltage is 10v, which will easily handle the +10v required for saturation.

Electrical Characteristics. RDS(on) is the "on-resistance," which only occurs when fully saturated. Note the Test Conditions define the saturated
state with $V_{GS}=10v$. When in the linear region, $R_{DS}$ is the standard equation for $RL = \frac{V_{dd}}{2P_o}$.

$V_{gs(th)}$ is the gate voltage where drain current begins to flow. Note the huge range - typical of mosfets. Most devices will be about 3.5-4v. 

$L_D$ is the internal inductance that adds to the external inductance on the drain. In class E, where the drain inductance forms a tuned circuit, the value of $L_D$ is sufficiently low to not alter calculations. $C_{iss}$ and $C_{oss}$ are the input and output capacitances. These are very important, especially for class D/E/F. Note the test conditions are for $Vgs=0v$, that is, with no drain current flowing. With drain current, $Vds$ will drop from +12v to 0v (at saturation) and these values change, as shown in Fig. 3 on the data sheet. Timing parameters, $T_{d(on)}$, $T_r$ and $T_{d(off)}$ are defined in Fig. 6. For class D/E/F, the faster the better. Theoretically, the fastest a mosfet can switch is the time of $T_r+T_f+T_{d(on)}+T_{d(off)}$, which equals 54nS for the IRF510. Tf is assumed to be about $Tr$ if not listed. The maximum frequency would thus be $1/54nS = 18.5MHz$. $T_r$ and $T_f$ define the typical time to charge and discharge $C_{iss}$ and $C_{oss}$. These times can be increased a bit by increasing the gate drive current, as discussed in the article, and raising $f_{max}$ to some extent.

Fig. 1 shows drain current ($I_d$) vs the drain-source voltage ($V_{ds}$) at 25ºC. This is similar to the transfer characteristic curves for a BJT. Fig. 2 is the same, except at a device temperature of 175ºC. Note that as the IRF510 gets hotter, drain current gets less, protecting itself from thermal runaway. This is opposite the effect of a BJT, where the BJT gets hotter, more collector current flows, producing more heat, then more current, until the device destroys itself by thermal runaway. Again, a mosfet protects itself from thermal runaway. This explains why your class C IRF510 PA drops in output power as the device gets hot.

Fig. 4 is the transfer characteristics of the IRF510. This shows how much drain current flows vs. the gate voltage. Note that the graph begins at 4v, as less than that, the mosfet is in "cut off." Also note the drain current is less at 175ºC. This shows how device saturation occurs around $Vgs=8v$, where little further increase in drain current occurs with increasing $Vgs$. Below $Vgs=8v$ is the linear region, although it is not very linear (more "curved" in shape). The transfer curve is steepest between about 4 to 5v $Vgs$. This is the area of maximum gain. This shows why IRF510s have also been used as very high gain RF amplifiers or mixers, by exploiting a gate voltage only slightly above $Vgs(th)$.

Fig. 5 shows the maximum drain current vs. temperature. For class C QRP transmitters, device temperature can quickly rise to 150ºC on key down, but still in the safe operating region for 1A of drain current. Class D/E/F runs considerably cooler. In fact, a barely warm IRF510 after 30 seconds of keydown is the ultimate proof of the increased efficiency. Try that with class C and you’ll loose your fingerprint!

In Part 3 of this series will be two construction projects for you to build – a QRP Class D and E transmitter using the IRF510. Both can be added to about any QRP transmitter to produce 5W output, or for a "roll-your-own" transmitter.

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