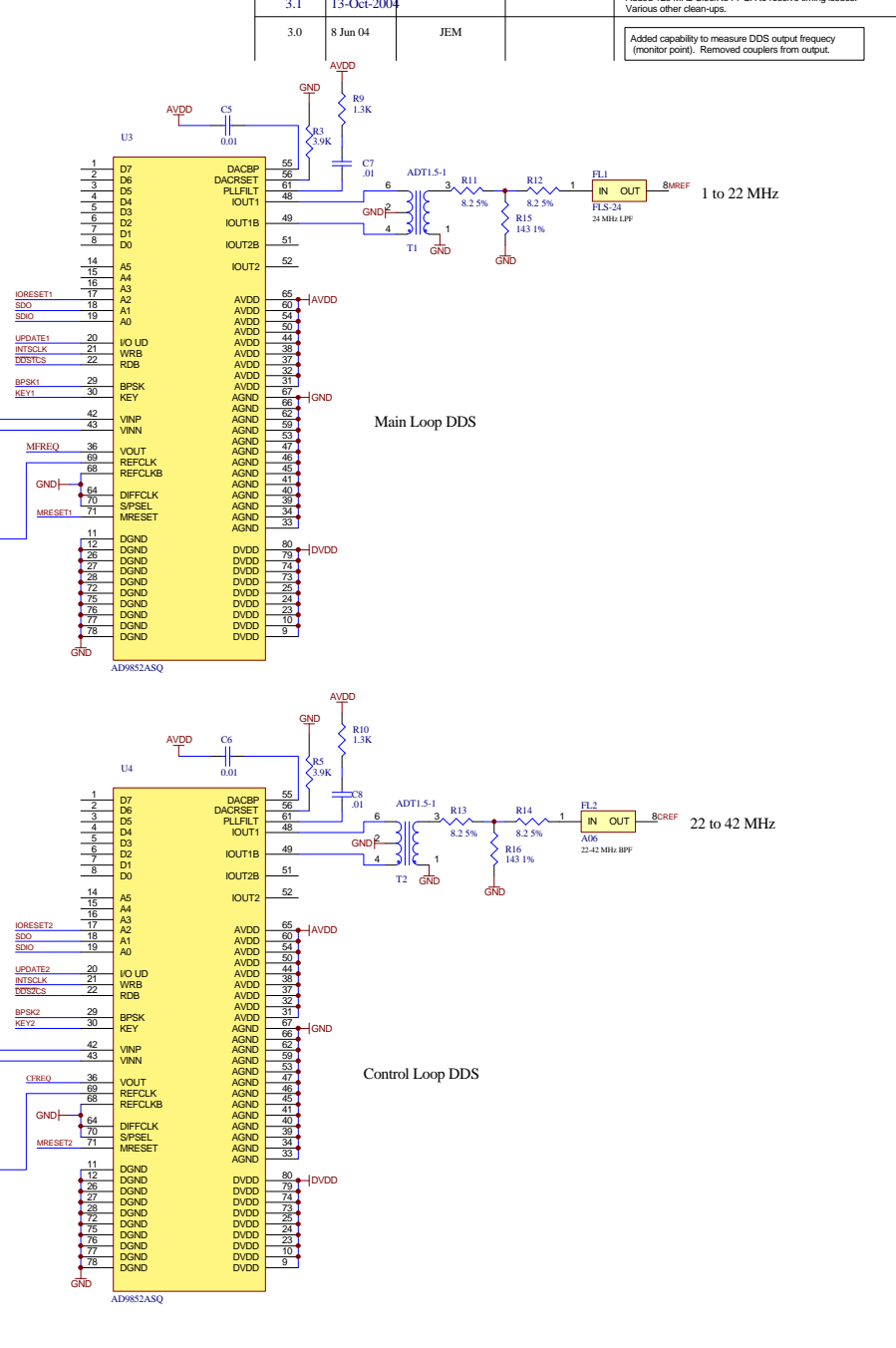
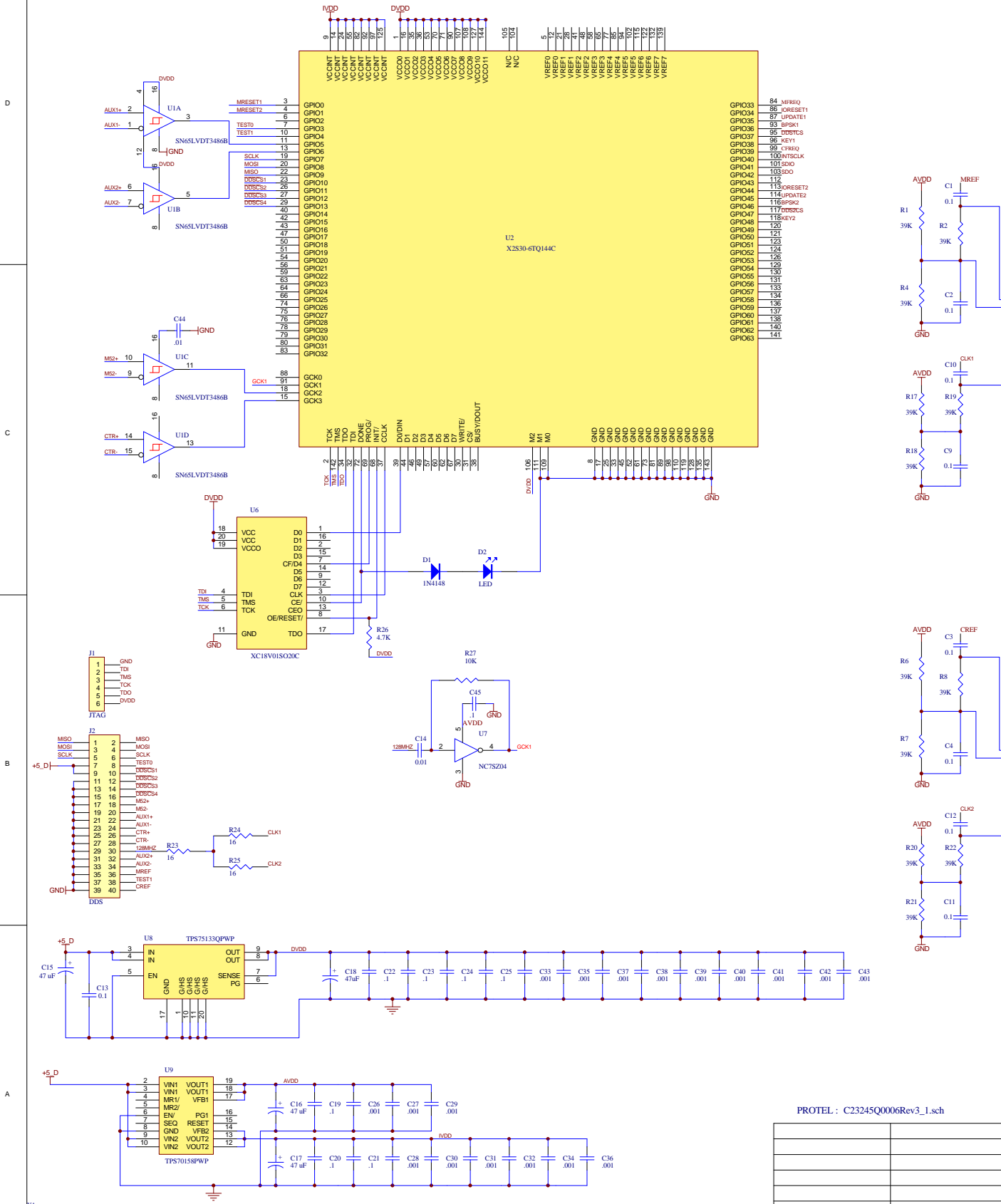


REV	DATE	DRAWN BY	APPRVD BY	DESCRIPTION
3.1	13-Oct-2004			Added 128 MHz Clock to FPGA to resolve timing issues. Various other clean-ups.
3.0	8 Jun 04	JEM		Added capability to measure DDS output frequency (monitor point). Removed couplers from output.



PROTEL : C23245Q0006Rev3_1.sch

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES 5/16"
4 PLACE DECIMALS (XXXX) 5/16"
3 PLACE DECIMALS (XXX) 5/16"
2 PLACE DECIMALS (XX) 5/16"
1 PLACE DECIMALS (X) 5/16"
MATERIAL :
FINISH :
NEXT ASSEMBLY :
DWG. TYPE :

E P R O J E C T	VLA Expansion Project		NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801			
	Antenna Electronics					
	Dual Direct Digital Synthesizer					
	DRAWN BY J. Muehlberg					
T I T L E	DATE Sep 04		DESIGNED BY M. Revnell			
	DATE					
SHEET NUMBER	1	OF	1	DRAWING NUMBER 23230-S0001	REV. 3.1	SCALE