# REQUIREMENTS AND FUNCTIONAL SPECIFICATION

# EVLA Correlator Power Monitor and Control System

RFS Document: **A25026N0000**

Revision: 2.1a

B. Carlson, April 8, 2009

*National Research Council Canada*
*Herzberg Institute of Astrophysics*
*Dominion Radio Astrophysical Observatory*

*P.O. Box 248, 717 White Lake Rd*
*Penticton, B.C., Canada*
*V2A 6J9*

# Table of Contents

# List of Figures

# List of Tables

# List of Abbreviations and Acronyms

**CBE –** Correlator Backend. A collection of COTS computers used for correlator output data processing.

**COTS –** Commercial Off-The-Shelf.

**CPCC –** Correlator Power Control Computer.

**EVLA –** Expanded Very Large Array.

**FMEA –** Failure Modes and Effects Analysis.

**MCCC –** Master Correlator Control Computer.

**MTBF –** Mean Time Between Failures. Usually expressed in hours.

**M&C –** Monitor and Control.

**NI –** National Instruments.

**PCB –** Printed Circuit Board.

**PMCS –** Power Monitor and Control System. This refers to all of the processing and embedded elements required for the functionality described by this document.

**PXI –** PCI eXtensions for Instrumentation. Rugged CompactPCI chassis with features for reliable instrumentation control.

**RPMIB –** Rack Power Monitor Interface Board. Unlike the "MIB" and the "CMIB", this board is a simple connection board with simple electronics and built-in redundancy to allow the NI 6509 card to monitor and control correlator rack components and Solid State Relays.

**SCSI –** Small Computer System Interface. Refers to a type of connector used by the NI 6509 card and RPMIB.

**SSR –** Solid State Relay. This is a relay that contains an opto-coupler and a high-current transistor element to control AC or DC voltage to a device.

**UPS –** Un-interruptable Power Supply.

# 1 Revision History

| Revision | Date | Changes/Notes | Author |
|---|---|---|---|
| DRAFT | May 5, 2006 | Initial DRAFT release for review. | B. Carlson |
| 1.0 | July 21, 2006 | First release after July 11 review. Simplify the Control Rack contents. Merge the CPCC and MCCC functions into one computer. Add protection features on the RPMIB. Present inexpensive rack-mount PCI chassis as cheaper alternative to PXI chassis. | B. Carlson |
| 2.0 | Oct. 19, 2007 | Changes to reflect new connectivity scheme, and add in-system programming of the X-bar Board FPGA serial configuration PROM. Power to CBE computers no longer controlled with RPMIB and AC SSRs, instead, rely on built-in capability of CBE computers to do this via Ethernet. | B. Carlson |
| 2.1 | Apr. 6, 2009 | Add interface requirements for HVAC, monitor and control, and smoke alarm monitor. Refer to section 4.1, bullets 4 and 12, and section 4.4, for interface and level requirements. | B. Carlson |
| 2.1a | Apr. 8, 2009 | Correct section 4.4 so that HVAC blowers ON is an OPEN contact, and OFF is a CLOSED contact. | B. Carlson |
| | | | |
| | | | |
| | | | |
| | | | |

## 2 Introduction

This document describes the requirements and functionality of the Power Monitor Control System (PMCS) for the EVLA Correlator.

The PMCS is responsible for monitor and control of all power supplies and systems in the correlator. It provides reliable, autonomous, and intelligent power monitor and control and has the ability to allow remote power cycling of all correlator boards and processors. The PMCS automatically handles system power up and system power down with minimal human interaction. Feedback and control allow for automatic load balancing of cooling systems in the correlator. An on/off control line to the correlator room HVAC systems allows the PMCS to optimally stage system power down and power up, most often due to mains power failure events.

In this document, requirements are defined and then a solid plan is presented to meet the requirements. This document is sufficiently detailed to allow implementation of required components of the PMCS to proceed at any time.

# 3 Overview

A simplified block diagram of the EVLA Correlator power system is shown in Figure 3-1. The system requires 110 VAC and –48 VDC. The CPCCs (Correlator Power Control Computers) are used to monitor and control power to each element as indicated in the figure. MCCC (Master Correlator Control Computer) functions are contained in the same computers as the CPCCs. Solid bold lines are direct power monitor and control lines, and dashed lines are network connections to elements' CPUs. Two CPCCs/MCCCs are included in the diagram for hot-standby redundancy.

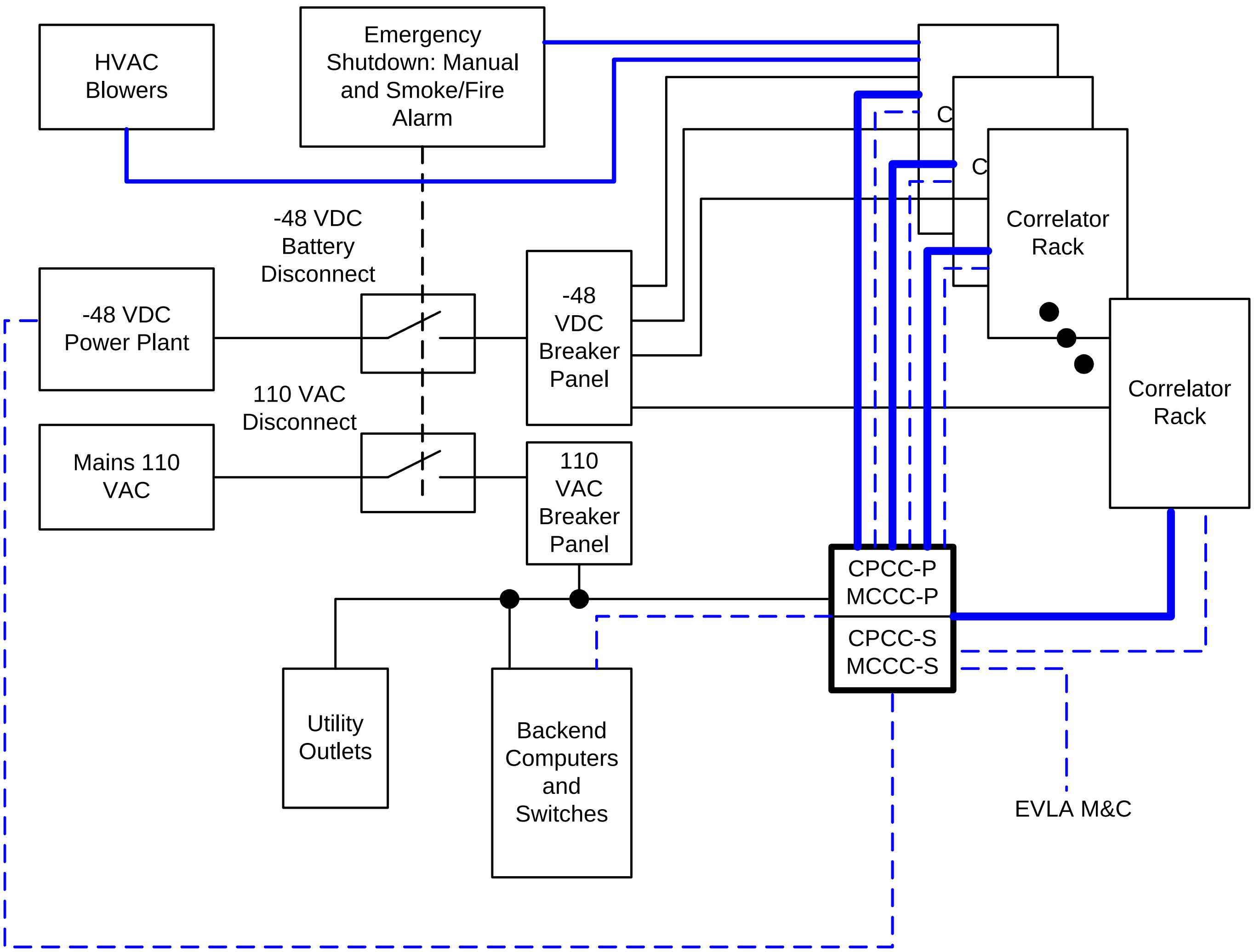


**Figure 3-1 Simplified EVLA Correlator power system block diagram.**

The correlator racks, and all components within them, are fed exclusively with –48 VDC power. The Backend computers, network switches (other than those in the correlator racks) and CPCCs/MCCCs are powered from system battery-backed 110 VAC.

There is no direct computer control of –48 VDC to the system, although the –48 VDC Power Plant has remote monitoring capability via the network. –48 VDC power can be cut to the system only via a manual emergency shutdown or automatically with the smoke or fire alarm.

The power monitor and control system (PMCS) consists of the CPCCs, software running on the CPCCs, and all embedded hardware and cables required for performing intended functions. Since the CPCCs perform a “mission-critical” function, they need to be robust and simple, redundant, and with safe and predictable failure modes.

There is no direct power control of Backend computers in Figure 3-1; it is assumed that power control of Backend computers will be performed over the network, as these sorts of computer systems are now including such features.

The CPCC computers, via the RPMIB in Station rack S001, control and monitor the HVAC blowers, as well monitor smoke alarm conditions.

# 4 Requirements

This section lists the requirements of the Power Monitor and Control System (PMCS). This system encompasses both hardware and software functions that, acting together, provide fully integrated power monitor and control capability. Single point-of-failures, if at all possible, must not exist, and failure modes must be acceptable and protect the correlator system at all times. The system must be able to recover automatically. If, in some failure mode scenarios, automatic recovery is not possible or is locked-out for system protection (requiring manual intervention), the steps required by personnel to return the system to normal functioning must be as simple as absolutely possible.

## 4.1 Functional Requirements

1. Centralized and reliable monitoring of the health of all active elements in the correlator system. An element is defined as a COTS computer, custom correlator hardware printed circuit board (PCB), a network switch, or any other intelligent equipment the correlator relies on for normal operation. Health monitoring may be direct (e.g. voltage and temperature measurements), or indirect (i.e. the equipment responds to network queries), as appropriate and required for a particular element.

2. Centralized and reliable control of power to all active elements that may need to be remotely shutdown if failure has occurred, or remotely power cycled to attempt recovery.

3. Centralized and reliable correlator rack cooling fan speed monitor and control. Fans must be controllable in 32 approximately equal steps from OFF to FULL SPEED. The primary monitor requirement is to determine if a fan is rotating so that it can be replaced if it fails. It is a desired secondary requirement to determine rotation speed of each fan approximately once per minute.

4. Ability to turn ON or OFF the correlator room HVAC (air conditioning) blowers via 4 TTL control lines. This control function allows the PMCS to properly sequence power cycles and cooling to maintain heat capacity and minimize the chance of a thermal cycle in the correlator. HVAC blower status is monitored via 4 monitor pairs. Refer to section 4.4 for interface requirements.

5. Primary monitoring of the temperature and voltage of custom correlator hardware PCBs that contain embedded processors with a network connection. Secondary monitoring of the health of custom correlator hardware PCBs' power supplies via a separate and direct power supply monitor signal.

6. Distributed electronics forming part of the PMCS that cannot be hot-swap replaced must be very simple, contain no more than the minimum of elementary electronics to perform intended functions, and contain built-in redundancy. It must be possible to automatically test for failed PMCS hardware during

maintenance days, and allow for subsequent in-situ replacement of failed hardware.

7. Centralized electronics that cannot be hot-swap replaced should have the ability to be configured for redundant hot-standby or concurrent operation. It must be possible to power down and repair one of the redundant elements of the system with no negative impact on the operation of the system.

8. Standard COTS hardware, packaged suitably for an office environment, should be used as much as is reasonably possible. If possible, standard form factors and products with industry support should be used.

9. It is necessary to monitor the health of the –48 VDC power plant and restart, reset, or shutdown power plant modules that are indicating problems (as allowed for via the power plant's network interface). However, there is no requirement to allow the centralized power control processors (CPCCs) to remotely shutdown the –48 VDC system power supply.

10. Manual emergency shutdown for the entire correlator system and room as a whole, best accomplished with a wall-mount red "mushroom" panic switch in a conspicuous location (or multiple locations). This switch, if engaged, immediately kills –48 VDC power to the correlator and all 110 VAC power. Manual restart requires only releasing the engaged switch, at which point the CPCCs will start up the system automatically.

11. Automatic smoke detector and fire alarm shutdown of all correlator room equipment. When a smoke or fire alarm is tripped, it engages a switch to immediately kill power, and this switch can only be released manually. Manual restart required for recovery, at which time the CPCCs will start up the system automatically.

12. The CPCC monitors 3 smoke alarm conditions (ultra-sensitive, $1^{st}$ low sensitivity, $2^{nd}$ low sensitivity). 60 seconds after the $2^{nd}$ low sensitivity alarm goes off (provided the other 2 alarms have been triggered), power is cut, and so the CPCC begins the correlator shutdown sequence immediately after the $2^{nd}$ low sensitivity alarm. Refer to section 4.4 for interface requirements.

13. Any processors (CPCCs) used for power monitor and control must use the Linux operating system, and allow application software access to interface card device drivers or provide sufficient information to allow custom device drivers to be written.

14. Power monitor and control functions are relatively simple and require relatively minimal real-time performance. Monitor and control software should thus be relatively simple. However, reliability, predictability, and solid error-free functionality are of primary concern in the design, implementation, and test of CPCC software.

15. The CPCCs must respond to requests from the external EVLA monitor and control system to power ON or OFF the system, power cycle one or more selected elements, power OFF one or more selected elements, power ON one or more selected elements, report warning and error conditions, report temperatures and voltages etc.

16. The CPCCs must autonomously take appropriate action to deal with modules that are overheating, that have failed voltages or voltages out of range, or that are not responding. While doing so, the CPCC must report the problem and action taken in an appropriate way to the EVLA monitor and control system, and the correlator's MCCCs.

17. Automatic keep alive reporting to the EVLA monitor and control system from each CPCC processor. Settable report interval.

18. The CPCCs must autonomously be able to equalize cooling and temperature in the correlator racks via the fan speed control, using the correlator PCBs temperature monitoring capability. "Equalized cooling and temperature" requires further definition, but likely means a minimum mean temperature with a peak deviation about the mean of no more than ~5 $^{o}$C. For this test, presumably the hottest temperature in each rack is used in the calculation.

19. In the event of an extended power failure the CPCC must control the shutdown of correlator systems in a systematic way, based on the duration of the power failure. This includes taking steps to put the correlator in a "sleep" mode with the intent of preserving battery power for as long as possible and to preserve the correlator's temperature to avoid a temperature cycle.

20. When mains power becomes available, at least one CPCC must be the first computer to become active. This computer will then autonomously orchestrate the start-up of the correlator system including equipment in all racks, the CBE computers, and the HVAC system. Once the system is fully active again (and fully active means that the embedded processors boot and configure the boards), the CPCC will provide the EVLA monitor and control system with an indication of the status of the system. Note that the CPCC is not responsible for performing any correlator self-tests, it is responsible only to ensure that all active elements are powered-up and responding to network queries.

21. It must be possible, in off-line test mode, to automatically run tests to determine the health of redundant PMCS control, monitor, and switching elements in the system. Typically these tests will be run only when the correlator system is off-line for maintenance.

### 4.2 Performance/Reliability Requirements

1. It should be possible to configure the PMCS in a manner that has a calculated MTBF greater than the 20-year lifetime of the correlator. i.e. PMCS failures have a very low probability of causing correlator down time.

2. The PMCS must report to the EVLA M&C system, and take autonomous action if necessary, within 10 seconds, any condition that could immediately or eventually precipitate partial or complete shutdown of the correlator.

3. There are no hard real-time requirements for this system. The CPCCs can poll monitor inputs for status, and control outputs need only be set to the desired state within a reasonable period of time and need not be hard-synchronized to correlator system timing signals.

### 4.3 Environmental Requirements

1. The PMCS will operate in a cooled, clean office environment with a mean temperature of approximately 20 $^{o}$C. Refer to A25012N0000 for more detailed information on the environment.

2. All central PMCS components are 19" rack-mount, with in-situ service/repair capability.

### 4.4 Interface Requirements

1. 100/1000BaseT Ethernet interface to the EVLA M&C system, 1000BaseT Ethernet interface to correlator rack switches and the master CBE switch/node, and 10BaseT Ethernet connection to the –48 VDC Power Plant CPUs.

2. HVAC blower control uses the SPARE-0, SPARE-1, SPARE-2, and SPARE-3 Control lines of Station rack S001 RPMIB. **For blower control, TTL high is OFF, and LOW/no connect is on.**

3. HVAC blower monitor uses the SPARE-0, SPARE-1, SPARE-2, and SPARE-3 Monitor lines of Station rack **S001** RPMIB. One (either) wire of each pair is grounded at the RPMIB, and one wire routes into the monitor input, pulled high with 2 k pullup resistor to +5V at the RPMIB. Note that there is no +5V terminal accessible at the RPMIB, so use Control output "6U-9" (pin 46, P3.1, Out-25 in Table 5-5), set HIGH, as a pseudo +5V pullup terminal. **Thus, the BLOWER OFF condition is LOW (wire pair CLOSED), and the BLOWER ON CONDITION is HIGH (wire pair OPEN).**

4. The 3 smoke alarm monitors are 3 pairs of lines, which use the SPARE-0 (ultra-sensitive alarm), SPARE-1 (1st low sens), and SPARE-2 (2nd low sens) inputs of Station rack **S002** RPMIB. One (either) wire of each pair is grounded at the RPMIB, and one wire routes into the monitor input, pulled high with 2 k pullup

resistor to +5V at the RPMIB. Note that there is no +5V terminal accessible, so use Control output “6U-9” (pin 46, P3.1, Out-25 in Table 5-5), set HIGH, as a pseudo +5V pullup terminal. **Thus, the non-alarm normal condition is HIGH (wire pair OPEN), and an ALARM CONDITION is LOW (wire pair CLOSED).**

# 5 Functional Specifications

## 5.1 Overview

A simplified block diagram of the PMCS (Power Monitor Control System) for the correlator is shown in Figure 5-1. This figure contains all of the hardware and processing elements required to meet all requirements. This system is shown with redundant capability, but could be configured without it by just deleting one Control Rack.

Figure 5-1 contains the following PMCS elements:

1. **Correlator Boards** in the diagram refer to custom-built correlator hardware and include the Station Board, Baseline Board, and X-bar Board. Each board has one control input and one monitor output. The control input enables the on-board power supply, effectively turning the board on. The monitor output is high if all on-board power supplies are operational and producing voltages within specification. If any power supply is not functioning this output will be low or pulsing low. The Station Board and Baseline Board contain embedded Linux processors with a network connection to each Control Rack Ethernet Switch. Each of these boards contains additional voltage and temperature monitors that can be read via the network.
2. **Correlator Racks** contain circuit boards, fans, a **Rack Power M&C Interface Board** (RPMIB), and a 24-port Ethernet switch (2 switches in the case of the Station Rack, for the FORM mezzanine cards). The fans have an analog speed control input over a 0-10 V range, and a tach output that generates 3 pulses per revolution, both referenced to –48 V. The Ethernet Switch is powered off –48 VDC, and power to the switch is controlled via a DC SSR (Solid State Relay). The **–48 V Breaker Panel** contains a number of 15 A breaker circuits (one for each large board or group of small boards, and one for the fans), as well as a direct, in-line, red mushroom kill switch.
3. The **RPMIB** is a simple custom-built interface board that breaks-out the 96 digital I/O signals on the 100-pin SCSI connector to screw terminals for connection to power monitor and control points within the rack. This board contains two 100-pin SCSI connectors and simple diode-ORing circuitry for redundant operation. In addition, it contains circuitry to drive and receive signals for fan speed control and monitor. The RPMIB is fed with –48 VDC power via one circuit of the –48 VDC Breaker Panel. The RPMIB is mounted inside the back of the rack. Refer to Figure 5-2 for a complete functional schematic of the RPMIB.

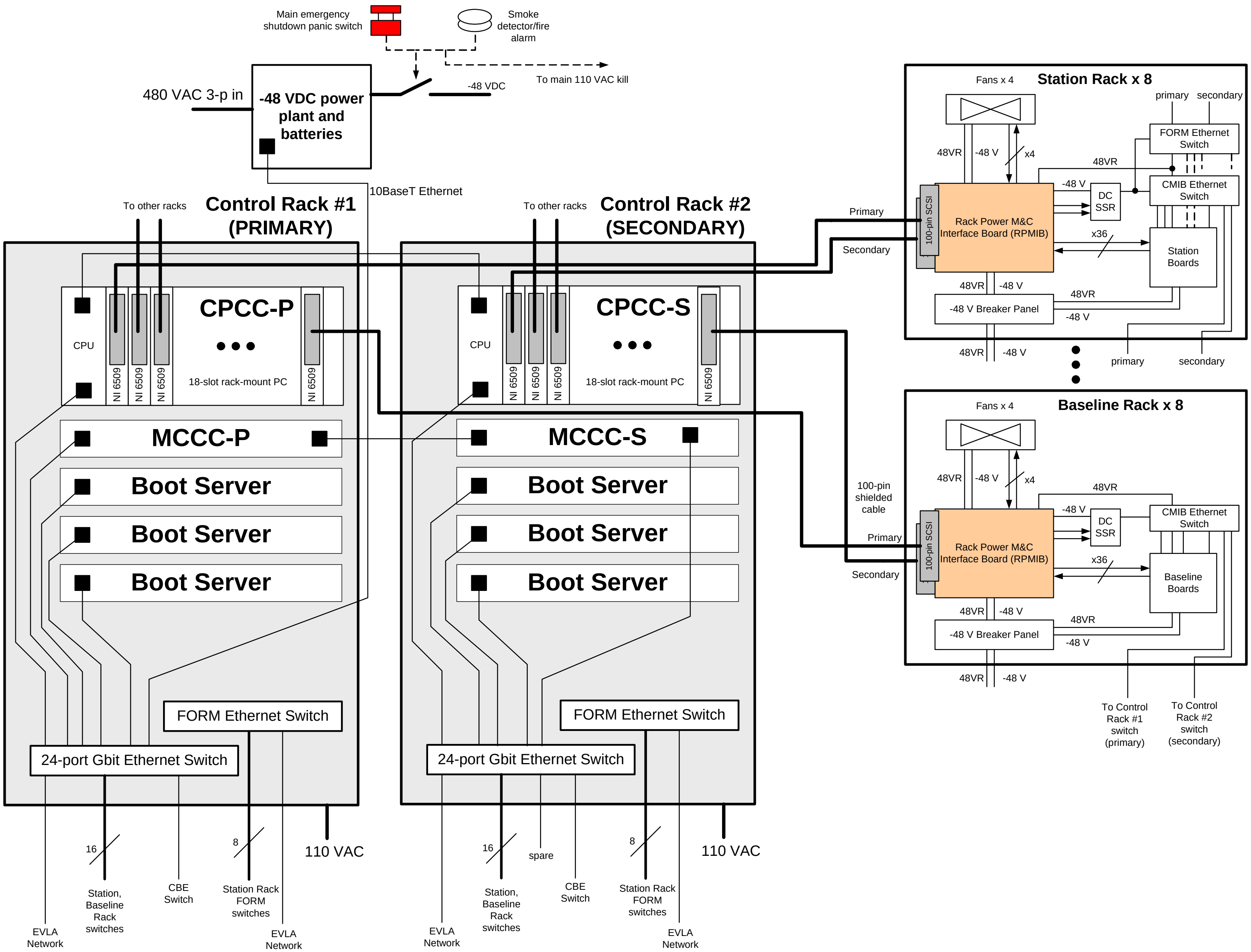


**Figure 5-1 Simplified block diagram of the Power Monitor and Control System**

4. The **Control Racks** each contain the elements shown in the figure, and described in the next few bullets. For full redundant operation, there are two Control Racks in the system. If two Control Racks are used for redundant operation, the software running on the racks' processors must be designed for redundant operation. It is possible, in the redundant configuration, to power-off a Control Rack for servicing without interrupting normal correlator functioning.

5. **CPCC**. There is one CPCC (Correlator Power Control Computer) in each Control Rack (fault-tolerant, identical operation). CPCCs are rack-mount Linux PCs with up to 18 slots for NI6509 cards. For reliability, there is a direct Ethernet connection between the two CPCCs to allow uninterrupted communication; if this link goes down, secondary communication through the CBE switch or any of the rack switches is possible. This computer could be a more rugged CompactPCI or PXI chassis.

   CPCC functions include continuously monitoring, through low frequency polling, the health of every rack in the system, reporting exceptions, and taking autonomous action when necessary. Each board has on-board temperature and voltage sensors accessed via the network, as well as a direct power supply good/bad indication via the RPMIB. Fan tach outputs are monitored to detect fan failures. The CPCC-P can talk to the –48 VDC power plant to determine its status although this is not a system-critical function.

6. **MCCC**. There is one Master Correlator Control Computer in each Control Rack. The MCCC performs real-time correlator system monitor and control functions. MCCCs in each Control Rack are connected together by their own dedicated Ethernet port and cable for reliability. If this link goes down, secondary communication through the CBE switch or any of the rack switches is possible.

7. **Boot Server**. There are 1 or more boot servers in each Control Rack (3 are shown). Boot Servers are used for network boot of embedded CMIB CPUs on all of the correlator's 256 boards.

8. **NI 6509**. This is a COTS National Instruments PCI 96-line programmable digital I/O card. Lines are controllable as inputs or outputs in banks of 8. Outputs drive high (5 V) or low (0 V) and can source or sink 24 mA. Inputs are TTL compatible with 0.8 V and 2 V thresholds. This card contains a 100-pin SCSI connector for connection via cable to an RPMIB. This connector also includes a +5 V output @ 1 A, self-fused.

9. **Ethernet Switches.** Each Control Rack contains an Ethernet switch for connection to rack CMIBs, the CBE, and the EVLA network, as well as an Ethernet switch for FORM PC/104 CPUs (to form a completely separate network for the FORM CPUs). A 24-port switch allows all connections but with no spare capacity, and so a 48-port switch may be required.

10. **DC SSR**. This is a DC Solid State Relay that allows for remote control of the –48 VDC voltage to the rack Ethernet switch. It is controlled from the CPCCs via the RPMIB.

11. **Main emergency shutdown panic switch**. This is a keyed, re-settable “mushroom” switch, that when activated immediately kills –48 VDC power via a battery disconnect switch, kills the –48 VDC power plant, kills 110 VAC power, and kills secondary 110 VAC power. It does this with a shorting connection. The switch is cleared with a key, at which point the –48 VDC power plant starts up, main 110 VAC is restored, the Control Rack CPUs start up etc.

12. **Smoke detector/fire alarm**. This engages the same switch contacts as the manual emergency switch. Once the smoke/alarm condition has cleared it requires keyed manual intervention to start the power-up sequence as described above. These systems are beyond the scope of this document and are NRAO’s responsibility.

Not shown are the monitor/control lines that allow the CPCC to turn on/off room **HVAC** systems, or smoke alarm monitor lines. Refer to section 4.1 bullets 4. and 12. and section 4.4.

The following sections describe each of the PMCS elements, failure and recovery modes, and software functionality in considerably more detail than outlined in this overview.

## 5.2 Rack Power M&C Interface Board (RPMIB)

A functionally complete schematic of the RPMIB is shown in Figure 5-2. This board is custom built to meet the needs of the system and to interface to the NI 6509 interface card via one or two 100-pin SCSI connectors. This approach is chosen so that reliable, centralized and redundant fault-tolerant operation is possible—no complex power control electronics is located in the correlator racks.

The electronics on the board is all low-speed and very simple. It consists of diodes, resistors, and opto-isolators and is likely a double-sided plated-through PCB with no power or ground planes. This board is wired into the rack’s monitor and control points and is therefore not hot-replaceable. Keeping the electronics simple significantly improves its reliability and robustness. In addition it contains fault-tolerant redundant circuitry to further reduce the probability that a failure will require shutdown of a rack for repair.

The fan speed control is an optically-isolated 5-bit pseudo-DAC (Digital to Analog Converter), properly biased to –48 VDC (i.e. since the fans are +’ve voltage fans, -48 VDC connects to the 0 V or ground input of the fan). Each of the 4 fans has its own “opto-DAC” circuit, although all 4 are driven by the same control lines (i.e. there is no requirement to individually control the speed of each fan). The “Fan speed control” input to the fan itself is 100 k ohms input impedance. This circuit is mirrored for the secondary SCSI connector, with a jumper to disable the secondary circuit if unused.

The equation relating the control voltage, $V_c$, and the opto-isolator LED current $I_{LED}$ for the bias resistors chosen is as follows:

$$V_c\left(\frac{1}{2.2k}+\frac{1}{8.4k}\right)\cong -I_{LED}+\frac{48}{8.4k}$$

This assumes a 100 % current transfer ratio from the $I_{LED}$ to $I_{CE}$ for the opto-isolator, approximately the case for the H11A617 opto-isolator. The LED current is approximately:

$$I_{LED}\cong\frac{4.3-1.2}{R}$$

Where R is the resistor in series with the control line diode. Resistors with values of 18.2k, 9.1k, 4.7k, 2.4k, and 1.2k yield decreasing control voltages ($V_c$) in approximately 0.3 V equal steps with increasing binary values on inputs B0-B4. This assumes a full 5 V control voltage from the NI 6509. The maximum output current from any single line of the NI 6509 is 10.3 mA—less than ½ the maximum 24 mA capability.

The fan speed monitor lines to the NI 6509 are individually optically-coupled to the tachometer outputs of the fans. The tachometer output from the fan is open collector with a 680 ohm impedance, referenced to –48 VDC. A square wave with three pulses per revolution is produced. Pulse width is inversely proportional to speed, with minimum pulse width approximately 4 milliseconds at full speed. Pulse rise time is about 4 μsec.

There are two 48 VDC screw terminals for connecting to a breaker in the breaker panel. The power connections for each fan are provided on this board for convenience. Individual fuses to each fan power line are provided to protect fans and fan wiring.

The 43 control outputs from the primary SCSI connector are diode-OR'd with the same outputs from the secondary SCSI connector. 38 monitor inputs are routed to both connectors through current limiting resistors (i.e. to prevent contention if the NI 6509 input happens to accidentally be set to an output).

The –48 VDC supply is optically coupled to a monitor input. This allows the CPCC to determine if 48 VDC is available, and in which racks; although there is no provision for determining the actual 48 VDC level except through the –48 VDC Power Plant network interface. Separate circuits for each of the primary and secondary SCSI connectors are provided since these circuits require +5 VDC from the respective connector.

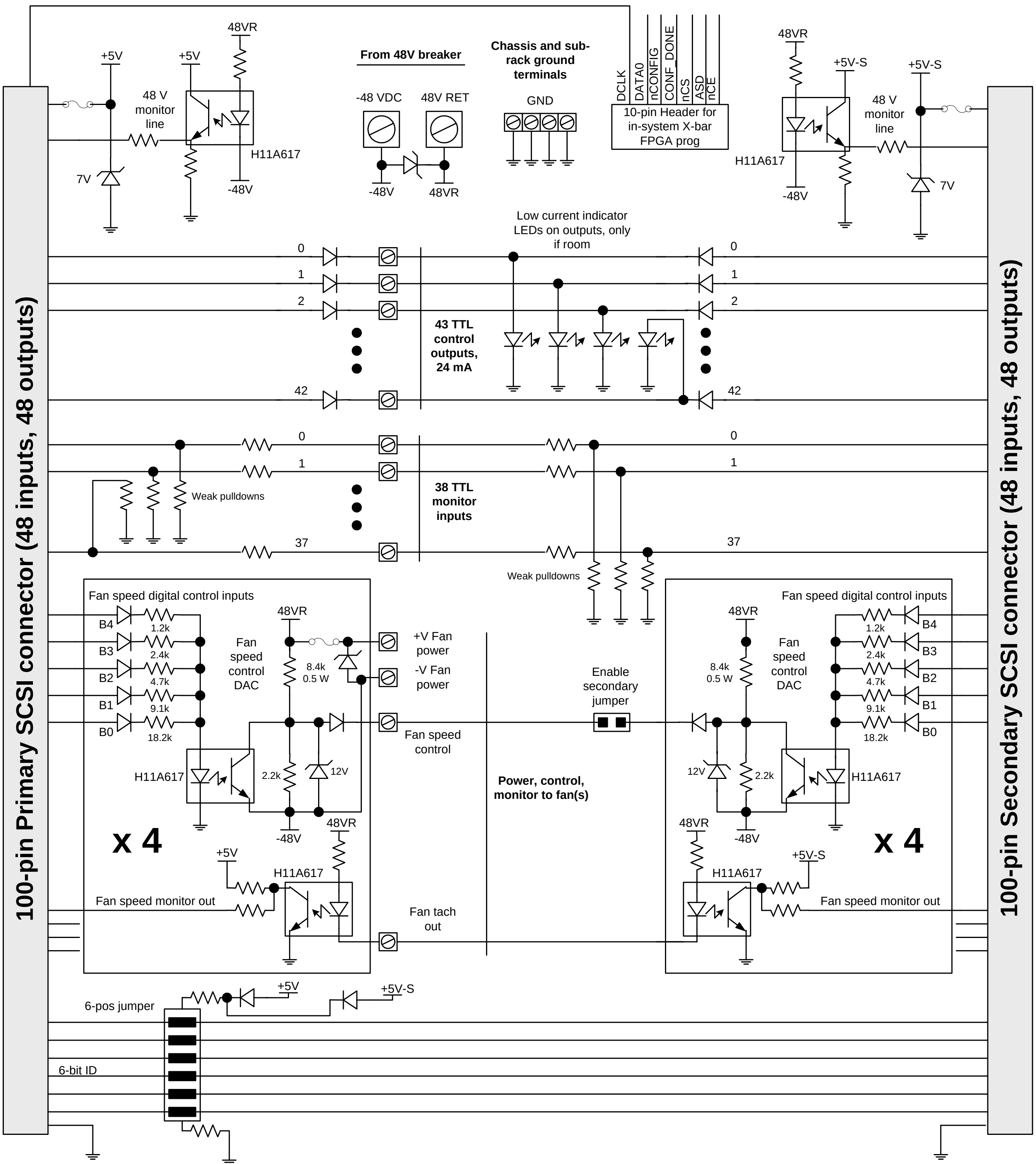


**Figure 5-2 RPMIB functional schematic.**

A 6-bit jumper or DIP-switch (DIP switches are unreliable and should be avoided) ID is provided so that the CPCC can empirically determine which rack/RPMIB a particular NI 6509 card is connected to. The +V supply for this switch is provided with a diode-OR connection from each SCSI connector. Signals are provided via a 10-pin header for X-bar Board FPGA in-system programming (or rather, in-system updates of the serial configuration PROM)

Refer to Table 5-5 for SCSI connector pinouts.

The RPMIB can operate with just the primary SCSI connector active (connected to a NI 6509 card) or, for redundant operation, with both the primary and secondary connectors active.

### 5.2.1 RPMIB Failure Modes and Effects Analysis (FMEA)

The RPMIB is designed to be simple, redundant, and fault tolerant. Table 5-1 is a FMEA of the RPMIB with only the primary 100-pin SCSI connection to a NI 6509 interface card. The FMEA considers the impact all the way through to and including the NI 6509, Control Module/CPU, and CPCC chassis power supply.

In this scenario it is clear that there are some severe effects requiring immediate action or lost correlator/telescope time. Also, in some cases, considerable debugging is required to determine the cause of the failure so it can be fixed.

| Failure | Effect | Action Required/Taken |
|---|---|---|
| Fan control opto-coupler fails (CE open) | Fan runs at full speed. Fan speed monitor indicates full speed. | Maintenance day debug to find problem. |
| Fan speed monitor opto-coupler fails | CPCC senses that fan has quit. Fan inspected, found to be ok. | Next maintenance day the RPMIB or connections need checking/replacement. |
| Correlator board power control line fails/disconnects | Correlator module shuts down, monitor line indicates power is off, CMIB does not respond. No manual restart possible. | Requires servicing/debugging to determine if it is control circuit or the correlator board itself that failed. Can likely be done on-line with volt meter. |
| Correlator board power monitor line fails | Indication is that power on the module is off. CMIB responds to queries and no other problems found. Conclude monitor line has failed. | Maintenance day debug required to determine if it is the RPMIB, cable, or NI 6509 card. |
| -48 V monitor | Indication is that –48 VDC has failed, | Maintenance day debug |

| | | |
|---|---|---|
| line fails | however fan speed is still ok, CMIBs responding[1]. Conclude that monitor line has failed. | required to determine if it is the RPMIB, cable, or NI 6509. |
| 5-bit ID changes | No operational effect. Software must be designed to be robust to this failure. | Maintenance day debug required to determine if it is the RPMIB, cable, or NI 6509. |
| SCSI-100 cable connector comes loose. | Fans may run at full speed. One or several correlator modules shutdown. Indication is that one or more fans have quit and that one or more modules have quit. –48 VDC monitor could indicate –48 VDC power lost. Rack is effectively lost, taking out up to 4 antennas or one entire sub-band. | Manual debug required to determine if –48 VDC breaker has tripped, RPMIB has massively failed, cable is bad/disconnected, or NI 6509 card is dead. |
| NI 6509 card PCI bus interface fails. | Rack likely will keep running ok[2]. Indication is that rack is experiencing multiple failures. May not want rack to continue to run since limited monitoring available, and no power control possible. | Manual debug to determine problem. Requires power-cycle of part or all of correlator system to replace NI 6509 card. |
| CPCC CPU fails. | Likely auto-reboot. The NI 6509 "safe mode" is all control outputs on. All racks continue to operate normally, all fans at full speed, but monitor and control is lost. | Manual debug to find problem…continuous reboot cycles of the processor reasonably quickly diagnosed. Requires power cycle of part or all of correlator system. |
| CPCC power supply fails. | Correlator system, or part of it (depending on if it is CPCC-P or CPCC-S) immediately completely shuts down. | Immediate action to find cause and repair. Requires power supply replacement through rear of rack. Could take ~1 hour if spare available. Could take a few days or weeks if no spare available. |

**Table 5-1 FMEA of the PMCS with no hot-standby redundant CPCC (i.e. no Control Rack #2).**

[1] The rack Ethernet switch, fans, and RPMIB are on the same –48 VDC breaker line.
[2] Assuming the card holds all control outputs high if PCI bus interface fails.

Table 5-2 is the FMEA if there are redundant CPCCs (i.e. two Control Racks, each with two CPCCs) connected to the RPMIB secondary 100-pin SCSI connector. In this case the failure effects are much less severe, there is no lost correlator time, and it is possible during maintenance day to more easily find failed hardware than in Table 5-1.

| **Failure** | **Effect** | **Action Required/Taken** |
|---|---|---|
| Fan control opto-coupler fails (CE open) | Fan runs at full speed. Fan speed monitor indicates full speed. | Maintenance day debug to find problem. Could be RPMIB, cable, or NI 6509. |
| Fan speed monitor opto-coupler fails | CPCC senses that fan has quit. Redundant CPCC sees that fan is ok. No manual inspection required. | Maintenance day the RPMIB, cable, or NI 6509 need checking and possible replacement. |
| Correlator board power control line fails/disconnects | Correlator module continues to run, and no immediate indication of failure condition. | Maintenance day check finds problem. Debug to determine if RPMIB, cable, or NI 6509 failure. |
| Correlator board power monitor line fails | Indication is that power on the module is off. Redundant CPCC sees its ok, and CMIB responds. | Maintenance day debug required to determine if it is the RPMIB, cable, or NI 6509 card. |
| -48 V monitor line fails | Indication is that –48 VDC has failed. Redundant CPCC says ok. Fan speed is still ok, CMIBs responding[3]. Conclude that monitor line has failed. | Maintenance day debug required to determine if it is the RPMIB, cable, or NI 6509. |
| 5-bit ID changes | No operational effect. Redundant CPCC sees same problem. Software must be designed to be robust to this failure. | Manual debug required to determine if it is the RPMIB, cable, or NI 6509. |
| SCSI-100 cable connector comes loose. | Fans may run at full speed. Correlator boards continue to run. Indication is that one or more fans have quit and that one or more modules have quit. –48 VDC monitor could indicate –48 VDC power lost. Redundant CPCC says everything is ok, but fans are running too fast. | Maintenance day debug required to determine if RPMIB has massively failed, cable is bad/disconnected, or NI 6509 card is dead. No lost correlator time. |
| NI 6509 card PCI bus interface fails. | Rack keeps running ok. Indication is that rack is experiencing multiple failures. Redundant CPCC says | Maintenance day debug to determine problem. Requires power-cycle of |

[3] The rack Ethernet switch, fans, and RPMIB are on the same –48 VDC breaker line.

| | | |
|---|---|---|
| | everything ok. Power control may be lost[4]. | affected CPCC to replace NI 6509 card. No correlator interruption. |
| CPCC CPU fails. | Auto-reboot may or may not restore CPCC. NI 6509 "safe mode" is all control outputs hi-Z. All racks continue to operate normally, all fans at full speed. Full monitor and control provided by redundant CPCC. | Manual debug to find problem…continuous reboot cycles of the processor reasonably quickly diagnosed. Requires defective CPCC power down and CPU replacement. No lost correlator time. |
| CPCC power supply fails. | Redundant CPCC provides M&C functions. Correlator remains on-line. | Replace defective power supply or entire unit the next day to bring failed CPCC back on line. No lost correlator time. |

**Table 5-2 FMEA with hot-standby redundant CPCC wired to secondary connector on all RPMIB modules.**

[4] If the NI 6509 card is set to hold all outputs high. If outputs set to hi-Z in this failure mode, then monitor and control still retained.

### 5.2.2 RPMIB PCB Design

A straw-man design for the RPMIB PCB is shown in Figure 5-3. All connections, except for the SCSI connectors and the 10-pin header, are screw terminals.

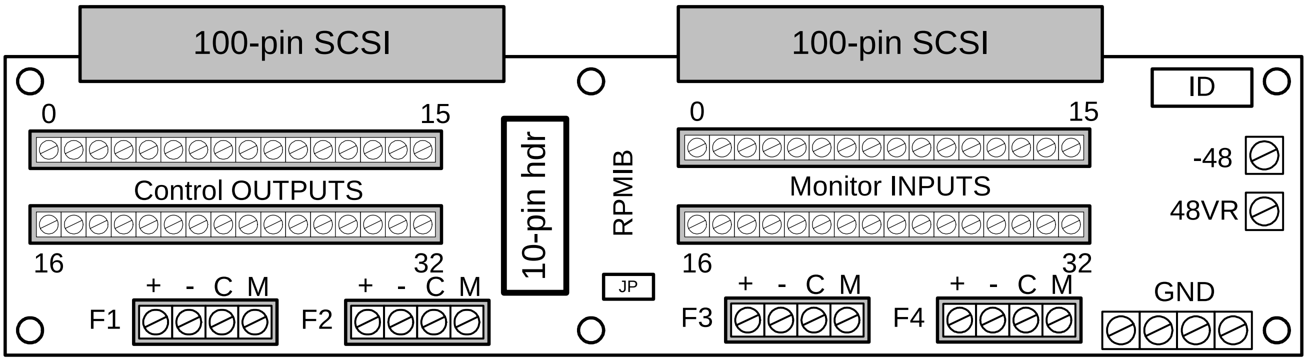


**Figure 5-3 Straw-man design of the RPMIB PCB.**

## 5.3 Correlator Rack

Each Correlator Rack contains an RPMIB wired to correlator hardware as shown in Figure 5-1. The RPMIB contains screw terminals, as shown in Figure 5-2, to attach to –48 VDC power, the fans, the Ethernet switch DC SSR control, and to correlator boards. Each correlator board, including X-bar Boards, are individually monitored and controlled via the RPMIB. The GND terminals connect to a ground wire from each sub-rack rail, and a ground wire to a chassis grounding point.

The DC SSR (DC Solid State Relay, similar to Figure 5-5) is controlled with the RPMIB. It is a good idea to make this redundant as well since an SSR failure (open circuit) cuts off communication to the network, effectively taking down the rack. The redundant SSR is wired in parallel, with separate control lines to the RPMIB. If an SSR does go open circuit the switch will continue to run and it is possible to find the failure with system checks on the next maintenance day.

In the redundant RPMIB configuration, separate 100-pin cables are run from each RPMIB back to CPCCs in Control Rack #1 and Control Rack #2. This will provide redundant fault-tolerant operation as described in the previous section (Table 5-2).

### 5.3.1 RPMIB Mounting

The RPMIB is mounted inside the back of each correlator rack (refer to the RFS document A25017N0005). The RPMIB PCB is oriented so the 100-pin SCSI cables entering from the roof of the rack plug into the board. The mounting plate also contains the DC SSRs for the Ethernet switch. Figure 5-4 is a straw-man layout of the mounting plate, RPMIB PCB, and DC SSRs. Figure 5-5 shows a panel-mount DC SSR.

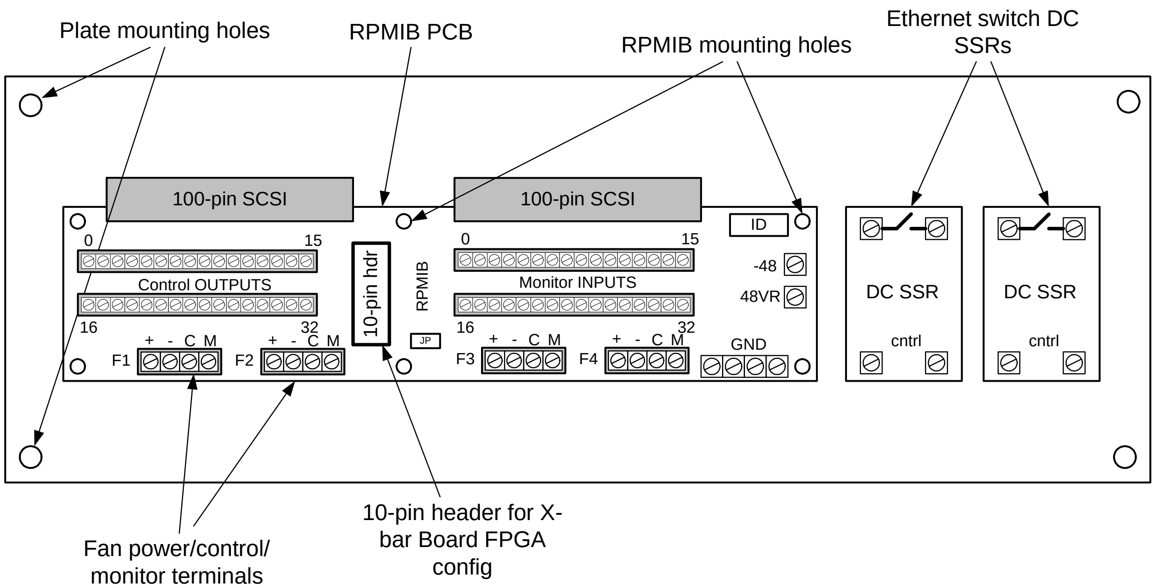


**Figure 5-4 RPMIB mechanical mounting in the correlator rack.**

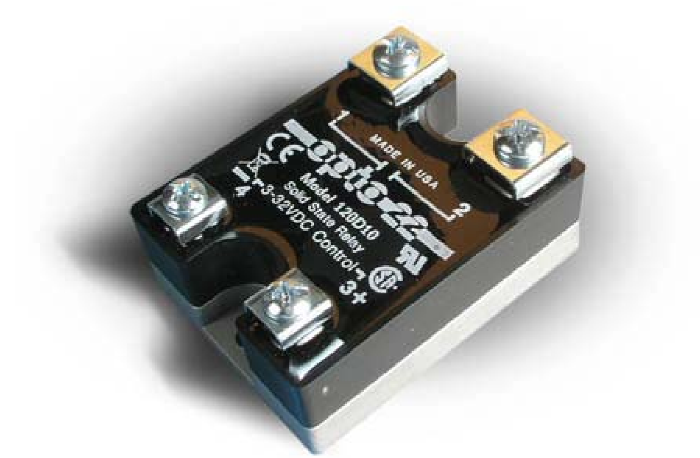


**Figure 5-5 Panel-mount DC Solid State Relay with 3-30 VDC control voltage.**

## 5.4 CBE AC Switch Boxes

This section has been removed. Reliance will be made on remote power control of CBE computers via Ethernet, using capability built into those systems.

## 5.5 Control Rack

The 19” Control Rack shown in Figure 5-1 contains CPCC, MCCC, and Boot Server computers. The baseline plan is that the CPCC is an 18-PCI-slot rack-mount PC. MCCC and Boot Server computers are rack-mount “pizza-box” computers. The CPCC and MCCC computers are separate for reliable operation (i.e. to keep CPCC functionality simple).

Definition of MCCC functionality is beyond the scope of this document. .

### *5.5.1 CPCC Rack-mount Computer*

The most cost-effective platform for the CPCC computer is a COTS 3U or 4U 19” rack-mount PC with 18 PCI slots. These slots can be used to hold the NI-PCI-6509 cards, with cable access at the rear of the box. These are ruggedized PCs, and there is (apparently) an EIA physical standard (RS-310C) for these systems. Cooling fan filters, fans, and drives are easily replaceable without having to remove the unit from the rack. One such system is the “SuperLogics” SL-R4U-3.0-1024-XP-18PCI, and it contains 18 slots, a 3.0 GHz Pentium 4 processor, lots of RAM, big hard drives and with 10/100/1000 Ethernet. This system costs $2395. A picture of this system is shown in Figure 5-6. This system will likely be mounted in the rack on sliding rails for easy servicing.

A cost estimate for a complete redundant PMCS system (excluding the Category 5E cable [very cheap anyway]) for the correlator is as follows:

| Item | Qty | Description | Price ea | Ext Price |
|---|---|---|---|---|
| 1 | 2 | Rack-mount PC with 18 PCI slots. (CPCC) | $2395 | $4790 |
| 2 | 8 | Pizza-box 1U PC | $500(est) | $4000 |
| 3 | 32 | NI-PCI-6509 | $264 | $8,448 |
| 4 | 32 | 100-in SCSI cable, up to 20 m in length | $242 | $7,644 |
| 5 | 16 | RPMIB | $400(est) | $6400 |
| 6 | 4 | Allied Telesyn AT9424-T/GB | $1200 | $4,800 |
| 7 | 2 | 19” x 5 ft rack, with side panels and door | $700(est) | $1400 |
| | | | **TOTAL** | **$37,500 (US)** |

**Table 5-3 Price table for PMCS with rack-mount, 18 PCI slot PC.**

**Figure 5-6 Picture of a rack-mount PC system with 18 PCI slots.**

The data sheet for this chassis is appended to the end of this document. There are many other suppliers of similar systems. There is no reliability data for this system, so likely the reliability is typically the same as a desktop PC, which the Telcordia SR-332 specification states is about 2200 hours (91 days).

### *5.5.2 18-slot NI PXI Chassis*

This section has been removed. Use of CompactPCI or PXI computers for anything other than the CPCC is cost prohibitive and unnecessary.

### *5.5.3 NI 6509 Digital I/O Card*

The 3U CompactPCI 6509 card provides 96 digital I/O lines, operating at 5 V logic levels. Each output has a full 24 mA source/sink drive capability. Lines can be configured as inputs or outputs in banks of 8, and the RPMIB is structured accordingly. The card contains a watchdog timer to put the outputs into a pre-programmed safe state when a fault condition is detected. Where there are two Control Racks, in the redundant configuration, the "safe state" output would likely be high impedance to allow the secondary CPCC to still control the system as outlined in Table 5-2.

The NI 6509 card contains an FPGA, although it cannot be programmed by the user.

Each NI-PXI-6509 card is listed at $410 CAD (whilst the NI-PCI-6509 card for the rack-mount PC is listed at $300 CAD). The MTBF is not known, but is likely greater than the MTBF of the CPU module and so conservatively it could be 124,400 hours.

The data sheet for this card is appended to the end of this document.

### *5.5.4 CPCC Reliability*

With a rack-mount PC with a reliability of 2200 hours (Telcordia SR-332), and assuming 124,400 hours for NI-PCI-6509 card, a fully loaded CPCC (16 NI-6509 cards) has an MTBF of approximately 1700 hours. If it takes 1 hour to repair a failure in a Control Rack, the probability of the other Control Rack failing within that 1 hour is 1/(1700hr)=~$10^{-3}$. The combined MTBF is then 70,000 days or 194 years. More likely if spares are available, it could take 24 hours to repair a Control Rack, and so the probability of a failure of the other Control Rack in that 24 hours is 24/1700=14x$10^{-3}$. **The combined MTBF is then 1700 hrs / 14x$10^{-3}$ = 5000 days = 14 years**.

## 5.6 Startup and Shutdown Sequences

A likely startup sequence, following the reset of a manual emergency shutdown or after power is restored after an extended power failure, is as follows:

1. –48 VDC power plant self-starts. After batteries are sufficiently charged (or right away, depending on system capability), the battery disconnect is re-engaged to energize –48 VDC power to the system. All correlator modules and rack Ethernet switches are turned off at this point since the CPCCs are configured for all output controls to be OFF or high impedance on startup, and are clearly OFF if the CPCC has no power.

2. At the same time as step 1., main 110 VAC is restored thus providing 110 VAC to the computers in the Control Rack (Figure 5-1). The CPUs boot from on-board hard drives.

3. The CPCCs try to establish network communications with the EVLA M&C system, and with the companion CPCC in the other Control Rack.

4. Once contact amoungst CPCCs is established, each one verifies that –48 VDC is present in each correlator rack by reading the –48 VDC status lines. If there is disagreement between them, then the disagreement is reported to the EVLA M&C system, if communications has been established.

5. Both CPCCs go through the same timed sequence of starting up modules in correlator racks and the CBE and switches, communicating to each other sequencing and status information. It does not matter if timing between the CPCCs is not exact, since the redundant nature of the RPMIB will easily handle timing discrepancies, provided modules are not powered up too quickly.
This power-up procedure happens independently of whether communications with the EVLA M&C system has occurred or not.

6. At the same time that modules are being powered up, the CPCC sequences up the 4 HVAC blowers. Exact sequencing is TBD, but generally starts with 1$^{st}$ blower on, bring up ¼ of the modules, next blower on, bring up the next ¼ etc. Experimentation is likely required to get the sequence right to minimize heat changes, and may involved feedback/monitor of board temperatures in a control loop.

7. Once power is on to all modules, power status is ok, and some time has elapsed to allow the CMIBs and CBE computers to boot, the CPCCs go into the steady state condition where they are independently monitoring and controlling the system—checking power status lines, checking module voltages and temperatures, adjusting fan speeds, polling processors to determine if they are alive or not, checking the status of the –48 VDC power plant etc. Also in this state, the MCCC functions are started, communications are established with CMIBs, BIST tests are run etc.

   In this state, the CPCCs periodically let each other know that they are alive, let the EVLA M&C system know they are alive, and report any fault conditions to the EVLA M&C system. If a CPCC does not get the keep alive signal for a period of time, it informs the EVLA M&C system that the redundant CPCC is down. This condition requires a manual check of the situation to repair it at the next available time when service personnel are on site.

A likely <u>shutdown sequence</u> in response to a power failure is as follows:

1. The CPCCs get an indication of mains power failure by talking to the –48 VDC power plant and, if possible, by talking to the secondary AC UPS. (If a 2$^{nd}$ smoke alarm indication occurs, a faster shutdown sequence, occurring within 60 seconds is required.)

2. Once a power failure condition is detected, a "Toff" timer is started that, at various configurable epochs, causes a sequence of events to occur as described in the remaining bullets. If, at any time, an indication from the power plant that main power is restored, appropriate start up action will occur. At this point the

HVAC system loses active cooling, although blower fans are still running and there is still inherent cooling capacity left in cooling coils.

3. Toff=TSLEEP. Once this epoch is reached, it is time to put the correlator into a sleep mode to conserve power and maintain heat capacity. At this point all correlator processing will cease. CMIBs are told (either directly or via the MCCC) to go into sleep mode, temperatures are monitored, and fans are slowed down considerably to maintain heat capacity. HVAC blower fans turned off. CBE computers and switches are turned off to reduce main 110 VAC load to the minimum.

4. Toff=TPDWN. This epoch is reached automatically when the –48 VDC power plant shuts down because battery capacity is exhausted. Thus, correlator boards and fans automatically shut down, and therefore automatically retain as much heat capacity as possible. This condition is determined when the –48 VDC power monitor lines indicate that power is lost and confirmed by the inability to contact the power plant via the network.

5. Toff=T_CNTRL_PDWN. This epoch is reached when the 110 VAC mains power is lost. The CPUs lose power and shutdown.

If mains power is restored at some point in time prior to the T_CNTRL_PDWN epoch, then the system, under control of the CPCCs as described above, goes through the startup procedure, starting at the appropriate point. For example, if mains power is restored before the TSLEEP epoch has been reached, then no action is required since the system is still fully operational.

## 5.7 CPCC Software

CPCC software performs functions as described in previous sections, reporting warning and error conditions and taking autonomous protection action where necessary, as well as responding to commands from the EVLA M&C system. Table 5-4 indicates suggested command and response primitives that the CPCC software should be able to handle from/to the EVLA M&C system. Other command and response primitives may be necessary. It is likely that a PMCS GUI, tied into the main correlator or EVLA operator panel needs to be developed. Further software definition and design is required.

| **Command** | **Example response(s) or autonomous status messages** | **Action** |
|---|---|---|
| sysPowerOn<br>(*possibly not required…*) | CBE_Started: node 0…<br>Corr_Started: SB0-0-4… | Start up the correlator boards and the CBE. Report status as boards and computers power up. All components in the Control Rack are always ON. |
| sysPowerOff<br>(*possibly not required, since the system should never shutdown, except* | CBE_Stopped: node 0…<br>Corr_Stopped: SB0-0-4… | Power down the correlator boards and the CBE. Report status as boards and computers power down. All components in the Control Rack are |

| | | |
|---|---|---|
| *for emergency*) | | always ON. |
| modulePowerCycle | ModulePowerOff: SB0-0-4<br>ModulePowerOn: SB0-0-4 | Power cycle a module for a specified duration of time. |
| modulePowerOff | ModulePowerOff: SB0-0-4 | Power OFF a particular module. |
| modulePowerOn | ModulePowerOn: SB0-0-4 | Power ON a particular module. |
| checkTemp | SysNote: SB0-0-4: 50 C<br>SysNote: BB101-1-5: 55 C | Reports the maximum temperature found on each board with a temperature sensor. |
| checkVoltageRange | SysNote: SB0-0-4: ok<br>SysNote: BB101-1-5: margin warning: V3.3: 0.05 V | Reports if any voltages are out of range, or starting to approach out range. |
| | SysWarn: TempHigh: SB-0-0-4: 60 C | Autonomously reports any over temperature conditions found every 30 sec |
| | SysErr: Rack 1: Fan Stopped<br>SysErr: SB-0-0-4: overtemp shutdown | Autonomously reports any error conditions requiring action; continuous reports every 30 sec? |
| | SysErr: Power fail detect…system sleep mode in 2.5 minutes. | On power failure, reports detection and when shutdown epochs reached. |
| | SysNote: Power restored…restarting system… | When power restored, reports detection and when modules turned on and system ready. |
| | SysNote: CPCC-P-1 alive | Automatic keep alive reporting. |
| startMaintCheck | SysNote: checking rack 0… | Perform maintenance checks to find and report faulty redundant circuitry. This takes the correlator off-line, and should be done only during scheduled maintenance times. |

**Table 5-4 Some suggested command and response primitives from/to the EVLA M&C system.**

## 5.8 NI 6509 Monitor and Control Routing

A suggested routing table for the 100-pin NI 6509 SCSI connector, through the RPMIB, to devices in the Correlator Rack is shown in Table 5-5. The 100-pin SCSI connector is taken from the NI 6509 data sheet and is shown in Figure 5-7.

Note: Crate 0 is the TOP crate, and Crate 1 is the BOTTOM crate.

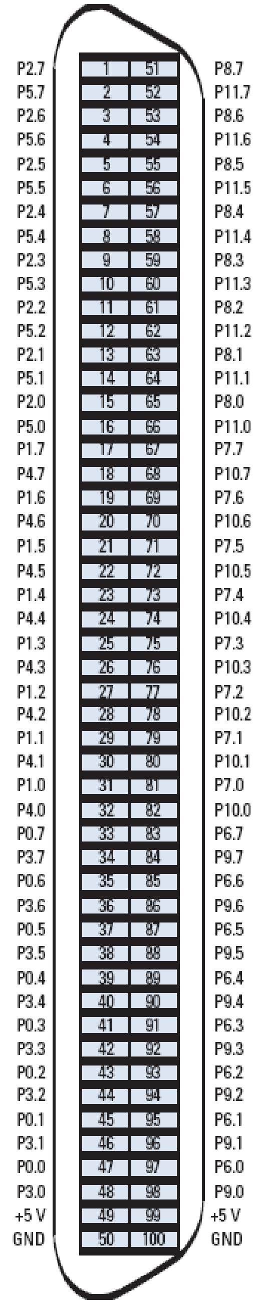


**Figure 5-7 NI 6509 100-pin SCSI connector.**

**Table 5-5 Possible NI 6509 port/RPMIB/correlator rack connections.**

| Outputs/Control | | | | | Inputs/Monitor | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin #** | **NI 6509 Port** | **RPMIB screw terminal** | **Rack connection** | | **Pin #** | **NI 6509 Port** | **RPMIB screw terminal** | **Rack connection** |
| 47 | P0.0 | Out-0 | Crate 0, Slot 0 | | 97 | P6.0 | In-0 | Crate 0, Slot 0 |
| 45 | P0.1 | Out-1 | Crate 0, Slot 1 | | 95 | P6.1 | In-1 | Crate 0, Slot 1 |
| 43 | P0.2 | Out-2 | Crate 0, Slot 2 | | 93 | P6.2 | In-2 | Crate 0, Slot 2 |
| 41 | P0.3 | Out-3 | Crate 0, Slot 3 | | 91 | P6.3 | In-3 | Crate 0, Slot 3 |
| 39 | P0.4 | Out-4 | Crate 0, Slot 4 | | 89 | P6.4 | In-4 | Crate 0, Slot 4 |
| 37 | P0.5 | Out-5 | Crate 0, Slot 5 | | 87 | P6.5 | In-5 | Crate 0, Slot 5 |
| 35 | P0.6 | Out-6 | Crate 0, Slot 6 | | 85 | P6.6 | In-6 | Crate 0, Slot 6 |
| 33 | P0.7 | Out-7 | Crate 0, Slot 7 | | 83 | P6.7 | In-7 | Crate 0, Slot 7 |
| 31 | P1.0 | Out-8 | Crate 1, Slot 0 | | 81 | P7.0 | In-8 | Crate 1, Slot 0 |
| 29 | P1.1 | Out-9 | Crate 1, Slot 1 | | 79 | P7.1 | In-9 | Crate 1, Slot 1 |
| 27 | P1.2 | Out-10 | Crate 1, Slot 2 | | 77 | P7.2 | In-10 | Crate 1, Slot 2 |
| 25 | P1.3 | Out-11 | Crate 1, Slot 3 | | 75 | P7.3 | In-11 | Crate 1, Slot 3 |
| 23 | P1.4 | Out-12 | Crate 1, Slot 4 | | 73 | P7.4 | In-12 | Crate 1, Slot 4 |
| 21 | P1.5 | Out-13 | Crate 1, Slot 5 | | 71 | P7.5 | In-13 | Crate 1, Slot 5 |
| 19 | P1.6 | Out-14 | Crate 1, Slot 6 | | 69 | P7.6 | In-14 | Crate 1, Slot 6 |
| 17 | P1.7 | Out-15 | Crate 1, Slot 7 | | 67 | P7.7 | In-15 | Crate 1, Slot 7 |
| 15 | P2.0 | Out-16 | 6U Crate Slot 0 | | 65 | P8.0 | In-16 | 6U Crate Slot 0 |
| 13 | P2.1 | Out-17 | 6U Crate Slot 1 | | 63 | P8.1 | In-17 | 6U Crate Slot 1 |
| 11 | P2.2 | Out-18 | 6U Crate Slot 2 | | 61 | P8.2 | In-18 | 6U Crate Slot 2 |
| 9 | P2.3 | Out-19 | 6U Crate Slot 3 | | 59 | P8.3 | In-19 | 6U Crate Slot 3 |
| 7 | P2.4 | Out-20 | 6U Crate Slot 4 | | 57 | P8.4 | In-20 | 6U Crate Slot 4 |
| 5 | P2.5 | Out-21 | 6U Crate Slot 5 | | 55 | P8.5 | In-21 | 6U Crate Slot 5 |
| 3 | P2.6 | Out-22 | 6U Crate Slot 6 | | 53 | P8.6 | In-22 | 6U Crate Slot 6 |
| 1 | P2.7 | Out-23 | 6U Crate Slot 7 | | 51 | P8.7 | In-23 | 6U Crate Slot 7 |
| 48 | P3.0 | Out-24 | 6U Crate Slot 8 | | 98 | P9.0 | In-24 | 6U Crate Slot 8 |
| 46 | P3.1 | Out-25 | 6U Crate Slot 9 | | 96 | P9.1 | In-25 | 6U Crate Slot 9 |
| 44 | P3.2 | Out-26 | DC SSR 1 | | 94 | P9.2 | In-26 | Spare-0 |
| 42 | P3.3 | Out-27 | DC SSR 2 | | 92 | P9.3 | In-27 | Spare-1 |
| 40 | P3.4 | Out-28 | Spare-0 | | 90 | P9.4 | In-28 | Spare-2 |
| 38 | P3.5 | Out-29 | Spare-1 | | 88 | P9.5 | In-29 | Spare-3 |
| 36 | P3.6 | Out-30 | Spare-2 | | 86 | P9.6 | In-30 | Spare-4 |
| 34 | P3.7 | Out-31 | Spare-3 | | 84 | P9.7 | In-31 | Spare-5 |
| 32 | P4.0 | FPGA hdr | DCLK | | 82 | P10.0 | FPGA hdr | CONF_DONE |
| 30 | P4.1 | FPGA hdr | DATA0 | | 80 | P10.1 | N/A | ID B0 |
| 28 | P4.2 | FPGA hdr | ASD | | 78 | P10.2 | N/A | ID B1 |
| 26 | P4.3 | FPGA hdr | nCS | | 76 | P10.3 | N/A | ID B2 |
| 24 | P4.4 | FPGA hdr | nCE | | 74 | P10.4 | N/A | ID B3 |
| 22 | P4.5 | FPGA hdr | nCONFIG | | 72 | P10.5 | N/A | ID B4 |
| 18 | P4.6 | | unused | | 70 | P10.6 | N/A | ID B5 |
| 18 | P4.7 | | unused | | 68 | P10.7 | N/A | unused |
| 16 | P5.0 | N/A | Fan speed B0 | | 66 | P11.0 | N/A | -48 V mon |
| 14 | P5.1 | N/A | Fan speed B1 | | 64 | P11.1 | N/A | Fan-1 mon |
| 12 | P5.2 | N/A | Fan speed B2 | | 62 | P11.2 | N/A | Fan-2 mon |
| 10 | P5.3 | N/A | Fan speed B3 | | 60 | P11.3 | N/A | Fan-3 mon |
| 8 | P5.4 | N/A | Fan speed B4 | | 58 | P11.4 | N/A | Fan-4 mon |
| 6 | P5.5 | | unused | | 56 | P11.5 | | unused |
| 4 | P5.6 | | unused | | 54 | P11.6 | | unused |
| 2 | P5.7 | | unused | | 52 | P11.7 | | unused |

The “FPGA hdr” signals on wires P4.0-P4.5 and P10.0 are used for in-system programming of the X-bar Board serial configuration PROMs in passive serial mode. Since the levels on these signals are not 3.3 V, a tri-state buffer on each X-bar Board is required to drive signals. Note that this interface requires a suitable 10-pin male header on the RPMIB, and connects only to the primary SCSI connector.

The 100-pin shielded cables running to the correlator racks may have to be up to 15 m long, and will have to be custom built. Cables are long and therefore have considerable high frequency attenuation. This is not a problem since all monitor and control lines are low frequency, and everything except for the fan speed monitor lines are effectively DC. These cables will be routed in the overhead signal cable trays. A quotation from the cable build company L-Com, indicates these cables will cost about $240 each, with a minimum order quantity of 50 pieces.

Wires running from correlator board monitor and control points will be routed and fastened to the rack chassis sidewall (or RPMIB attachment plate) before being securely attached to RPMIB screw terminals. The RPMIB and DC SSRs are attached to the mounting plate as shown in Figure 5-4.

## 5.9 Maintenance Actions and Scheduling

During scheduled maintenance days, checks should be run to find failures of redundant components. These checks can be performed automatically, on command from EVLA M&C, by the two CPCC-P processors. They work together to alternately turning OFF (or ON, depending on the function) control lines from one Control Rack and then the other to ensure that the alternate Control Rack still retains functionality.