# REQUIREMENTS AND FUNCTIONAL SPECIFICATION

# Station Board VSI Test FPGA

RFS Document: **A25050N0000**

Revision: 1.7

Dave Fort, 01 April 2011

*National Research Council Canada*
*Herzberg Institute of Astrophysics*
*Dominion Radio Astrophysical Observatory*

*P.O. Box 248, 717 White Lake Rd*
*Penticton, B.C., Canada*
*V2A 6J9*

# Table of Contents

# List of Figures

# List of Tables

# List of Abbreviations and Acronyms

| | |
|---|---|
| **CMIB** | Correlator Monitor & control Interface Board |
| **EVLA** | Expanded Very Large Array |
| **FPGA** | Field Programmable Gate Array |
| **ISR** | Interrupt Service Routine |
| **HM** | Hard Metric (2 mm 8+2 ) |
| **PCB** | Printed Circuit Board |
| **PPS** | Pulse Per Second |
| **RFI** | Radio Frequency Interference |
| **VLBA** | Very Long Baseline Array |
| **VLBI** | Very Long Baseline Interferometry |
| **VSI** | VLBI Standard Interface |
| **WIDAR** | Wideband Interferometric Digital ARchitecture |
| **XOR** | bitwise eXclusive OR |

Revision History

| **Revision** | **Date** | **Changes/Notes** | **Author** |
|---|---|---|---|
| DRAFT | 1 Jul 2006 | Initial Draft | D. Fort |
| 1.0 | 15 Oct 2006 | Changes are highlighted | D. Fort |
| 1.1 | 15 Jan 2007 | Input delays replaced by DDR clocking. Changes from 1.0 are highlighted. | D. Fort |
| 1.2 | 25 Jan 2007 | Minor test changes. Changes from 1.1 are highlighted. | D. Fort |
| 1.3 | 25 Apr 2007 | Added loop back tick counter. Removed *protect* function. Added STICK delay. Changes from 1.2 are highlighted. | D. Fort |
| 1.4 | 25 May 2007 | Changes from 1.3 are highlighted. | D. Fort |
| 1.5 | 20 Sep 2009 | Added hop count to PPSCODE generator. Added ability to set hop count and second count in PPSCODE generator and to force a CRC error in PPSCODE. Crystal clock no longer used. Changes from 1.4 are highlighted. | D. Fort |
| 1.6 | 02 Mar 2010 | Added PLL reset. Added STICK measurement. Changes are highlighted. | D. Fort |
| 1.7 | 01 Apr 2011 | Added pinouts, etc. | D. Fort |

# 1 Introduction

This document would normally describe the detailed requirements and design concepts for the VSI (VLBI Standard Interface) FPGA but, instead, will describe the design needed for testing the Station Board PCB.

The VSI Test FPGA will allow testing of the inputs from the Filter FPGAs and the VSI connections to the rear connector using an external cable. In addition, it can generate the time code that would normally be supplied by the system time code generator so that the Station Board can be tested by itself. Each Station Board contains two VSI FPGAs and hence two cables are needed to test the VSI connections. However, only one time code can be generated because only one of the VSI FPGAs (bank A) is fed by an external crystal oscillator and connected to the output connector.

The development plan for the VSI FPGA is as follows:

1. Develop and test a design in a Xilinx Virtex-4 FPGA (SX35) that allows the Station Board PCB to be completely tested. The design will be done in Verilog HDL. This design also contains a time code generator for prototype testing.

2. The main VSI design will be done at a later time.

# 2 Overview

VSI FPGAs reside on the Station Board. The Station Board receives two wide bands and sends up to 18 narrow bands from each of the wide bands on to the baseline part of the correlator. The primary functions of the VSI Test FPGA is to

1. test the narrow band data connections from the filter FPGAs.

2. test the VSI connections between the Station Board and the VSI backplanes.

3. produce a time code for testing the Station Board PCB.

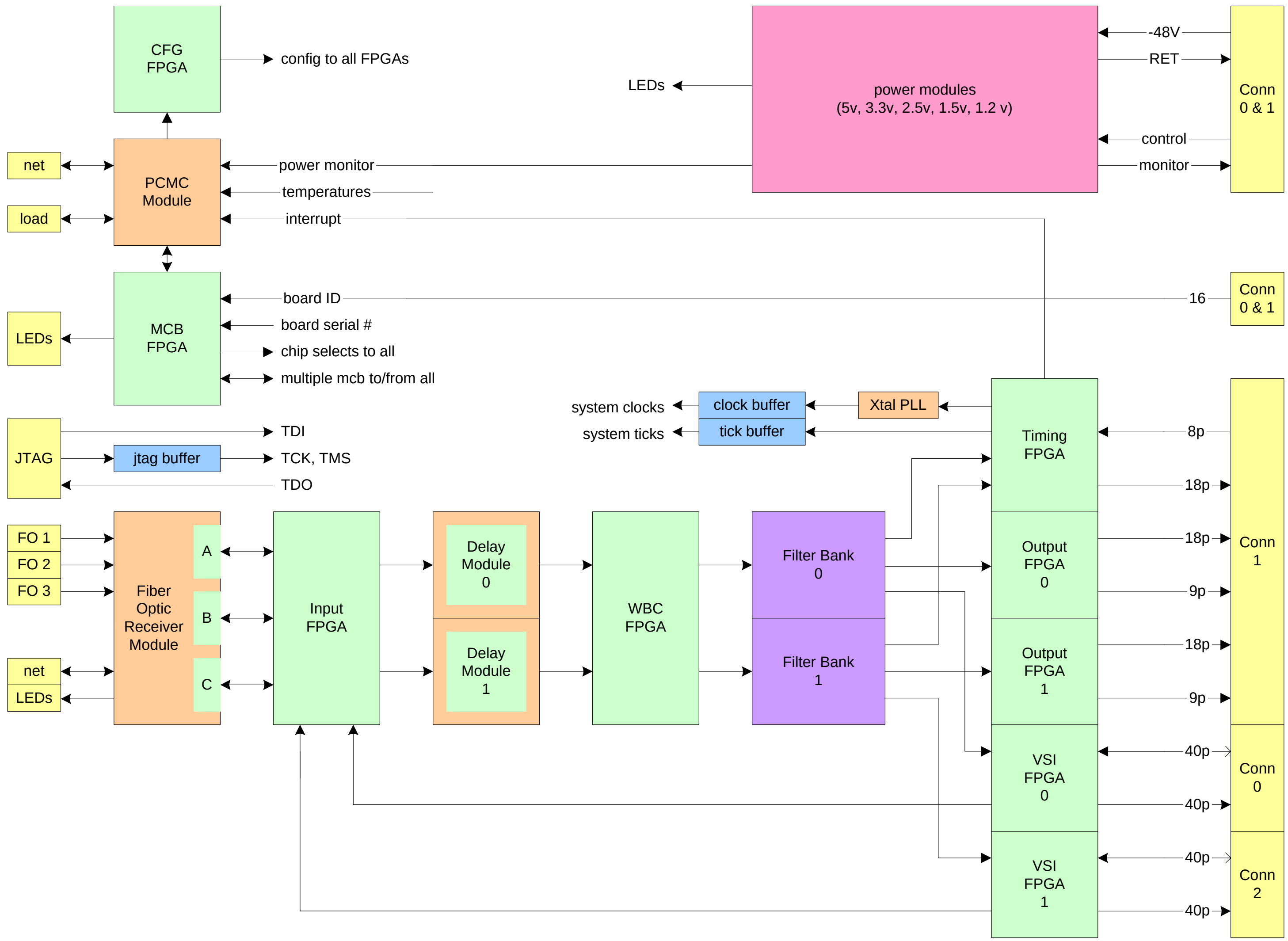


**Figure 2-1 Block diagram of the Station Board.**

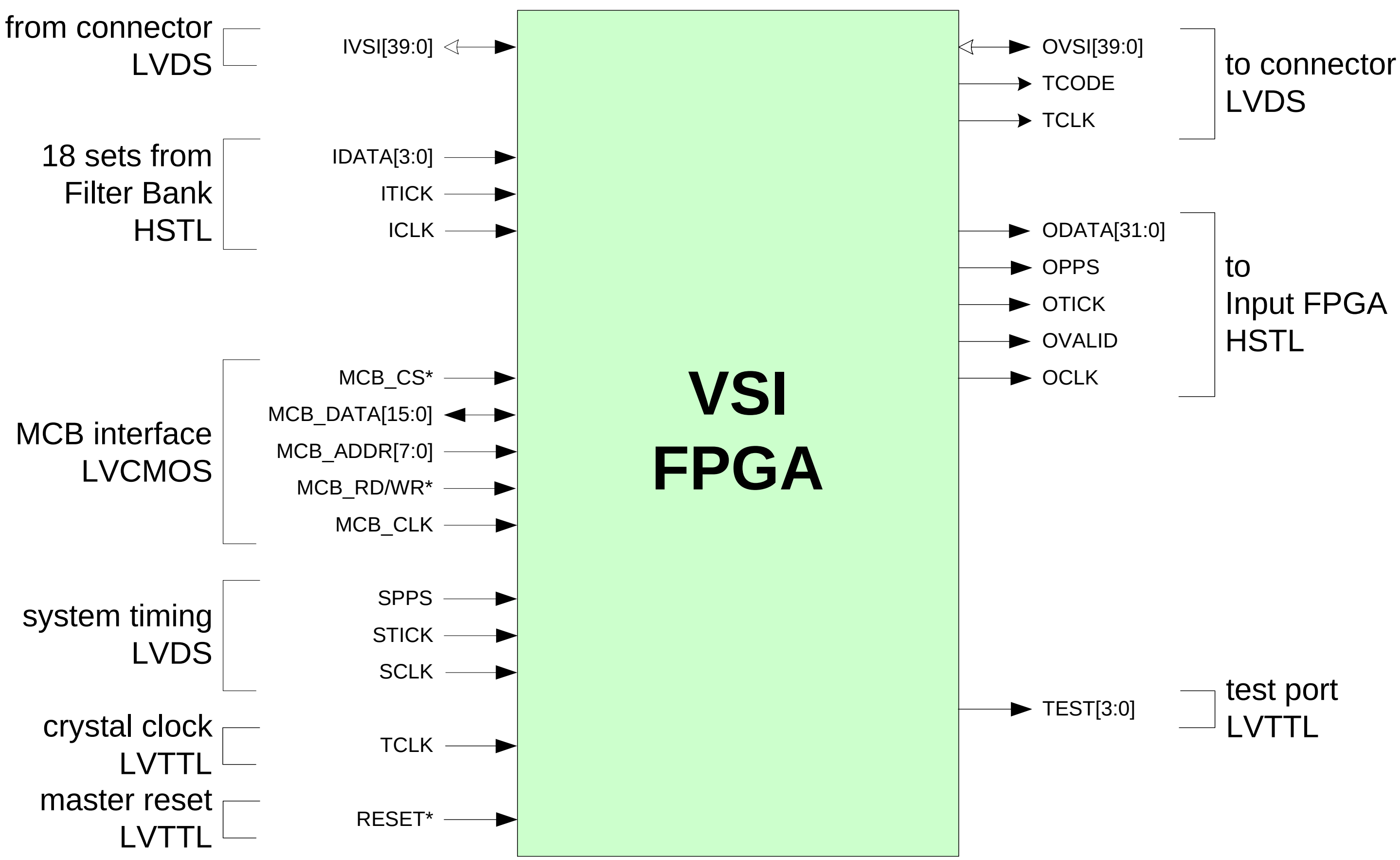


**Figure 2-2 Input/Output diagram of the VSI Test FPGA.**

A simplified input/output diagram of the VSI FPGA is shown above. The JTAG interface and configuration interface is not shown.

Each VSI FPGA sends and receives 40 LVDS pairs to and from the Station Board HM connector. In addition, each VSI FPGA receives 4-bit data, tick and 128 MHz clock from each of the 18 Filter FPGAs in its Filter Bank and sends 32-bit data, tick, pps, valid and 128 MHz clock to the Input FPGA. For test purposes, a 64 MHz clock from a crystal oscillator is used to produce a 128 Mb/s coded time code and associated 64 MHz clock.

# 3 Requirements

The following is a list of filter FPGA requirements.

## 3.1 Functional Requirements

1. Implement the CRC checking scheme on the inputs from the Filter FPGAs.
2. Implement the CRC checking scheme on the outputs to the Input FPGA.
3. Implement a checking scheme for the PCB traces to the HM connector assuming a loop back cable on the outside of the connector.
4. Generate a time code for independent testing of the Station Board Timing FPGA according to ICD A25022N0090 using the 64 MHz Crystal Oscillator on the Station Board.

## 3.2 Performance Requirements

1. The VSI Test FPGA shall operate on the input sampled data and control signals from the Station Board Filter FPGAs with a clock rate of 256 MHz. The FPGA will take a 128 MHz input clock, perform double-edged sampling of the data and develop its own internal 256 MHz clock.
2. The VSI Test FPGA shall produce a 128 Mb/s time code and associated 64 MHz clock. The phase relationship between the code and the clock is not important.
3. The synchronous MCB interface shall be capable of operating with a clock that is neither frequency nor phase synchronous with the 128 MHz or 256 MHz data clock. The FPGA will support an MCB interface clock with a maximum rate of 33 MHz.
4. The power dissipation of the FPGA, running at 256 MHz shall not exceed 3 Watts; however, the goal for the maximum power dissipation is 2 Watts.

## 3.3 Environmental Requirements

1. The VSI FPGA will be surface mounted on the Station Board PCB. It is likely that a single large heat spreader/sink will cover most of the FPGAs including the VSI FPGAs. This monolithic heat sink will be required to keep the junction temperatures below 50 °C. The MTBF is reduced by a factor of about two for each 10 °C increase in the junction temperature.

2. The VSI FPGA must be packaged in a “flip-chip” (cavity down) package no larger than 35 mm on a side for board space and thermal considerations. A smaller package is desirable. The actual package is “flip-chip” 27 mm square.

3. The board will use forced-air cooling with a normal operating ambient temperature of 10-15 °C and with a maximum ambient temperature of 40 °C.

## 3.4 Interface Requirements

### *3.4.1 Master Reset*

- RESET* is the input low-true master reset signal.
- RESET* is LVTTL.

### *3.4.2 System Input Signals*

- SCLK is the system 128 MHz clock. This clock is derived on the Station Board from a 64 MHz that comes from the TIMECODE Generator Box (RFS Document AN25151N0000) using a crystal phase-locked loop. All FPGAs on the Station Board use SCLK in order to prevent the buildup of clock jitter. Input signals from the previous FPGA are delayed using CMIB controlled tapped delay lines in each IOB and then clocked in using a zero delay buffered 2X version of SCLK, namely SCLK_256. The amount of delay required is dependent on the length of PCB traces and will be constant for a specific FPGA on all boards.

- STICK is the system timing tick (10 millisecond period). It is used, along with a time interval counter, to help determine the best setting for the wide band input signal tapped delay line.

- All system input signals are 2.5V LVDS.

### *3.4.3 Test Input Clock*

- TCLK is the test 64 MHz clock. This clock is no longer used – the system clock is used. The Station Board generating the PPSCODE should be fed with an external clock.

### 3.4.4 VLBI Interface Signals

- IVSI are 40 LVDS pairs from the external VSI device and are terminated inside the VSI FPGA.

- OVSI are 40 LVDS pairs to the external VSI device.

### 3.4.5 Narrow Band Input signals

- IDATA, ITICK and ICLK come from each of the Filter FPGAs in one of the two Filter Banks on the Station Board. They are HSTL Class III terminated inside the VSI FPGA.

### 3.4.6 Narrow Band Output Signals

- ODATA, OPPS, OTICK and OVALID and OCLK are HSTL and are sent to the Input FPGA.

### 3.4.7 Test Time Code Output Signals

- TCODE and TCLK are LVDS outputs and are sent to the Timing FPGA via HM connector and external cable. Both these signals are produced from SCLK.

### 3.4.8 MCB Interface Signals

- MCB_ADDR[7:0] is the input 8-bit address bus for accessing internal Filter FPGA configuration, monitor and control registers.

- MCB_DATA[15:0] is the bi-directional 16-bit microprocessor data bus.

- MCB_CS* is the input low-true FPGA select that enables the MCB interface drivers.

- MCB_CLK is the input clock for the synchronous MCB interface. The phase and frequency of MCB_CLK is independent of SCLK.

- MCB_RD/WR* is the input read/write enable.

- All MCB signals are LVTTL.

### 3.4.9 Test Port

These four outputs can be attached to a number of internal signals TBD to provide a simple diagnostic capability.

### *3.4.10 System Interface Timing Requirements*

Shown below is the functional relative timing for the system input signals.

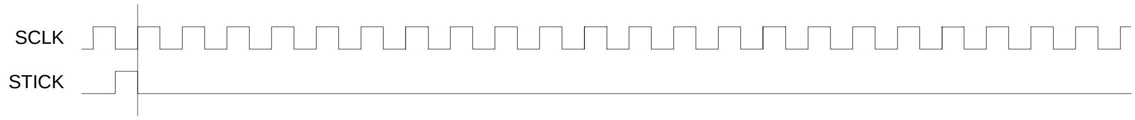


**Figure 3-1 System Input Functional Relative Timing**

The relative timing inside and outside the FPGA are the same as shown below. The left vertical line indicates the position of the internally generated rising clock edge that is used to clock the I/O registers. The actual position of the 256 MHz clock is at 0.75 of the bit cell. Changes in the value of the output data coincides with the falling edge of the tick, regardless of the decimation ratio.

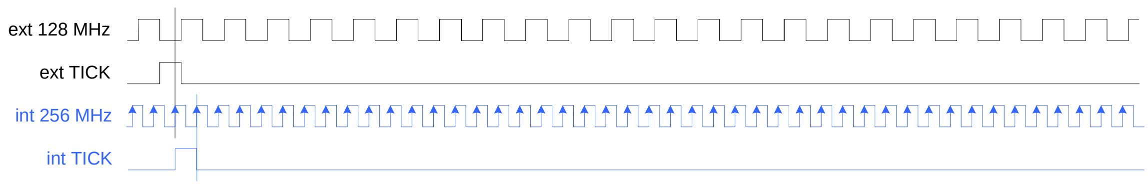


**Figure 3-2 External/Internal Functional Relative Timing**

### *3.4.11 VLBI Interface Timing Requirements*

These signals are for testing the Station Board PCB traces and connectors. Of the 40 LVDS pairs, 38 are internally generated data, one is a 10 millisecond tick and one is a 128 MHz clock.

### *3.4.12 Time Code Interface Timing Requirements*

The contents of the time code are given in ICD A25022N0090. The relative timing of the accompanying clock is not important but is given here for completeness.

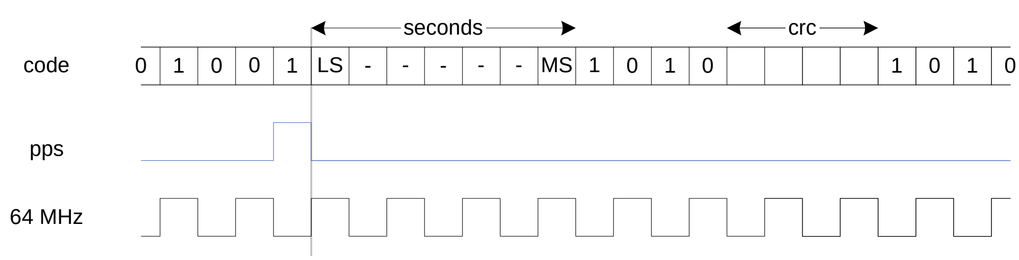


**Figure 3-3 Time Code Output Functional Relative Timing**

### 3.4.13 Narrow Band Data Interface Timing Requirements

Shown below is the functional relative timing for the narrow band input signals.

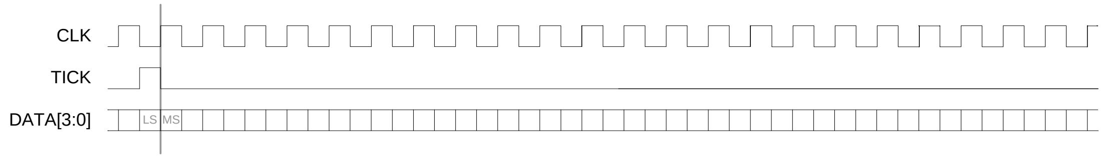


**Figure 3-4 Narrow Band Input Functional Relative Timing**

The DATA waveform shows the position of the LS and MS nibbles of 8-bit data relative to TICK.

### 3.4.14 MCB Interface Timing Requirements

The MCB (Monitor & Control Bus) interface allows a microprocessor (CMIB) to write to and read from the FPGA. Writing will be used to configure and control the hardware. Reading will be used to verify the configuration, receive status indicators and obtain monitor information and other data.

The single write cycle is shown in Figure 4-5. The microprocessor writes to the FPGA by putting the data on the MCB_DATA bus, the target register address on the MCB_ADDR bus, driving MCB_RD/WR* and MCB_CS* low after a rising edge of the MCB_CLK (**A**) and keeping the signals stable until after the next rising edge of the MCB_CLK (**B**). The Filter FPGA captures the information at this time (**B**).

The single read cycle is shown in Figure 4-6. The microprocessor reads from a FPGA by driving MCB_RD/WR* high, putting the desired register address on the MCB_ADDR bus and driving the corresponding MCB_CS* low after a rising edge of MCB_CLK. The address is valid at the next rising edge of MCB_CLK (**B**). The Filter FPGA places the requested data onto the MCB_DATA bus before the next rising edge of MCB_CLK (**C**) and holds it stable for as long as MCB_CS* is low. It should be noted that for the read case, the MCB_CLK from the PCMC through the MCB FPGA and into the Filter FPGA suffers a delay. For the data path back to the PCMC the delay is even worse (bus selectors in the MCB FPGA); therefore, the data should be placed onto the MCB_DATA bus as soon as possible.

The burst mode write is shown in Figure 4-7. It is similar to the single write in that data should be taken by the Filter FPGA at every rising clock edge for which MCB_CS* is low (**B**, **C** and **E**). The corresponding internal storage pointer should increment at this time. MCB_CS* may go high for any number of clock cycles any number of times during a long transfer (**D**).

The burst mode read is shown in Figure 4-8. The burst read is similar to the single read in that it takes two clock cycles for the first read (**C**) but it only needs one clock cycle for each subsequent read (**D** and **F**). The corresponding internal storage pointer should increment at **C**, **D** and **F**. MCB_CS* may go high for any number of clock cycles any number of times during a long transfer (**E**).

Setup time $t_{su}$ > 15 ns.

Clock to Output time $t_{co}$ < 13 ns.

Hold Time $t_{ho}$ > ? ns.

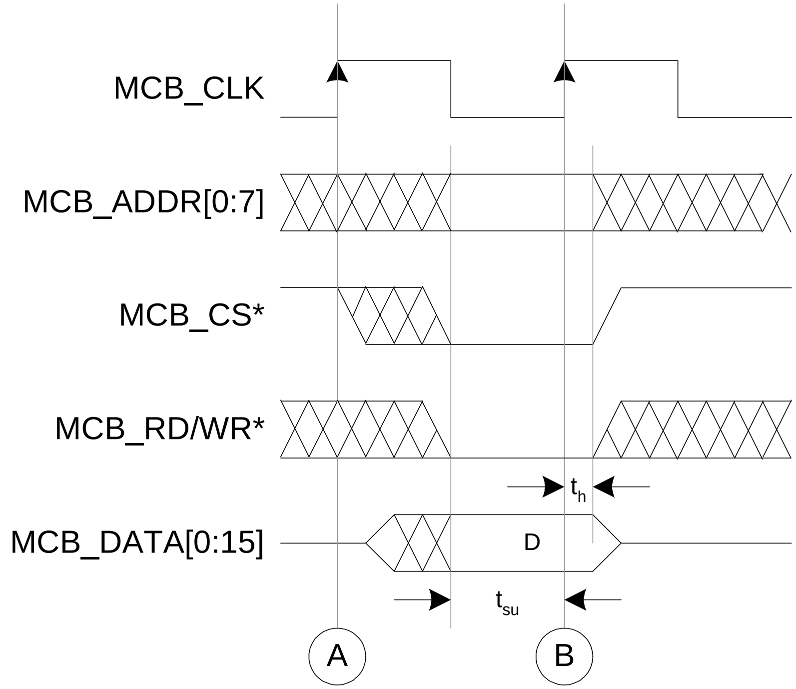


**Figure 3-5 MCB Interface Single WRITE Functional Relative Timing**

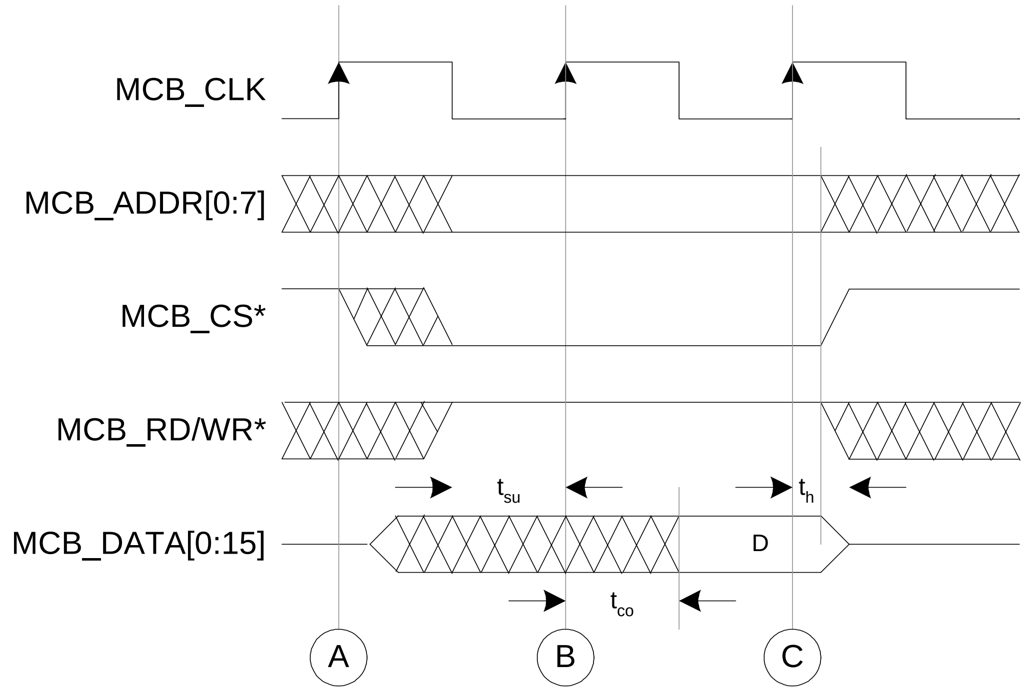


**Figure 3-6 MCB Interface Single READ Functional Relative Timing**

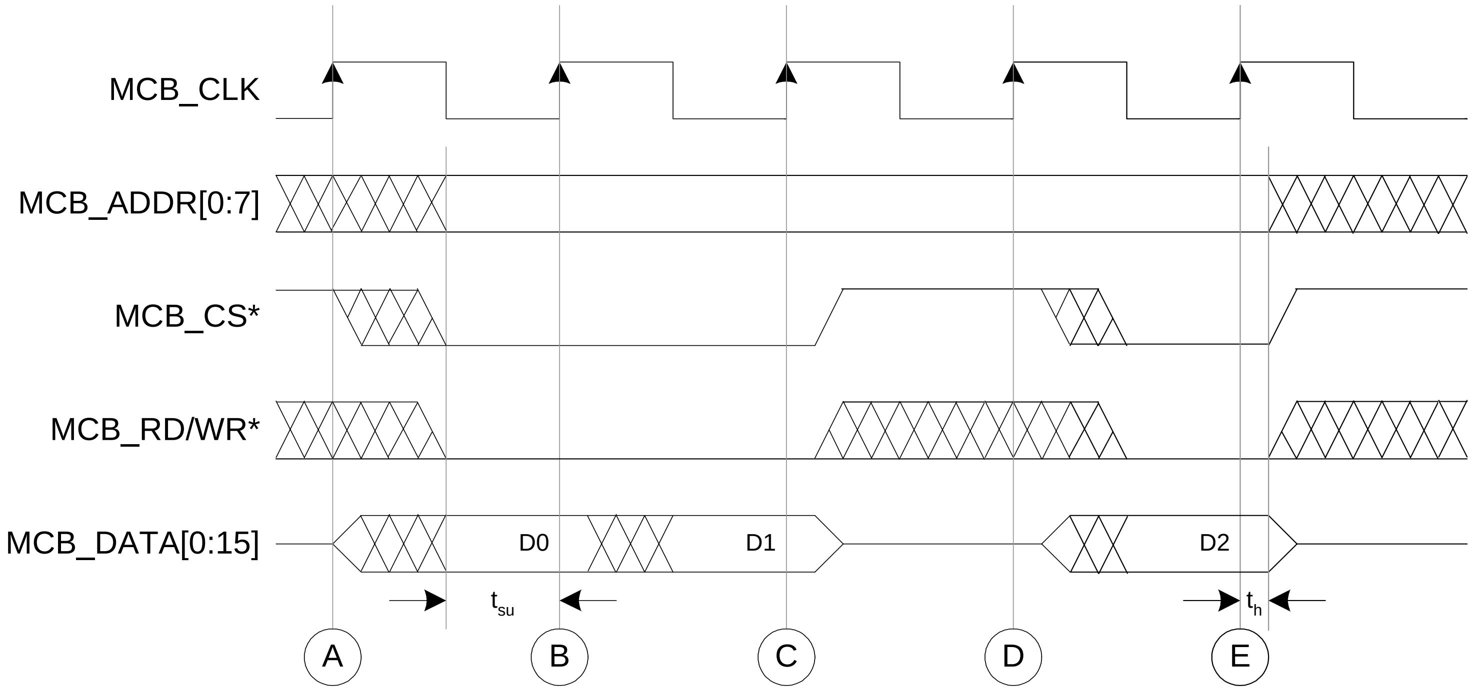


**Figure 3-7 MCB Interface Burst WRITE Functional Relative Timing**

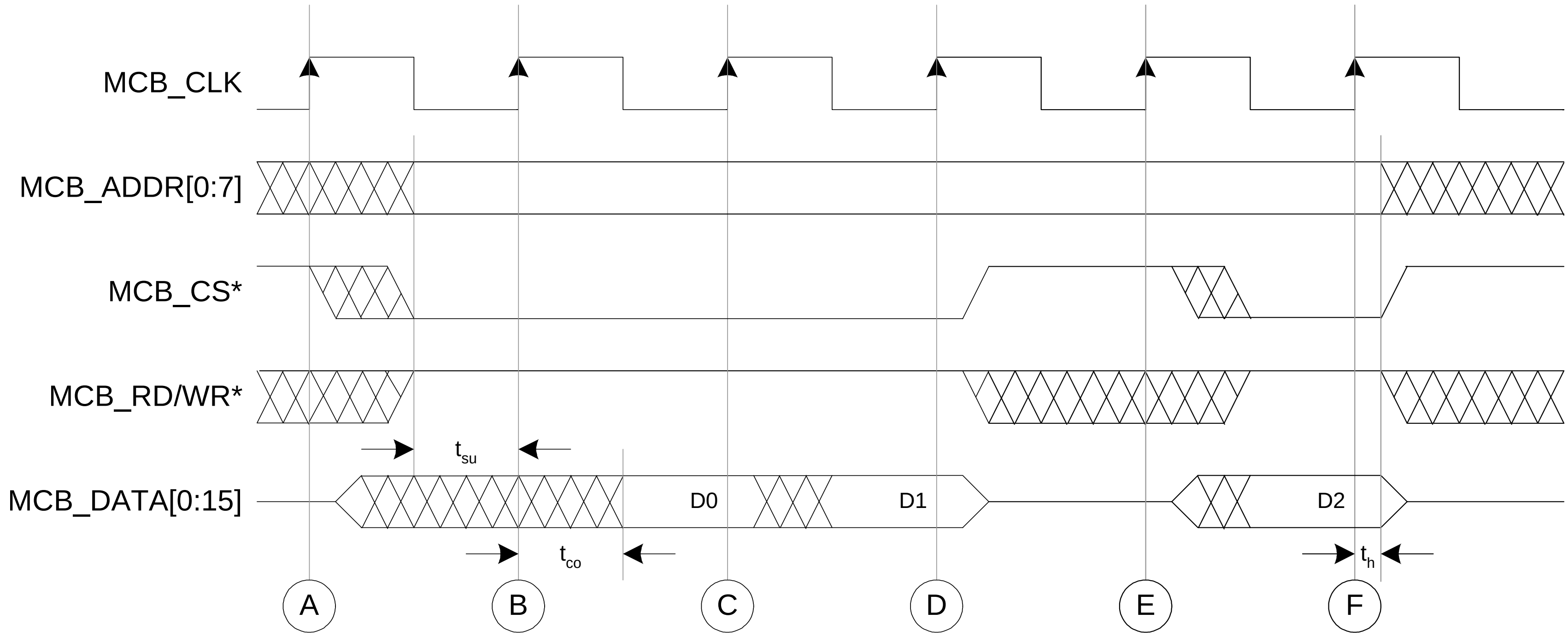


**Figure 3-8 MCB Interface Burst READ Functional Relative Timing**

The microprocessor will be interrupted on a version of STICK that has been delayed sufficiently to make sure that all FPGAs on the board have received their local version of the TICK. This allows a pipeline delay through the FPGAs on the board, including the tap registers in the filter FPGA.

Configuration information sent from the microprocessor to the VSI FPGA may take effect immediately and should only be sent when the output of the FPGA is irrelevant.

Monitor information, such as the time interval count and CRC values, read by the microprocessor from within the ISR will be the result of operations occurring between the previous two TICKS.

Status information, such as error bits, will show any occurrence of an error since the last read of that information. Another method would be to latch the status information on the TICK and clear the primary register. This method assumes that the status information is read every TICK by the ISR. Control information may include bits which, if set, cause a specified error to occur to allow testing of the reaction of the software to that error.

# 4 Hardware Functional Design

The VSI Test FPGA is divided into five blocks as shown below.

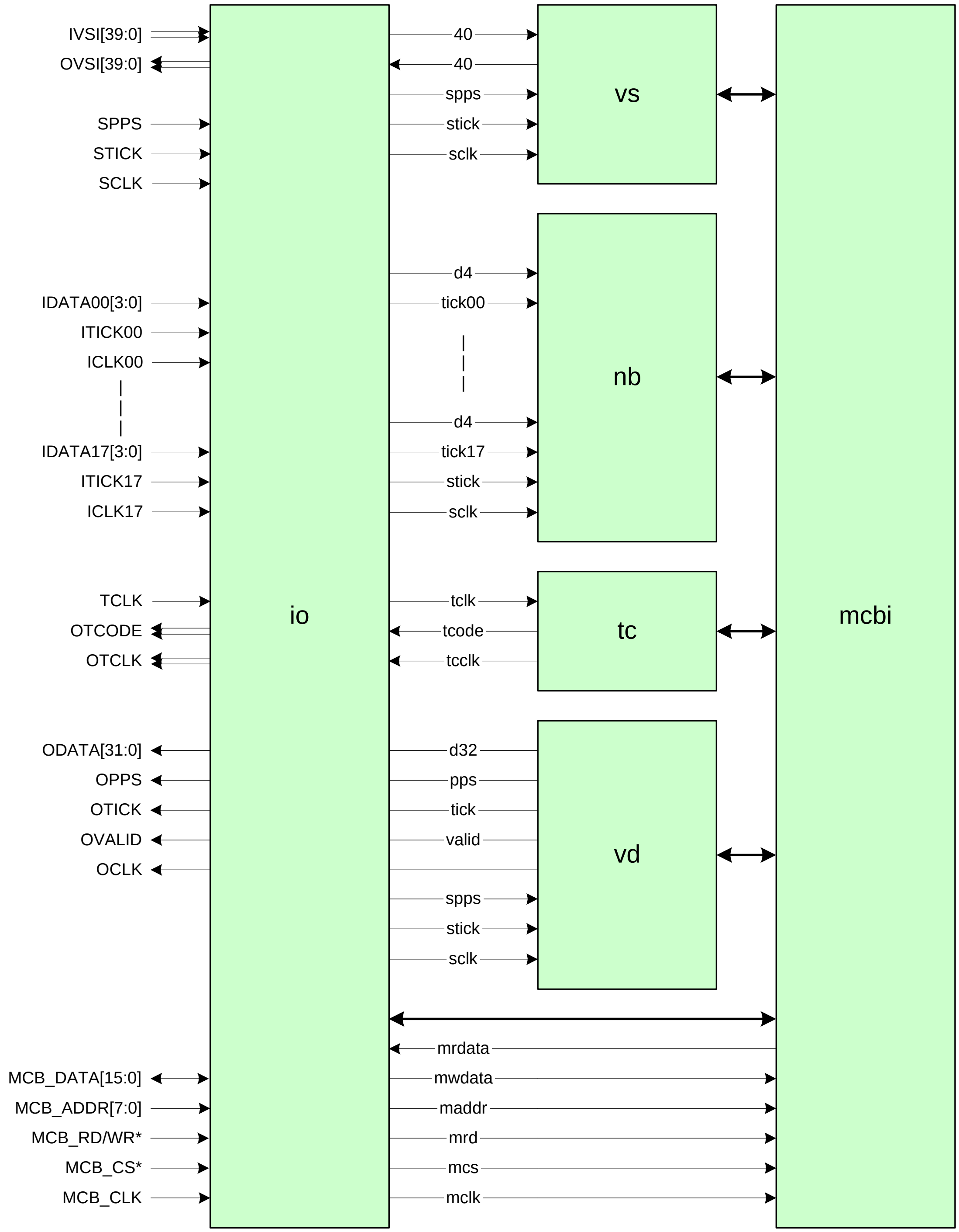


**Figure 4-1 VSI Test FPGA Block Diagram**

## 4.1 IO Block

The IO (Input/Output) block interfaces all the FPGA inputs and outputs to actual pins on the device. It contains the DLLs for re-generating the clocks and the logic required to reliably capture the input signals.

## 4.2 VS Block

The VS (VSI) block is meant for testing the VSI signals which are 40 LVDS pairs in and 40 LVDS pairs out. This is done by connecting a set of ten standard EVLA cable wafers between the input and output pins of each of the two HM VSI ports. The VS block generates 40 signals (38 data, one 10 millisecond tick and one 128 MHz clock) and compares them, one at a time, to the received data using the standard Station Board CRC scheme. The CMIB cycles through all 40 (38 data lines?) signals and checks that the VS status bit is zero (input CRC = output CRC).

## 4.3 NB Block

The NB (Narrow Band) block calculates a 4-bit CRC on the selected bit of all 18 Filter FPGA outputs. The CMIB reads the CRCs and compares them with those obtained from the corresponding Filter FPGA.

## 4.4 TC Block

The TC (Time Code) block generates the PPSCODE (Figure 3-3) once a second from the system clock (SCLK) and sends it to the VSI HM connector along with a 128 MHz clock. A single wafer cable would then transport it to the center HM connector and on to the Timing FPGA. If the PPSCODE outputs are fed to the PPSCODE inputs of the same board producing it, then the board should be connected to an external 128 MHz clock.

## 4.5 VD Block

The VD (VLBI Data) block generates data to send to the Input FPGA. It also calculates the 4-bit CRC for the selected data stream which the CMIB compares to the corresponding value from the Input FPGA.

## 4.6 MC Block

The MC (Monitor and Control) block interfaces the MCB to the FPGA. All the CMIB reads and writes go through this block.

# 5 Software Design Information

## 5.1 MCB Interface Register Map Summary

A summary of the registers for the VSI FPGA is shown below. Note that the number of bits reflects the actual hardware register but on read the upper bits in the register are sign extended or zero; therefore, no masking by the CMIB is necessary when reading the full 16-bit register.

| Address | Name | Dir | Bits | Description |
|---|---|---|---|---|
| | | | | |
| **CM** | | | | **Common** |
| 0x00 | CM_STS | R/W | 15:0 | Status Register |
| 0x01 | CM_CFG | R/W | 15:0 | Configuration Register |
| 0x02 | CM_CTL | R/W | 15:0 | Control Register |
| 0x03 | CM_ERR | R/W | 15:0 | Error Register |
| 0x04 | CM_DEF | R/W | 15:0 | Default Register |
| 0x05 | CM_DID | R | 15:0 | Design ID |
| 0x06 | CM_TST0 | R/W | 7:0 | Address of signal to connect to test port 0 |
| 0x07 | CM_TST1 | R/W | 7:0 | Address of signal to connect to test port 1 |
| 0x08 | CM_TST2 | R/W | 7:0 | Address of signal to connect to test port 2 |
| 0x09 | CM_TST3 | R/W | 7:0 | Address of signal to connect to test port 3 |

| Address | Name | Dir | Bits | Description |
|---|---|---|---|---|
| **IO** | | | | **Input/Output** |
| 0x10 | IO_NSEL0 | R/W | 15:0 | Select DDR clock edge for NB inputs [15:0] |
| 0x11 | IO_NSEL1 | R/W | 1:0 | Select DDR clock edge for NB inputs [17:16] |
| 0x12 | IO_VINT1 | R | 5:0 | MS VSI time interval count |
| 0x13 | IO_VINT0 | R | 15:0 | LS VSI time interval count |
| 0x14 | IO_STDLY | R/W | 15:0 | System Tick Delay for IO_TINT |
| 0x15-1B | | | | Not used |
| 0x1C | IO_ICER0 | R | 15:0 | Input data clock error for inputs [15:0] |
| 0x1D | IO_ICER1 | R | 1:0 | Input data clock error for inputs [17:16] |
| 0x1E | IO_TSEL | R/W | 4:0 | Input to select for time interval counter |
| 0x1F | IO_TINT1 | R | 5:0 | MS time interval count |
| 0x20 | IO_TINT0 | R | 15:0 | LS time interval count |
| **VS** | | | | **VSI loop back testing** |
| 0x21 | VS_VSEL | R/W | 5:0 | Select bit stream for CRC checking and read CRCs |
| **NB** | | | | **Narrow band CRC checking** |
| 0x22 | NB_DSEL | R/W | 1:0 | Select bit stream for CRC calculation |
| 0x23 | NB_CRC0 | R/W | 15:0 | 4-bit CRC for inputs 0 to 3 |
| 0x24 | NB_CRC1 | R/W | 15:0 | 4-bit CRC for inputs 4 to 7 |
| 0x25 | NB_CRC2 | R/W | 15:0 | 4-bit CRC for inputs 8 to 11 |
| 0x26 | NB_CRC3 | R/W | 15:0 | 4-bit CRC for inputs 12 to 15 |
| 0x27 | NB_CRC4 | R/W | 7:0 | 4-bit CRC for inputs 16 and 17 |

| Address | Name | Dir | Bits | Description |
|---|---|---|---|---|
| **TC** | | | | **Test time code generation** |
| 0x28 | TC_TLEN1 | R/W | 4:0 | MS number of 128 MHz clocks per tick minus one |
| 0x29 | TC_TLEN0 | R/W | 15:0 | LS number of 128 MHz clocks per tick minus one |
| 0x2A | TC_PLEN | R/W | 6:0 | Number of ticks per pps minus one |
| **VD** | | | | **VLBI data CRC checking** |
| 0x2B | VD_DSEL | R/W | 5:0 | Select bit stream for CRC calculation |
| 0x2C | VD_CRC | R/W | 3:0 | 4-bit CRC |
| **Test** | | | | **VLBI data CRC checking** |
| 0x30 | VD_ESEL | R/W | 5:0 | Error select for VLBI output CRC. |
| 0x31 | VS_ESEL | R/W | 6:0 | Error select for VSI output CRC. |
| 0x32 | CM_SEED | R/W | 15:0 | Seed for all pseudo random bit stream generators. |
| 0x33 | TC_HOPC | R/W | 7:0 | Hop count for test PPSCODE generator. |
| 0x34 | TC_SECS | R/W | 5:0 | Set seconds in test PPSCODE generator. |

**Table 5-1 Register Map of VSI Test FPGA**

## 5.2 Input Clock Edge Selection

Signals coming into the VSI FPGA have to be time aligned with the internal system clock due to different PCB trace lengths. The alignment is done using DDR input which clocks data in on both the positive and negative going edges of the internal 256 MHz system clock derived from the external 128 MHz system clock. The CMIB can set which edge is actually used by writing to registers CM_CFG, IO_NSEL0 and IO_NSEL1. It is assumed that all signals on the same bus will need the same clock edge for reliable clocking because the trace lengths for a given bus are controlled on the PCB. The settings will be determined during prototype testing using the CRC checking feature and should be the same for all Station Boards.

# 6 Detailed Register Description

The following is a detailed description of the VSI FPGA register set for each block of the design. The number of bits reflects the actual hardware register but on read the upper bits in the register are sign extended or zero; therefore, no masking by the CMIB is necessary when reading the full 16-bit register.

## 6.1 COMMON

The following registers are used by all blocks for status, configuration, control, error, testing and design identifier. The status, configuration, control and error registers are collections of single bits gathered together for simplicity.

| Address | Name | Dir | Bits | Description |
|---|---|---|---|---|
| 0x00 | CM_STS | R/W | 15:0 | Status Register. The status register indicates various error conditions in the Filter FPGA as shown in Table 7-1. Each bit has a separate meaning. The status bits are saved and the working register cleared on the tick; therefore, the ISR should read the status register every interrupt to avoid the loss of an error indicator. The register should be all zero if there are no errors. To create errors for software test purposes, write bits to the register. The original status bits will be inverted wherever the written bits are 1. |
| 0x01 | CM_CFG | R/W | 15:0 | Configuration Register. This register is composed of individual bits that are normally set during configuration and then left alone during operation. See Table 7-2. |
| 0x02 | CM_CTL | R/W | 15:0 | Control Register. This register is composed of individual bits that can be changed during operation. See Table 7-3. |
| 0x03 | CM_ERR | R/W | 2:0 | Error Register. This register should always be zero. If not, one of the errors in Table 7-4 has occurred since it was last cleared. To clear the register, write zero to it. To create errors, commit an error or write a non-zero value to the register. |

| | | | | |
|---|---|---|---|---|
| 0x04 | CM_DEF | R/W | 15:0 | Default Register. This register will contain the last attempt to write to a non-existent or read-only register and will be returned if an attempt is made to read from a non-existent register. It can also used as a test register. |
| 0x05 | CM_DID | R | 15:0 | Design identifier. The bits are divided into design, revision and version. Since the Filter FPGA is programmable, different designs are possible. |
| 0x06 | CM_TST0 | R/W | 7:0 | Address of signal to connect to test port 0 |
| 0x07 | CM_TST1 | R/W | 7:0 | Address of signal to connect to test port 1 |
| 0x08 | CM_TST2 | R/W | 7:0 | Address of signal to connect to test port 2 |
| 0x09 | CM_TST3 | R/W | 7:0 | Address of signal to connect to test port 3 |

**Table 6-1 Common Registers**

The meaning of bits in the status registers is shown below.

| Bit | Block | Meaning (1 = error) |
|---|---|---|
| 0 | | No longer used |
| 1 | IO | 1 => SPPS error (not aligned with STICK) |
| 2 | IO | 1 => SPPS error (width) |
| 3 | IO | 1 => STICK error (width) |
| 4 | IO | 1 => SCLK not locked |
| 5 | IO | 1 => TCLK not locked |
| 6 | VS | 1 => ICRC and OCRC of the selected VSI bit are not the same. |
| 7 | VS | 1 => selected VSI bit > 39. |
| 8 | IO | 1 => STICK with edge + matches STICK with edge - (test only). |
| 9 | IO | 1 => STICK with chosen edge leads STICK not chosen (test only). |
| 10 | IO | 1 => DCM phase shift is complete (test only). |
| 11 | IO | 1 => DCM phase shift overflow or underflow (test only). |

**Table 6-2 Status Bit Definitions for VSI Test FPGA**

The meaning of bits in the configuration registers is shown below.

| Bit | Block | Meaning (default = 0) |
|---|---|---|
| 0 | | Not used |
| 1 | IO | Select the DDR clock edge for capturing STICK and SPPS. |
| 2 | IO | Select the DDR clock edge for capturing the VSI signals. |
| 3 | TC | 0 => normal, 1 => enable test PPSCODE data and clock output. |
| 4 | TC | 0 => normal, 1 => force CRC error in PPSCODE. |

**Table 6-3 Configuration Bit Definitions for VSI Test FPGA**

The meaning of bits in the control registers is shown below.

| Bit | Block | Meaning |
|---|---|---|
| 0 | IO | 1 => software reset, 0 => don't. Momentary reset. |
| 1 | IO | 1 => disable clocking, 0 => don't. This bit can be used to disable clocking in order to reduce heat production. |
| 2 | IO | 1 => increment DCM phase, 0 => decrement DCM phase |
| 3 | IO | 1 => shift DCM phase (must return to zero before another shift) |
| 15 | IO | 1 => reset PLL, 0 => don't. |

**Table 6-4 Control Bit Definitions for VSI Test FPGA**

The meaning of bits in the error registers is shown below.

| Bit | Meaning |
|---|---|
| 0 | 1=> attempt to write to a read-only register |
| 1 | 1=> attempt to write to a non-existent register |
| 2 | 1 => attempt to read from a non-existent register |

**Table 6-5 Error Bit Definitions for VSI Test FPGA**

| ID Part | Bits | CM_DID |
|---|---|---|
| Design | 8 | [15:8] |
| Version | 4 | [7:4] |
| Revision | 4 | [3:0] |

**Table 6-6 Design ID Definition**

## 6.2 INPUT/OUTPUT

| Address | Name | Dir | Bits | Description |
|---|---|---|---|---|
| 0x10 | IO_NSEL0 | R/W | 15:0 | Select DDR clock edge for NB inputs [15:0]. |
| 0x11 | IO_NSEL1 | R/W | 1:0 | Select DDR clock edge for NB inputs [17:16] |
| 0x12 | IO_VINT1 | R/(W) | 15:14<br>5:0 | 00=>dtick>stick, 01=>dtick,10=>stick, 11=>stick>dtick<br>MS VSI time interval count. |
| 0x13 | IO_VINT0 | R | 15:0 | LS VSI time interval count |
| 0x14 | IO_STDLY | R/W | 15:0 | System Tick Delay for IO_TINT. Can be set to make IO_TINT small and positive. |
| 0x15-1B | | | | Not used. |
| 0x1C | IO_ICER0 | R/W | 15:0 | Input data clock error for inputs 0 to 15. The error for input 0 is in bit 0. |
| 0x1D | IO_ICER1 | R/W | 1:0 | Input data clock error for inputs 16 to 17. The error for input 16 is in bit 0. |
| 0x1E | IO_TSEL | R/W | 4:0 | Input to select for time interval counter. The counter is started by the selected tick and stopped by the system tick. Values 0 to 17 select input ticks 0 to 17. Any other value measures the VSI tick. The selected tick can be changed in the ISR and takes effect at the next tick. |
| 0x1F | IO_TINT1 | R/(W) | 15:14<br>5:0 | 00=>dtick>stick, 01=>dtick,10=>stick, 11=>stick>dtick<br>MS time interval count. |
| 0x20 | IO_TINT0 | R | 15:0 | LS time interval count |

**Table 6-7 IO Registers**

## 6.3 VSI LOOP BACK

| Address | Name | Dir | Bits | Description |
|---|---|---|---|---|
| 0x21 | VS_DSEL | R/W | 5:0 | Select bit for CRC calculation. It is used to select which of the 40 bits to check. This register is set by the ISR to take effect on the next tick. For test purposes the input CRC and the output CRC are in the bits [15:12] and [11:8] respectively on read. |

**Table 6-8 VS Registers**

## 6.4 NARROW BAND

| Address | Name | Dir | Bits | Description |
|---|---|---|---|---|
| 0x22 | NB_DSEL | R/W | 2:0 | Select bit for CRC calculation. It is used to select which of the 4 bits to check. This register is set by the ISR to take effect on the next tick. If NB_DSEL[2] = 1, SIND is substituted for DATA[0]. |
| 0x23 | NB_CRC0 | R/W | 15:0 | 4-bit CRC for inputs 0 to 3. It is used to check correct data transmission between FPGAs. The CMIB sets the bit in the last FPGA to be the same as the bit in this FPGA and checks that the CRCs are the same. This register is read by the ISR and is the CRC for the last interrupt interval. The CRC for input 0 is in [3:0]. |
| 0x24 | NB_CRC1 | R/W | 15:0 | 4-bit CRC for inputs 4 to 7 (as above). The CRC for input 4 is in [3:0]. |
| 0x25 | NB_CRC2 | R/W | 15:0 | 4-bit CRC for inputs 8 to 11 (as above). The CRC for input 8 is in [3:0]. |
| 0x26 | NB_CRC3 | R/W | 15:0 | 4-bit CRC for inputs 12 to 15 (as above). The CRC for input 12 is in [3:0]. |
| 0x27 | NB_CRC4 | R/W | 7:0 | 4-bit CRC for inputs 16 and 17 (as above). The CRC for input 16 is in [3:0]. |

**Table 6-9 NB Registers**

### 6.5 TIME CODE

| Address | Name | Dir | Bits | Description |
|---|---|---|---|---|
| 0x28 | TC_TLEN1 | R/W | 4:0 | MS number of 128 MHz clocks per tick minus one. This quantity is used for simulation (to shorten the simulation time for checking the time code) but must be set correctly here. The correct value is 1280000-1 = 0x13(87FF) |
| 0x29 | TC_TLEN0 | R/W | 15:0 | LS number of 128 MHz clocks per tick minus one. This register should be set to 1280000-1 = 0x(13)87FF. |
| 0x2A | TC_PLEN | R/W | 6:0 | Number of ticks per pps minus one. This quantity is used for simulation (to shorten the simulation time for checking the time code) but must be set correctly here. The correct value is 100-1 = 0x63 |

**Table 6-10 TC Registers**

### 6.6 VLBI DATA

| Address | Name | Dir | Bits | Description |
|---|---|---|---|---|
| 0x2B | VD_DSEL | R/W | 5:0 | Select bit for CRC calculation. It is used to select which of the 32 bits to check. This register is set by the ISR to take effect on the next tick. If VD_DSEL[5] = 1, valid and dclk are substituted for wires 0 and 1 respectively. |
| 0x2C | VD_CRC | R | 3:0 | 4-bit CRC for the selected bit. It is used to check correct data transmission between FPGAs. The CMIB sets the bit in the next FPGA to be the same as the bit in this FPGA and checks that the CRCs are the same. This register is read by the ISR and is the CRC for the last interrupt interval. |

**Table 6-11 VD Registers**

## 6.7 TEST ONLY

| Address | Name | Dir | Bits | Description |
|---|---|---|---|---|
| 0x30 | VD_ESEL | R/W | 5:0 | Error select for VLBI output CRC. If bit 5 is set to 1, bits [4:0] will cause an inverted CRC whenever VD_DSEL is set to these bits. This can be used to create CRC errors on a specific wire to test the software. |
| 0x31 | VS_ESEL | R/W | 6:0 | Error select for VSI output CRC. If bit 6 is set to 1, bits [5:0] will cause an inverted CRC whenever VS_DSEL is set to these bits. This can be used to create CRC errors on a specific wire to test the software. |
| 0x32 | CM_SEED | R/W | 15:0 | Seed for all pseudo random bit stream generators. This is present so that the two VSI chips can be made to generate different data. Default value is 0x1357. |
| 0x33 | TC_HOPC | R/W | 7:0 | The hop count written here appears in the test PPSCODE. |

**Table 6-11 Test Registers**

# 7 Pinouts, Pin Location and Programming Notes

## 7.1 Pinout by signal name

Note: UNUSED and NC pins have been removed.

```
Release 10.1.03 - par K.39 (nt)
Copyright (c) 1995-2008 Xilinx, Inc.  All rights reserved.

Tue Mar 02 16:38:16 2010

INPUT FILE:       vsi_top_map.ncd
OUTPUT FILE:      vsi_top_pad.txt
PART TYPE:        xc4vsx35
SPEED GRADE:      -10
PACKAGE:          ff668
```

| Pin | Signal Name | Pin Usage | Pin Name | Direction | IO Standard | IO Bank |
|---|---|---|---|---|---|---|
| W2 | clk_G01 | IOB | IO_L1P_8 | INPUT | HSTL_III_DCI | 8 |
| R4 | clk_G02 | IOB | IO_L20P_10 | INPUT | HSTL_III_DCI | 10 |
| L8 | clk_G03 | IOB | IO_L9N_CC_LC_10 | INPUT | HSTL_III_DCI | 10 |
| G10 | clk_G04 | IOB | IO_L9P_CC_LC_6 | INPUT | HSTL_III_DCI | 6 |
| C7 | clk_G05 | IOB | IO_L11N_6 | INPUT | HSTL_III_DCI | 6 |
| D2 | clk_G06 | IOB | IO_L25P_CC_LC_6 | INPUT | HSTL_III_DCI | 6 |
| M8 | clk_G07 | IOB | IO_L9P_CC_LC_10 | INPUT | HSTL_III_DCI | 10 |
| R7 | clk_G08 | IOB | IO_L25N_CC_LC_10 | INPUT | HSTL_III_DCI | 10 |
| Y1 | clk_G09 | IOB | IO_L6N_8 | INPUT | HSTL_III_DCI | 8 |
| Y6 | clk_G10 | IOB | IO_L9P_CC_LC_8 | INPUT | HSTL_III_DCI | 8 |
| U4 | clk_G11 | IOB | IO_L29N_10 | INPUT | HSTL_III_DCI | 10 |

| | | | | | | |
|---|---|---|---|---|---|---|
| M2 | clk_G12 | IOB | IO_L11P_10 | INPUT | HSTL_III_DCI | 10 |
| F3 | clk_G13 | IOB | IO_L27N_6 | INPUT | HSTL_III_DCI | 6 |
| C10 | clk_G14 | IOB | IO_L1N_6 | INPUT | HSTL_III_DCI | 6 |
| D10 | clk_G15 | IOB | IO_L1P_6 | INPUT | HSTL_III_DCI | 6 |
| G2 | clk_G16 | IOB | IO_L30P_6 | INPUT | HSTL_III_DCI | 6 |
| P7 | clk_G17 | IOB | IO_L21P_10 | INPUT | HSTL_III_DCI | 10 |
| U7 | clk_G18 | IOB | IO_L31N_10 | INPUT | HSTL_III_DCI | 10 |
| W7 | data_G01<0> | IOB | IO_L3P_8 | INPUT | HSTL_III_DCI | 8 |
| W6 | data_G01<1> | IOB | IO_L5P_8 | INPUT | HSTL_III_DCI | 8 |
| W5 | data_G01<2> | IOB | IO_L5N_8 | INPUT | HSTL_III_DCI | 8 |
| W4 | data_G01<3> | IOB | IO_L4P_8 | INPUT | HSTL_III_DCI | 8 |
| R2 | data_G02<0> | IOB | IO_L22P_10 | INPUT | HSTL_III_DCI | 10 |
| R1 | data_G02<1> | IOB | IO_L22N_10 | INPUT | HSTL_III_DCI | 10 |
| P2 | data_G02<2> | IOB | IO_L16N_10 | INPUT | HSTL_III_DCI | 10 |
| P3 | data_G02<3> | IOB | IO_L16P_10 | INPUT | HSTL_III_DCI | 10 |
| L7 | data_G03<0> | IOB | IO_L5P_10 | INPUT | HSTL_III_DCI | 10 |
| L6 | data_G03<1> | IOB | IO_L5N_10 | INPUT | HSTL_III_DCI | 10 |
| L3 | data_G03<2> | IOB | IO_L8N_CC_LC_10 | INPUT | HSTL_III_DCI | 10 |
| K7 | data_G03<3> | IOB | IO_L3P_10 | INPUT | HSTL_III_DCI | 10 |
| G9 | data_G04<0> | IOB | IO_L9N_CC_LC_6 | INPUT | HSTL_III_DCI | 6 |
| G8 | data_G04<1> | IOB | IO_L10N_6 | INPUT | HSTL_III_DCI | 6 |
| G7 | data_G04<2> | IOB | IO_L19N_6 | INPUT | HSTL_III_DCI | 6 |
| F7 | data_G04<3> | IOB | IO_L19P_6 | INPUT | HSTL_III_DCI | 6 |
| A9 | data_G05<0> | IOB | IO_L13P_6 | INPUT | HSTL_III_DCI | 6 |
| A8 | data_G05<1> | IOB | IO_L3P_6 | INPUT | HSTL_III_DCI | 6 |
| A7 | data_G05<2> | IOB | IO_L3N_6 | INPUT | HSTL_III_DCI | 6 |
| B7 | data_G05<3> | IOB | IO_L11P_6 | INPUT | HSTL_III_DCI | 6 |
| C5 | data_G06<0> | IOB | IO_L12P_6 | INPUT | HSTL_III_DCI | 6 |
| D4 | data_G06<1> | IOB | IO_L16N_6 | INPUT | HSTL_III_DCI | 6 |
| D3 | data_G06<2> | IOB | IO_L22P_6 | INPUT | HSTL_III_DCI | 6 |
| D1 | data_G06<3> | IOB | IO_L25N_CC_LC_6 | INPUT | HSTL_III_DCI | 6 |
| M6 | data_G07<0> | IOB | IO_L13P_10 | INPUT | HSTL_III_DCI | 10 |
| M5 | data_G07<1> | IOB | IO_L13N_10 | INPUT | HSTL_III_DCI | 10 |
| M4 | data_G07<2> | IOB | IO_L12P_10 | INPUT | HSTL_III_DCI | 10 |

| | | | | | | |
|---|---|---|---|---|---|---|
| L4 | data_G07<3> | IOB | IO_L8P_CC_LC_10 | INPUT | HSTL_III_DCI | 10 |
| T8 | data_G08<0> | IOB | IO_L31P_10 | INPUT | HSTL_III_DCI | 10 |
| T7 | data_G08<1> | IOB | IO_L27P_10 | INPUT | HSTL_III_DCI | 10 |
| T6 | data_G08<2> | IOB | IO_L27N_10 | INPUT | HSTL_III_DCI | 10 |
| T4 | data_G08<3> | IOB | IO_L26P_10 | INPUT | HSTL_III_DCI | 10 |
| AA4 | data_G09<0> | IOB | IO_L7P_8 | INPUT | HSTL_III_DCI | 8 |
| AA3 | data_G09<1> | IOB | IO_L7N_8 | INPUT | HSTL_III_DCI | 8 |
| Y4 | data_G09<2> | IOB | IO_L8P_CC_LC_8 | INPUT | HSTL_III_DCI | 8 |
| Y3 | data_G09<3> | IOB | IO_L8N_CC_LC_8 | INPUT | HSTL_III_DCI | 8 |
| AA9 | data_G10<0> | IOB | IO_L21P_8 | INPUT | HSTL_III_DCI | 8 |
| Y9 | data_G10<1> | IOB | IO_L21N_8 | INPUT | HSTL_III_DCI | 8 |
| Y8 | data_G10<2> | IOB | IO_L26N_8 | INPUT | HSTL_III_DCI | 8 |
| AA7 | data_G10<3> | IOB | IO_L20P_8 | INPUT | HSTL_III_DCI | 8 |
| V2 | data_G11<0> | IOB | IO_L30P_10 | INPUT | HSTL_III_DCI | 10 |
| V1 | data_G11<1> | IOB | IO_L30N_10 | INPUT | HSTL_III_DCI | 10 |
| U3 | data_G11<2> | IOB | IO_L28P_10 | INPUT | HSTL_III_DCI | 10 |
| U1 | data_G11<3> | IOB | IO_L24P_CC_LC_10 | INPUT | HSTL_III_DCI | 10 |
| N5 | data_G12<0> | IOB | IO_L15P_10 | INPUT | HSTL_III_DCI | 10 |
| N4 | data_G12<1> | IOB | IO_L15N_10 | INPUT | HSTL_III_DCI | 10 |
| N3 | data_G12<2> | IOB | IO_L14P_10 | INPUT | HSTL_III_DCI | 10 |
| N2 | data_G12<3> | IOB | IO_L14N_10 | INPUT | HSTL_III_DCI | 10 |
| F4 | data_G13<0> | IOB | IO_L27P_6 | INPUT | HSTL_III_DCI | 6 |
| E5 | data_G13<1> | IOB | IO_L18N_6 | INPUT | HSTL_III_DCI | 6 |
| E4 | data_G13<2> | IOB | IO_L22N_6 | INPUT | HSTL_III_DCI | 6 |
| E3 | data_G13<3> | IOB | IO_L24P_CC_LC_6 | INPUT | HSTL_III_DCI | 6 |
| D9 | data_G14<0> | IOB | IO_L2P_6 | INPUT | HSTL_III_DCI | 6 |
| D8 | data_G14<1> | IOB | IO_L4P_6 | INPUT | HSTL_III_DCI | 6 |
| D6 | data_G14<2> | IOB | IO_L17N_6 | INPUT | HSTL_III_DCI | 6 |
| E6 | data_G14<3> | IOB | IO_L18P_6 | INPUT | HSTL_III_DCI | 6 |
| F9 | data_G15<0> | IOB | IO_L7N_6 | INPUT | HSTL_III_DCI | 6 |
| E10 | data_G15<1> | IOB | IO_L5N_6 | INPUT | HSTL_III_DCI | 6 |
| E9 | data_G15<2> | IOB | IO_L7P_6 | INPUT | HSTL_III_DCI | 6 |
| E7 | data_G15<3> | IOB | IO_L17P_6 | INPUT | HSTL_III_DCI | 6 |
| G1 | data_G16<0> | IOB | IO_L30N_6 | INPUT | HSTL_III_DCI | 6 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| F1 | data_G16<1> | IOB | IO_L26N_6 | INPUT | HSTL_III_DCI | 6 | |
| E1 | data_G16<2> | IOB | IO_L26P_6 | INPUT | HSTL_III_DCI | 6 | |
| H2 | data_G16<3> | IOB | IO_L32P_6 | INPUT | HSTL_III_DCI | 6 | |
| P6 | data_G17<0> | IOB | IO_L21N_10 | INPUT | HSTL_III_DCI | 10 | |
| P5 | data_G17<1> | IOB | IO_L18P_10 | INPUT | HSTL_III_DCI | 10 | |
| N8 | data_G17<2> | IOB | IO_L19N_10 | INPUT | HSTL_III_DCI | 10 | |
| N7 | data_G17<3> | IOB | IO_L17P_10 | INPUT | HSTL_III_DCI | 10 | |
| V7 | data_G18<0> | IOB | IO_L3N_8 | INPUT | HSTL_III_DCI | 8 | |
| V6 | data_G18<1> | IOB | IO_L2P_8 | INPUT | HSTL_III_DCI | 8 | |
| V5 | data_G18<2> | IOB | IO_L2N_8 | INPUT | HSTL_III_DCI | 8 | |
| V4 | data_G18<3> | IOB | IO_L29P_10 | INPUT | HSTL_III_DCI | 10 | |
| AA13 | mcb_addr_p<0> | IOB | IO_L4N_D8_VREF_LC_2 | INPUT | LVCMOS25 | 2 | |
| AB13 | mcb_addr_p<1> | IOB | IO_L4P_D9_LC_2 | INPUT | LVCMOS25 | 2 | |
| AA15 | mcb_addr_p<2> | IOB | IO_L3N_D10_LC_2 | INPUT | LVCMOS25 | 2 | |
| AA16 | mcb_addr_p<3> | IOB | IO_L3P_D11_LC_2 | INPUT | LVCMOS25 | 2 | |
| AC11 | mcb_addr_p<4> | IOB | IO_L2N_D12_LC_2 | INPUT | LVCMOS25 | 2 | |
| AC12 | mcb_addr_p<5> | IOB | IO_L2P_D13_LC_2 | INPUT | LVCMOS25 | 2 | |
| AB14 | mcb_addr_p<6> | IOB | IO_L1N_D14_CC_LC_2 | INPUT | LVCMOS25 | 2 | |
| AA14 | mcb_addr_p<7> | IOB | IO_L1P_D15_CC_LC_2 | INPUT | LVCMOS25 | 2 | |
| AE14 | mcb_clk_p | IOB | IO_L5P_GC_LC_4 | INPUT | LVCMOS25 | 4 | |
| AE12 | mcb_cs_p | IOB | IO_L1N_GC_LC_4 | INPUT | LVCMOS25 | 4 | |
| D12 | mcb_data_p<0> | IOB | IO_L8N_D16_CC_LC_1 | BIDIR | LVCMOS25 | 1 | |
| E13 | mcb_data_p<1> | IOB | IO_L8P_D17_CC_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F15 | mcb_data_p<10> | IOB | IO_L3N_D26_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F16 | mcb_data_p<11> | IOB | IO_L3P_D27_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F11 | mcb_data_p<12> | IOB | IO_L2N_D28_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F12 | mcb_data_p<13> | IOB | IO_L2P_D29_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F13 | mcb_data_p<14> | IOB | IO_L1N_D30_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F14 | mcb_data_p<15> | IOB | IO_L1P_D31_LC_1 | BIDIR | LVCMOS25 | 1 | |
| C16 | mcb_data_p<2> | IOB | IO_L7N_D18_LC_1 | BIDIR | LVCMOS25 | 1 | |
| D16 | mcb_data_p<3> | IOB | IO_L7P_D19_LC_1 | BIDIR | LVCMOS25 | 1 | |
| D11 | mcb_data_p<4> | IOB | IO_L6N_D20_LC_1 | BIDIR | LVCMOS25 | 1 | |
| C11 | mcb_data_p<5> | IOB | IO_L6P_D21_LC_1 | BIDIR | LVCMOS25 | 1 | |
| E14 | mcb_data_p<6> | IOB | IO_L5N_D22_LC_1 | BIDIR | LVCMOS25 | 1 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | mcb_data_p<7> | IOB | IO_L5P_D23_LC_1 | BIDIR | LVCMOS25 | 1 | |
| D13 | mcb_data_p<8> | IOB | IO_L4N_D24_VREF_LC_1 | BIDIR | LVCMOS25 | 1 | |
| D14 | mcb_data_p<9> | IOB | IO_L4P_D25_LC_1 | BIDIR | LVCMOS25 | 1 | |
| AF12 | mcb_rw_p | IOB | IO_L1P_GC_LC_4 | INPUT | LVCMOS25 | 4 | |
| Y10 | odata_100PPS | IOB | IO_L27P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD2 | odata_clk | IOB | IO_L16P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AB9 | odata_PPS | IOB | IO_L29N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF3 | odata_val | IOB | IO_L15P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AA8 | odata<0> | IOB | IO_L26P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AB6 | odata<1> | IOB | IO_L24N_CC_LC_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC4 | odata<10> | IOB | IO_L11P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC3 | odata<11> | IOB | IO_L18N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AB1 | odata<12> | IOB | IO_L10P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AE9 | odata<13> | IOB | IO_L31N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC6 | odata<14> | IOB | IO_L24P_CC_LC_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC5 | odata<15> | IOB | IO_L13P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD4 | odata<16> | IOB | IO_L22N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD3 | odata<17> | IOB | IO_L18P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC1 | odata<18> | IOB | IO_L14N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF9 | odata<19> | IOB | IO_L31P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AB5 | odata<2> | IOB | IO_L13N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD8 | odata<20> | IOB | IO_L32P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF7 | odata<21> | IOB | IO_L25N_CC_LC_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AE6 | odata<22> | IOB | IO_L30P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD5 | odata<23> | IOB | IO_L22P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AE4 | odata<24> | IOB | IO_L17N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AE3 | odata<25> | IOB | IO_L15N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC2 | odata<26> | IOB | IO_L14P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD1 | odata<27> | IOB | IO_L16N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF8 | odata<28> | IOB | IO_L25P_CC_LC_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF6 | odata<29> | IOB | IO_L19P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AB4 | odata<3> | IOB | IO_L11N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF5 | odata<30> | IOB | IO_L19N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF4 | odata<31> | IOB | IO_L17P_8 | OUTPUT | HSTL_III_DCI | 8 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| AB3 | odata<4> | IOB | IO_L12P_8 | OUTPUT | HSTL_III_DCI | 8 |
| AA1 | odata<5> | IOB | IO_L10N_8 | OUTPUT | HSTL_III_DCI | 8 |
| AA10 | odata<6> | IOB | IO_L27N_8 | OUTPUT | HSTL_III_DCI | 8 |
| AC9 | odata<7> | IOB | IO_L29P_8 | OUTPUT | HSTL_III_DCI | 8 |
| AC8 | odata<8> | IOB | IO_L32N_8 | OUTPUT | HSTL_III_DCI | 8 |
| AC7 | odata<9> | IOB | IO_L28P_8 | OUTPUT | HSTL_III_DCI | 8 |
| B10 | reset_N | IOB | IO_L6N_GC_LC_3 | INPUT | LVCMOS25 | 3 |
| C14 | sclk_128_N | LOWCAPIOB | IO_L3N_GC_LC_3 | INPUT | LVDS_25 | 3 |
| C15 | sclk_128_P | LOWCAPIOB | IO_L3P_GC_LC_3 | INPUT | LVDS_25 | 3 |
| B14 | sys_100PPS_N | IOB | IO_L1N_GC_CC_LC_3 | INPUT | LVDS_25 | 3 |
| B15 | sys_100PPS_P | IOB | IO_L1P_GC_CC_LC_3 | INPUT | LVDS_25 | 3 |
| A15 | sys_PPS_N | IOB | IO_L5N_GC_LC_3 | INPUT | LVDS_25 | 3 |
| A16 | sys_PPS_P | IOB | IO_L5P_GC_LC_3 | INPUT | LVDS_25 | 3 |
| AD26 | TC_N<0> | IOBS | IO_L11N_7 | OUTPUT | LVDS_25 | 7 |
| T20 | TC_N<1> | IOBS | IO_L30N_9 | OUTPUT | LVDS_25 | 9 |
| AD25 | TC_P<0> | IOBM | IO_L11P_7 | OUTPUT | LVDS_25 | 7 |
| T21 | TC_P<1> | IOBM | IO_L30P_9 | OUTPUT | LVDS_25 | 9 |
| AF11 | test_port<0> | IOB | IO_L4P_GC_LC_4 | OUTPUT | LVCMOS25 | 4 |
| AC17 | test_port<1> | IOB | IO_L3N_GC_LC_4 | OUTPUT | LVCMOS25 | 4 |
| AB17 | test_port<2> | IOB | IO_L3P_GC_LC_4 | OUTPUT | LVCMOS25 | 4 |
| AB10 | test_port<3> | IOB | IO_L2N_GC_LC_4 | OUTPUT | LVCMOS25 | 4 |
| W1 | tick_G01 | IOB | IO_L1N_8 | INPUT | HSTL_III_DCI | 8 |
| P4 | tick_G02 | IOB | IO_L18N_10 | INPUT | HSTL_III_DCI | 10 |
| K6 | tick_G03 | IOB | IO_L3N_10 | INPUT | HSTL_III_DCI | 10 |
| F8 | tick_G04 | IOB | IO_L10P_6 | INPUT | HSTL_III_DCI | 6 |
| B9 | tick_G05 | IOB | IO_L13N_6 | INPUT | HSTL_III_DCI | 6 |
| C6 | tick_G06 | IOB | IO_L8N_CC_LC_6 | INPUT | HSTL_III_DCI | 6 |
| M7 | tick_G07 | IOB | IO_L17N_10 | INPUT | HSTL_III_DCI | 10 |
| R8 | tick_G08 | IOB | IO_L25P_CC_LC_10 | INPUT | HSTL_III_DCI | 10 |
| Y2 | tick_G09 | IOB | IO_L6P_8 | INPUT | HSTL_III_DCI | 8 |
| Y5 | tick_G10 | IOB | IO_L9N_CC_LC_8 | INPUT | HSTL_III_DCI | 8 |
| U5 | tick_G11 | IOB | IO_L32N_10 | INPUT | HSTL_III_DCI | 10 |
| M1 | tick_G12 | IOB | IO_L11N_10 | INPUT | HSTL_III_DCI | 10 |
| G4 | tick_G13 | IOB | IO_L28P_6 | INPUT | HSTL_III_DCI | 6 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| C8 | tick_G14 | IOB | IO_L2N_6 | INPUT | HSTL_III_DCI | 6 | |
| F10 | tick_G15 | IOB | IO_L5P_6 | INPUT | HSTL_III_DCI | 6 | |
| H1 | tick_G16 | IOB | IO_L32N_6 | INPUT | HSTL_III_DCI | 6 | |
| P8 | tick_G17 | IOB | IO_L19P_10 | INPUT | HSTL_III_DCI | 10 | |
| U6 | tick_G18 | IOB | IO_L32P_10 | INPUT | HSTL_III_DCI | 10 | |
| M24 | VSI_in_N<0> | IOB | IO_L11N_9 | INPUT | LVDS_25 | 9 | |
| N24 | VSI_in_N<1> | IOB | IO_L15N_9 | INPUT | LVDS_25 | 9 | |
| U21 | VSI_in_N<10> | IOB | IO_L29N_9 | INPUT | LVDS_25 | 9 | |
| T19 | VSI_in_N<11> | IOB | IO_L31N_9 | INPUT | LVDS_25 | 9 | |
| U24 | VSI_in_N<12> | IOB | IO_L28N_VREF_9 | INPUT | LVDS_25 | 9 | |
| V25 | VSI_in_N<13> | IOB | IO_L32N_9 | INPUT | LVDS_25 | 9 | |
| V23 | VSI_in_N<14> | IOB | IO_L27N_9 | INPUT | LVDS_25 | 9 | |
| V20 | VSI_in_N<15> | IOB | IO_L5N_7 | INPUT | LVDS_25 | 7 | |
| W26 | VSI_in_N<16> | IOB | IO_L2N_7 | INPUT | LVDS_25 | 7 | |
| W24 | VSI_in_N<17> | IOB | IO_L4N_VREF_7 | INPUT | LVDS_25 | 7 | |
| W22 | VSI_in_N<18> | IOB | IO_L3N_7 | INPUT | LVDS_25 | 7 | |
| Y26 | VSI_in_N<19> | IOB | IO_L6N_7 | INPUT | LVDS_25 | 7 | |
| N22 | VSI_in_N<2> | IOB | IO_L16N_9 | INPUT | LVDS_25 | 9 | |
| Y24 | VSI_in_N<20> | IOB | IO_L8N_CC_LC_7 | INPUT | LVDS_25 | 7 | |
| Y23 | VSI_in_N<21> | IOB | IO_L12N_VREF_7 | INPUT | LVDS_25 | 7 | |
| Y21 | VSI_in_N<22> | IOB | IO_L20N_VREF_7 | INPUT | LVDS_25 | 7 | |
| AA26 | VSI_in_N<23> | IOB | IO_L10N_7 | INPUT | LVDS_25 | 7 | |
| AB25 | VSI_in_N<24> | IOB | IO_L7N_7 | INPUT | LVDS_25 | 7 | |
| AA23 | VSI_in_N<25> | IOB | IO_L14N_7 | INPUT | LVDS_25 | 7 | |
| AC26 | VSI_in_N<26> | IOB | IO_L9N_CC_LC_7 | INPUT | LVDS_25 | 7 | |
| AC24 | VSI_in_N<27> | IOB | IO_L16N_7 | INPUT | LVDS_25 | 7 | |
| AE24 | VSI_in_N<28> | IOB | IO_L22N_7 | INPUT | LVDS_25 | 7 | |
| AE23 | VSI_in_N<29> | IOB | IO_L19N_7 | INPUT | LVDS_25 | 7 | |
| P24 | VSI_in_N<3> | IOB | IO_L18N_9 | INPUT | LVDS_25 | 9 | |
| AB22 | VSI_in_N<30> | IOB | IO_L13N_7 | INPUT | LVDS_25 | 7 | |
| AB21 | VSI_in_N<31> | IOB | IO_L24N_CC_LC_7 | INPUT | LVDS_25 | 7 | |
| AD21 | VSI_in_N<32> | IOB | IO_L32N_SM1_7 | INPUT | LVDS_25 | 7 | |
| AF22 | VSI_in_N<33> | IOB | IO_L30N_SM3_7 | INPUT | LVDS_25 | 7 | |
| AC20 | VSI_in_N<34> | IOB | IO_L28N_VREF_7 | INPUT | LVDS_25 | 7 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| W19 | VSI_in_N<35> | IOB | IO_L18N_7 | INPUT | LVDS_25 | 7 | |
| AF20 | VSI_in_N<36> | IOB | IO_L17N_7 | INPUT | LVDS_25 | 7 | |
| AC19 | VSI_in_N<37> | IOB | IO_L25N_CC_SM7_LC_7 | INPUT | LVDS_25 | 7 | |
| AE18 | VSI_in_N<38> | IOB | IO_L31N_SM2_7 | INPUT | LVDS_25 | 7 | |
| AB18 | VSI_in_N<39> | IOB | IO_L29N_SM4_7 | INPUT | LVDS_25 | 7 | |
| P22 | VSI_in_N<4> | IOB | IO_L19N_9 | INPUT | LVDS_25 | 9 | |
| R25 | VSI_in_N<5> | IOB | IO_L20N_VREF_9 | INPUT | LVDS_25 | 9 | |
| U26 | VSI_in_N<6> | IOB | IO_L26N_9 | INPUT | LVDS_25 | 9 | |
| R23 | VSI_in_N<7> | IOB | IO_L22N_9 | INPUT | LVDS_25 | 9 | |
| P19 | VSI_in_N<8> | IOB | IO_L21N_9 | INPUT | LVDS_25 | 9 | |
| T23 | VSI_in_N<9> | IOB | IO_L24N_CC_LC_9 | INPUT | LVDS_25 | 9 | |
| M25 | VSI_in_P<0> | IOB | IO_L11P_9 | INPUT | LVDS_25 | 9 | |
| N25 | VSI_in_P<1> | IOB | IO_L15P_9 | INPUT | LVDS_25 | 9 | |
| U22 | VSI_in_P<10> | IOB | IO_L29P_9 | INPUT | LVDS_25 | 9 | |
| U20 | VSI_in_P<11> | IOB | IO_L31P_9 | INPUT | LVDS_25 | 9 | |
| U25 | VSI_in_P<12> | IOB | IO_L28P_9 | INPUT | LVDS_25 | 9 | |
| V26 | VSI_in_P<13> | IOB | IO_L32P_9 | INPUT | LVDS_25 | 9 | |
| U23 | VSI_in_P<14> | IOB | IO_L27P_9 | INPUT | LVDS_25 | 9 | |
| W20 | VSI_in_P<15> | IOB | IO_L5P_7 | INPUT | LVDS_25 | 7 | |
| W25 | VSI_in_P<16> | IOB | IO_L2P_7 | INPUT | LVDS_25 | 7 | |
| W23 | VSI_in_P<17> | IOB | IO_L4P_7 | INPUT | LVDS_25 | 7 | |
| W21 | VSI_in_P<18> | IOB | IO_L3P_7 | INPUT | LVDS_25 | 7 | |
| Y25 | VSI_in_P<19> | IOB | IO_L6P_7 | INPUT | LVDS_25 | 7 | |
| N23 | VSI_in_P<2> | IOB | IO_L16P_9 | INPUT | LVDS_25 | 9 | |
| AA24 | VSI_in_P<20> | IOB | IO_L8P_CC_LC_7 | INPUT | LVDS_25 | 7 | |
| Y22 | VSI_in_P<21> | IOB | IO_L12P_7 | INPUT | LVDS_25 | 7 | |
| Y20 | VSI_in_P<22> | IOB | IO_L20P_7 | INPUT | LVDS_25 | 7 | |
| AB26 | VSI_in_P<23> | IOB | IO_L10P_7 | INPUT | LVDS_25 | 7 | |
| AB24 | VSI_in_P<24> | IOB | IO_L7P_7 | INPUT | LVDS_25 | 7 | |
| AB23 | VSI_in_P<25> | IOB | IO_L14P_7 | INPUT | LVDS_25 | 7 | |
| AC25 | VSI_in_P<26> | IOB | IO_L9P_CC_LC_7 | INPUT | LVDS_25 | 7 | |
| AC23 | VSI_in_P<27> | IOB | IO_L16P_7 | INPUT | LVDS_25 | 7 | |
| AF24 | VSI_in_P<28> | IOB | IO_L22P_7 | INPUT | LVDS_25 | 7 | |
| AF23 | VSI_in_P<29> | IOB | IO_L19P_7 | INPUT | LVDS_25 | 7 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| P25 | VSI_in_P<3> | IOB | IO_L18P_9 | INPUT | LVDS_25 | 9 |
| AC22 | VSI_in_P<30> | IOB | IO_L13P_7 | INPUT | LVDS_25 | 7 |
| AC21 | VSI_in_P<31> | IOB | IO_L24P_CC_LC_7 | INPUT | LVDS_25 | 7 |
| AE21 | VSI_in_P<32> | IOB | IO_L32P_SM1_7 | INPUT | LVDS_25 | 7 |
| AF21 | VSI_in_P<33> | IOB | IO_L30P_SM3_7 | INPUT | LVDS_25 | 7 |
| AB20 | VSI_in_P<34> | IOB | IO_L28P_7 | INPUT | LVDS_25 | 7 |
| Y19 | VSI_in_P<35> | IOB | IO_L18P_7 | INPUT | LVDS_25 | 7 |
| AF19 | VSI_in_P<36> | IOB | IO_L17P_7 | INPUT | LVDS_25 | 7 |
| AD19 | VSI_in_P<37> | IOB | IO_L25P_CC_SM7_LC_7 | INPUT | LVDS_25 | 7 |
| AF18 | VSI_in_P<38> | IOB | IO_L31P_SM2_7 | INPUT | LVDS_25 | 7 |
| AC18 | VSI_in_P<39> | IOB | IO_L29P_SM4_7 | INPUT | LVDS_25 | 7 |
| P23 | VSI_in_P<4> | IOB | IO_L19P_9 | INPUT | LVDS_25 | 9 |
| R26 | VSI_in_P<5> | IOB | IO_L20P_9 | INPUT | LVDS_25 | 9 |
| T26 | VSI_in_P<6> | IOB | IO_L26P_9 | INPUT | LVDS_25 | 9 |
| R24 | VSI_in_P<7> | IOB | IO_L22P_9 | INPUT | LVDS_25 | 9 |
| P20 | VSI_in_P<8> | IOB | IO_L21P_9 | INPUT | LVDS_25 | 9 |
| T24 | VSI_in_P<9> | IOB | IO_L24P_CC_LC_9 | INPUT | LVDS_25 | 9 |
| L20 | VSI_out_N<0> | IOBS | IO_L6N_9 | OUTPUT | LVDS_25 | 9 |
| D17 | VSI_out_N<1> | IOBS | IO_L1N_5 | OUTPUT | LVDS_25 | 5 |
| D19 | VSI_out_N<10> | IOBS | IO_L4N_VREF_5 | OUTPUT | LVDS_25 | 5 |
| E20 | VSI_out_N<11> | IOBS | IO_L19N_5 | OUTPUT | LVDS_25 | 5 |
| G20 | VSI_out_N<12> | IOBS | IO_L22N_5 | OUTPUT | LVDS_25 | 5 |
| C22 | VSI_out_N<13> | IOBS | IO_L14N_5 | OUTPUT | LVDS_25 | 5 |
| B21 | VSI_out_N<14> | IOBS | IO_L6N_5 | OUTPUT | LVDS_25 | 5 |
| E18 | VSI_out_N<15> | IOBS | IO_L11N_5 | OUTPUT | LVDS_25 | 5 |
| G21 | VSI_out_N<16> | IOBS | IO_L23N_VRP_5 | OUTPUT | LVDS_25 | 5 |
| H25 | VSI_out_N<17> | IOBS | IO_L32N_5 | OUTPUT | LVDS_25 | 5 |
| C23 | VSI_out_N<18> | IOBS | IO_L21N_5 | OUTPUT | LVDS_25 | 5 |
| A19 | VSI_out_N<19> | IOBS | IO_L13N_5 | OUTPUT | LVDS_25 | 5 |
| F17 | VSI_out_N<2> | IOBS | IO_L5N_5 | OUTPUT | LVDS_25 | 5 |
| M20 | VSI_out_N<20> | IOBS | IO_L13N_9 | OUTPUT | LVDS_25 | 9 |
| E22 | VSI_out_N<21> | IOBS | IO_L18N_5 | OUTPUT | LVDS_25 | 5 |
| A21 | VSI_out_N<22> | IOBS | IO_L15N_5 | OUTPUT | LVDS_25 | 5 |
| E24 | VSI_out_N<23> | IOBS | IO_L27N_5 | OUTPUT | LVDS_25 | 5 |

| | | | | | | |
|---|---|---|---|---|---|---|
| H21 | VSI_out_N<24> | IOBS | IO_L26N_5 | OUTPUT | LVDS_25 | 5 |
| C25 | VSI_out_N<25> | IOBS | IO_L20N_VREF_5 | OUTPUT | LVDS_25 | 5 |
| G23 | VSI_out_N<26> | IOBS | IO_L28N_VREF_5 | OUTPUT | LVDS_25 | 5 |
| H23 | VSI_out_N<27> | IOBS | IO_L30N_5 | OUTPUT | LVDS_25 | 5 |
| C24 | VSI_out_N<28> | IOBS | IO_L16N_5 | OUTPUT | LVDS_25 | 5 |
| E26 | VSI_out_N<29> | IOBS | IO_L29N_5 | OUTPUT | LVDS_25 | 5 |
| N20 | VSI_out_N<3> | IOBS | IO_L17N_9 | OUTPUT | LVDS_25 | 9 |
| J22 | VSI_out_N<30> | IOBS | IO_L2N_9 | OUTPUT | LVDS_25 | 9 |
| G25 | VSI_out_N<31> | IOBS | IO_L31N_5 | OUTPUT | LVDS_25 | 5 |
| J25 | VSI_out_N<32> | IOBS | IO_L4N_VREF_9 | OUTPUT | LVDS_25 | 9 |
| J20 | VSI_out_N<33> | IOBS | IO_L1N_9 | OUTPUT | LVDS_25 | 9 |
| K21 | VSI_out_N<34> | IOBS | IO_L3N_9 | OUTPUT | LVDS_25 | 9 |
| K20 | VSI_out_N<35> | IOBS | IO_L5N_9 | OUTPUT | LVDS_25 | 9 |
| L23 | VSI_out_N<36> | IOBS | IO_L10N_9 | OUTPUT | LVDS_25 | 9 |
| M26 | VSI_out_N<37> | IOBS | IO_L12N_VREF_9 | OUTPUT | LVDS_25 | 9 |
| M22 | VSI_out_N<38> | IOBS | IO_L14N_9 | OUTPUT | LVDS_25 | 9 |
| K23 | VSI_out_N<39> | IOBS | IO_L7N_9 | OUTPUT | LVDS_25 | 9 |
| A18 | VSI_out_N<4> | IOBS | IO_L3N_5 | OUTPUT | LVDS_25 | 5 |
| D18 | VSI_out_N<5> | IOBS | IO_L7N_5 | OUTPUT | LVDS_25 | 5 |
| B23 | VSI_out_N<6> | IOBS | IO_L10N_5 | OUTPUT | LVDS_25 | 5 |
| F19 | VSI_out_N<7> | IOBS | IO_L17N_5 | OUTPUT | LVDS_25 | 5 |
| D21 | VSI_out_N<8> | IOBS | IO_L12N_VREF_5 | OUTPUT | LVDS_25 | 5 |
| B20 | VSI_out_N<9> | IOBS | IO_L2N_5 | OUTPUT | LVDS_25 | 5 |
| L21 | VSI_out_P<0> | IOBM | IO_L6P_9 | OUTPUT | LVDS_25 | 9 |
| C17 | VSI_out_P<1> | IOBM | IO_L1P_5 | OUTPUT | LVDS_25 | 5 |
| D20 | VSI_out_P<10> | IOBM | IO_L4P_5 | OUTPUT | LVDS_25 | 5 |
| F20 | VSI_out_P<11> | IOBM | IO_L19P_5 | OUTPUT | LVDS_25 | 5 |
| H20 | VSI_out_P<12> | IOBM | IO_L22P_5 | OUTPUT | LVDS_25 | 5 |
| D22 | VSI_out_P<13> | IOBM | IO_L14P_5 | OUTPUT | LVDS_25 | 5 |
| C21 | VSI_out_P<14> | IOBM | IO_L6P_5 | OUTPUT | LVDS_25 | 5 |
| F18 | VSI_out_P<15> | IOBM | IO_L11P_5 | OUTPUT | LVDS_25 | 5 |
| G22 | VSI_out_P<16> | IOBM | IO_L23P_VRN_5 | OUTPUT | LVDS_25 | 5 |
| H26 | VSI_out_P<17> | IOBM | IO_L32P_5 | OUTPUT | LVDS_25 | 5 |
| D23 | VSI_out_P<18> | IOBM | IO_L21P_5 | OUTPUT | LVDS_25 | 5 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A20 | VSI_out_P<19> | IOBM | IO_L13P_5 | OUTPUT | LVDS_25 | 5 | |
| E17 | VSI_out_P<2> | IOBM | IO_L5P_5 | OUTPUT | LVDS_25 | 5 | |
| M21 | VSI_out_P<20> | IOBM | IO_L13P_9 | OUTPUT | LVDS_25 | 9 | |
| E23 | VSI_out_P<21> | IOBM | IO_L18P_5 | OUTPUT | LVDS_25 | 5 | |
| A22 | VSI_out_P<22> | IOBM | IO_L15P_5 | OUTPUT | LVDS_25 | 5 | |
| E25 | VSI_out_P<23> | IOBM | IO_L27P_5 | OUTPUT | LVDS_25 | 5 | |
| H22 | VSI_out_P<24> | IOBM | IO_L26P_5 | OUTPUT | LVDS_25 | 5 | |
| C26 | VSI_out_P<25> | IOBM | IO_L20P_5 | OUTPUT | LVDS_25 | 5 | |
| G24 | VSI_out_P<26> | IOBM | IO_L28P_5 | OUTPUT | LVDS_25 | 5 | |
| H24 | VSI_out_P<27> | IOBM | IO_L30P_5 | OUTPUT | LVDS_25 | 5 | |
| D24 | VSI_out_P<28> | IOBM | IO_L16P_5 | OUTPUT | LVDS_25 | 5 | |
| F26 | VSI_out_P<29> | IOBM | IO_L29P_5 | OUTPUT | LVDS_25 | 5 | |
| N21 | VSI_out_P<3> | IOBM | IO_L17P_9 | OUTPUT | LVDS_25 | 9 | |
| J23 | VSI_out_P<30> | IOBM | IO_L2P_9 | OUTPUT | LVDS_25 | 9 | |
| G26 | VSI_out_P<31> | IOBM | IO_L31P_5 | OUTPUT | LVDS_25 | 5 | |
| J26 | VSI_out_P<32> | IOBM | IO_L4P_9 | OUTPUT | LVDS_25 | 9 | |
| J21 | VSI_out_P<33> | IOBM | IO_L1P_9 | OUTPUT | LVDS_25 | 9 | |
| K22 | VSI_out_P<34> | IOBM | IO_L3P_9 | OUTPUT | LVDS_25 | 9 | |
| L19 | VSI_out_P<35> | IOBM | IO_L5P_9 | OUTPUT | LVDS_25 | 9 | |
| L24 | VSI_out_P<36> | IOBM | IO_L10P_9 | OUTPUT | LVDS_25 | 9 | |
| L26 | VSI_out_P<37> | IOBM | IO_L12P_9 | OUTPUT | LVDS_25 | 9 | |
| M23 | VSI_out_P<38> | IOBM | IO_L14P_9 | OUTPUT | LVDS_25 | 9 | |
| K24 | VSI_out_P<39> | IOBM | IO_L7P_9 | OUTPUT | LVDS_25 | 9 | |
| B18 | VSI_out_P<4> | IOBM | IO_L3P_5 | OUTPUT | LVDS_25 | 5 | |
| C19 | VSI_out_P<5> | IOBM | IO_L7P_5 | OUTPUT | LVDS_25 | 5 | |
| B24 | VSI_out_P<6> | IOBM | IO_L10P_5 | OUTPUT | LVDS_25 | 5 | |
| G19 | VSI_out_P<7> | IOBM | IO_L17P_5 | OUTPUT | LVDS_25 | 5 | |
| E21 | VSI_out_P<8> | IOBM | IO_L12P_5 | OUTPUT | LVDS_25 | 5 | |
| C20 | VSI_out_P<9> | IOBM | IO_L2P_5 | OUTPUT | LVDS_25 | 5 | |

**Table 7-1 Pinout by Signal Name**

## 7.2 Pinout by pin number

Note: UNUSED and NC pins have been removed.

Release 10.1.03 - par K.39 (nt)


Tue Mar 02 16:38:16 2010

INPUT FILE: vsi_top_map.ncd
OUTPUT FILE: vsi_top_pad.txt
PART TYPE: xc4vsx35
SPEED GRADE: -10
PACKAGE: ff668

| Pin | Signal Name | Pin Usage | Pin Name | Direction | IO Standard | IO Bank |
|---|---|---|---|---|---|---|
| A13 | | | GND | | | |
| A14 | | | GND | | | |
| A15 | sys_PPS_N | IOB | IO_L5N_GC_LC_3 | INPUT | LVDS_25 | 3 |
| A16 | sys_PPS_P | IOB | IO_L5P_GC_LC_3 | INPUT | LVDS_25 | 3 |
| A18 | VSI_out_N<4> | IOBS | IO_L3N_5 | OUTPUT | LVDS_25 | 5 |
| A19 | VSI_out_N<19> | IOBS | IO_L13N_5 | OUTPUT | LVDS_25 | 5 |
| A2 | | | GND | | | |
| A20 | VSI_out_P<19> | IOBM | IO_L13P_5 | OUTPUT | LVDS_25 | 5 |
| A21 | VSI_out_N<22> | IOBS | IO_L15N_5 | OUTPUT | LVDS_25 | 5 |
| A22 | VSI_out_P<22> | IOBM | IO_L15P_5 | OUTPUT | LVDS_25 | 5 |
| A25 | | | GND | | | |
| A7 | data_G05<2> | IOB | IO_L3N_6 | INPUT | HSTL_III_DCI | 6 |
| A8 | data_G05<1> | IOB | IO_L3P_6 | INPUT | HSTL_III_DCI | 6 |
| A9 | data_G05<0> | IOB | IO_L13P_6 | INPUT | HSTL_III_DCI | 6 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AA1 | odata<5> | IOB | IO_L10N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AA10 | odata<6> | IOB | IO_L27N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AA13 | mcb_addr_p<0> | IOB | IO_L4N_D8_VREF_LC_2 | INPUT | LVCMOS25 | 2 | |
| AA14 | mcb_addr_p<7> | IOB | IO_L1P_D15_CC_LC_2 | INPUT | LVCMOS25 | 2 | |
| AA15 | mcb_addr_p<2> | IOB | IO_L3N_D10_LC_2 | INPUT | LVCMOS25 | 2 | |
| AA16 | mcb_addr_p<3> | IOB | IO_L3P_D11_LC_2 | INPUT | LVCMOS25 | 2 | |
| AA2 | | | VCCO_8 | | | 8 | |
| AA21 | | | GND | | | | |
| AA22 | | | VCCO_7 | | | 7 | |
| AA23 | VSI_in_N<25> | IOB | IO_L14N_7 | INPUT | LVDS_25 | 7 | |
| AA24 | VSI_in_P<20> | IOB | IO_L8P_CC_LC_7 | INPUT | LVDS_25 | 7 | |
| AA25 | | | VCCO_7 | | | 7 | |
| AA26 | VSI_in_N<23> | IOB | IO_L10N_7 | INPUT | LVDS_25 | 7 | |
| AA3 | data_G09<1> | IOB | IO_L7N_8 | INPUT | HSTL_III_DCI | 8 | |
| AA4 | data_G09<0> | IOB | IO_L7P_8 | INPUT | HSTL_III_DCI | 8 | |
| AA5 | | | VCCO_8 | | | 8 | |
| AA6 | | | GND | | | | |
| AA7 | data_G10<3> | IOB | IO_L20P_8 | INPUT | HSTL_III_DCI | 8 | |
| AA8 | odata<0> | IOB | IO_L26P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AA9 | data_G10<0> | IOB | IO_L21P_8 | INPUT | HSTL_III_DCI | 8 | |
| AB1 | odata<12> | IOB | IO_L10P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AB10 | test_port<3> | IOB | IO_L2N_GC_LC_4 | OUTPUT | LVCMOS25 | 4 | |
| AB11 | | | VCCO_2 | | | 2 | |
| AB12 | | | GND | | | | |
| AB13 | mcb_addr_p<1> | IOB | IO_L4P_D9_LC_2 | INPUT | LVCMOS25 | 2 | |
| AB14 | mcb_addr_p<6> | IOB | IO_L1N_D14_CC_LC_2 | INPUT | LVCMOS25 | 2 | |
| AB15 | | | GND | | | | |
| AB16 | | | VCCO_2 | | | 2 | |
| AB17 | test_port<2> | IOB | IO_L3P_GC_LC_4 | OUTPUT | LVCMOS25 | 4 | |
| AB18 | VSI_in_N<39> | IOB | IO_L29N_SM4_7 | INPUT | LVDS_25 | 7 | |
| AB19 | | | VCCO_7 | | | 7 | |
| AB20 | VSI_in_P<34> | IOB | IO_L28P_7 | INPUT | LVDS_25 | 7 | |
| AB21 | VSI_in_N<31> | IOB | IO_L24N_CC_LC_7 | INPUT | LVDS_25 | 7 | |
| AB22 | VSI_in_N<30> | IOB | IO_L13N_7 | INPUT | LVDS_25 | 7 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AB23 | VSI_in_P<25> | IOB | IO_L14P_7 | INPUT | LVDS_25 | 7 | |
| AB24 | VSI_in_P<24> | IOB | IO_L7P_7 | INPUT | LVDS_25 | 7 | |
| AB25 | VSI_in_N<24> | IOB | IO_L7N_7 | INPUT | LVDS_25 | 7 | |
| AB26 | VSI_in_P<23> | IOB | IO_L10P_7 | INPUT | LVDS_25 | 7 | |
| AB3 | odata<4> | IOB | IO_L12P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AB4 | odata<3> | IOB | IO_L11N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AB5 | odata<2> | IOB | IO_L13N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AB6 | odata<1> | IOB | IO_L24N_CC_LC_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AB8 | | | VCCO_8 | | | 8 | |
| AB9 | odata_PPS | IOB | IO_L29N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC1 | odata<18> | IOB | IO_L14N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC11 | mcb_addr_p<4> | IOB | IO_L2N_D12_LC_2 | INPUT | LVCMOS25 | 2 | |
| AC12 | mcb_addr_p<5> | IOB | IO_L2P_D13_LC_2 | INPUT | LVCMOS25 | 2 | |
| AC17 | test_port<1> | IOB | IO_L3N_GC_LC_4 | OUTPUT | LVCMOS25 | 4 | |
| AC18 | VSI_in_P<39> | IOB | IO_L29P_SM4_7 | INPUT | LVDS_25 | 7 | |
| AC19 | VSI_in_N<37> | IOB | IO_L25N_CC_SM7_LC_7 | INPUT | LVDS_25 | 7 | |
| AC2 | odata<26> | IOB | IO_L14P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC20 | VSI_in_N<34> | IOB | IO_L28N_VREF_7 | INPUT | LVDS_25 | 7 | |
| AC21 | VSI_in_P<31> | IOB | IO_L24P_CC_LC_7 | INPUT | LVDS_25 | 7 | |
| AC22 | VSI_in_P<30> | IOB | IO_L13P_7 | INPUT | LVDS_25 | 7 | |
| AC23 | VSI_in_P<27> | IOB | IO_L16P_7 | INPUT | LVDS_25 | 7 | |
| AC24 | VSI_in_N<27> | IOB | IO_L16N_7 | INPUT | LVDS_25 | 7 | |
| AC25 | VSI_in_P<26> | IOB | IO_L9P_CC_LC_7 | INPUT | LVDS_25 | 7 | |
| AC26 | VSI_in_N<26> | IOB | IO_L9N_CC_LC_7 | INPUT | LVDS_25 | 7 | |
| AC3 | odata<11> | IOB | IO_L18N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC4 | odata<10> | IOB | IO_L11P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC5 | odata<15> | IOB | IO_L13P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC6 | odata<14> | IOB | IO_L24P_CC_LC_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC7 | odata<9> | IOB | IO_L28P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC8 | odata<8> | IOB | IO_L32N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AC9 | odata<7> | IOB | IO_L29P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD1 | odata<27> | IOB | IO_L16N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD15 | | | VCCO_4 | | | 4 | |
| AD18 | | | GND | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AD19 | VSI_in_P<37> | IOB | IO_L25P_CC_SM7_LC_7 | INPUT | LVDS_25 | 7 | |
| AD2 | odata_clk | IOB | IO_L16P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD21 | VSI_in_N<32> | IOB | IO_L32N_SM1_7 | INPUT | LVDS_25 | 7 | |
| AD24 | | | GND | | | | |
| AD25 | TC_P<0> | IOBM | IO_L11P_7 | OUTPUT | LVDS_25 | 7 | |
| AD26 | TC_N<0> | IOBS | IO_L11N_7 | OUTPUT | LVDS_25 | 7 | |
| AD3 | odata<17> | IOB | IO_L18P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD4 | odata<16> | IOB | IO_L22N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD5 | odata<23> | IOB | IO_L22P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD8 | odata<20> | IOB | IO_L32P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AD9 | | | GND | | | | |
| AE1 | | | GND | | | | |
| AE11 | | | VCCO_4 | | | 4 | |
| AE12 | mcb_cs_p | IOB | IO_L1N_GC_LC_4 | INPUT | LVCMOS25 | 4 | |
| AE14 | mcb_clk_p | IOB | IO_L5P_GC_LC_4 | INPUT | LVCMOS25 | 4 | |
| AE15 | | | VREFN_SM | | | | |
| AE16 | | | VREFP_SM | | | | |
| AE17 | | | AVSS_SM | | | | |
| AE18 | VSI_in_N<38> | IOB | IO_L31N_SM2_7 | INPUT | LVDS_25 | 7 | |
| AE19 | | | VCCO_7 | | | 7 | |
| AE2 | | | GND | | | | |
| AE21 | VSI_in_P<32> | IOB | IO_L32P_SM1_7 | INPUT | LVDS_25 | 7 | |
| AE22 | | | VCCO_7 | | | 7 | |
| AE23 | VSI_in_N<29> | IOB | IO_L19N_7 | INPUT | LVDS_25 | 7 | |
| AE24 | VSI_in_N<28> | IOB | IO_L22N_7 | INPUT | LVDS_25 | 7 | |
| AE25 | | | GND | | | | |
| AE26 | | | GND | | | | |
| AE3 | odata<25> | IOB | IO_L15N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AE4 | odata<24> | IOB | IO_L17N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AE5 | | | VCCO_8 | | | 8 | |
| AE6 | odata<22> | IOB | IO_L30P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AE8 | | | VCCO_8 | | | 8 | |
| AE9 | odata<13> | IOB | IO_L31N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF11 | test_port<0> | IOB | IO_L4P_GC_LC_4 | OUTPUT | LVCMOS25 | 4 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AF12 | mcb_rw_p | IOB | IO_L1P_GC_LC_4 | INPUT | LVCMOS25 | 4 | |
| AF13 | | | GND | | | | |
| AF14 | | | GND | | | | |
| AF17 | | | AVDD_SM | | | | |
| AF18 | VSI_in_P<38> | IOB | IO_L31P_SM2_7 | INPUT | LVDS_25 | 7 | |
| AF19 | VSI_in_P<36> | IOB | IO_L17P_7 | INPUT | LVDS_25 | 7 | |
| AF2 | | | GND | | | | |
| AF20 | VSI_in_N<36> | IOB | IO_L17N_7 | INPUT | LVDS_25 | 7 | |
| AF21 | VSI_in_P<33> | IOB | IO_L30P_SM3_7 | INPUT | LVDS_25 | 7 | |
| AF22 | VSI_in_N<33> | IOB | IO_L30N_SM3_7 | INPUT | LVDS_25 | 7 | |
| AF23 | VSI_in_P<29> | IOB | IO_L19P_7 | INPUT | LVDS_25 | 7 | |
| AF24 | VSI_in_P<28> | IOB | IO_L22P_7 | INPUT | LVDS_25 | 7 | |
| AF25 | | | GND | | | | |
| AF3 | odata_val | IOB | IO_L15P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF4 | odata<31> | IOB | IO_L17P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF5 | odata<30> | IOB | IO_L19N_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF6 | odata<29> | IOB | IO_L19P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF7 | odata<21> | IOB | IO_L25N_CC_LC_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF8 | odata<28> | IOB | IO_L25P_CC_LC_8 | OUTPUT | HSTL_III_DCI | 8 | |
| AF9 | odata<19> | IOB | IO_L31P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| B1 | | | GND | | | | |
| B10 | reset_N | IOB | IO_L6N_GC_LC_3 | INPUT | LVCMOS25 | 3 | |
| B11 | | | VCCO_3 | | | 3 | |
| B14 | sys_100PPS_N | IOB | IO_L1N_GC_CC_LC_3 | INPUT | LVDS_25 | 3 | |
| B15 | sys_100PPS_P | IOB | IO_L1P_GC_CC_LC_3 | INPUT | LVDS_25 | 3 | |
| B16 | | | VCCO_3 | | | 3 | |
| B18 | VSI_out_P<4> | IOBM | IO_L3P_5 | OUTPUT | LVDS_25 | 5 | |
| B19 | | | VCCO_5 | | | 5 | |
| B2 | | | GND | | | | |
| B20 | VSI_out_N<9> | IOBS | IO_L2N_5 | OUTPUT | LVDS_25 | 5 | |
| B21 | VSI_out_N<14> | IOBS | IO_L6N_5 | OUTPUT | LVDS_25 | 5 | |
| B22 | | | VCCO_5 | | | 5 | |
| B23 | VSI_out_N<6> | IOBS | IO_L10N_5 | OUTPUT | LVDS_25 | 5 | |
| B24 | VSI_out_P<6> | IOBM | IO_L10P_5 | OUTPUT | LVDS_25 | 5 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| B25 | | | GND | | | | |
| B26 | | | GND | | | | |
| B5 | | | VCCO_6 | | | 6 | |
| B7 | data_G05<3> | IOB | IO_L11P_6 | INPUT | HSTL_III_DCI | 6 | |
| B8 | | | VCCO_6 | | | 6 | |
| B9 | tick_G05 | IOB | IO_L13N_6 | INPUT | HSTL_III_DCI | 6 | |
| C10 | clk_G14 | IOB | IO_L1N_6 | INPUT | HSTL_III_DCI | 6 | |
| C11 | mcb_data_p<5> | IOB | IO_L6P_D21_LC_1 | BIDIR | LVCMOS25 | 1 | |
| C14 | sclk_128_N | LOWCAPIOB | IO_L3N_GC_LC_3 | INPUT | LVDS_25 | 3 | |
| C15 | sclk_128_P | LOWCAPIOB | IO_L3P_GC_LC_3 | INPUT | LVDS_25 | 3 | |
| C16 | mcb_data_p<2> | IOB | IO_L7N_D18_LC_1 | BIDIR | LVCMOS25 | 1 | |
| C17 | VSI_out_P<1> | IOBM | IO_L1P_5 | OUTPUT | LVDS_25 | 5 | |
| C18 | | | GND | | | | |
| C19 | VSI_out_P<5> | IOBM | IO_L7P_5 | OUTPUT | LVDS_25 | 5 | |
| C20 | VSI_out_P<9> | IOBM | IO_L2P_5 | OUTPUT | LVDS_25 | 5 | |
| C21 | VSI_out_P<14> | IOBM | IO_L6P_5 | OUTPUT | LVDS_25 | 5 | |
| C22 | VSI_out_N<13> | IOBS | IO_L14N_5 | OUTPUT | LVDS_25 | 5 | |
| C23 | VSI_out_N<18> | IOBS | IO_L21N_5 | OUTPUT | LVDS_25 | 5 | |
| C24 | VSI_out_N<28> | IOBS | IO_L16N_5 | OUTPUT | LVDS_25 | 5 | |
| C25 | VSI_out_N<25> | IOBS | IO_L20N_VREF_5 | OUTPUT | LVDS_25 | 5 | |
| C26 | VSI_out_P<25> | IOBM | IO_L20P_5 | OUTPUT | LVDS_25 | 5 | |
| C3 | | | GND | | | | |
| C5 | data_G06<0> | IOB | IO_L12P_6 | INPUT | HSTL_III_DCI | 6 | |
| C6 | tick_G06 | IOB | IO_L8N_CC_LC_6 | INPUT | HSTL_III_DCI | 6 | |
| C7 | clk_G05 | IOB | IO_L11N_6 | INPUT | HSTL_III_DCI | 6 | |
| C8 | tick_G14 | IOB | IO_L2N_6 | INPUT | HSTL_III_DCI | 6 | |
| C9 | | | GND | | | | |
| D1 | data_G06<3> | IOB | IO_L25N_CC_LC_6 | INPUT | HSTL_III_DCI | 6 | |
| D10 | clk_G15 | IOB | IO_L1P_6 | INPUT | HSTL_III_DCI | 6 | |
| D11 | mcb_data_p<4> | IOB | IO_L6N_D20_LC_1 | BIDIR | LVCMOS25 | 1 | |
| D12 | mcb_data_p<0> | IOB | IO_L8N_D16_CC_LC_1 | BIDIR | LVCMOS25 | 1 | |
| D13 | mcb_data_p<8> | IOB | IO_L4N_D24_VREF_LC_1 | BIDIR | LVCMOS25 | 1 | |
| D14 | mcb_data_p<9> | IOB | IO_L4P_D25_LC_1 | BIDIR | LVCMOS25 | 1 | |
| D15 | mcb_data_p<7> | IOB | IO_L5P_D23_LC_1 | BIDIR | LVCMOS25 | 1 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D16 | mcb_data_p<3> | IOB | IO_L7P_D19_LC_1 | BIDIR | LVCMOS25 | 1 | |
| D17 | VSI_out_N<1> | IOBS | IO_L1N_5 | OUTPUT | LVDS_25 | 5 | |
| D18 | VSI_out_N<5> | IOBS | IO_L7N_5 | OUTPUT | LVDS_25 | 5 | |
| D19 | VSI_out_N<10> | IOBS | IO_L4N_VREF_5 | OUTPUT | LVDS_25 | 5 | |
| D2 | clk_G06 | IOB | IO_L25P_CC_LC_6 | INPUT | HSTL_III_DCI | 6 | |
| D20 | VSI_out_P<10> | IOBM | IO_L4P_5 | OUTPUT | LVDS_25 | 5 | |
| D21 | VSI_out_N<8> | IOBS | IO_L12N_VREF_5 | OUTPUT | LVDS_25 | 5 | |
| D22 | VSI_out_P<13> | IOBM | IO_L14P_5 | OUTPUT | LVDS_25 | 5 | |
| D23 | VSI_out_P<18> | IOBM | IO_L21P_5 | OUTPUT | LVDS_25 | 5 | |
| D24 | VSI_out_P<28> | IOBM | IO_L16P_5 | OUTPUT | LVDS_25 | 5 | |
| D3 | data_G06<2> | IOB | IO_L22P_6 | INPUT | HSTL_III_DCI | 6 | |
| D4 | data_G06<1> | IOB | IO_L16N_6 | INPUT | HSTL_III_DCI | 6 | |
| D6 | data_G14<2> | IOB | IO_L17N_6 | INPUT | HSTL_III_DCI | 6 | |
| D8 | data_G14<1> | IOB | IO_L4P_6 | INPUT | HSTL_III_DCI | 6 | |
| D9 | data_G14<0> | IOB | IO_L2P_6 | INPUT | HSTL_III_DCI | 6 | |
| E1 | data_G16<2> | IOB | IO_L26P_6 | INPUT | HSTL_III_DCI | 6 | |
| E10 | data_G15<1> | IOB | IO_L5N_6 | INPUT | HSTL_III_DCI | 6 | |
| E11 | | | VCCO_1 | | | 1 | |
| E12 | | | GND | | | | |
| E13 | mcb_data_p<1> | IOB | IO_L8P_D17_CC_LC_1 | BIDIR | LVCMOS25 | 1 | |
| E14 | mcb_data_p<6> | IOB | IO_L5N_D22_LC_1 | BIDIR | LVCMOS25 | 1 | |
| E15 | | | GND | | | | |
| E16 | | | VCCO_1 | | | 1 | |
| E17 | VSI_out_P<2> | IOBM | IO_L5P_5 | OUTPUT | LVDS_25 | 5 | |
| E18 | VSI_out_N<15> | IOBS | IO_L11N_5 | OUTPUT | LVDS_25 | 5 | |
| E19 | | | VCCO_5 | | | 5 | |
| E20 | VSI_out_N<11> | IOBS | IO_L19N_5 | OUTPUT | LVDS_25 | 5 | |
| E21 | VSI_out_P<8> | IOBM | IO_L12P_5 | OUTPUT | LVDS_25 | 5 | |
| E22 | VSI_out_N<21> | IOBS | IO_L18N_5 | OUTPUT | LVDS_25 | 5 | |
| E23 | VSI_out_P<21> | IOBM | IO_L18P_5 | OUTPUT | LVDS_25 | 5 | |
| E24 | VSI_out_N<23> | IOBS | IO_L27N_5 | OUTPUT | LVDS_25 | 5 | |
| E25 | VSI_out_P<23> | IOBM | IO_L27P_5 | OUTPUT | LVDS_25 | 5 | |
| E26 | VSI_out_N<29> | IOBS | IO_L29N_5 | OUTPUT | LVDS_25 | 5 | |
| E3 | data_G13<3> | IOB | IO_L24P_CC_LC_6 | INPUT | HSTL_III_DCI | 6 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| E4 | data_G13<2> | IOB | IO_L22N_6 | INPUT | HSTL_III_DCI | 6 | |
| E5 | data_G13<1> | IOB | IO_L18N_6 | INPUT | HSTL_III_DCI | 6 | |
| E6 | data_G14<3> | IOB | IO_L18P_6 | INPUT | HSTL_III_DCI | 6 | |
| E7 | data_G15<3> | IOB | IO_L17P_6 | INPUT | HSTL_III_DCI | 6 | |
| E8 | | | VCCO_6 | | | 6 | |
| E9 | data_G15<2> | IOB | IO_L7P_6 | INPUT | HSTL_III_DCI | 6 | |
| F1 | data_G16<1> | IOB | IO_L26N_6 | INPUT | HSTL_III_DCI | 6 | |
| F10 | tick_G15 | IOB | IO_L5P_6 | INPUT | HSTL_III_DCI | 6 | |
| F11 | mcb_data_p<12> | IOB | IO_L2N_D28_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F12 | mcb_data_p<13> | IOB | IO_L2P_D29_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F13 | mcb_data_p<14> | IOB | IO_L1N_D30_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F14 | mcb_data_p<15> | IOB | IO_L1P_D31_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F15 | mcb_data_p<10> | IOB | IO_L3N_D26_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F16 | mcb_data_p<11> | IOB | IO_L3P_D27_LC_1 | BIDIR | LVCMOS25 | 1 | |
| F17 | VSI_out_N<2> | IOBS | IO_L5N_5 | OUTPUT | LVDS_25 | 5 | |
| F18 | VSI_out_P<15> | IOBM | IO_L11P_5 | OUTPUT | LVDS_25 | 5 | |
| F19 | VSI_out_N<7> | IOBS | IO_L17N_5 | OUTPUT | LVDS_25 | 5 | |
| F2 | | | VCCO_6 | | | 6 | |
| F20 | VSI_out_P<11> | IOBM | IO_L19P_5 | OUTPUT | LVDS_25 | 5 | |
| F21 | | | GND | | | | |
| F22 | | | VCCO_5 | | | 5 | |
| F25 | | | VCCO_5 | | | 5 | |
| F26 | VSI_out_P<29> | IOBM | IO_L29P_5 | OUTPUT | LVDS_25 | 5 | |
| F3 | clk_G13 | IOB | IO_L27N_6 | INPUT | HSTL_III_DCI | 6 | |
| F4 | data_G13<0> | IOB | IO_L27P_6 | INPUT | HSTL_III_DCI | 6 | |
| F5 | | | VCCO_6 | | | 6 | |
| F6 | | | GND | | | | |
| F7 | data_G04<3> | IOB | IO_L19P_6 | INPUT | HSTL_III_DCI | 6 | |
| F8 | tick_G04 | IOB | IO_L10P_6 | INPUT | HSTL_III_DCI | 6 | |
| F9 | data_G15<0> | IOB | IO_L7N_6 | INPUT | HSTL_III_DCI | 6 | |
| G1 | data_G16<0> | IOB | IO_L30N_6 | INPUT | HSTL_III_DCI | 6 | |
| G10 | clk_G04 | IOB | IO_L9P_CC_LC_6 | INPUT | HSTL_III_DCI | 6 | |
| G11 | | | CS_B_0 | | | | |
| G12 | | | D_IN_0 | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| G13 | | | TDN_0 | | | | |
| G14 | | | CCLK_0 | | | | |
| G15 | | | INIT_0 | | | | |
| G16 | | | HSWAPEN_0 | | | | |
| G19 | VSI_out_P<7> | IOBM | IO_L17P_5 | OUTPUT | LVDS_25 | 5 | |
| G2 | clk_G16 | IOB | IO_L30P_6 | INPUT | HSTL_III_DCI | 6 | |
| G20 | VSI_out_N<12> | IOBS | IO_L22N_5 | OUTPUT | LVDS_25 | 5 | |
| G21 | VSI_out_N<16> | IOBS | IO_L23N_VRP_5 | OUTPUT | LVDS_25 | 5 | |
| G22 | VSI_out_P<16> | IOBM | IO_L23P_VRN_5 | OUTPUT | LVDS_25 | 5 | |
| G23 | VSI_out_N<26> | IOBS | IO_L28N_VREF_5 | OUTPUT | LVDS_25 | 5 | |
| G24 | VSI_out_P<26> | IOBM | IO_L28P_5 | OUTPUT | LVDS_25 | 5 | |
| G25 | VSI_out_N<31> | IOBS | IO_L31N_5 | OUTPUT | LVDS_25 | 5 | |
| G26 | VSI_out_P<31> | IOBM | IO_L31P_5 | OUTPUT | LVDS_25 | 5 | |
| G4 | tick_G13 | IOB | IO_L28P_6 | INPUT | HSTL_III_DCI | 6 | |
| G7 | data_G04<2> | IOB | IO_L19N_6 | INPUT | HSTL_III_DCI | 6 | |
| G8 | data_G04<1> | IOB | IO_L10N_6 | INPUT | HSTL_III_DCI | 6 | |
| G9 | data_G04<0> | IOB | IO_L9N_CC_LC_6 | INPUT | HSTL_III_DCI | 6 | |
| H1 | tick_G16 | IOB | IO_L32N_6 | INPUT | HSTL_III_DCI | 6 | |
| H10 | | | VCCO_6 | | | 6 | |
| H11 | | | VCCAUX | | | | |
| H12 | | | RDWR_B_0 | | | | |
| H13 | | | TDP_0 | | | | |
| H14 | | | DONE_0 | | | | |
| H15 | | | PROGRAM_B_0 | | | | |
| H16 | | | VCCAUX | | | | |
| H17 | | | VCCAUX | | | | |
| H18 | | | VCCO_5 | | | 5 | |
| H19 | | | VCCO_5 | | | 5 | |
| H2 | data_G16<3> | IOB | IO_L32P_6 | INPUT | HSTL_III_DCI | 6 | |
| H20 | VSI_out_P<12> | IOBM | IO_L22P_5 | OUTPUT | LVDS_25 | 5 | |
| H21 | VSI_out_N<24> | IOBS | IO_L26N_5 | OUTPUT | LVDS_25 | 5 | |
| H22 | VSI_out_P<24> | IOBM | IO_L26P_5 | OUTPUT | LVDS_25 | 5 | |
| H23 | VSI_out_N<27> | IOBS | IO_L30N_5 | OUTPUT | LVDS_25 | 5 | |
| H24 | VSI_out_P<27> | IOBM | IO_L30P_5 | OUTPUT | LVDS_25 | 5 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| H25 | VSI_out_N<17> | IOBS | IO_L32N_5 | OUTPUT | LVDS_25 | 5 | |
| H26 | VSI_out_P<17> | IOBM | IO_L32P_5 | OUTPUT | LVDS_25 | 5 | |
| H9 | | | VCCO_6 | | | 6 | |
| J10 | | | VCCINT | | | | |
| J11 | | | VCCINT | | | | |
| J12 | | | VCCAUX | | | | |
| J13 | | | GND | | | | |
| J14 | | | GND | | | | |
| J15 | | | VCCO_0 | | | 0 | |
| J16 | | | VCCINT | | | | |
| J17 | | | VCCINT | | | | |
| J19 | | | VCCO_5 | | | 5 | |
| J20 | VSI_out_N<33> | IOBS | IO_L1N_9 | OUTPUT | LVDS_25 | 9 | |
| J21 | VSI_out_P<33> | IOBM | IO_L1P_9 | OUTPUT | LVDS_25 | 9 | |
| J22 | VSI_out_N<30> | IOBS | IO_L2N_9 | OUTPUT | LVDS_25 | 9 | |
| J23 | VSI_out_P<30> | IOBM | IO_L2P_9 | OUTPUT | LVDS_25 | 9 | |
| J24 | | | GND | | | | |
| J25 | VSI_out_N<32> | IOBS | IO_L4N_VREF_9 | OUTPUT | LVDS_25 | 9 | |
| J26 | VSI_out_P<32> | IOBM | IO_L4P_9 | OUTPUT | LVDS_25 | 9 | |
| J3 | | | GND | | | | |
| J8 | | | VCCO_6 | | | 6 | |
| K10 | | | VCCINT | | | | |
| K11 | | | GND | | | | |
| K12 | | | GND | | | | |
| K13 | | | GND | | | | |
| K14 | | | GND | | | | |
| K15 | | | GND | | | | |
| K16 | | | GND | | | | |
| K17 | | | VCCINT | | | | |
| K18 | | | VCCINT | | | | |
| K19 | | | VCCO_9 | | | 9 | |
| K20 | VSI_out_N<35> | IOBS | IO_L5N_9 | OUTPUT | LVDS_25 | 9 | |
| K21 | VSI_out_N<34> | IOBS | IO_L3N_9 | OUTPUT | LVDS_25 | 9 | |
| K22 | VSI_out_P<34> | IOBM | IO_L3P_9 | OUTPUT | LVDS_25 | 9 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| K23 | VSI_out_N<39> | IOBS | IO_L7N_9 | OUTPUT | LVDS_25 | 9 | |
| K24 | VSI_out_P<39> | IOBM | IO_L7P_9 | OUTPUT | LVDS_25 | 9 | |
| K6 | tick_G03 | IOB | IO_L3N_10 | INPUT | HSTL_III_DCI | 10 | |
| K7 | data_G03<3> | IOB | IO_L3P_10 | INPUT | HSTL_III_DCI | 10 | |
| K8 | | | VCCO_10 | | | 10 | |
| K9 | | | VCCINT | | | | |
| L10 | | | VCCINT | | | | |
| L11 | | | VCCINT | | | | |
| L12 | | | GND | | | | |
| L13 | | | GND | | | | |
| L14 | | | GND | | | | |
| L15 | | | GND | | | | |
| L16 | | | VCCINT | | | | |
| L17 | | | VCCINT | | | | |
| L18 | | | VCCINT | | | | |
| L19 | VSI_out_P<35> | IOBM | IO_L5P_9 | OUTPUT | LVDS_25 | 9 | |
| L2 | | | VCCO_10 | | | 10 | |
| L20 | VSI_out_N<0> | IOBS | IO_L6N_9 | OUTPUT | LVDS_25 | 9 | |
| L21 | VSI_out_P<0> | IOBM | IO_L6P_9 | OUTPUT | LVDS_25 | 9 | |
| L22 | | | VCCO_9 | | | 9 | |
| L23 | VSI_out_N<36> | IOBS | IO_L10N_9 | OUTPUT | LVDS_25 | 9 | |
| L24 | VSI_out_P<36> | IOBM | IO_L10P_9 | OUTPUT | LVDS_25 | 9 | |
| L25 | | | VCCO_9 | | | 9 | |
| L26 | VSI_out_P<37> | IOBM | IO_L12P_9 | OUTPUT | LVDS_25 | 9 | |
| L3 | data_G03<2> | IOB | IO_L8N_CC_LC_10 | INPUT | HSTL_III_DCI | 10 | |
| L4 | data_G07<3> | IOB | IO_L8P_CC_LC_10 | INPUT | HSTL_III_DCI | 10 | |
| L5 | | | VCCO_10 | | | 10 | |
| L6 | data_G03<1> | IOB | IO_L5N_10 | INPUT | HSTL_III_DCI | 10 | |
| L7 | data_G03<0> | IOB | IO_L5P_10 | INPUT | HSTL_III_DCI | 10 | |
| L8 | clk_G03 | IOB | IO_L9N_CC_LC_10 | INPUT | HSTL_III_DCI | 10 | |
| L9 | | | VCCINT | | | | |
| M1 | tick_G12 | IOB | IO_L11N_10 | INPUT | HSTL_III_DCI | 10 | |
| M10 | | | GND | | | | |
| M11 | | | GND | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| M12 | | | VCCINT | | | |
| M13 | | | GND | | | |
| M14 | | | GND | | | |
| M15 | | | VCCINT | | | |
| M16 | | | GND | | | |
| M17 | | | GND | | | |
| M18 | | | VCCO_9 | | | 9 |
| M2 | clk_G12 | IOB | IO_L11P_10 | INPUT | HSTL_III_DCI | 10 |
| M20 | VSI_out_N<20> | IOBS | IO_L13N_9 | OUTPUT | LVDS_25 | 9 |
| M21 | VSI_out_P<20> | IOBM | IO_L13P_9 | OUTPUT | LVDS_25 | 9 |
| M22 | VSI_out_N<38> | IOBS | IO_L14N_9 | OUTPUT | LVDS_25 | 9 |
| M23 | VSI_out_P<38> | IOBM | IO_L14P_9 | OUTPUT | LVDS_25 | 9 |
| M24 | VSI_in_N<0> | IOB | IO_L11N_9 | INPUT | LVDS_25 | 9 |
| M25 | VSI_in_P<0> | IOB | IO_L11P_9 | INPUT | LVDS_25 | 9 |
| M26 | VSI_out_N<37> | IOBS | IO_L12N_VREF_9 | OUTPUT | LVDS_25 | 9 |
| M4 | data_G07<2> | IOB | IO_L12P_10 | INPUT | HSTL_III_DCI | 10 |
| M5 | data_G07<1> | IOB | IO_L13N_10 | INPUT | HSTL_III_DCI | 10 |
| M6 | data_G07<0> | IOB | IO_L13P_10 | INPUT | HSTL_III_DCI | 10 |
| M7 | tick_G07 | IOB | IO_L17N_10 | INPUT | HSTL_III_DCI | 10 |
| M8 | clk_G07 | IOB | IO_L9P_CC_LC_10 | INPUT | HSTL_III_DCI | 10 |
| M9 | | | VCCAUX | | | |
| N1 | | | VCCO_10 | | | 10 |
| N10 | | | GND | | | |
| N11 | | | GND | | | |
| N12 | | | GND | | | |
| N13 | | | GND | | | |
| N14 | | | GND | | | |
| N15 | | | GND | | | |
| N16 | | | GND | | | |
| N17 | | | GND | | | |
| N18 | | | VCCAUX | | | |
| N2 | data_G12<3> | IOB | IO_L14N_10 | INPUT | HSTL_III_DCI | 10 |
| N20 | VSI_out_N<3> | IOBS | IO_L17N_9 | OUTPUT | LVDS_25 | 9 |
| N21 | VSI_out_P<3> | IOBM | IO_L17P_9 | OUTPUT | LVDS_25 | 9 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| N22 | VSI_in_N<2> | IOB | IO_L16N_9 | INPUT | LVDS_25 | 9 | |
| N23 | VSI_in_P<2> | IOB | IO_L16P_9 | INPUT | LVDS_25 | 9 | |
| N24 | VSI_in_N<1> | IOB | IO_L15N_9 | INPUT | LVDS_25 | 9 | |
| N25 | VSI_in_P<1> | IOB | IO_L15P_9 | INPUT | LVDS_25 | 9 | |
| N26 | | | GND | | | | |
| N3 | data_G12<2> | IOB | IO_L14P_10 | INPUT | HSTL_III_DCI | 10 | |
| N4 | data_G12<1> | IOB | IO_L15N_10 | INPUT | HSTL_III_DCI | 10 | |
| N5 | data_G12<0> | IOB | IO_L15P_10 | INPUT | HSTL_III_DCI | 10 | |
| N6 | | | GND | | | | |
| N7 | data_G17<3> | IOB | IO_L17P_10 | INPUT | HSTL_III_DCI | 10 | |
| N8 | data_G17<2> | IOB | IO_L19N_10 | INPUT | HSTL_III_DCI | 10 | |
| N9 | | | VCCAUX | | | | |
| P1 | | | GND | | | | |
| P10 | | | GND | | | | |
| P11 | | | GND | | | | |
| P12 | | | GND | | | | |
| P13 | | | GND | | | | |
| P14 | | | GND | | | | |
| P15 | | | GND | | | | |
| P16 | | | GND | | | | |
| P17 | | | GND | | | | |
| P18 | | | VCCAUX | | | | |
| P19 | VSI_in_N<8> | IOB | IO_L21N_9 | INPUT | LVDS_25 | 9 | |
| P2 | data_G02<2> | IOB | IO_L16N_10 | INPUT | HSTL_III_DCI | 10 | |
| P20 | VSI_in_P<8> | IOB | IO_L21P_9 | INPUT | LVDS_25 | 9 | |
| P21 | | | GND | | | | |
| P22 | VSI_in_N<4> | IOB | IO_L19N_9 | INPUT | LVDS_25 | 9 | |
| P23 | VSI_in_P<4> | IOB | IO_L19P_9 | INPUT | LVDS_25 | 9 | |
| P24 | VSI_in_N<3> | IOB | IO_L18N_9 | INPUT | LVDS_25 | 9 | |
| P25 | VSI_in_P<3> | IOB | IO_L18P_9 | INPUT | LVDS_25 | 9 | |
| P26 | | | VCCO_9 | | | 9 | |
| P3 | data_G02<3> | IOB | IO_L16P_10 | INPUT | HSTL_III_DCI | 10 | |
| P4 | tick_G02 | IOB | IO_L18N_10 | INPUT | HSTL_III_DCI | 10 | |
| P5 | data_G17<1> | IOB | IO_L18P_10 | INPUT | HSTL_III_DCI | 10 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P6 | data_G17<0> | IOB | IO_L21N_10 | INPUT | HSTL_III_DCI | 10 | |
| P7 | clk_G17 | IOB | IO_L21P_10 | INPUT | HSTL_III_DCI | 10 | |
| P8 | tick_G17 | IOB | IO_L19P_10 | INPUT | HSTL_III_DCI | 10 | |
| P9 | | | VCCAUX | | | | |
| R1 | data_G02<1> | IOB | IO_L22N_10 | INPUT | HSTL_III_DCI | 10 | |
| R10 | | | GND | | | | |
| R11 | | | GND | | | | |
| R12 | | | VCCINT | | | | |
| R13 | | | GND | | | | |
| R14 | | | GND | | | | |
| R15 | | | VCCINT | | | | |
| R16 | | | GND | | | | |
| R17 | | | GND | | | | |
| R18 | | | VCCAUX | | | | |
| R2 | data_G02<0> | IOB | IO_L22P_10 | INPUT | HSTL_III_DCI | 10 | |
| R23 | VSI_in_N<7> | IOB | IO_L22N_9 | INPUT | LVDS_25 | 9 | |
| R24 | VSI_in_P<7> | IOB | IO_L22P_9 | INPUT | LVDS_25 | 9 | |
| R25 | VSI_in_N<5> | IOB | IO_L20N_VREF_9 | INPUT | LVDS_25 | 9 | |
| R26 | VSI_in_P<5> | IOB | IO_L20P_9 | INPUT | LVDS_25 | 9 | |
| R4 | clk_G02 | IOB | IO_L20P_10 | INPUT | HSTL_III_DCI | 10 | |
| R7 | clk_G08 | IOB | IO_L25N_CC_LC_10 | INPUT | HSTL_III_DCI | 10 | |
| R8 | tick_G08 | IOB | IO_L25P_CC_LC_10 | INPUT | HSTL_III_DCI | 10 | |
| R9 | | | VCCO_10 | | | 10 | |
| T10 | | | VCCINT | | | | |
| T11 | | | VCCINT | | | | |
| T12 | | | GND | | | | |
| T13 | | | GND | | | | |
| T14 | | | GND | | | | |
| T15 | | | GND | | | | |
| T16 | | | VCCINT | | | | |
| T17 | | | VCCINT | | | | |
| T18 | | | VCCINT | | | | |
| T19 | VSI_in_N<11> | IOB | IO_L31N_9 | INPUT | LVDS_25 | 9 | |
| T2 | | | VCCO_10 | | | 10 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| T20 | TC_N<1> | IOBS | IO_L30N_9 | OUTPUT | LVDS_25 | 9 | |
| T21 | TC_P<1> | IOBM | IO_L30P_9 | OUTPUT | LVDS_25 | 9 | |
| T22 | | | VCCO_9 | | | 9 | |
| T23 | VSI_in_N<9> | IOB | IO_L24N_CC_LC_9 | INPUT | LVDS_25 | 9 | |
| T24 | VSI_in_P<9> | IOB | IO_L24P_CC_LC_9 | INPUT | LVDS_25 | 9 | |
| T25 | | | VCCO_9 | | | 9 | |
| T26 | VSI_in_P<6> | IOB | IO_L26P_9 | INPUT | LVDS_25 | 9 | |
| T4 | data_G08<3> | IOB | IO_L26P_10 | INPUT | HSTL_III_DCI | 10 | |
| T5 | | | VCCO_10 | | | 10 | |
| T6 | data_G08<2> | IOB | IO_L27N_10 | INPUT | HSTL_III_DCI | 10 | |
| T7 | data_G08<1> | IOB | IO_L27P_10 | INPUT | HSTL_III_DCI | 10 | |
| T8 | data_G08<0> | IOB | IO_L31P_10 | INPUT | HSTL_III_DCI | 10 | |
| T9 | | | VCCINT | | | | |
| U1 | data_G11<3> | IOB | IO_L24P_CC_LC_10 | INPUT | HSTL_III_DCI | 10 | |
| U10 | | | VCCINT | | | | |
| U11 | | | GND | | | | |
| U12 | | | GND | | | | |
| U13 | | | GND | | | | |
| U14 | | | GND | | | | |
| U15 | | | GND | | | | |
| U16 | | | GND | | | | |
| U17 | | | VCCINT | | | | |
| U18 | | | VCCINT | | | | |
| U19 | | | VCCO_9 | | | 9 | |
| U20 | VSI_in_P<11> | IOB | IO_L31P_9 | INPUT | LVDS_25 | 9 | |
| U21 | VSI_in_N<10> | IOB | IO_L29N_9 | INPUT | LVDS_25 | 9 | |
| U22 | VSI_in_P<10> | IOB | IO_L29P_9 | INPUT | LVDS_25 | 9 | |
| U23 | VSI_in_P<14> | IOB | IO_L27P_9 | INPUT | LVDS_25 | 9 | |
| U24 | VSI_in_N<12> | IOB | IO_L28N_VREF_9 | INPUT | LVDS_25 | 9 | |
| U25 | VSI_in_P<12> | IOB | IO_L28P_9 | INPUT | LVDS_25 | 9 | |
| U26 | VSI_in_N<6> | IOB | IO_L26N_9 | INPUT | LVDS_25 | 9 | |
| U3 | data_G11<2> | IOB | IO_L28P_10 | INPUT | HSTL_III_DCI | 10 | |
| U4 | clk_G11 | IOB | IO_L29N_10 | INPUT | HSTL_III_DCI | 10 | |
| U5 | tick_G11 | IOB | IO_L32N_10 | INPUT | HSTL_III_DCI | 10 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| U6 | tick_G18 | IOB | IO_L32P_10 | INPUT | HSTL_III_DCI | 10 | |
| U7 | clk_G18 | IOB | IO_L31N_10 | INPUT | HSTL_III_DCI | 10 | |
| U8 | | | VCCO_10 | | | 10 | |
| U9 | | | VCCINT | | | | |
| V1 | data_G11<1> | IOB | IO_L30N_10 | INPUT | HSTL_III_DCI | 10 | |
| V10 | | | VCCINT | | | | |
| V11 | | | VCCINT | | | | |
| V12 | | | VCCO_0 | | | 0 | |
| V13 | | | GND | | | | |
| V14 | | | GND | | | | |
| V15 | | | VCCAUX | | | | |
| V16 | | | VCCINT | | | | |
| V17 | | | VCCINT | | | | |
| V19 | | | VCCO_7 | | | 7 | |
| V2 | data_G11<0> | IOB | IO_L30P_10 | INPUT | HSTL_III_DCI | 10 | |
| V20 | VSI_in_N<15> | IOB | IO_L5N_7 | INPUT | LVDS_25 | 7 | |
| V23 | VSI_in_N<14> | IOB | IO_L27N_9 | INPUT | LVDS_25 | 9 | |
| V24 | | | GND | | | | |
| V25 | VSI_in_N<13> | IOB | IO_L32N_9 | INPUT | LVDS_25 | 9 | |
| V26 | VSI_in_P<13> | IOB | IO_L32P_9 | INPUT | LVDS_25 | 9 | |
| V3 | | | GND | | | | |
| V4 | data_G18<3> | IOB | IO_L29P_10 | INPUT | HSTL_III_DCI | 10 | |
| V5 | data_G18<2> | IOB | IO_L2N_8 | INPUT | HSTL_III_DCI | 8 | |
| V6 | data_G18<1> | IOB | IO_L2P_8 | INPUT | HSTL_III_DCI | 8 | |
| V7 | data_G18<0> | IOB | IO_L3N_8 | INPUT | HSTL_III_DCI | 8 | |
| V8 | | | VCCO_8 | | | 8 | |
| W1 | tick_G01 | IOB | IO_L1N_8 | INPUT | HSTL_III_DCI | 8 | |
| W10 | | | VCCAUX | | | | |
| W11 | | | VCCAUX | | | | |
| W12 | | | TCK_0 | | | | |
| W13 | | | PWRDWN_B_0 | | | | |
| W14 | | | M2_0 | | | | |
| W15 | | | M0_0 | | | | |
| W16 | | | VCCAUX | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| W17 | | | VCCO_7 | | | 7 | |
| W18 | | | VCCO_7 | | | 7 | |
| W19 | VSI_in_N<35> | IOB | IO_L18N_7 | INPUT | LVDS_25 | 7 | |
| W2 | clk_G01 | IOB | IO_L1P_8 | INPUT | HSTL_III_DCI | 8 | |
| W20 | VSI_in_P<15> | IOB | IO_L5P_7 | INPUT | LVDS_25 | 7 | |
| W21 | VSI_in_P<18> | IOB | IO_L3P_7 | INPUT | LVDS_25 | 7 | |
| W22 | VSI_in_N<18> | IOB | IO_L3N_7 | INPUT | LVDS_25 | 7 | |
| W23 | VSI_in_P<17> | IOB | IO_L4P_7 | INPUT | LVDS_25 | 7 | |
| W24 | VSI_in_N<17> | IOB | IO_L4N_VREF_7 | INPUT | LVDS_25 | 7 | |
| W25 | VSI_in_P<16> | IOB | IO_L2P_7 | INPUT | LVDS_25 | 7 | |
| W26 | VSI_in_N<16> | IOB | IO_L2N_7 | INPUT | LVDS_25 | 7 | |
| W4 | data_G01<3> | IOB | IO_L4P_8 | INPUT | HSTL_III_DCI | 8 | |
| W5 | data_G01<2> | IOB | IO_L5N_8 | INPUT | HSTL_III_DCI | 8 | |
| W6 | data_G01<1> | IOB | IO_L5P_8 | INPUT | HSTL_III_DCI | 8 | |
| W7 | data_G01<0> | IOB | IO_L3P_8 | INPUT | HSTL_III_DCI | 8 | |
| W8 | | | VCCO_8 | | | 8 | |
| W9 | | | VCCO_8 | | | 8 | |
| Y1 | clk_G09 | IOB | IO_L6N_8 | INPUT | HSTL_III_DCI | 8 | |
| Y10 | odata_100PPS | IOB | IO_L27P_8 | OUTPUT | HSTL_III_DCI | 8 | |
| Y11 | | | TMS_0 | | | | |
| Y12 | | | TDI_0 | | | | |
| Y13 | | | TDO_0 | | | | |
| Y14 | | | DOUT_BUSY_0 | | | | |
| Y15 | | | M1_0 | | | | |
| Y16 | | | VBATT_0 | | | | |
| Y19 | VSI_in_P<35> | IOB | IO_L18P_7 | INPUT | LVDS_25 | 7 | |
| Y2 | tick_G09 | IOB | IO_L6P_8 | INPUT | HSTL_III_DCI | 8 | |
| Y20 | VSI_in_P<22> | IOB | IO_L20P_7 | INPUT | LVDS_25 | 7 | |
| Y21 | VSI_in_N<22> | IOB | IO_L20N_VREF_7 | INPUT | LVDS_25 | 7 | |
| Y22 | VSI_in_P<21> | IOB | IO_L12P_7 | INPUT | LVDS_25 | 7 | |
| Y23 | VSI_in_N<21> | IOB | IO_L12N_VREF_7 | INPUT | LVDS_25 | 7 | |
| Y24 | VSI_in_N<20> | IOB | IO_L8N_CC_LC_7 | INPUT | LVDS_25 | 7 | |
| Y25 | VSI_in_P<19> | IOB | IO_L6P_7 | INPUT | LVDS_25 | 7 | |
| Y26 | VSI_in_N<19> | IOB | IO_L6N_7 | INPUT | LVDS_25 | 7 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Y3 | data_G09<3> | IOB | IO_L8N_CC_LC_8 | INPUT | HSTL_III_DCI | 8 |
| Y4 | data_G09<2> | IOB | IO_L8P_CC_LC_8 | INPUT | HSTL_III_DCI | 8 |
| Y5 | tick_G10 | IOB | IO_L9N_CC_LC_8 | INPUT | HSTL_III_DCI | 8 |
| Y6 | clk_G10 | IOB | IO_L9P_CC_LC_8 | INPUT | HSTL_III_DCI | 8 |
| Y8 | data_G10<2> | IOB | IO_L26N_8 | INPUT | HSTL_III_DCI | 8 |
| Y9 | data_G10<1> | IOB | IO_L21N_8 | INPUT | HSTL_III_DCI | 8 |

**Table 7-2 Pinout by Pin Number**

## 7.3 Xilinx XC4VSX35-10FF668-CS2 Package Drawing

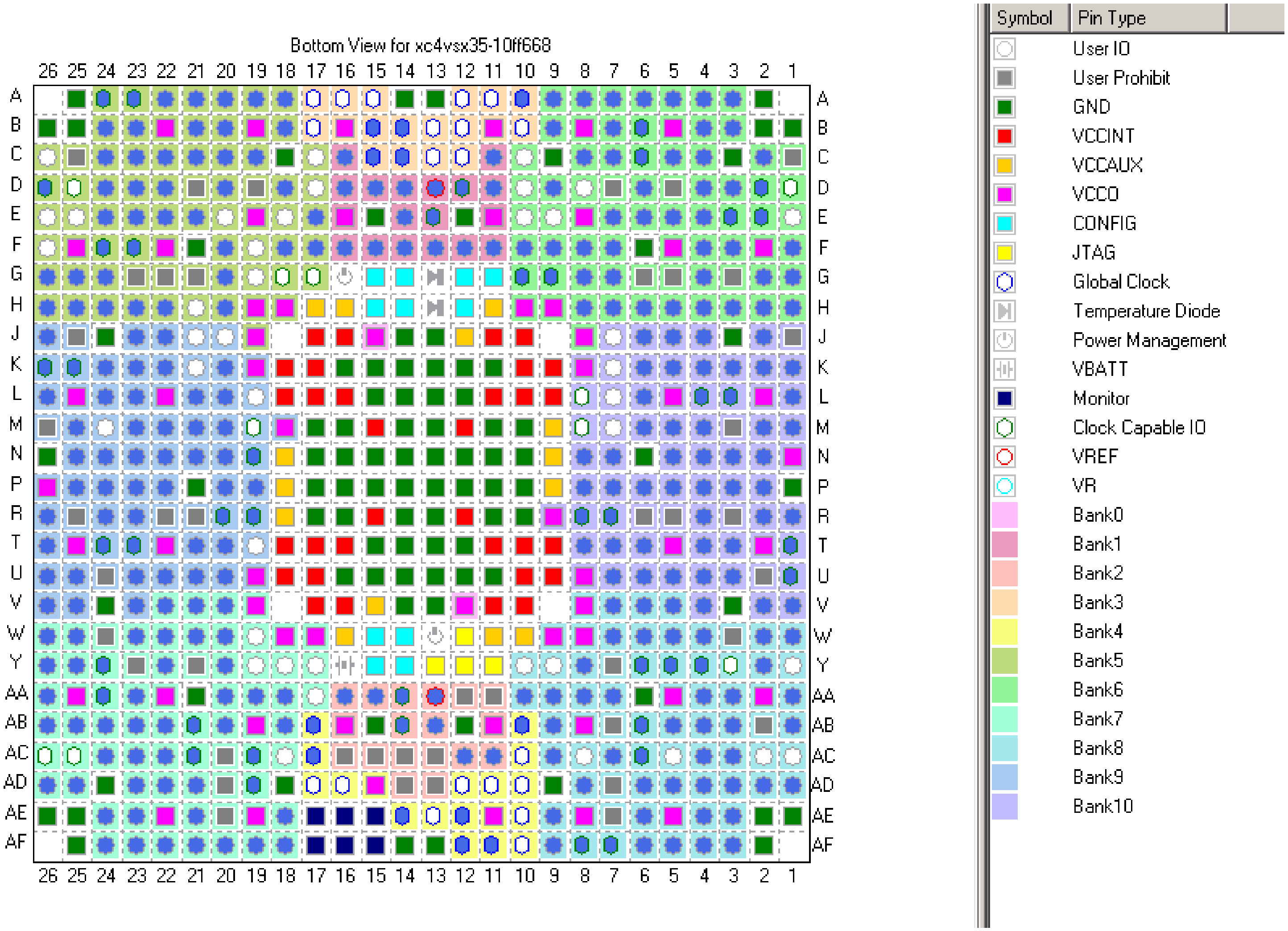


**Figure 7-1 Pin Location**

### 7.4 Programming Notes

All FPGAs on the Station Board are programmed through their 8-bit wide configuration port. The Station Board CMIB software requires the Binary (.bin) output file to program the Xilinx FPGAs. This is set by selecting “Properties…” from the “Process” pull-down menu in the Xilinx ISE software. Select the “General Options” and check “Create Binary Configuration File”.

# 8 References

Brent Carlson, “Refined EVLA WIDAR Correlator Architecture”, NRC-EVLA Memo# 014, October 2, 2001.

Heng Zhang, “TIMECODE and Clock External Interface Specification”, ICD A25022N0090, February 22, 2005.

# 9 Index