TEST AND VERIFICATION PLAN

Prototype Station Board

TVP Document: **A25040N0004**

Revision: 1.1

Dave Fort, 12 December 2007

National Research Council Canada
Herzberg Institute of Astrophysics
Dominion Radio Astrophysical Observatory

P.O. Box 248, 717 White Lake Rd
Penticton, BC, Canada
V2A 6J9

Table of Contents

List of Figures

List of Abbreviations and Acronyms

CBE	Correlator Back End
CMIB	Correlator Module Interface Board
DLL	Delay Locked Loop
DUT	Device Under Test
ESD	Electro-Static Discharge
EVLA	Expanded Very Large Array
FORM	Fibre Optic Receiver Module
FPGA	Field Programmable Gate Array
IOB	Input Output Buffer
ISR	Interrupt Service Routine
JTAG	Joint Test Action Group (Boundary Scan Architecture)
MHz	Megahertz (10^6 cycles per second)
Ms/s	Mega Samples per Second
MTBF	Mean Time Before Failure
Mw/s	Mega Words per Second
PCB	Printed Circuit Board
PLL	Phase Locked Loop
RFI	Radio Frequency Interference
TCGB	Time Code Generator Board
VLBA	Very Long Baseline Array
VLBI	Very Long Baseline Interferometry
WIDAR	Wideband Interferometric Digital ARchitecture

Revision History

Revision	Date	Changes/Notes	Author
1.0	15 May 2007	Expand HW tests	D. Fort
1.1	12 Dec 2007	Add Functional Test Tables	D. Fort

1 Introduction

This document expands on the Station Board Test Plan (A25040N0003) in that it gives a more detailed description of testing the Prototype Station Board.
The stages in this plan are as follows:

1. PCB testing.
2. Functionality testing.
3. Comparison testing.
4. Automatic testing.

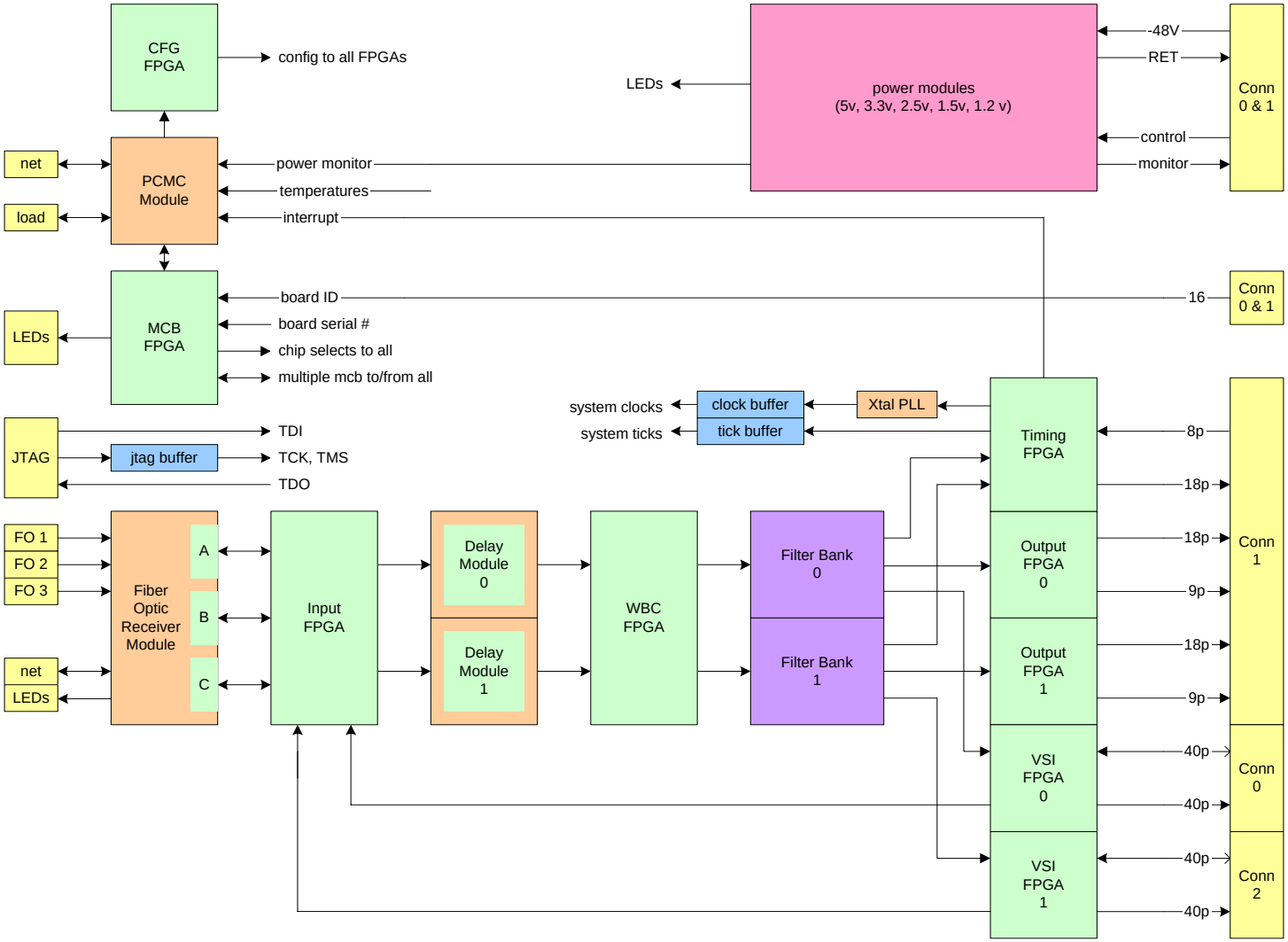

Figure 3-1 Station Board block diagram

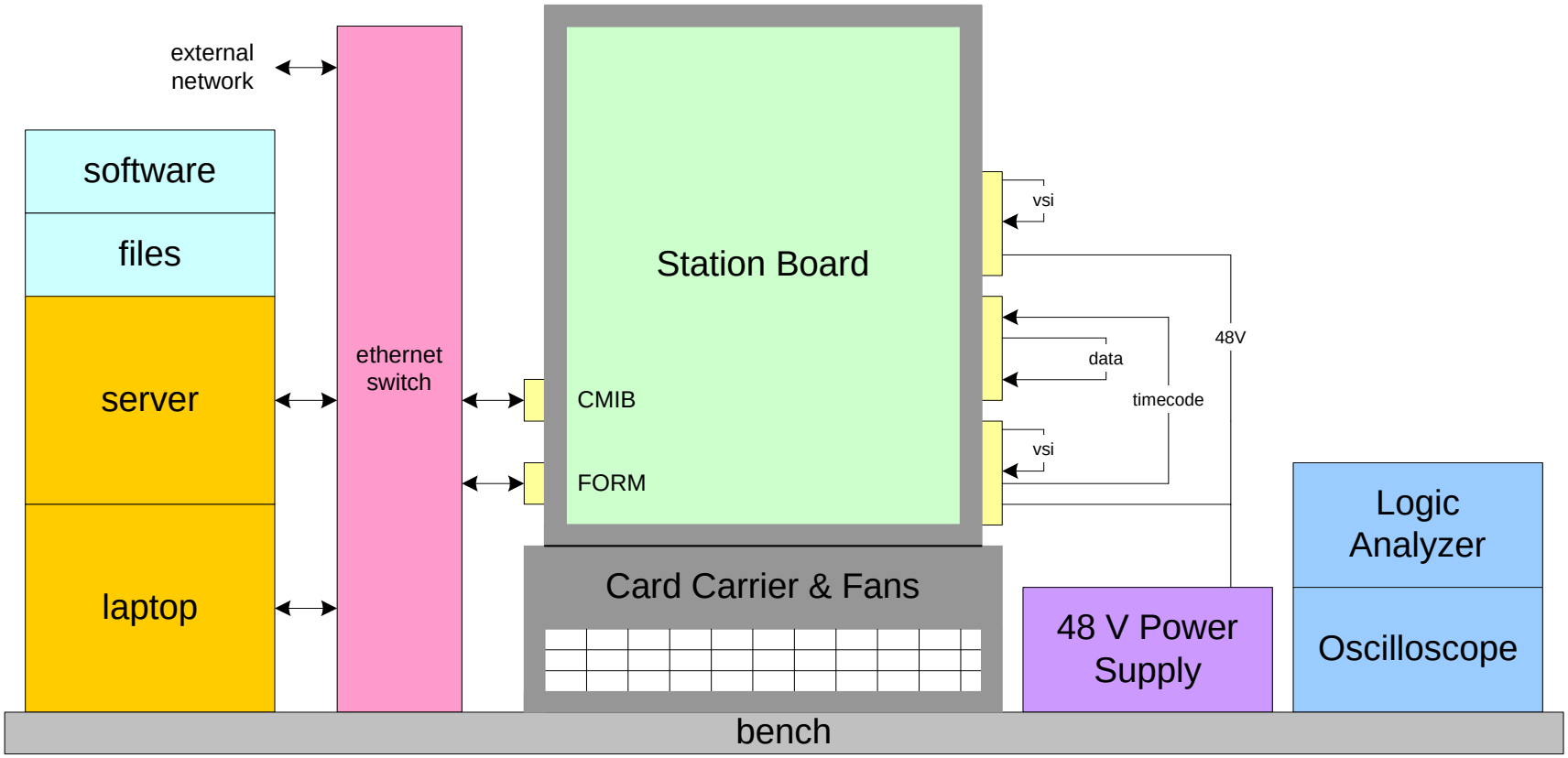

Figure 3-2 Prototype Station Board test setup

2 PCB Testing

This section is concerned with testing the printed circuit board (PCB) without worrying about the detailed functioning of the FPGAs. If all of these tests succeed, then the PCB must be OK and all copper interconnects are functioning at speed.

2.1 Pre-configuration Board Tests

Description
Check front panel mechanical
Check heat sink mechanical
Check board insertion mechanics
Check power supply voltages
Check maximum voltage drop on each power plane
Check PCMC operation
Check voltage monitors and LEDs
Check temperature monitors
Check loading of all FPGAs
Check that JTAG test can be performed
Check writing and reading of test register on each FPGA
Check backplane Board ID bits can be read
Check the board serial number

2.2 Post-configuration Board Tests

Description
After simple configuration:
Check clock distribution using FPGA status bits
Check tick distribution using time interval counters on FPGAs
Check interconnections at speed using CRC scheme
Check clock edge selection
Check Raltron operation
After 4-stage filter configuration
Check power consumption using 48V current meter
Check standby mode for all FPGAs
Check software resets for all FPGAs

3 Functional Testing

This section is concerned with whether the FPGAs are producing the correct output. This is the most difficult part of the testing.

3.1 MCB FPGA Tests

Description
Check write operation
Check read operation

3.2 CFG FPGA Tests

Description
Check configuration operation
Check individual configuration scheme

3.3 FORM Tests

Description
Check TPG operation using PRN generator
Check TPG operation using data files
Check CRC operation (bit select and CRC output)
Check validity propagation

3.4 Input FPGA Tests

Description
Check ability to load and read back translation tables
Check 4-bit state counts using single state translation tables
Check 8-bit state counts using single state translation tables
Check data conversion using FORM TPG
Check internal TPG operation
Check data path crossbar switch using FORM TPG, VSI and internal TPG
Check selection of FORM or VSI input
Check band selection of state counters
Check output format
Check noise diode on/off generator
Check validity propagation
Check antenna pps time interval counter and CMIB indicator

3.5 Delay Module Tests

Description
Check test vector loading and output
Check delay operation using FORM TPG, Filter FPGA TEX
Check delay error output
Check validity propagation
Check delay function for 4, 8, 16, 32 and 64-bit “samples”

3.6 WBC FPGA Tests

Description
Check cross-correlation function using internal TPG
Check cross-correlation function for different data organizations (bands and bits)
Check cross-correlation function using DM files
Check selection of inputs to cross-correlation using DM files

3.7 Filter FPGA Tests

Description
Check ability to load and read back all LUTs
Check 1st stage 4-bit operation using WBC Delta TPG
Check 2nd, 3rd, 4th stage using WBC Delta TPG
Check flipper, quantizer using WBC Delta TPG
Check all measurement values
Check one FPGA produces constant measurements with time
Check that all Filter FPGAs produce the same measurements
Check state counter
Check phase error output to Timing FPGA
Check phase error timing to Timing FPGA
Check wide band delay using WBC Delta TPG with TEX
Check 1st stage 8-bit operation
Check 1st stage fractional bit operation
Check mixer stage operation
Check AC balance operation
Check bit 7 valid operation
Check invalid stretchers
Check RFI detection operation
Check input rates < 256 Mwords/s

3.8 Timing FPGA Tests

Description
Check external clock selection
Check system clock output
Check system tick output
Check system pps output
Check interrupt operation
Check interrupt delay
Check interrupt delay range
Connect all Gb/s outputs (4 wafers at a time) to Baseline Board
Check TIMECODE
Check DUMPTRIG
Check PHASEMOD
Check PHASERR

3.9 Output FPGA Tests

Description
Check recording mode operation
Check recording mode operation sub-band selection
Check pulsar gate generation
Check pulsar gate invalidation
Check timed and “permanent” invalidation
Check ID insertion using Baseline Board
Check crossbar switch using Baseline Board
Check Gb/s outputs using Baseline Board

3.10 VSI FPGA Tests

Description
Check VSI loop back operation
Check PPSCODE generation for testing

4 Comparison Testing

This section deals with a relatively simple method of testing that is also quite powerful and informative. It requires that some sort of data processing is going on but not that the processing is correct. It requires that relevant quantities are saved to a file usually after some integration. Special purpose software would then compare the quantities that should be the same inside the file or compare the file with another produced under the same conditions. It may even be possible to compare the file with one produced by a simulator. The 'relevant' quantities are those that contain measurements (CRC values, state counts, power, time intervals, …) made by some or all of the FPGAs with the same input and configured the same way on a given board or across multiple boards. It would be useful to be able to continue the comparison over a long period of time to look for intermittent problems. It is also necessary that the configuration parameters need to be set so that the quantities compared have non-trivial values.

The quantities that can and should be compared are:

1. All time interval measurements
2. All CRC values
3. All status values
4. Input FPGA state counts
5. Filter FPGA clip counts
6. Filter FPGA pre-requantizer power measurements
7. Filter FPGA RFI counts
8. Filter FPGA post-requantizer state counts
9. Filter FPGA post-requantizer power measurements
10. Filter FPGA post-requantizer tone extractor results
11. WBC FPGA products
12. Output FPGA radar mode data
13. Timing FPGA phase error data (not yet implemented)

5 Automatic Testing

This type of testing, which is an extension of comparison testing, would be used during production of new boards to be sure that all parts of the board function correctly and to help determine the faulty parts if errors are found. The same tests could be used during EVLA operation to repair faulty boards. These tests would be performed in a small system including PPSCODE generation (XBAR Board), STNBs and BSLBs interconnected to allow testing of all board inputs and outputs. In production testing, it would be preferable to have a FORM in place to test its connections to the Input FPGA but this may be impractical. It is assumed that the Delay Modules and PCMC are in place.

It is desired that the operator start a program or script, a sequence of tests are performed and a report is generated saying 'YAY' or 'NAY'. If NAY, the report would contain the tests that failed and the parts that need replacing or the areas that need physical scrutiny, perhaps using an X-ray machine. A few things must be determined visually such as the LEDs (power and status indicators).

The sequence of tests would change the configuration of the board and may download special bit files, different from those used during normal operation. The sequence would first check the correct functioning of the STNBs and the BSLBs. The output of the STNBs are checked by the BSLBs. The output of the BSLBs are checked by the CBE.

The following is a list of test categories – exception details will come later. Only one new board is inserted into the test rack at a time (once we have a set of working boards).

1. Power on system and perform ‘smoke’ test.
2. JTAG test – could be done in another place but needs power.
3. Check all PCMCs by reboot.
4. Check download and other functions of the PCMC FPGA.
5. Check all voltage and temperature monitors and repeat at intervals.
6. Check that DC-DC converters can be turned off and on (CPCC).
7. Check voltage LEDs visually with human speed pattern.
8. Check download of FPGA bit files using DONE bits.
9. Check write/read to all FPGAs using designated 16-bit register.
10. Check status LEDs visually with human speed pattern.
11. Check reception of time codes and 64 MHz clocks by Timing FPGA.
12. Check operation of crystal PLL with and without 64 MHz clocks – Timing FPGA.
13. Check existence of system clock at all FPGAs.
14. Check existence of system tick using time interval measurements at all FPGAs.
15. Perform CRC tests using special bit files that wiggle all lines.
16. Generate test output sequences for the BSLBs – Timing and Output FPGAs.

This could be the end of the tests if we believe that the rest of the FPGA works because all interconnections have been tested and all FPGA input/output pins have been used. However, one or more high level functional tests probably need to be performed to test more of the FPGAs on the STNBs and the Correlator Chip and FPGAs on the BSLBs. This would likely take the form of comparing the BSLB output frames with a ‘golden’ file. This would test both the STNB and the BSLB. The ‘radar mode’ of the STNB could also be compared with a ‘golden’ file to help to decide between the STNB and the BSLB as a source of any errors. This type of test would probably use Delay Module test vector sets.

In order to determine the location of the error on the STNB further tests would be necessary.

6 Software Testing

During the above testing the software itself will get a fairly thorough testing. One type of software error that might not get tested so thoroughly is its error reporting. The FPGAs on the Station Board have the ability to generate errors by altering status bits and CRC values. The tester can create errors by writing a binary bit mask to status or CRC registers (which would normally be read only) and observing the reaction of software to these errors. The software should notice errors and generate error messages. A value of 1 in the mask inverts the corresponding bit in the value read. The mask is set to zero on reset and retains any value written to it until another reset or write. This behaviour forces the CMIB to throttle its error messages by (say) counting the number of a given error message per second before reporting.

6.1 Output Table Tests

Description
Check Input State Counts Table
Check Clip Count Table
Check Power Table
Check RFI Count Table
Check Filter State Counts Table
Check Tone Extractor Table
Check WBC Products Table
Check Radar Data Table
Check TIC Table
Check CRC Table
Check Status Table

6.2 Main GUI Tests

Description
Check board level GUI
Check Input FPGA GUI
Check Delay FPGA GUI
Check WBC FPGA GUI
Check Filter FPGA GUI
Check Timing FPGA GUI
Check Output FPGA GUI
Check VSI FPGA GUI

6.3 RTDD GUI Tests

Description
Check CRC RTDD GUI
Check Input FPGA RTDD GUI
Check WBC FPGA RTDD GUI
Check Filter FPGA RTDD GUI
Check Output FPGA RTDD GUI
Check Diagnostic RTDD GUI

6.4 Model Tests

Description
Check BB Delay Model
Check SB Delay Model
Check SB Phase Model => PHASEMOD
Check SB Tone Model
Check SB Mixer Model
Check DUMPTRIG Generation (simple, recirculation, pulsar)
Check Pulsar Gate Model
Check Noise Diode Switching Model

6.5 High Level Tests

Description
Check interrupt enable/disable
Check Configuration Save and Restore
Check Observation RUN/HALT
Check FPGA Programming
Check board reset
Check board reboot
Check LUT loading/verification
Check Standby (Cool) mode
Check Output Table enable/disable)

7 References

All information referenced in this document can be found at
Station Board Documents
http://www.drao-ofr.hia-iha.nrc-cnrc.gc.ca/science/widar/private/Station_Board.html