

REQUIREMENTS AND FUNCTIONAL SPECIFICATION

Station Board

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List of Abbreviations and Acronyms

CMIB	Correlator Monitor & control Interface Board
eMERLIN	expanded Multi-Element Radio Linked Interferometer Network
EVLA	Expanded Very Large Array
FIFO	First-In-First-Out
FORM	Fiber Optic Receiver Module
FOTS	Fiber Optic Transmission System
FPGA	Field Programmable Gate Array
ISR	Interrupt Service Routine
LVDS	Low Voltage Differential Signaling
PCB	Printed Circuit Board
PCMC	PC/104 Monitor/Control Mezzanine Card
PLL	Phase Locked Loop
RFI	Radio Frequency Interference
TGB	TIMECODE Generator Box
VLA	Very Large Array
VLBA	Very Long Baseline Array
VLBI	Very Long Baseline Interferometry
WIDAR	Wideband Interferometric Digital ARchitecture

1 Revision History

Revision	Date	Changes/Notes	Author
0.0	13 Nov 2003	Initial Draft	D. Fort

2 Introduction

This document describes an overview of the requirements and design concepts for the station board. Detailed requirements and design concepts are presented in separate documents for each component of the board.

Background on the station board can be found in NRC-EVLA Memo #014 (EVLA Memo 31).

The development plan for the station board is as follows:

1. Develop and test a prototype station board together with the other elements of the correlator both in Penticton and on the sky at the VLA.
2. Go into production.

3 Context

The station board is the main module of the station sub-system. It requires four station boards to process the data from one antenna. Each board processes the data from one of the four base band pairs (normally from the right and left circularly polarized feeds).

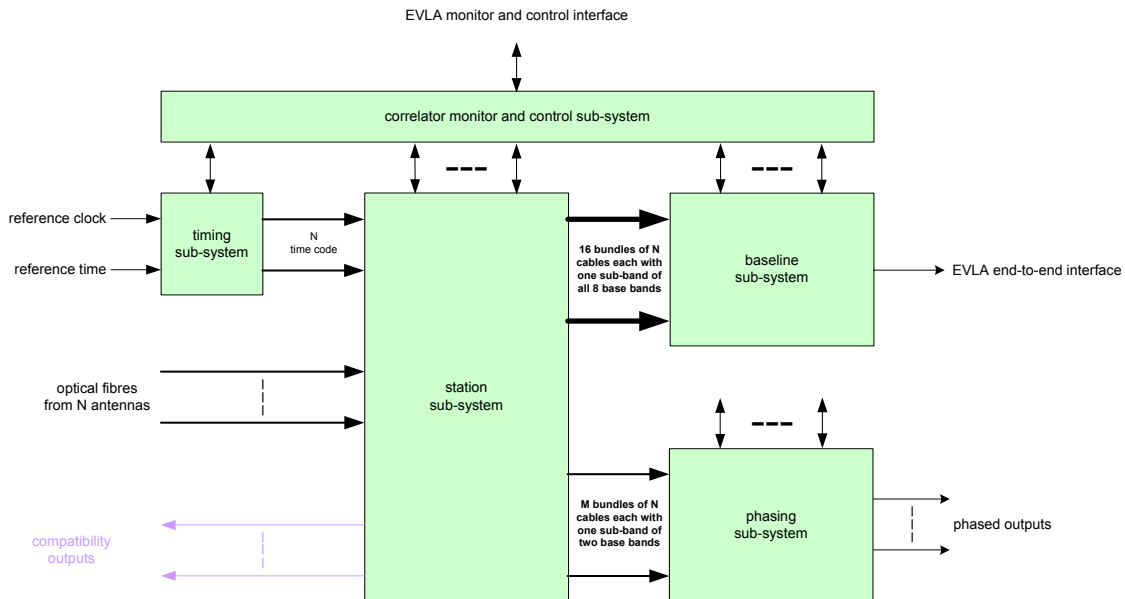


Figure 3-1 Block diagram of the WIDAR Correlator.

4 Overview

A simplified input/output diagram of the station board is shown below.

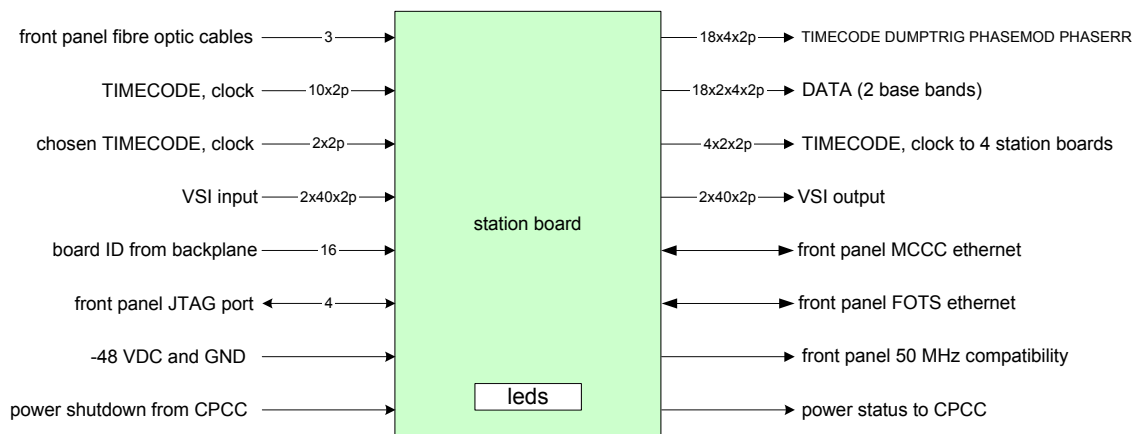


Figure 4-1 Input/Output diagram of the station board.

Each station board will receive two 2 GHz base bands when digitized to 3-bit samples or one 1 GHz base band when digitized to 8-bit samples. The Fiber Optic Receiver Module supplied by NRAO will convert from fiber to copper to produce two 64(48)-bit wide data paths, one for each base band (3-bit case) or one 64-bit wide data path (8-bit case). The main functions of the station board are to delay the data to compensate for the path length differences suffered by the RF signals arriving at different antennas due to geometry and to divide the base bands into 16 manageable sub-bands, attaching timing and model information and then sending the results to the baseline sub-system.

The 64 incoming data lines can be arranged in multiple ways as listed in the table below.

Bands	Width (MHz)	Streams	Bits	Mode
1	2048	16	4	1
2	1024	8	4	2
4	512	4	4	3
8	256	2	4	4
16	$128/2^n$ n=0,...12	1	4	5
1	1024	8	8	6
2	512	4	8	7
4	256	2	8	8
8	$128/2^n$ n=0,...12	1	8	9

Table 4-1 Input data organizations.

Modes 1 and 6 are the standard EVLA data organizations. Mode 7 is for the 8-bit eMERLIN case. Mode 5 could be used by the current (recording) VLBA and represents cases where the bandwidth is 128 MHz or less. The others are included for completeness. The station board chips should deal with all of the above organizations, if possible.

- 4.1 **Timing Input Signals**
- 4.2 **Wideband Input Signals**
- 4.3 **Sub-band Output Signals**

5 Requirements

The following is a list of station board requirements.

5.1 Functional Requirements

The detailed functional requirements for the individual chips are given in the corresponding RFS.

5.2 Performance Requirements

5.3 Environmental Requirements

5.4 Interface Requirements

5.4.1 *MCB Interface Chip Map*

Address	Chip	BB	SB
0x0000	Decode		
0x0100	FORM	R&L	
0x0200	Input	A&B	
0x0300	Delay Module	A	
0x0400	Delay Module	B	
0x0500	Autocor	A&B	
0x0600	Filter	A	0
0x0700	Filter	A	1
0x0800	Filter	A	2
0x0900	Filter	A	3
0x0A00	Filter	A	4
0x0B00	Filter	A	5
0x0C00	Filter	A	6
0x0D00	Filter	A	7
0x0E00	Filter	A	8
0x0F00	Filter	A	9
0x1000	Filter	A	10

Address	Chip	BB	SB
0x1100	Filter	A	11
0x1200	Filter	A	12
0x1300	Filter	A	13
0x1400	Filter	A	14
0x1500	Filter	A	15
0x1600	Filter	A	16
0x1700	Filter	A	17
0x1800	Filter	B	0
0x1900	Filter	B	1
0x1A00	Filter	B	2
0x1B00	Filter	B	3
0x1C00	Filter	B	4
0x1D00	Filter	B	5
0x1E00	Filter	B	6
0x1F00	Filter	B	7
0x2000	Filter	B	8
0x2100	Filter	B	9
0x2200	Filter	B	10
0x2300	Filter	B	11
0x2400	Filter	B	12
0x2500	Filter	B	13
0x2600	Filter	B	14

Address	Chip	BB	SB
0x2700	Filter	B	15
0x2800	Filter	B	16
0x2900	Filter	B	17
0x2A00	Timing	A&B	
0x2B00	Output	A	
0x2C00	Output	B	
0x2D00	Record	A&B	
0x2E00	Playback	R&L	

Table 5-1 Chip Address Map.

5.4.2 PC/104 Monitor/Control Mezzanine Card (PCMC)

MCB

JTAG

FPGA

5.4.3 Fiber Optic Receiver Module (FORM)

5.4.4 Timecode Generator Box (TGB)

5.4.5 VLBI Standard Interface (VSI)

6 Functional Specifications

A simplified block diagram of the station board is shown below.

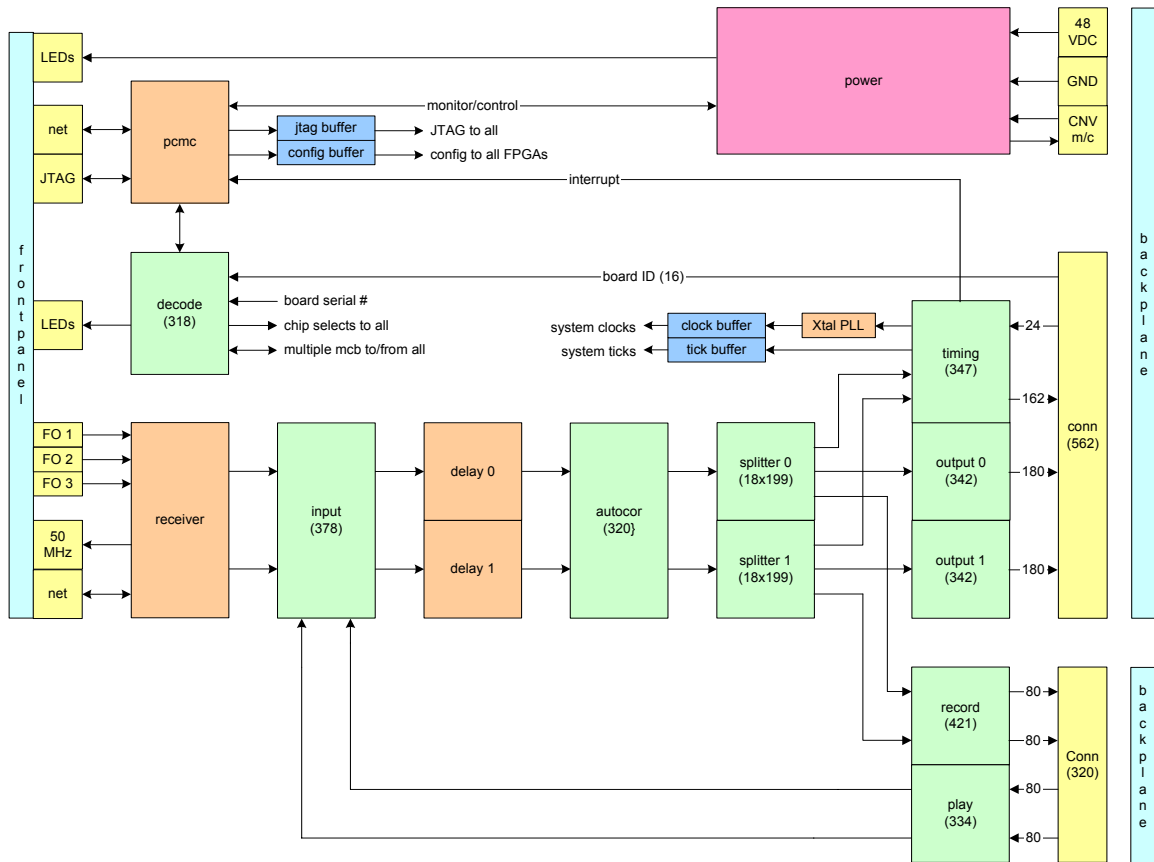


Figure 6-1 Block diagram of the station board

6.1 Mechanical Design

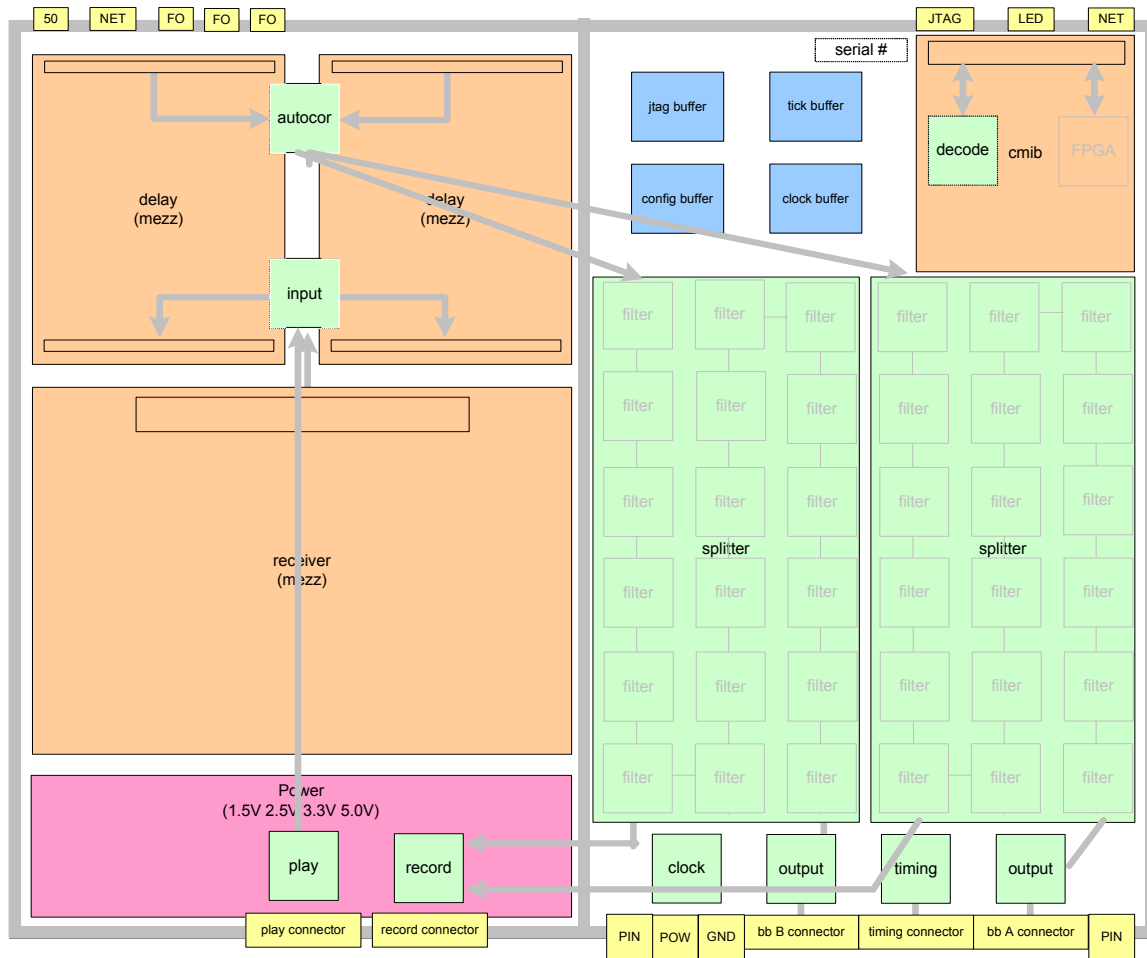


Figure 6-2 Possible Layout of the station board

6.2 Timing Distribution

The EVLA correlator uses four station boards for each antenna. One of the four boards is the “master” and it produces all of the sub-band timing signals. The other three boards are identical but their timing signals are not connected to anything. On the other hand, eMERLIN uses only one station board per antenna and it is the master. The TGB sends each master station board two sets of 4 TIMECODEs plus 64 MHz clock. The *timing* chip on the master chooses which of the two sets (and which of the 4 TIMECODEs in that set) to use and sends copies of the chosen signals to each of the boards connected to the same antenna (including itself). Each board receives the chosen TIMECODE and clock, decodes TIMECODE and sends the clock to a crystal PLL. The PLL is used to produce a low jitter 128 MHz board clock locked to the VLA frequency standard. The decoded TIMECODE is used to produce the board PPS, board TICK (10 millisecond period) and CMIB interrupt.

The board clock, TICK and PPS define the time on the board. The board TICK represents the actual time on the board and should occur at the same time for all boards in the whole correlator, apart from cable length differences (which are compensated for by the baseline board). The board PPS and the actual time label for the board TICK does not have to be the same over the whole correlator (as would be the case for simultaneous real-time and recorded experiments). The TICK may also represent different time intervals as would occur for recorded experiments that are being played back faster than real time (note that only 10 millisecond point-slope model updates times are supported). The TIMECODE received by the master station board can be delayed by the TGB in units of 10 milliseconds to account for the transmission time of the data from the antennas over the FOTS. Normally, the TGB would be told to delay the TIMECODE by an amount that is longer than the longest possible transmission delay plus the longest possible difference in the arrival times of the astronomical signals. This delay cannot exceed 0.26 seconds, the capacity of the Delay Modules on the station board. The CMIBs (via supplied models) instruct the delay modules to delay a particular base band so that the same received wave front emerges from the corresponding delay module for all antennas in a sub-array.

The Fiber Optic Receiver Module (FORM) decodes the data from the antenna that arrives at the station board on three fibers. In addition, the FORM buffers the data and clocks it out to the *input* chip using a 64 MHz version of the board clock supplied by the station board. The data from the antenna is accompanied by an antenna PPS (to which noise diode switching is synchronized). This PPS may occur close to UTC at the antenna but this does not matter. The antenna PPS is measured against the board PPS for diagnostic purposes only (the time interval between the two PPSs should stay constant). The *input* chip will add the board TICK and board PPS it receives (suitably delayed to account for the pipeline delay of the chip) to the data stream that goes to the Delay Module.

The same scheme applies to all the chips – each chip will add the board TICK it receives (suitably delayed to account for the pipeline delay of the chip) to the data stream that goes to the next chip. Note that the delay module receives the board PPS and the antenna PPS so that it can check its operation; otherwise the PPSs are not necessary and are not supplied to the remaining chips in the chain. The pipeline delay of the Delay Module will be about 70 microseconds and that of the filter chip could be as large as 275 microseconds (for the 31.25 KHz bandwidth). A chip could use the TICK accompanying the data to derive the output TICK but using the board TICK is probably better for initial testing of the board (it does not depend on the correct functioning of the previous chip) along with a measurement of the time interval between the two.

The total pipeline delay could be as large as 345 microseconds and since the models and other functions depend on the delayed board TICK, the interrupt to the CMIB should not occur until the longest delayed board TICK occurs. A suitably delayed interrupt will be produced by the timing chip using a delay provided by the CMIB. This delay shortens the available interrupt time by $\sim 1/3$ of a millisecond. The filter chip has a mixer in stage 2 and a tone extractor after all the stages. Both of these functions require CMIB models

but have different pipeline delays; therefore, a pipelined TICK will accompany the data even inside the chip to assure that the models are applied at the correct time.

Only one TIMECODE accompanies the data on the sub-band cable that connects a station board to a baseline board; therefore, *timing* chip contains a programmable delay line to delay TIMECODE by the pipeline delay of the processing chain thereby matching the data (same for DUMPTRIG, PHASEMOD and PHASERR). This same cable carries all eight base bands that could have different sub-band bandwidths; therefore, the filter chip contains a 256-microsecond programmable delay line that allows wide bands to match the timing of the narrowest possible band.

6.3 Power Distribution

6.4 PCMC Interface

6.5 Data Distribution

The high-speed signals on the station board are connected point-to-point, probably with HSTL. The high-speed clocks are also point-to-point using LVDS. The lower speed signals (the MCB interface, the FPGA configuration interface and the JTAG interface) are point-to-multi-point probably limited to a fan-out of about six. The data interface between chips consists of 4-bit nibbles or 64-bit parallel samples as well as valid, noise diode on/off, a 10-millisecond “tick” running at 256 Mbits/s and a 128 MHz clock. Given the problems caused by path delays in the FPGAs, it is probably prudent to clock in the data on both edges of the clock and retain the doublewide result running at 128 MHz rather singlewide at 256 MHz. In some cases, the filter chip, for example, it may be necessary to run internally at 256 MHz to conserve resources. Running at a clock rate of 256 MHz will likely require extensive floor planning in current FPGAs.

Other signals that come to each chip are the board 128 MHz clock and the board 10-millisecond tick. The purpose of the board 128 MHz clock is to prevent the build-up of clock jitter that would likely occur if the clock were passed from chip to chip. The input of each chip will then have a small FIFO. Data is written into the FIFO by the clock that accompanies the data and read from the FIFO by the board clock. The internal clock (and the clock that accompanies the data to the next chip) is derived from the board clock. The write address for the FIFO is synchronized by the tick that accompanies the data and the read address is synchronized by the board tick. The board TICK delay is set by the CMIB to account for the preceding accumulated pipeline delay and any trace delay. This arrangement considerably relaxes the routing of the station PCB because the copper traces for the data and accompanying signals do not need to be a specific length (although they need to be the same length as each other). The board clock and board tick traces can also be any length as long as they are the same as each other. There is also a board PPS which is given to the *input* FPGA and then passed on to the delay modules to allow measurement against the antenna PPS coming from the FORM.

In order to assess signal integrity problems, each chip will generate 4-bit CRCs for a selected data bit stream on both the input and output of the chip. The CRC will be generated in the same way for all chips and latched on the tick. The CMIB can then compare the CRC at the output of one chip against the CRC for the same bit stream at the input of the next chip. Involving the CRC in this way does not require any additional wires between the chips. Hopefully, the FORM can also implement this scheme. Doing so would require that the *input* FPGA send the FORM a tick and that the FORM return the same tick, suitable pipelined, with the data it sends to the input FPGA.

6.6 Front Panel

6.7 Rear Connectors

6.8 Provisions for VLBI

6.9 Provisions for Phased Arrays

7 References

Brent Carlson, "Refined EVLA WIDAR Correlator Architecture", NRC-EVLA Memo# 014, October 2, 2001.

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