REQUIREMENTS AND FUNCTIONAL SPECIFICATION

Station Board Input FPGA

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List of Abbreviations and Acronyms

CMIB	Correlator Monitor & control Interface Board
CRC	Cyclic Redundancy Check
DCM	Digital Clock Manager.
eMERLIN	Expanded Multi-Element Radio-Linked Interferometer Network
EVLA	Expanded Very Large Array
FIFO	First In First Out.
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
FORM	Fiber Optical Receiver Module (Revel's board)
HSTL	High Speed Transceiver Logic
ISR	Interrupt Service Routine
LVTTL	Low Voltage Transistor-Transistor Logic
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed Circuit Board
PPS	Pulse Per Second (one pulse per second).
PPS/10	Pulse Per Second/10 (one pulse every 10 seconds).
RAM	Random Access Memory
RFI	Radio Frequency Interference
SB	Station Board
SBIC	Station Board Input Chip
TBD	To Be Determined
TPG	Test Pattern Generator
VLBA	Very Long Baseline Array
VLBI	Very Long Baseline Interferometry
VSI	VLBI Standard Interface
WIDAR	Wideband Interferometric Digital ARchitecture

1 Revision History

Revision	Date	Changes/Notes	Author
0.0	15 Nov 2003	Initial Draft	D. Fort
0.1	27 Aug 2004	Updated initial Draft for review	Z.Ljusic
0.2	10 Sep 2004	Implemented changes based on the peer review	Z.Ljusic
1.0	1 March 2005	Corrected a typo within memory map section	Z. Ljusic
2.0	13 April 2007	Implemented changes based on the prototype testing, mainly within MCB interface.	Z. Ljusic
2.1	April 30, 2007	Added three new registers used in data path fine-tuning on board level.	Z. Ljusic
2.2	22 Nov 2007	The noise diode generation was changed to improve the timing. FORM 'Odd' lines change.	D. Fort
2.3	1 May 2008	Added Test Port Signal Select Registers.	D. Fort
2.4	26 May 2008	Made corrections to version 2.3. Added wide band test pattern generator. Changed Noise Diode ON/OFF generator. Added Noise Diode ON/OFF counters.	D. Fort
2.5	06 Apr 2010	Documentation omission – SW Reset. Added SCLK PLL reset. Added FORM detector. Added clock phase shifter to determine edge value and range. Improved wide band noise generator.	D. Fort
2.6	01 Apr 2011	Added pinouts, etc.	D. Fort

2 Introduction

This document describes detailed requirements and design concepts for the Station Board Input Chip, SBIC. The SBIC takes the data from the Fiber Optic Receiver Module or the VSI input, re-arranges the bits, makes some useful measurements (state counts) and sends the results on to the Delay Module. In addition, the chip can produce output needed to test the Station Board in the absence of the Fiber Optic Receiver Module.

The development plan for the SBIC is as follows:

1. Develop and test the design in an FPGA. The design will be done in Verilog HDL.

3 Context

The SBIC resides on the Station Board. The Station Board receives two wide bands and sends up to 18 narrow bands from each of the wide bands on to the baseline part of the correlator. A simplified block diagram of the Station Board is shown below.

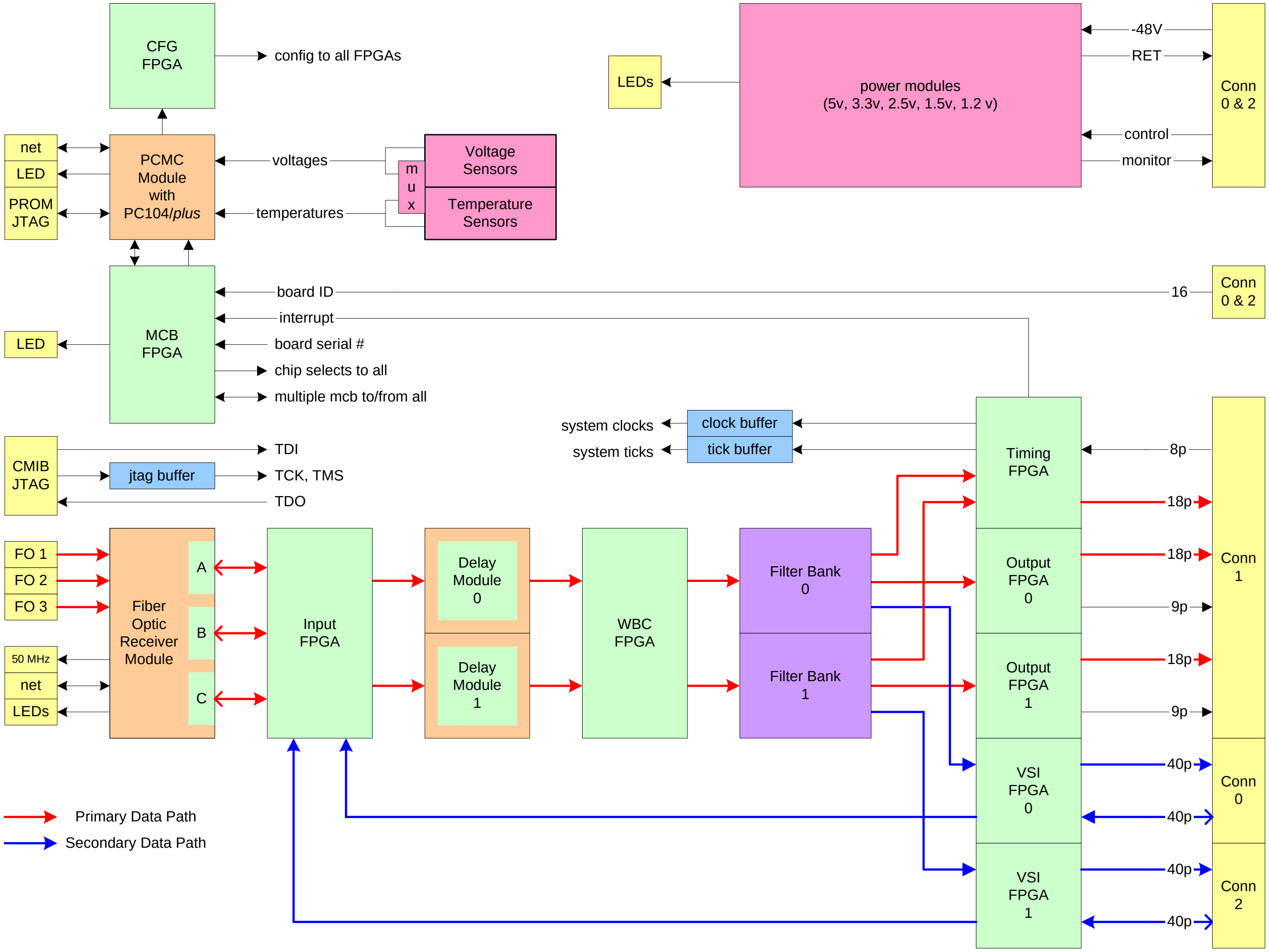


Figure 3-1 Block diagram of the Station Board.

4 Overview

A simplified input/output diagram of the *SBIC* is shown below. The JTAG interface and configuration interface are not shown.

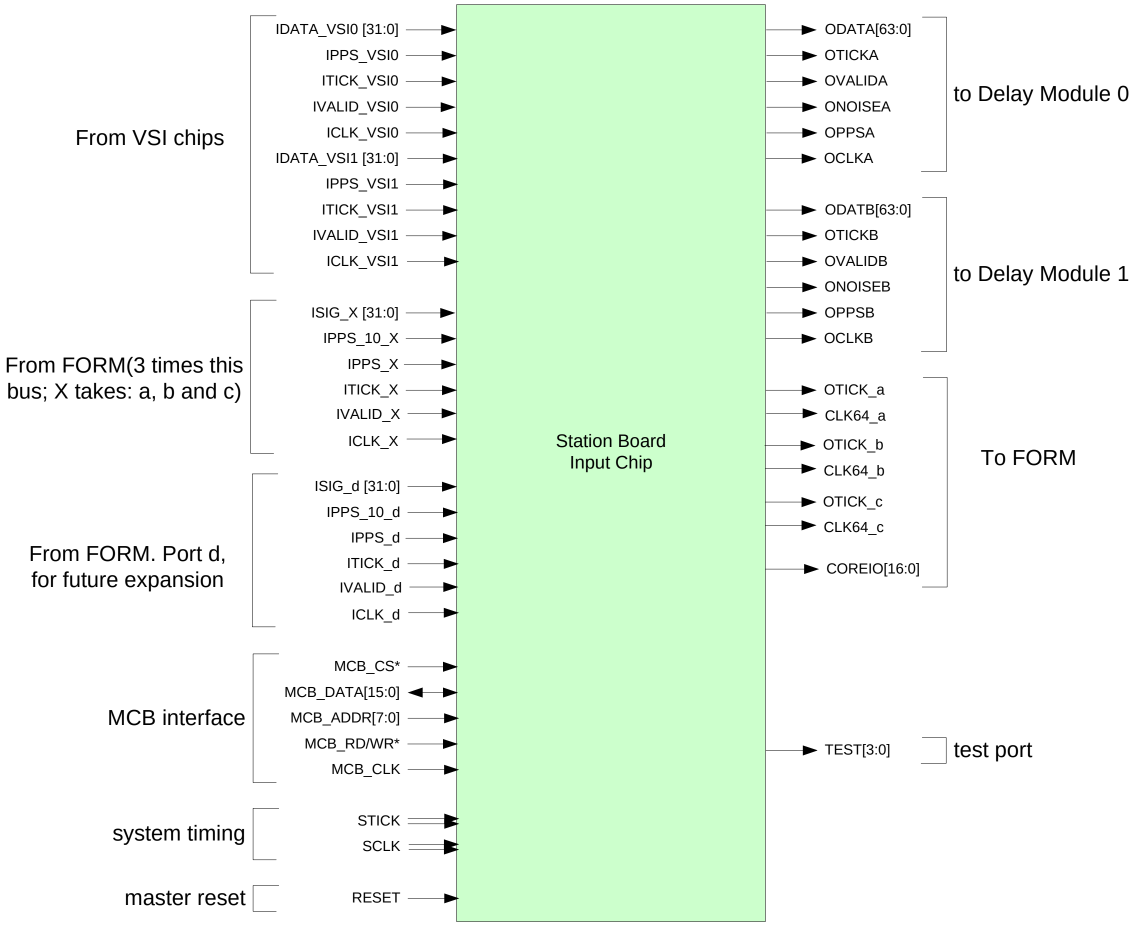


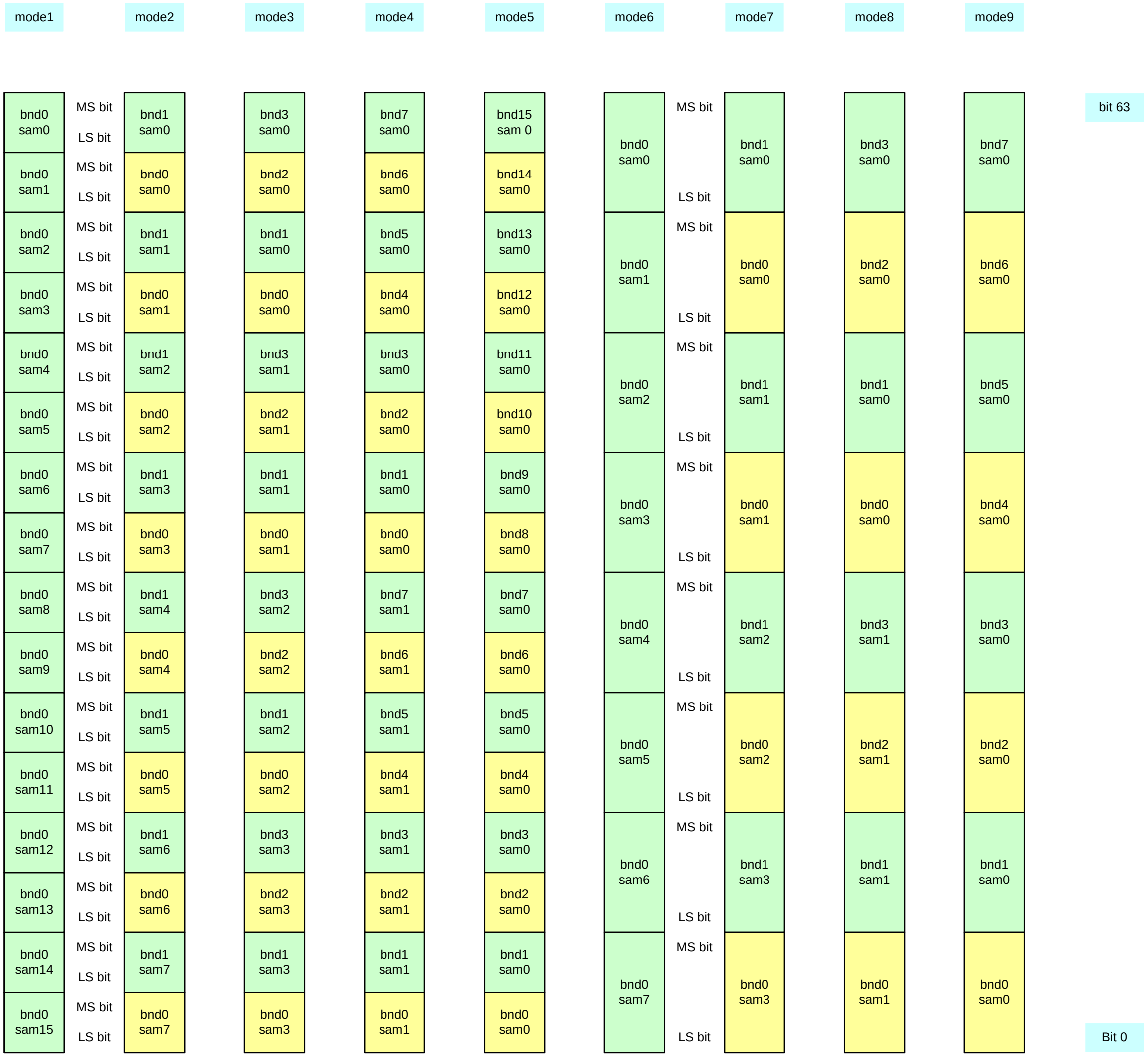
Figure 4-1 Input/Output diagram of the SBIC.

There are three data ports from the FORM board: a, b, and c port. The COREIO 17 bit wide bus is there just in case that the Station Board's CMIB has to take control of the FORM. The current plan does not assume this. The idea is that all the FORMs within the system will be controlled by a separate network.

The 64 output data lines can be arranged in multiple ways as listed in the table below.

Number of Bands	Width (MHz)	Demux Factor	Bits/Sample	Mode
1	2048	16	4	4_16
2	1024	8	4	4_8
4	512	4	4	4_4
8	256	2	4	4_2
16	$128/2^n$ n=0,...12	1	4	4_1
1	1024	8	8	8_8
2	512	4	8	8_4
4	256	2	8	8_2
8	$128/2^n$ n=0,...12	1	8	8_1

Table 4-1 Output data organizations.



mode1		mode2	mode3	mode4	mode5	mode6		mode7	mode8	mode9	
bnd0 sam0	MS bit LS bit	bnd1 sam0	bnd3 sam0	bnd7 sam0	bnd15 sam 0	bnd0 sam0	MS bit	bnd1 sam0	bnd3 sam0	bnd7 sam0	bit 63
bnd0 sam1	MS bit LS bit	bnd0 sam0	bnd2 sam0	bnd6 sam0	bnd14 sam0		LS bit				
bnd0 sam2	MS bit LS bit	bnd1 sam1	bnd1 sam0	bnd5 sam0	bnd13 sam0	bnd0 sam1	MS bit	bnd0 sam0	bnd2 sam0	bnd6 sam0	
bnd0 sam3	MS bit LS bit	bnd0 sam1	bnd0 sam0	bnd4 sam0	bnd12 sam0		LS bit				
bnd0 sam4	MS bit LS bit	bnd1 sam2	bnd3 sam1	bnd3 sam0	bnd11 sam0	bnd0 sam2	MS bit	bnd1 sam1	bnd1 sam0	bnd5 sam0	
bnd0 sam5	MS bit LS bit	bnd0 sam2	bnd2 sam1	bnd2 sam0	bnd10 sam0		LS bit				
bnd0 sam6	MS bit LS bit	bnd1 sam3	bnd1 sam1	bnd1 sam0	bnd9 sam0	bnd0 sam3	MS bit	bnd0 sam1	bnd0 sam0	bnd4 sam0	
bnd0 sam7	MS bit LS bit	bnd0 sam3	bnd0 sam1	bnd0 sam0	bnd8 sam0		LS bit				
bnd0 sam8	MS bit LS bit	bnd1 sam4	bnd3 sam2	bnd7 sam1	bnd7 sam0	bnd0 sam4	MS bit	bnd1 sam2	bnd3 sam1	bnd3 sam0	
bnd0 sam9	MS bit LS bit	bnd0 sam4	bnd2 sam2	bnd6 sam1	bnd6 sam0		LS bit				
bnd0 sam10	MS bit LS bit	bnd1 sam5	bnd1 sam2	bnd5 sam1	bnd5 sam0	bnd0 sam5	MS bit	bnd0 sam2	bnd2 sam1	bnd2 sam0	
bnd0 sam11	MS bit LS bit	bnd0 sam5	bnd0 sam2	bnd4 sam1	bnd4 sam0		LS bit				
bnd0 sam12	MS bit LS bit	bnd1 sam6	bnd3 sam3	bnd3 sam1	bnd3 sam0	bnd0 sam6	MS bit	bnd1 sam3	bnd1 sam1	bnd1 sam0	
bnd0 sam13	MS bit LS bit	bnd0 sam6	bnd2 sam3	bnd2 sam1	bnd2 sam0		LS bit				
bnd0 sam14	MS bit LS bit	bnd1 sam7	bnd1 sam3	bnd1 sam1	bnd1 sam0	bnd0 sam7	MS bit	bnd0 sam3	bnd0 sam1	bnd0 sam0	
bnd0 sam15	MS bit LS bit	bnd0 sam7	bnd0 sam3	bnd0 sam1	bnd0 sam0		LS bit				Bit 0

Figure 4-2 Output data placement.

Modes 1 and 6 are the standard EVLA data organizations. Mode 7 is for the 8-bit eMERLIN case. Mode 5 could be used by the current (recording) VLBA and represents cases where the bandwidth is 128 MHz or less. The others are included for completeness. The Station Board chips should deal with all of the above organizations, if possible.

4.1 System Timing Input Signals

- SCLK is the system 128 MHz clock supplied as an LVDS pair. This clock is a first generation version of the 128 MHz sine wave supplied to the Station Board by the Time Generator Box (RFS Document AN25151N0000). All chips on the Station Board use SCLK in order to prevent the buildup of clock jitter.

- STICK is the system timing tick (10 millisecond period) supplied as an LVDS pair. A delayed version of STICK along with the accompanying tick (ITICK) is used to re-time the input data thereby keeping the output timing constant relative to the system time.

4.2 FORM Wideband Input Signals

Each of the three ports from the FORM consists if the following signals (X takes: a, b and c):

- ICLK_X is a clock that can be used for clocking in its accompanying data.
- ISIG_X [31:0] is 32-bit wide data bus (256 Mb/s rate) clocked in by 2x ICLK.
- IPPS_10_X is clocked in by 2x ICLK (256 MHz). The noise diode switch performs an integral number of cycles in 10 seconds. IPPS/10_X is coincident with one IPPS_X. The length of IPPS/10_X is one half a cycle of ICLK.
- IPPS_X is clocked in by 2x ICLK. This one-second tick may or may not represent actual time at the antenna. The length of IPPS_X is one half a cycle of ICLK.
- ITICK_X is clocked in by 2x ICLK. ITICK_X is a single high bit every tick time (10 milliseconds) and marks the first sample in IDATA_X as being associated with the tick time. The length of ITICK_X is one half a cycle of SCLK.

All these signals are HSTL class III.

4.3 VSI Wideband Input Signals

There are two VSI chips, VSI0 and VSI1, connected to SBIC. The signals described below are the same for both VSI chips.

- ICLK is a clock that can be used for clocking in its accompanying data.
- IDATA [31:0] is clocked in by 2x ICLK.
- IVALID is clocked in by 2x ICLK. If low, the associated data is invalid.
- IPPS is clocked in by 2x ICLK. IPPS is a single high bit every second. The length of ITICK is one half a cycle of SCLK.
- ITICK is clocked in by 2x ICLK. ITICK is a single high bit every tick time (10 milliseconds) and marks the first sample in IDATA as being associated with the tick time. The length of ITICK is one half a cycle of SCLK.

All these signals are HSTL class III.

4.4 Wideband Output Signals (2 sets)

- ODATA [63:0] is clocked out by 2x SCLK. ODATA is the output data highway and can be in any of the organizations listed in Table 4-1. ODATA [63] is the most significant bit of the oldest fine sample.

- OPPS is clocked out by 2x SCLK. OPPS is a single high bit every second and represents the PPS at the antenna. The length of OPPS is one half a cycle of SCLK.

- OTICK is clocked out by 2x SCLK. OTICK is a single high bit every tick time (10 milliseconds) and marks the oldest sample in ODATA as being associated with the tick time. The length of OTICK is one half a cycle of SCLK.

- OVALID is clocked out by 2x SCLK. If low, the associated data is invalid.

- ONOISE is clocked out by 2x SCLK. If high, the calibration noise diode at the antenna was on for the associated samples. If low, the noise source was off.

- OCLK is the data clock derived from SCLK. It is used to clock in its accompanying data by the next chip in the chain.

All these signals are HSTL class III.

4.5 MCB Interface Signals

- MCB_ADDR [7:0] is the input 8-bit address bus for accessing internal filter chip configuration, monitor and control registers.

- MCB_DATA [15:0] is the bi-directional 16-bit microprocessor data bus.

- MCB_CS* is the input low-true chip select that enables the MCB interface drivers.

- MCB_CLK is the input clock for the synchronous MCB interface. The phase and frequency of MCB_CLK is independent of SCLK.

- MCB_RD/WR* is the input read/write enable.

All the MCB Interface signals are LVTTL.

4.6 Test Port

These four outputs can be attached to a number of internal signals TBD to provide a simple diagnostic capability.

5 Requirements

The following is a list of filter chip requirements.

5.1 Functional Requirements

1. Re-arrange, re-map, bits for 3-bit and 8-bit (EVLA) or 1-bit and 2-bit (VLBI) sampling.

2. Recode 1-, 2-, and 3-bit data to 4-bit data with an odd number of levels (this could be done later). To save resources, 8-bit data remains the same until it is used.

3. Base band crossbar switch allowing full connectivity between inputs and outputs.

4. Output the data in the proper format for the Delay Module and the rest of the chips on the Station Board. Bit 63 of the data path is the MS bit of the oldest sample.

5. Simple Test Pattern Generator (TPG) and allow the CMIB to choose between real data and the TPG output. Perhaps a suitable test pattern is one that goes through all the states of the data (a ramp). Other possibilities include a square wave and a constant. One way of providing all of this is to allow the CMIB to load a RAM with a pattern that is read out in synchronism to the system tick. The RAM should have a depth of at least 256 64-bit words. There should be one RAM for each base band.

6. Generate noise diode on/off bit, one for each band. Generator needs phase and phase rate every system tick. Define resolution and width.

7. Produce wideband state counts. Could be 1-16 simultaneous counters (as many as possible).

8. Measure system PPS against antenna PPS. Mark antenna PPS occurrence for CMIB

9. Mark antenna 0.1 PPS occurrence for CMIB (bit could be read by ISR).

10. Ensure signal integrity of data from FORM. By sending a tick to the FORM, it could generate CRC for a chosen bit and return the data with the (suitable delayed) tick.

5.2 Performance Requirements

1. The SBIC shall operate on the input sampled data and control signals with a clock rate of 256 MHz. The chip will take a 128 MHz input clock, perform double-edged sampling of the data and develop its own internal 256 MHz clock (or perform the operations on double wide data at 128 MHz).

2. The synchronous MCB interface shall be capable of operating with a clock that is neither frequency nor phase synchronous with the 128 MHz data clock. The chip will support an MCB interface clock with a maximum rate of 33 MHz.

3. The power dissipation of the chip shall not exceed 3 Watts; however, the goal for the maximum power dissipation is 2 Watts.

5.3 Environmental Requirements

1. The SBIC will be surface mounted on the Station Board PCB. Additional heat sinks may be attached to the chip to reduce temperature.

2. The board will use forced-air cooling with a normal operating ambient temperature of 20 °C and with a maximum ambient temperature of 40 °C.

5.4 Interface Requirements

As shown in Figure 4-1, the *SBIC* has several interfaces. The following sections show the functional relative timing between the signals comprising each interface.

5.4.1 System Timing Interface Requirements

Shown below is the functional timing for the signals described in section 4.1.

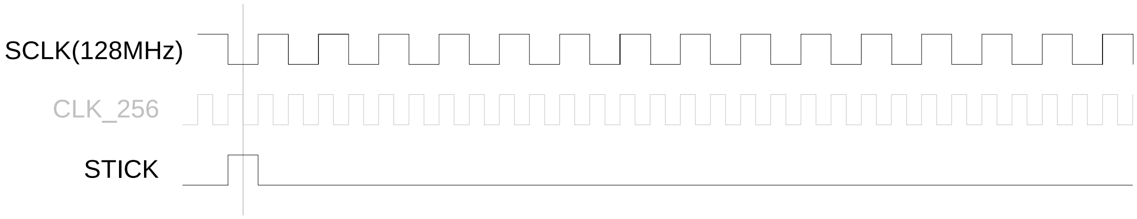


Figure 5-1 System Functional Timing

5.4.2 FORM Data Interface Requirements

Shown below is the functional timing for the signals described in section 4.2.

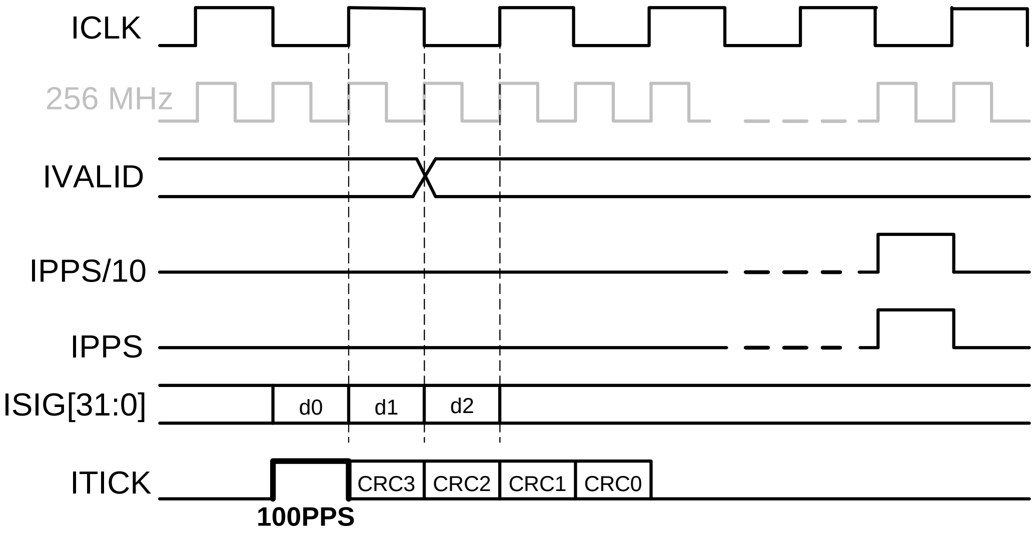


Figure 5-2 Data from FORM Functional Timing

There are three sets of data coming to the SB. The first four bits after the 100PPS pulse are CRC calculation result. The calculation is performed on one out of 32 data lines between the ticks.

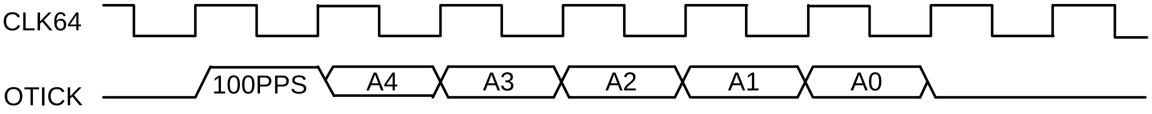
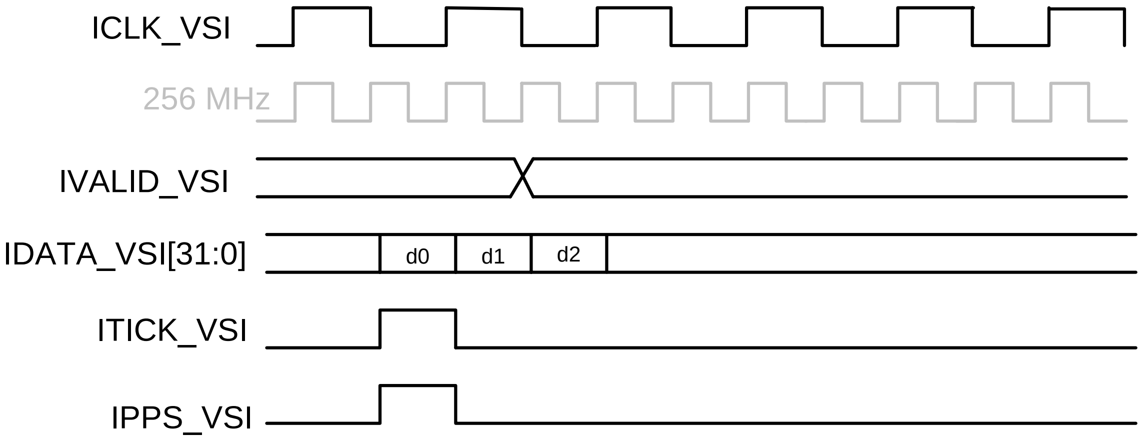


Figure 5-3 Data from SB to FORM Functional Timing

The figure above represents one, out of three, couple of lines going from the SB to FORM. Clock being sent is 64MHz and the system tick. Following the system tick are five bits of data that set a mux within the FORM. This mux selects a data line on which the CRC calculation is performed.

5.4.3 VSI Data Interface Requirements

Shown below is the functional timing for the signals described in section 4.3



5.4.4 Output Data Interface Requirements

Shown below is the functional timing for the signals described in section 4.4.

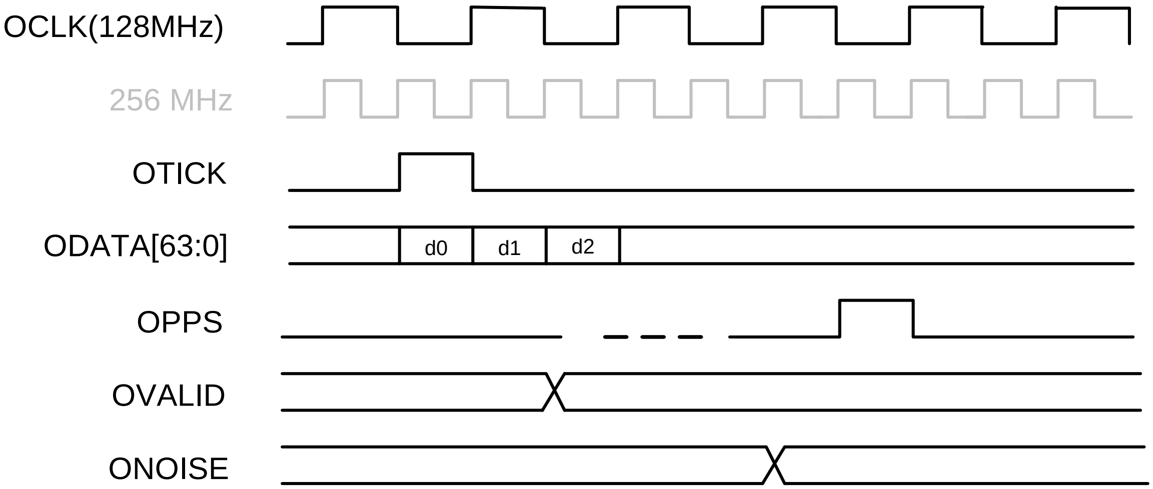


Figure 5-4 Output Data Functional Timing Diagram

5.4.5 MCB Interface Requirements

The MCB (Monitor & Control Bus) interface allows a microprocessor interface to write into the SBIC to configure and control it and to read from it to verify configuration information and obtain status and monitor information.

When the microprocessor wants to write to a SBIC, it puts the data on the MCB_DATA bus, the target register address on the MCB_ADDR bus and drives MCB_RD/WR* and MCB_CS* low some time before a rising edge of the MCB_CLK and keeps the signals stable until some time after the rising edge of the MCB_CLK. If MCB_CS* and MCB_RD/WR* are both low, the SBIC then writes the data into the specified register on the rising edge of MCB_CLK. A write requires one clock cycle as shown below.

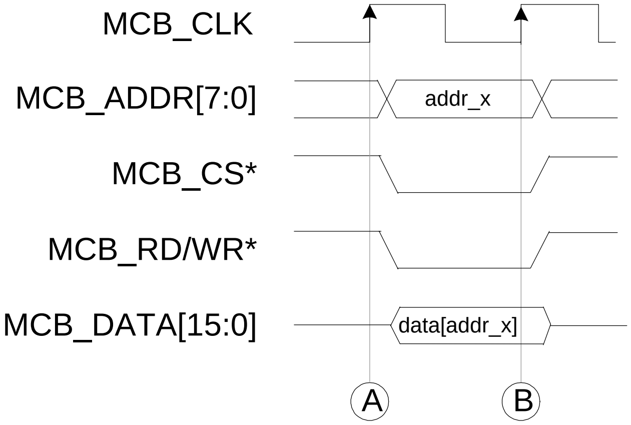


Figure 5-5 MCB Interface WRITE Functional Timing

When the microprocessor wants to read from an SBIC, it drives MCB_RD/WR* high, puts the desired register address on the MCB_ADDR bus and drives the corresponding MCB_CS* low. Read cycles require one clock cycle to setup and an additional clock cycle to read as shown below. Subsequent reads at the same address may take only one clock cycle depending on the microprocessor.

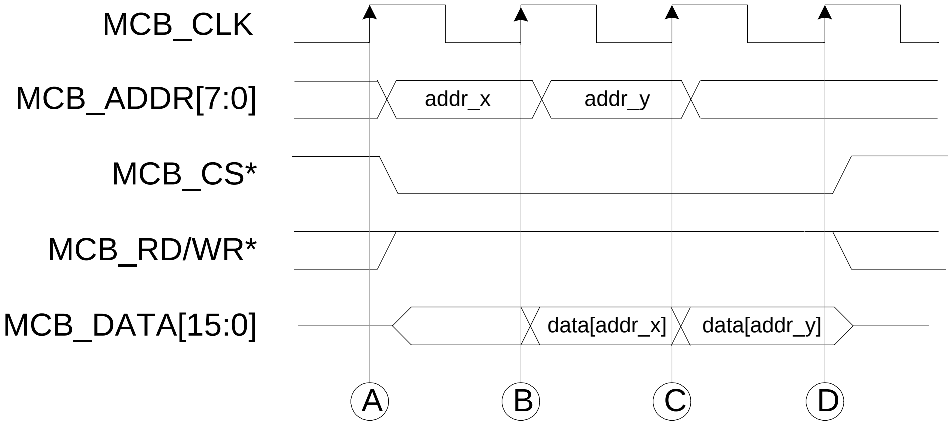


Figure 5-6 MCB Interface READ Functional Timing

The microprocessor will be interrupted on a version of STICK that has been delayed sufficiently to make sure that all chips on the board have received their local version of the TICK. This allows a pipeline delay through the chips on the board. Configuration information sent from the microprocessor to the SBIC may take effect immediately and should only be sent when the output of the chip is irrelevant.

Status information, such as error bits, will show any occurrence of an error since the last read of that information. Another method would be to latch the status information on the TICK and clear the primary register. This method assumes that the status information is read every TICK by the ISR. Control information may include bits which, if set; cause a specified error to occur to allow testing of the reaction of the software to that error.

6 Functional specifications

This section describes the actual design of the SBIC. A top-level block diagram is given on the Figure 6-1.

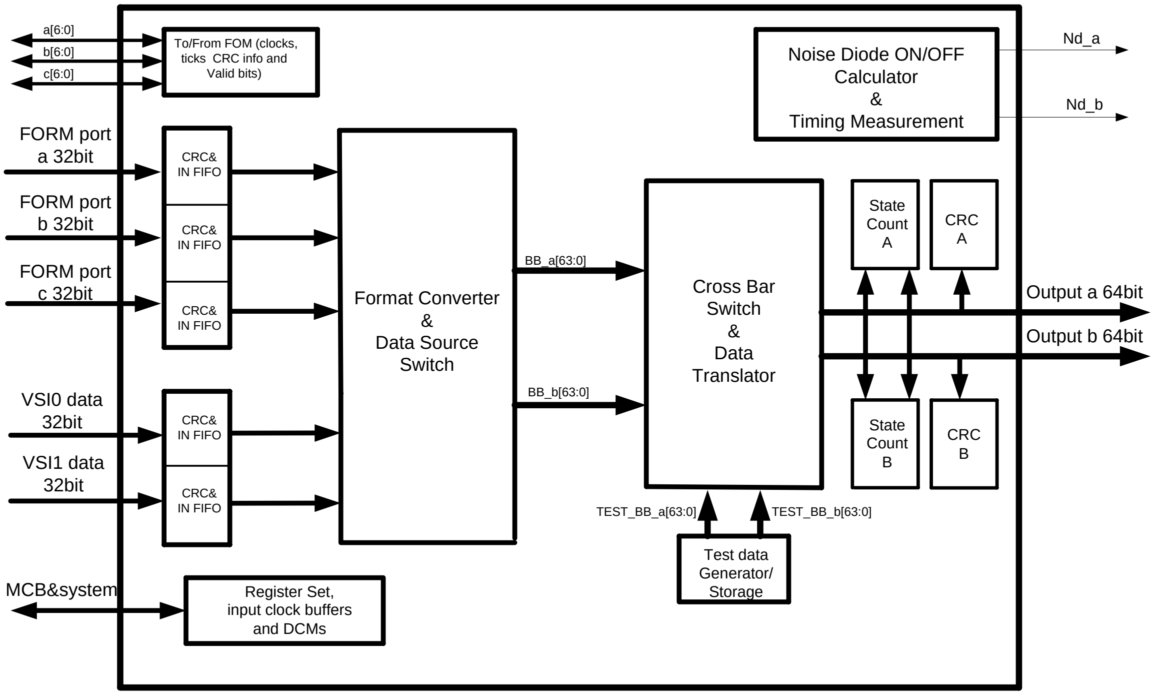


Figure 6-1 SBIC Top-level Functional Block Diagram

The figure above represents a top-level functional block diagram of the SBIC. The main block within the chip are: CRC&IN FIFO, Format Convertor&Data Source Switch, Cross Bar Switch& Data Translator Block, State Counters Block, Noise Diode ON/OFF&Timing Measurement Block and Test Generator Block. Each block is described in more detail in the sections that follow.

6.1 CRC and Input FIFO Block

This is a simple block, which performs two functions. The first function is CRC calculation. This function is performed on a selected bit within a data bus. The calculation takes place immediately after input flip flop using its own data clock. The calculation is performed during each 10ms period i.e. between two data ticks. The MCB selects which bit to calculate CRC for and the result of the calculation is presented to the MCB for an entire 10ms time.

The second function is re-clocking the data from its original clock domain to the chip clock domain. This is achieved by using a simple 33 wide and eight bit deep FIFO. The FIFO memory is based on distributed RAM.

6.2 Format Converter and Data Source Switch Block

This block performs tow functions as well. The first one is input data format conversion. The first format conversion is done for the four-bit VLBI mode. There are only three bits coming to the SBIC, a bit from each FORM port. Therefore, a logical zero is inserted as a fourth bit. This is shown on the Figure 6-2.

The second format conversion is applicable for two modes of operation, 8-bit VLBI and eMERLIN. This is presented on the Figure 6-3.

The last data format conversion is performed for the VSI input data. This is shown on the Figure 6-4.

The second function of the block is selecting the output based on the MCD request. The choices are the above mentioned. In the 8-bits VLBI and eMERLIN mode, there is only one 64-bits wide base band data bus. The second one is created by simply copying the original one.

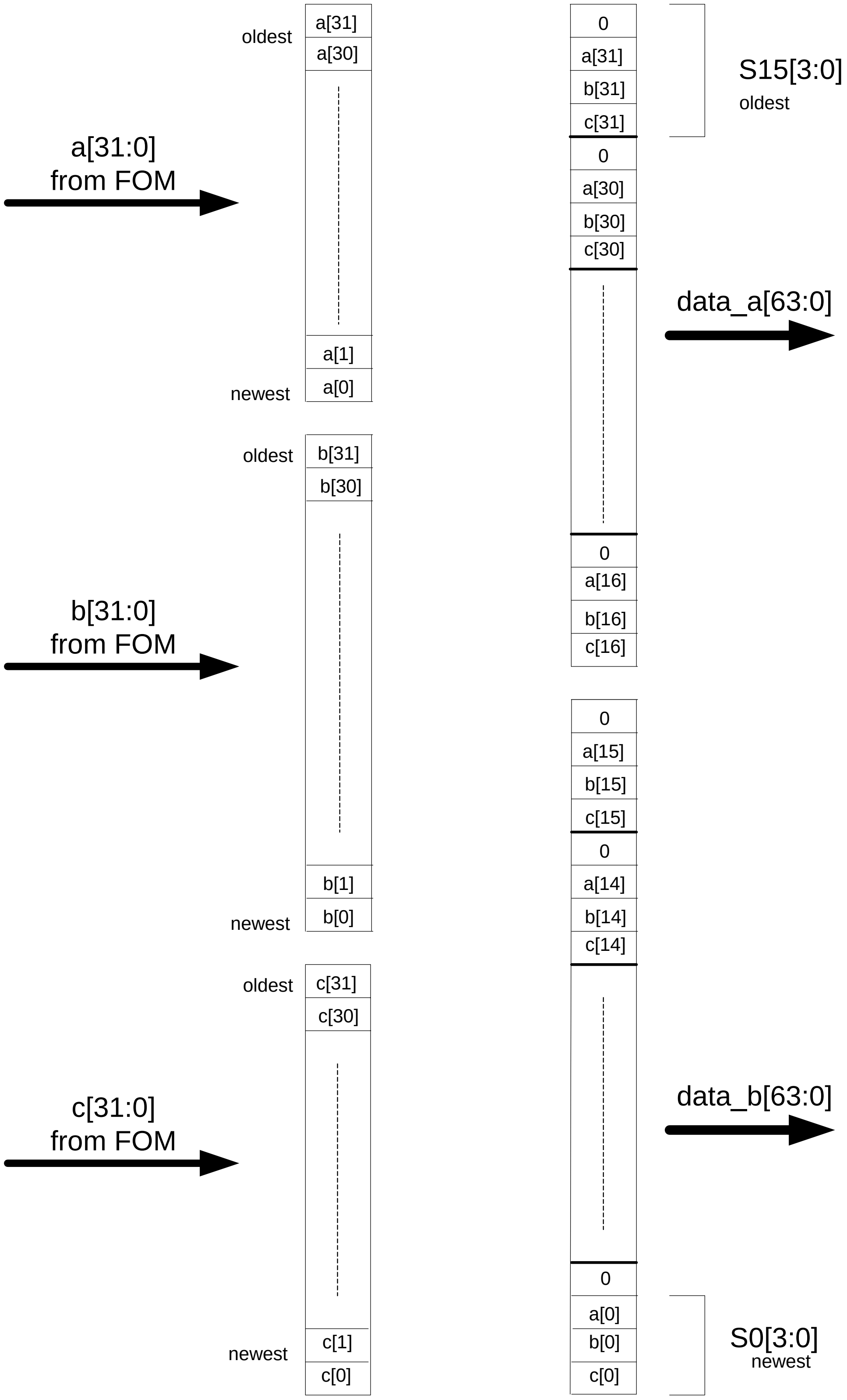


Figure 6-2 Three bit to four bit EVLA data format conversion

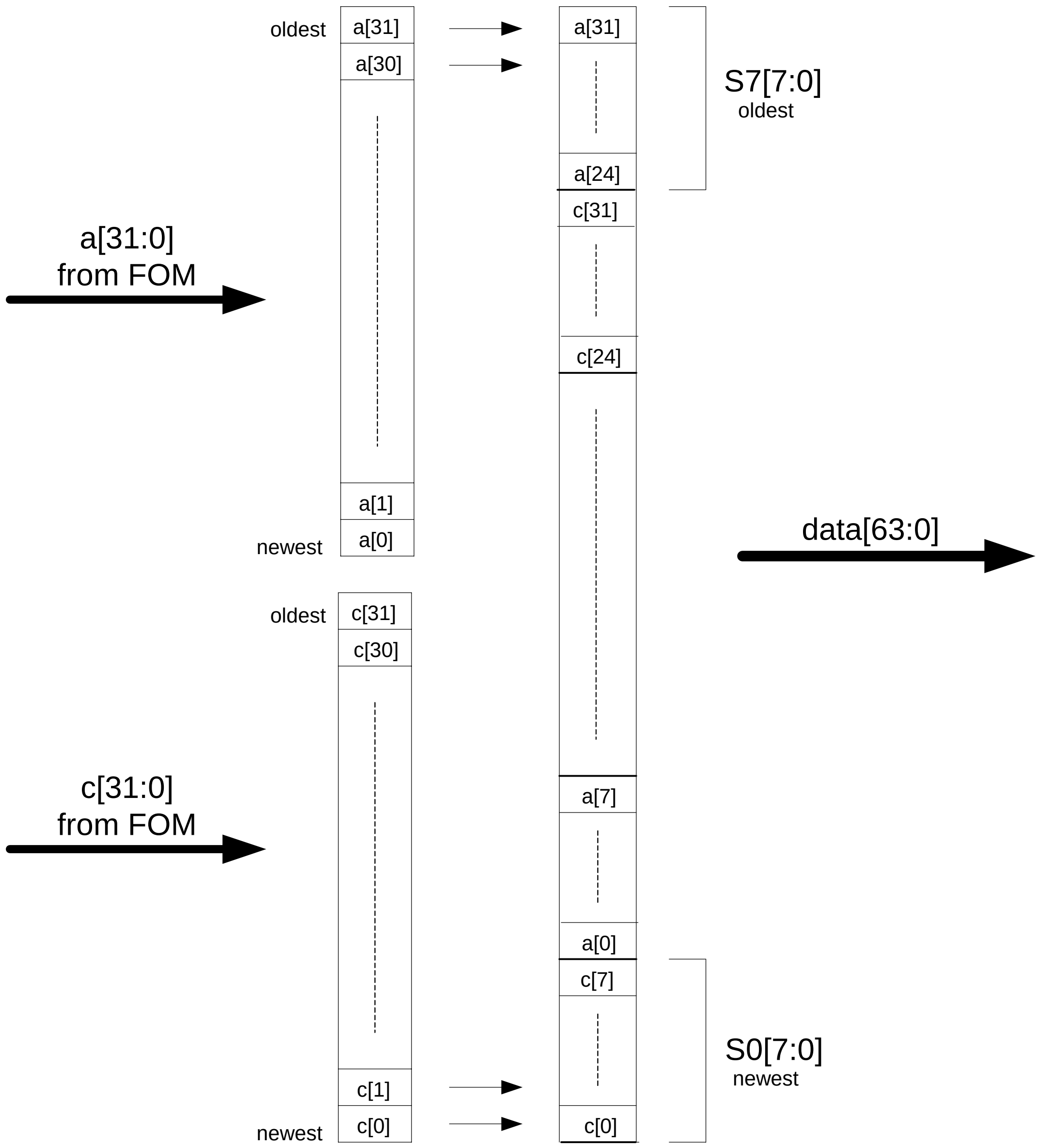


Figure 6-3 Eight Bit EVLI and eMERLIN data format conversion

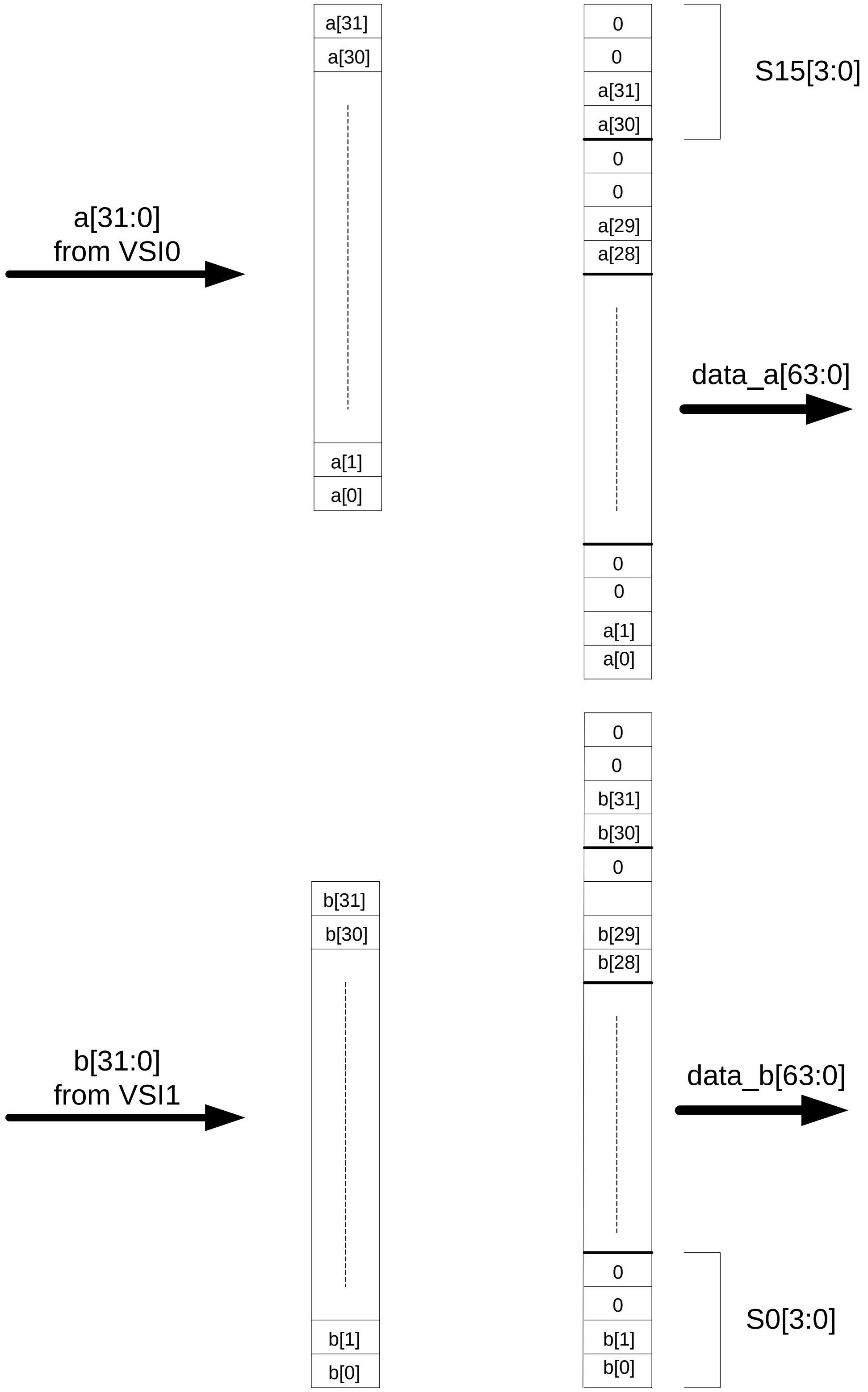


Figure 6-4 VSI data format conversion

6.3 Cross-Bar Switch and Data Translator Block

The next block within the data path is Cross-Bar Switch and Data Translator Block. This dual port RAM based memory space enables MCB to translate the incoming data. The memory can be used to store test data to enable system testing in absence of the FORM module. The functional block diagram of the block is given on the Figure 6-5.

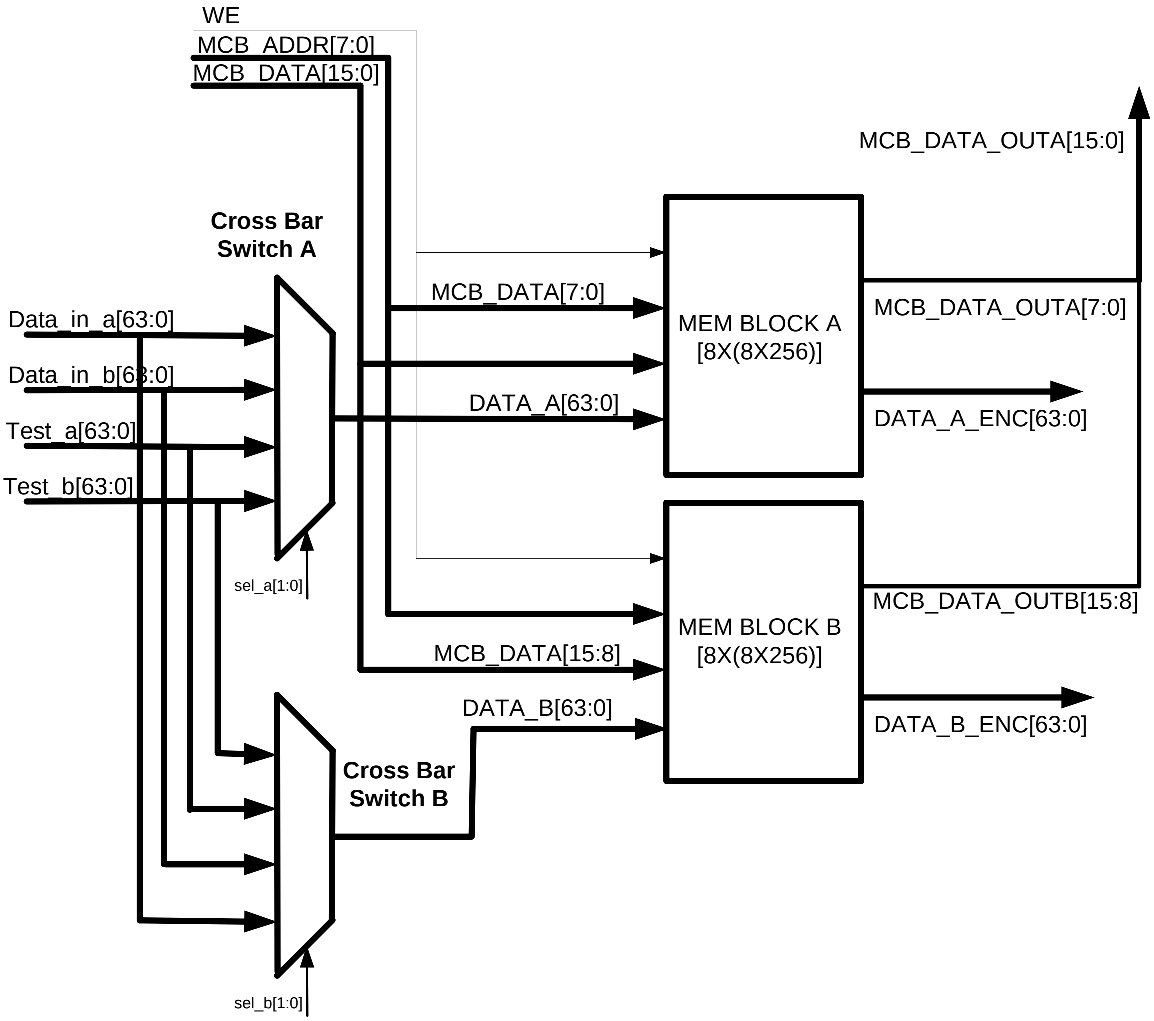


Figure 6-5 Data Translator and Cross Bar Switch functional block diagram

The Cross Bar Switch is implemented as two sub switches, Cross-Bar Switch A and Cross Bar Switch B. Each switch is controlled by the MCB via 'sel_a' and "sel_b' signals. The Cross-Bar Switch A selects A wide band 64-bits bus for the Data Translator block and the Cross-Bar Switch B selects B wide band data. Full connectivity from the inputs to the outputs is provided.

The memory space consists of two main RAM blocks. Each of the blocks is responsible for translating one 64-bits data bus. Each 64X256 RAM block is made of eight 8X256

Dual Port RAM sub blocks. The figure below shows block A. Block B looks the same except for the MCB data. All of eight sub blocks are loaded with the same contents. Block A and B could have different contents.

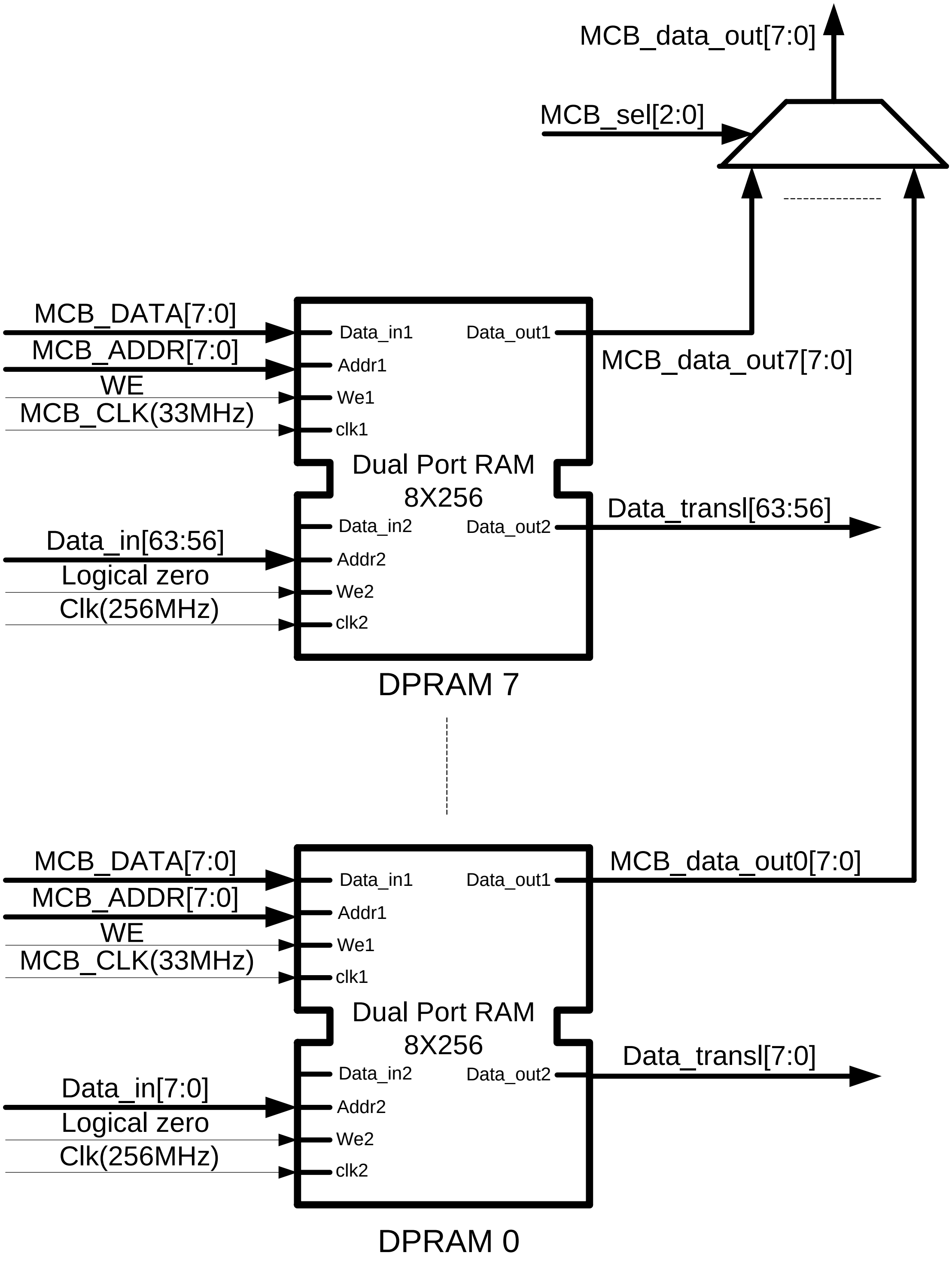


Figure 6-6 Data Translator’s memory organization

Initially the contents of all sixteen Dual Port RAM memory blocks are loaded as follows:

Addr 0x00 Data 0x00; Addr 0x01 Data 0x01; …………Addr 0xFF Data 0xFF.

This means no translating at all, what comes in goes out unchanged. The MCB can load different content to the memory space by asserting 0xFF address (called mem_address) and making MCB_ RD/WR and MCB_CS signals low. Each time the above is true the logic inside will write MCD_DATA to an internal memory location and increase internal counter value by one. Read is performed in the same way, only MCB_ RD/WR is kept high.

6.4 Noise Diode ON/OFF Calculator and Timing Measurement Block

There is no Noise Diode on/off signal coming to Station Board from FORM; therefore, the signal has to be manufactured on the SB itself. The algorithm used to produce this signal is given on the figure below.

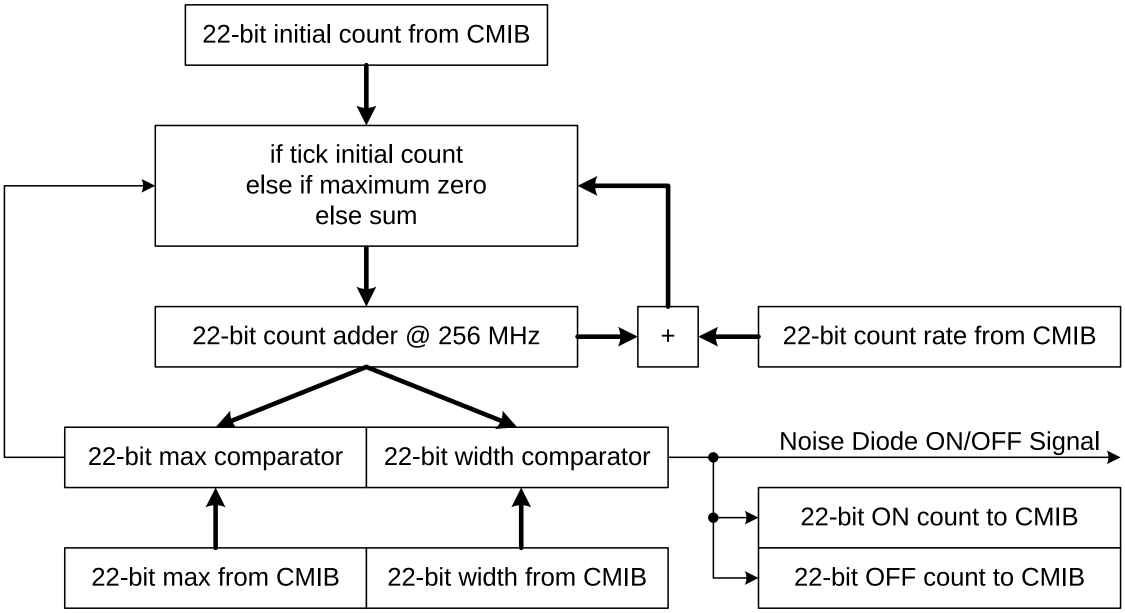


Figure 6-7 Noise Diode ON/OFF signal calculation functional block diagram

There are four 22-bit values involved in the calculation – initial count, count rate, count width and count maximum. These values may be written anytime and become active at the next tick. The initial count determines the time of the first transition, the rate is usually set to 1 or -1, the maximum determines the period and the width determines the duty cycle of the ON/OFF switching cycle. The count is incremented by the rate at 256 MHz and the local noise diode waveform is ON when the count is less than the width. The initial phase has to be determined from knowing when the switching took place in the antenna. Normally, this switching would be related to the antenna time sent from the

FORM. Both the antenna tick and the data tick are measured relative to the system tick in the Input FPGA. The CMIB should provide a new set of values after each 10ms interrupt. Failing to do so causes incorrect calculation. If the initial phase is set to zero, the local noise diode waveform will become ON at the next data tick.

The second function of the block, Timing Measurement, refers to five counters that measure the distance between PPS from each port with respect to system tick. The info is send to the MCB. In addition, this block checks for simultaneous appearance of the PPS and PPS/10 (Pulse Per 10 Seconds) for each port that comes from FORM. This info is sent to the MCB as well.

6.5 State Counters Block

Last logic block described here is the state counters block. The next two figures present the organization of the block. On the Figure 6-8, a basic counter block is presented. There are two counters, ‘higher’ and ‘lower’ counter. The names come as reference to the ‘state_sel’ 8-bit input. In the four-bit mode the ‘state_sel’ can be divided into two sub busses, nibbles, higher and lower nibble. Therefore, the counter, which operates based on the higher nibble, is called ‘higher’ counter. The same convention applies to the ‘lower’ counter. The ‘state_sel’ represents a state which appearance is to be counted during 10ms time interval. When a band is represented by four bits, four-bit mode, the ‘state_sel’ defines two states. The choices are as follows:

a) Both nibbles are the same in which case four bit input data busses should be different, ‘data_h’ and ‘data_l’. This case represents counting the same state within two different sub-bands.

b) The nibbles are not the same. If the ‘data_h’ and ‘data_l’ are the same then this is counting different states within the same band. If input data is different, then this is counting different states within different sub-bands.

The frame of operation in four-bit band mode is 16 different states within one band or one state is counted within 16 different bands.

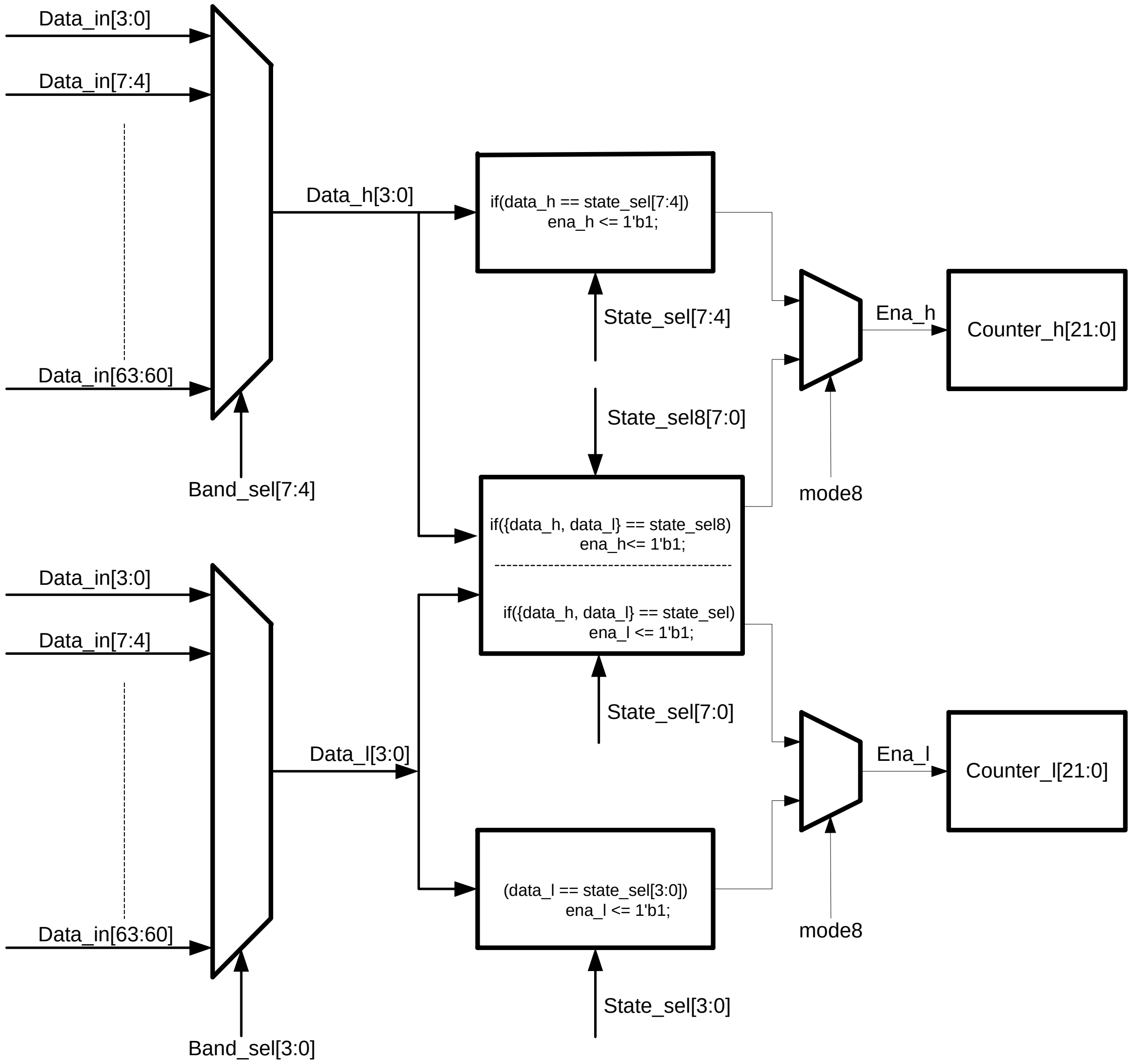


Figure 6-8 State Counter block diagram

The logic enters 8-bit mode when ‘mode8’ signal is asserted. In this case, there are eight data bands. Muxes selection signals, ‘band_sel’, should be selected so that input data really represents a data band. For example ‘ band_sel = 8’b0001_0000’ selects {data_in[7:4], data_in[3:0]}. This selection represents first band, first 8 out of 64 data bits. Value ‘ band_sel = 8’b0001_0001’ is legal but does not provide any useful info in this mode. For a selected band, two states are counted. The states are presented by the ‘state_sel’ and ‘state_sel8’ values. Appearance of the ‘state_sel’ state is counted by the ‘lower’ counter and appearance of the ‘state_sel8’ state is counted by the ‘higher’ counter.

The frame of operation for the eight-bit mode is 1 band and 16 different states and 8 bands and 2 different states.

In both modes the counters values are latched on the system tick and are available to the MCB until next tick.

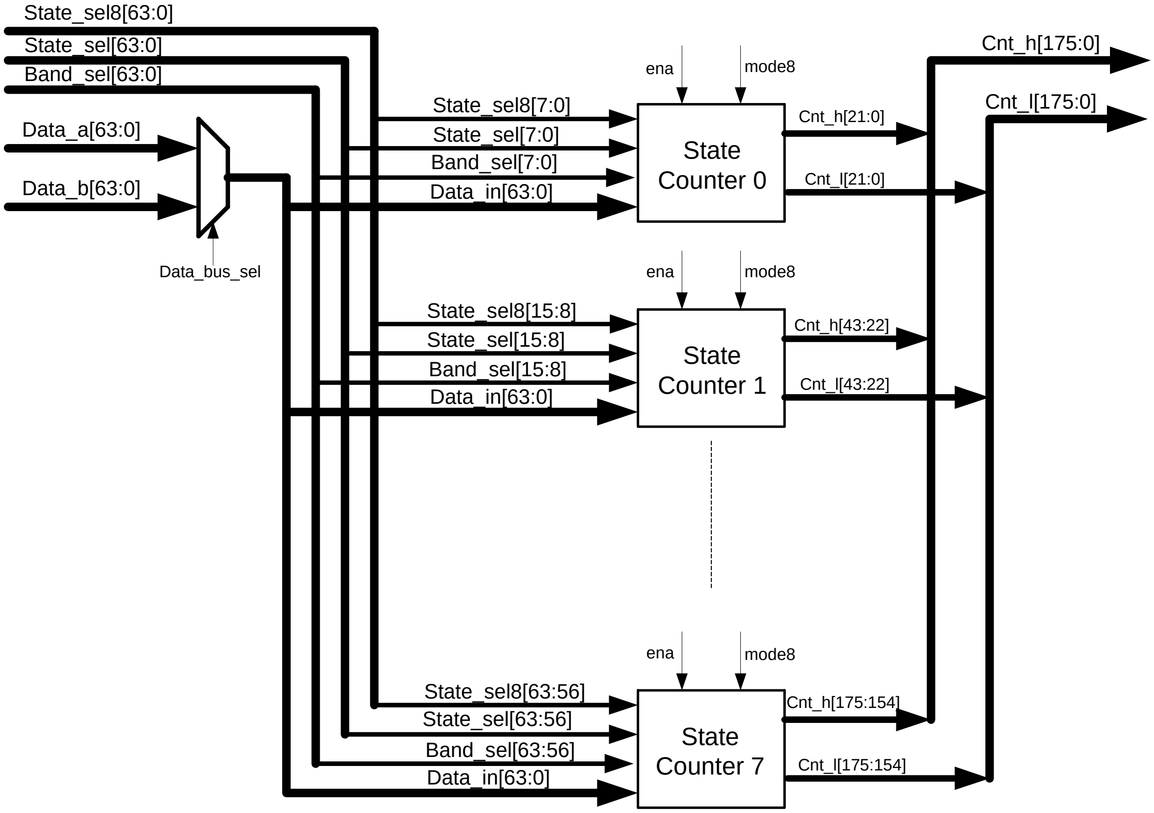


Figure 6-9 State Counters per one Base Band

The Figure 6-9 represents entire State Counters block. Input data can be data bus ‘a’ or data bus ‘b’. There are two of the above blocks within the SBIC.

7 MCB Interface Register Map

7.1 Register Map Summary

Address	Mnemonic	Register Name	Access	Reset Value
0x00	FVR	DM FPGA Version/Revision	R	0x0001
0x01	RBT	Read Back Test register	R/W	0x0000
0x02	MEMA	MEMory Address register	R/W	0x00ff
0x03	CRCFS	CRC FORM Selection register	R/W	0x0000
0x04	CRCIS	CRC Input Selection register	R/W	0x0000
0x05	CRCOS	CRC Output Selection register	R/W	0x0000
0x06	CRCVS	CRC VSI Selection register	R/W	0x0000
0x07	DP	Data Path register	R/W	0x0000
0x08	IOS	Input/Output Setup register	R/W	0x0000
0x09	DCML	DCM Lock register	R	0x0000
0x0A	CRCFV	CRC FORM Value register	R	0x0000
0x0B	CRCIV	CRC Input Value register	R	0x0000
0x0C	CRCVOV	CRC VSI & Output Value register	R	0x0000
0x0D	SCC	State Counters Control signals register	R/W	0x0000
0x0E	NDWH	Noise Diode Width High register	R/W	0x0000
0x0F	NDWL	Noise Diode Width Low register	R/W	0x0000
0x10	NDPH	Noise Diode Phase High register	R/W	0x0000
0x11	NDPL	Noise Diode Phase Low register	R/W	0x0000

0x12	NDRH	Noise Diode Rate High Register	R/W	0x0000
0x13	NDRL	Noise Diode Rate Low Register	R/W	0x0000
0x14	NDPCH	Noise Diode Max Count High Register	R/W	0x0000
0x15	NDPCL	Noise Diode Max Count Low Register	R/W	0x0000
0x16	ITS	Input Ticks Status register	R	0x0000
0x17	PATCH	Port A Tick Counter High register	R	0x0000
0x18	PATCL	Port A Tick Counter Low register	R	0x0000
0x19	PBTCH	Port B Tick Counter High register	R	0x0000
0x1A	PBTCL	Port B Tick Counter Low register	R	0x0000
0x1B	PCTCH	Port C Tick Counter High register	R	0x0000
0x1C	PCTCL	Port C Tick Counter Low register	R	0x0000
0x1D	V0TCH	VSI0 Tick Counter High register	R	0x0000
0x1E	V0TCL	VSI0 Tick Counter Low register	R	0x0000
0x1F	STDV	System Tick Delay VSI register	R/W	0x0000
0x20	V1TCH	VSI1 Tick Counter High register	R	0x0000
0x21	V1TCL	VSI1 Tick Counter Low register	R	0x0000
0x22	STDF	System Tick Delay FORM register	R/W	0x0000
0x23	IPD	Input Ports Delay register	R/W	0x0000
0x24	BSL1	Band Selection register 1	R/W	0x0000
0x25	BSL2	Band Selection register 2	R/W	0x0000
0x26	BSL3	Band Selection register 3	R/W	0x0000
0x27	BSL4	Band Selection register 4	R/W	0x0000
0x28	SSL1	State Selection register 1	R/W	0x0000

0x29	SSL2	State Selection register 2	R/W	0x0000
0x2A	SSL3	State Selection register 3	R/W	0x0000
0x2B	SSL4	State Selection register 4	R/W	0x0000
0x2C	8SSL1	8-bits mode State Selection register 1	R/W	0x0000
0x2D	8SSL2	8-bits mode State Selection register 2	R/W	0x0000
0x2E	8SSL3	8-bits mode State Selection register 3	R/W	0x0000
0x2F	8SSL4	8-bits mode State Selection register 4	R/W	0x0000
0x30	SCLB0_6	State Counter Lower Block0 top 6 bits	R	0x0000
0x31	SCLB0_16	State Counter Lower Block0 lower 16 bits	R	0x0000
0x32	SCHB0_6	State Counter Higher Block0 top 6 bits	R	0x0000
0x33	SCHB0_16	State Counter Higher Block0 lower 16 bits	R	0x0000
0x34	SCLB1_6	State Counter Lower Block1 top 6 bits	R	0x0000
0x35	SCLB1_16	State Counter Lower Block1 lower 16 bits	R	0x0000
0x36	SCHB1_6	State Counter Higher Block1 top 6 bits	R	0x0000
0x37	SCHB1_16	State Counter Higher Block1 lower 16 bits	R	0x0000
0x38	SCLB2_6	State Counter Lower Block2 top 6 bits	R	0x0000
0x39	SCLB2_16	State Counter Lower Block2 lower 16 bits	R	0x0000
0x3A	SCHB2_6	State Counter Higher Block2 top 6 bits	R	0x0000
0x3B	SCHB2_16	State Counter Higher Block2 lower 16 bits	R	0x0000
0x3C	SCLB3_6	State Counter Lower Block3 top 6 bits	R	0x0000
0x3D	SCLB3_16	State Counter Lower Block3 lower 16 bits	R	0x0000
0x3E	SCHB3_6	State Counter Higher Block3 top 6 bits	R	0x0000
0x3F	SCHB3_16	State Counter Higher Block3 lower 16 bits	R	0x0000

0x40	SCLB4_6	State Counter Lower Block4 top 6 bits	R	0x0000
0x41	SCLB4_16	State Counter Lower Block4 lower 16 bits	R	0x0000
0x42	SCHB4_6	State Counter Higher Block4 top 6 bits	R	0x0000
0x43	SCHB4_16	State Counter Higher Block4 lower 16 bits	R	0x0000
0x44	SCLB5_6	State Counter Lower Block5 top 6 bits	R	0x0000
0x45	SCLB5_16	State Counter Lower Block5 lower 16 bits	R	0x0000
0x46	SCHB5_6	State Counter Higher Block5 top 6 bits	R	0x0000
0x47	SCHB5_16	State Counter Higher Block5 lower 16 bits	R	0x0000
0x48	SCLB6_6	State Counter Lower Block6 top 6 bits	R	0x0000
0x49	SCLB6_16	State Counter Lower Block6 lower 16 bits	R	0x0000
0x4A	SCHB6_6	State Counter Higher Block6 top 6 bits	R	0x0000
0x4B	SCHB6_16	State Counter Higher Block6 lower 16 bits	R	0x0000
0x4C	SCLB7_6	State Counter Lower Block7 top 6 bits	R	0x0000
0x4D	SCLB7_16	State Counter Lower Block7 lower 16 bits	R	0x0000
0x4E	SCHB7_6	State Counter Higher Block7 top 6 bits	R	0x0000
0x4F	SCHB7_16	State Counter Higher Block7 lower 16 bits	R	0x0000
0x50	TEST_0	Test Port 0 signal select register	R/W	0x0000
0x51	TEST_1	Test Port 1 signal select register	R/W	0x0000
0x52	TEST_2	Test Port 2 signal select register	R/W	0x0000
0x53	TEST_3	Test Port 3 signal select register	R/W	0x0000

0x54	NDONH	Noise Diode ON count [21:16]	R	0x0000
0x55	NDONL	Noise Diode ON count [15:0]	R	0x0000
0x56	NDOFH	Noise Diode OFF count [21:16]	R	0x0000
0x57	NDOFL	Noise Diode OFF count [15:0]	R	0x0000
0x58	TCNTRLA	Wideband Test Signal Generator Control	R/W	0x0000
0x59	TCNTRLB	Wideband Test Signal Generator Control	R/W	0x0000
0x5A	TSEEDA	Wideband Test Signal Generator Seed	R/W	0x1357
0x5B	TSEEDB	Wideband Test Signal Generator Seed	R/W	0x1357
0x5C	CPSCTL0	Clock Phase Shift Control (data)	R/W	0x0000
0x5D	CPSCTL1	Clock Phase Shift Control (FORM/system)	R/W	0x0000

Table 7-1 SBIC Memory Map

7.2 Register Details

7.2.1 FPGA Version/Revision Number register – FVR

This register specifies the FPGA Version/Revision.

Address	**15:8**	**7:4**	**3:0**	**Access**	**Reset**
0x00	Design	Version	Revision	R	0x0001

Table 7-2 FPGA Version/Revision – FVR register

The fields within the register are defined as follows:

Design [15:8]: The design could be different for different purposes.

Version [7:4]: This version number is to be incremented whenever the new FPGA load is incompatible with the previous version from the software standpoint and would require change to the driver. The initial version will be numbered 1(b0001). Version 0 is reserved for prototyping and proof of concept.

Revision [3:0]: This revision number is to be incremented whenever the new FPGA load incorporates new functionality but does not require software upgrades.

7.2.2 Read Back register – RBT

This is a test register. Writes to this register will have no effect. It simply provides means for communication verification between the FPGA and the MCB. The register keeps its last value until next write to its location.

Address	**15:0**	**Access**	**Reset**
0x01	Read Back	R/W	0x0000

Table 7-3 Read Back - RBT register

The fields within the register are defined as follows:

Read Back [15:0]: any 16 bits long combination of zeros and ones.

7.2.3 Memory Address register - MEMA

This register is used to control RAM read and write operation within the Data Translator block and to select access between the two State Counters blocks.

Address	**11**	**10**	**9**	**8**	**7:0**	**Access**	**Reset**
0x02	TCS	SCS	PD	RMC	MEMA	R/W	0x00ff

Table 7-4 Memory Address – MEMA register

Address	**15:13**	**12**	**Access**	**Reset**
0x02	**Unused**	NDSL	R/W	0x00ff

Table 7-5 Memory Address – MEMA register

The fields within the register are defined as follows:

MEMA [7:0]: asserting this address activates read/write within the Data Translator block. By default, the address is set to 0xff but this can be altered by the MCB. The value should be one that is not already used within the chip.

RMC[8]: This bit is used to reset the RAM address counter within the Data Translator block.

0: the address counter is not under reset.

1: the address counter is under reset.

PD[9]: this bit enables or disables the FPGA re-loading with a bit stream. This means that depend on the bit the FPGA can receive new configuration load or not. This function can be used when multiple FPGAs seat on one configuration bus. After configuring them with the same bit stream, each device can be re-loaded separately by disabling the rest of them.

0: receiving the bit, configuration, file is enabled.

1: receiving the bit, configuration, file is not enabled.

SCS[10]: this bit selects access to one of the two State Counters blocks, block a or block b. In order not to make the Register Set block to big, this approach is adopted.

0: all the registers regarding the State Counters block will be referring to the State Counters block a.

1: all the registers regarding the State Counters block will be referring to the State Counters block b.

TCS[11]: Tick Counter Selects. This bit controls what tick counters for each port counts.

0: counters count distance between data ticks and system tick for VSI ports and distance between antenna ticks and system tick for A, B and C ports.

1: counters count distance between data PPS and system tick for VSI ports and distance between data ticks and system ticks for A, B and C ports.

NDSL[12]: Noise Diode Self Lock. Asserting this bit puts the noise diode calculating logic in self-lock mode of operation.

0: noise diode calculator is not in self-lock mode.

1: noise diode calculator is in self-lock mode.

7.2.4 CRC FORM Selection register – CRCFS

This register defines which data line, out of 32, is used for the CRC calculation for each port within the FORM. A five-bit value is serialized and sent to FORM.

Address	15	14:10	9:5	4:0	Access	Reset
0x03	Unused	CRCFS_c	CRCFS_b	CRCFS_a	R/W	0x0000

Table 7-6 CRC FORM Selection – CRCFS register

The fields within the register are defined as follows:

CRCFS_a[4:0]: defines the line for the CRC calculation within the FORM port a.

CRCFS_b[9:5]: defines the line for the CRC calculation within the FORM port b.

CRCFS_c[14:10]: defines the line for the CRC calculation within the FORM port c.

7.2.5 CRC Input Selection register – CRCIS

This register defines which data line, out of 32, is used for the CRC calculation for each input port, receiving data from FORM, within the chip. For the proper operation of the CRC scheme, these values have to be the same as the values in the previous register.

Address	15	14:10	9:5	4:0	Access	Reset
0x04	Unused	CRCIS_c	CRCIS_b	CRCIS_a	R/W	0x0000

Table 7-7 CRC Input Selection – CRCIS register

The fields within the register are defined as follows:

CRCIS_a[4:0]: defines the line for the CRC calculation within the input port a.

CRCIS_b[9:5]: defines the line for the CRC calculation within the input port b.

CRCIS_c[14:10]: defines the line for the CRC calculation within the input port c.

7.2.6 CRC Output Selection register – CRCOS

This register defines which output data line, out of 64, is selected for the CRC calculation.

Address	**15:12**	**11:6**	**5:0**	**Access**	**Reset**
0x05	Unused	CRCOS_b	CRCOS_a	R/W	0x0000

Table 7-8 CRC Output Selection – CRCOS register

The fields within the register are defined as follows:

CRCOS_a[5:0]: defines the line for the CRC calculation within the output port a.

CRCOS_b[11:6]: defines the line for the CRC calculation within the output port b.

7.2.7 CRC VSI Selection register – CRCVS

This register defines which input VSI data line, out of 32, is selected for the CRC calculation.

Address	**15:11**	**10:5**	**4:0**	**Access**	**Reset**
0x06	Unused	CRCVS_1	CRCVS_0	R/W	0x0000

Table 7-9 CRC VSI selection – CRCVS register

The fields within the register are defined as follows:

CRCVS_0[4:0]: defines the line for the CRC calculation within the VSI port 0.

CRCVS_1[10:5]: defines the line for the CRC calculation within the VSI port 1.

7.2.8 Data Path register – DP

This register defines data path. The fields within the register are defined as follows:

Addr	15	.	10	9	8:6	5:4	3:2	1:0	Access	Reset
0x07	PR	R	SR	TE	RDS	SW_b	SW_a	STF	R/W	0x0000

Table 7-10 Data Path – DP register

STF[1:0]: defines selected data organization:

00: selects the four-bit organization, Figure 6-2.

01: selects the eight-bit organization, Figure 6-3.

10: selects VSI data organization, Figure 6-4.

11: selects wide band TPG output.

SW_a[3:2]: these two lines are shown on the Figure 6-5 as ‘sel_a[1:0]’ and they control the mux, which selects data for A data bus.

00: selects input ‘a’.

01: selects input ‘b’.

10: selects input ‘test_a’.

11: selects input ‘test_b’.

SW_b[5:4]: these two lines are shown on the Figure 6-5 as ‘sel_b[1:0]’ and they control the mux, which selects data for B data bus.

00: selects input ‘b’.

01: selects input ‘a’.

10: selects input ‘test_b’.

11: selects input ‘test_a’.

RDS[8:6]: these three bits are used to select from which two 8X256 RAM blocks to read data when verifying the content. There are eight of these 8X256 RAM sub blocks within A and B RAM block. The lines control mux shown on the Figure 6-6.

TE[9]: this is Test Enable signal. It enables test data generation when such data are needed. When test data is not being used, this bit should be set to zero.

1: the test data are being generated.

0: the test data are not being generated.

SR[10]: Software Reset. If this bit is set to 1 a reset of the FPGA will occur which returns all internal bits to their hardware default value.

PR[15]: PLL Reset. If this bit is set to 1 the SCLK PLL will be held in reset.

7.2.9 Input/Output Setup register – IOS

This register is used to enable proper clocking in of the input data. There is a bit per input port that enables DDR data stream selection. The bits are defined as follows:

Address	6	5	4	3	2	1	0	Access	Reset
0x08	S	VSI1	VSI0	C	B	A	SB	R/W	0x0000

Table 7-11 Input/Output Setup – IOS register

Address	15:14	13	12	11	10	9	8	7	Access	Reset
0x08	R	OB	OA	IV1	IV0	IC	IB	IA	R/W	0x0000

Table 7-12 Input/Output Setup – IOS register

SB[0]: When asserted puts the FPGA into stand-by mode.

1: FPGA is in stand-by mode.

0: FPGA is not in stand-by mode.

A[1]: Selects DDR stream for the port A.

1: Selects rising edge data stream.

0: Selects falling edge data stream.

The rest of the bits, B, C, VSI0 and VSI1, are defined in the same fashion for their corresponding ports.

S[6]: Selects DDR stream for the system tick and system PPS.

0: Selects rising edge data stream.

1: Selects falling edge data stream.

IA[7]: Selects wires for CRC checking at input port A.

0: selects 32 data wires for CRC checking.

1: replaces lowest 4 lines with so called “odd wires”.

The replacement is as follows:

Data_in[0] replace with input data valid line.

Data_in[1] replace with spare input line, formerly data clock signal.

This bit is sent to the FORM on the same wire as data tick and CRC MUX selection information.

Bits **IB[8]** and **IC[9]** control CRC checking for input ports B and C in the same fashion.

IV0[10]: Selects wires for CRC checking at input port VSI0.

0: selects 32 data wires for CRC checking.

1: replaces lowest 3 lines with so called “odd wires”.

The replacement is as follows:

Data_in[0] replace with input data valid line.

Data_in[1] replace with PPS line.

Data_in[2] replace with spare input line, formerly data clock signal.

V1[11] controls input port VSI1 in the same fashion as IV0[10].

OA[12]: Selects wires for CRC checking at output port A.

0: selects 32 data wires for CRC checking.

1: replaces lowest 4 lines with so called “odd wires”.

The replacement is as follows:

Data_out[0] replace with output data valid line.

Data_out[1] replace with noise diode line.

Data_out[2] replace with PPS out line.

Data_out[3] replace with spare output, formerly data clock signal.

OB[13] controls output port B in the same fashion as OA[12].

7.2.10 DCM Lock register – DCML

This is a status register. It reports the state of the system DCM and the internal RAM address within the Data Translator block.

Address	**15:14**	**13:6**	**5**	**4:3**	**2**	**1:0**	**Access**	**Reset**
0x09	R	RAM_ADD	S	R	NF	DWD	R	0x0000

Table 7-13 DCM Lock – DCML register

The fields within the register are defined as follows:

DWD[0]: Double Width Detector bit for system PPS. The bit reports an error regarding the pulse duration, which is 4ns. If the pulse lasts 8ns or more this bit goes high. The bit is reset on read.

1: system PPS duration is more than 4ns.

0: system PPS duration is 4ns.

DWD[1]: Double Width Detector bit for system tick, 100PPS. The bit reports an error regarding the pulse duration, which is 4ns. If the pulse lasts 8ns or more this bit goes high. The bit is reset on read.

1: system tick, 100PPS, duration is more than 4ns.

0: system tick, 100PPS, duration is 4ns.

NF[2]: This bit is high if the FORM is not present. If the FORM is not present, the Wide Band Test Generator will be enabled.

S[5]: This bit reports status of the system DCM and it is defined as follows:

1: The system DCM is locked to the system clock.

0: The system DCM is not locked to the system clock.

RAM_ADD[13:6]: eight bit internal RAM memory address.

7.2.11 CRC FORM Value register – CRCFV

This register reports calculated CRC values for each output port within the FORM module.

Address	15:12	11:8	7:4	3:0	Access	Reset
0x0A	Unused	CRCFV_c	CRCFV_b	CRCFV_a	R	0x0000

Table 7-14 CRC FORM Value – CRCFV register

The fields within the register are defined as follows:

CRCFV_a[3:0]: calculated CRC value for the output port ‘a’ within the FORM module.

CRCFV_b[7:4]: calculated CRC value for the output port ‘b’ within the FORM module.

CRCFV_c[11:8]: calculated CRC value for the output port ‘c’ within the FORM module.

7.2.12 CRC Input Value register – CRCIV

This register reports calculated CRC values for each input port within the chip.

Address	15:12	11:8	7:4	3:0	Access	Reset
0x0B	Unused	CRCIV_c	CRCIV_b	CRCIV_a	R	0x0000

Table 7-15 CRC Input Value – CRCIV register

The fields within the register are defined as follows:

CRCIV_a[3:0]: calculated CRC value for the input port ‘a’.

CRCIV_b[7:4]: calculated CRC value for the input port ‘b’.

CRCIV_c[11:8]: calculated CRC value for the input port ‘c’.

7.2.13 CRC VSI & Output Value register – CRCVOV

This register reports calculated CRC values for the two input VSI ports and two output ports.

Address	15:12	11:8	7:4	3:0	Access	Reset
0x0C	CRCOB	CRCOA	CRCIV1	CRCIV0	R	0x0000

Table 7-16 CRC VSI & Output Value – CRCVOV register

The fields within the register are defined as follows:

CRCIV0[3:0]: calculated CRC value for the input port VSI0.

CRCIV1[7:4]: calculated CRC value for the input port VSI1.

CRCOA[11:8]: calculated CRC value for the output port ‘a’.

CRCOB[15:12]: calculated CRC value for the output port ‘b’

.

7.2.14 State Counters Control signals register – SCC

This register controls operation of the State Counters, Figure 6-9.

Address	15:3	2	1	0	Access	Reset
0x0D	Unused	Bus_sel	Mode8	Ena	R/W	0x0000

Table 7-17 State Counters Control signals – SCC register

The bits within the register are defined as follows:

Ena[0]: enables counters. The idea is that when the state counts are not needed the counters do not need to count and unnecessary consume power.

1: State Counters are enabled.

0: State Counters are disabled.

Mode8[1]: this bit determines mode of the State Counters operation.

1: mode of operation is 8-bits mode.

0: mode of operation is 4-bits mode.

Bus_sel[2]: selects data bus for state counting.

1: selects data bus ’b’.

0: selects data bus ‘a’.

7.2.15 Noise Diode Width registers – NDWH and NDWL

The value defines the duty cycle of the Noise Diode ON/OFF signal.

Address	**15:6**	**5:0**	**Access**	**Reset**
0x0E	reserved	NDWH	R/W	0x0000

Table 7-18 Noise Diode Width High – NDWH register

This register represents the 6 highest bits of the Noise Diode Width value.

Address	**15:0**	**Access**	**Reset**
0x0F	NDWL	R/W	0x0000

Table 7-19 Noise Diode Width Low – NDWL register

This register represents 16 lowest bits of the Noise Diode Width value.

7.2.16 Noise Diode Phase registers – NDPH and NDPL

The value defines the phase of the Noise Diode ON/OFF signal.

Address	15:6	5:0	Access	Reset
0x10	reserved	NDPH	R/W	0x0000

Table 7-20 Noise Diode Phase High – NDPH register

This register represents 6 highest bits of the noise diode phase value, Figure 6-7.

Address	15:0	Access	Reset
0x11	NDPL	R/W	0x0000

Table 7-21 Noise Diode Phase Low – NDPL register

This register represents 16 lowest bits of the noise diode phase value.

7.2.17 Noise Diode Rate registers – NDRH and NDRL

The value defines the counting rate of the Noise Diode ON/OFF signal.

Address	15:6	5:0	Access	Reset
0x12	reserved	NDRH	R/W	0x0000

Table 7-22 Noise Diode Rate High – NDRH register

This register represents 6 highest bits of the noise diode rate value.

Address	15:0	Access	Reset
0x13	NDRL	R/W	0x0000

Table 7-23 Noise Diode Rate Low – NDRL register

This register represents the 16 lowest bits of the noise diode rate value.

7.2.18 Noise Diode Maximum registers – NDMH and NDML

The value defines the period of the Noise Diode ON/OFF signal.

Address	15:6	5:0	Access	Reset
0x14	reserved	NDMH	R/W	0x0000

Table 7-24 Noise Diode Maximum High– NDMH register

This register represents the 6 highest bits of the noise diode maximum.

Address	15:0	Access	Reset
0x15	NDML	R/W	0x0000

Table 7-25 Noise Diode Maximum Low– NDML register

This register represents the 16 lowest bits of the noise diode maximum.

7.2.19 Input Ticks Status register – ITS

This register reports appearance of the PPS/10, PPS and PPS100 pulse on ports A, B and C and appearance of the PPS and PPS100 on VSI ports. PPS/10 means one pulse every 10s, PPS means one pulse per one second, and PPS100 means 100 pulses per one second. Logical 1 indicates that a pulse had appeared within 10ms before last system tick interrupt. These bits are reset on the next interrupt.

Address	5	4	3	2	1	0	Access	Reset
0x16	B10	B1	B01	A10	A1	A01	R	0x0000

Table 7-26 Input Ticks Status – ITS register

Address	12	11	10	9	8	7	6	Access	Reset
0x16	V11	V101	V01	V001	C10	C1	C01	R	0x0000

Table 7-27 Input Ticks Status – ITS register

A01[0]: Data tick, PPS100**,** appearance on **A** port.

1: The pulse PPS100 appeared within the previous 10ms interval.

0: The pulse PPS100 did not appear within the previous 10ms interval.

A1[1]: One Pulse Per Second, PPS**,** appearance on **A** port.

1: The pulse PPS appeared within the previous 10ms interval.

0: The pulse PPS did not appear within the previous 10ms interval.

A10[2]: One Per 10s Second, PPS/10**,** appearance on **A** port.

1: The pulse PPS/10 appeared within the previous 10ms interval.

0: The pulse PPS/10 did not appear within the previous 10ms interval.

Bits [5:3] - B port and [8:6] – C port are defined in the same way as bits within port A.

V001[9]: Data tick, PPS100**,** appearance on VSI0 port.

1: The pulse PPS100 appeared within the previous 10ms interval.

0: The pulse PPS100 did not appear within the previous 10ms interval.

V01[10]: One Pulse Per Second, PPS**,** appearance on VSI0 port.

1: The pulse PPS appeared within the previous 10ms interval.

0: The pulse PPS did not appear within the previous 10ms interval.

V101[11]: Data tick, PPS100**,** appearance on VSI1 port.

1: The pulse PPS100 appeared within the previous 10ms interval.

0: The pulse PPS100 did not appear within the previous 10ms interval.

V11[12]: One Pulse Per Second, PPS**,** appearance on VSI1 port.

1: The pulse PPS appeared within the previous 10ms interval.

0: The pulse PPS did not appear within the previous 10ms interval.

7.2.20 Port ‘A’ Tick Counter High and Low registers – PATCH and PATCL

These registers represent the time distance between the antenna tick and the system tick when TCS[11] at 0x02 low or data tick and system tick when TCS high expressed in number of 256MHz clock cycles.

Address	15:6	5:0	Access	Reset
0x17	Unused	PATCH	R	0x0000

Table 7-28 Port ‘A’ Counter High – PATCH register

This register represents six upper bits, out of 22, of the ‘A’ port tick counter.

Address	15:0	Access	Reset
0x18	PATCL	R	0x0000

Table 7-29 Port ‘A’ Counter Low – PATCL register

The register represents lower sixteen bits of the port ’A’ tick counter.

7.2.21 Port ‘B’ Tick Counter High and Low registers – PBTCH and PBTCL

These registers represent the time distance between the antenna tick and the system tick when TCS[11] at 0x02 low or data tick and system tick when TCS high expressed in number of 256MHz clock cycles.

Address	15:6	5:0	Access	Reset
0x19	Unused	PBTCH	R	0x0000

Table 7-30 Port ‘B’ Counter High – PBTCH register

This register represents six upper bits, out of 22, of the ‘B’ port tick counter.

Address	15:0	Access	Reset
0x1A	PBTCL	R	0x0000

Table 7-31 Port ‘B’ Counter Low – PBTCL register

The register represents lower sixteen bits of the port ’B’ tick counter.

7.2.22 Port ‘C’ Tick Counter High and Low registers – PCTCH and PCTCL

These registers represent the time distance between the antenna tick and the system tick when TCS[11] at 0x02 low or data tick and system tick when TCS high expressed in number of 256MHz clock cycles.

Address	15:6	5:0	Access	Reset
0x1B	Unused	PCTCH	R	0x0000

Table 7-32 Port ‘C’ Counter High – PCTCH register

This register represents six upper bits, out of 22, of the ‘C’ port tick counter.

Address	15:0	Access	Reset
0x1C	PCTCL	R	0x0000

Table 7-33 Port ‘C’ Counter Low – PCTCL register

The register represents lower sixteen bits of the port ’C’ tick counter.

7.2.23 VSI0 Tick Counter High register – V0TCH

These registers represent the time distance between the data tick and the system tick when TCS[11] at 0x02 low or data PPS and system tick when TCS high expressed in number of 256MHz clock cycles.

Address	15:6	5:0	Access	Reset
0x1D	Unused	V0TCH	R	0x0000

Table 7-34 Port VSI0 Counter High – V0TCH register

This register represents six upper bits, out of 22, of the VSI0 port tick counter.

Address	15:0	Access	Reset
0x1E	V0TCL	R	0x0000

Table 7-35 Port VSI0 Counter Low – V0TCL register

The register represents lower sixteen bits of the port VSI0 tick counter.

7.2.24 System Tick Delay VSI register – STDV

This register defines for how many 256MHz clock cycles system tick is to be delayed for tick measurements purposes only on VSI0 and VSI1 ports.

Address	15:0	Access	Reset
0x1F	STDV[15:0]	R/W	0x0000

Table 7-36 System Tick Delay VSI – STDV register

7.2.25 VSI1 Tick Counter High register – V1TCH

These registers represent the time distance between the data tick and the system tick when TCS[11] at 0x02 low or data PPS and system tick when TCS high expressed in number of 256MHz clock cycles.

Address	15:6	5:0	Access	Reset
0x20	Unused	V1TCH	R	0x0000

Table 7-37 Port VSI1 Counter High – V1TCH register

This register represents six upper bits, out of 22, of the VSI1 port tick counter.

Address	15:0	Access	Reset
0x21	V1TCL	R	0x0000

Table 7-38 Port VSI1 Counter Low – V1TCL register

The register represents lower sixteen bits of the port VSI1 tick counter.

7.2.26 System Tick Delay FORM register – STDF

This register defines for how many 256MHz clock cycles system tick is to be delayed for tick measurements purposes only on ports A, B and C.

Address	15:0	Access	Reset
0x22	STDF[15:0]	R/W	0x0000

Table 7-39 System Tick Delay FORM – STDF register

7.2.27 Input Ports Delay register – IPD

The register defines how many pipeline stages to add on any of the input ports.

Address	15:10	9:8	7:6	5:4	3:2	1:0	Access	Reset
0x23	Unus.	PDV1	PDV0	PDC	PDB	PDA	R/W	0x0000

Table 7-40 Input Ports Delay – IPD register

PDA[1:0]: Port Delay A. The bits are defined as follows:

00: No additional delay.

01: Adds one stage of pipeline delay.

10: Adds two stages of pipeline delay.

11: Adds three stages of pipeline delay.

The rest of the bits are defined in the same manner for the remaining input ports; B, C, VSI0 and VSI1.

7.2.28 Band Selection registers – BSL1, BSL2, BSL3 and BSL4

This register determines which band/bands for which the given states are to be counted.

Address	15:8	7:0	Access	Reset
0x24	BSL1[15:8]	BSL1[7:0]	R/W	0x0000

Table 7-41 Band Selection 1 – BSL1 register

It defines selected bands for two counters blocks, Figure 6-9 . BSL1[7:0] defines bands for CNT_BLOCK0 and BSL1[15:8] defines bands for CNT_BLOCK1.

When operating in 4-bits mode each nibble within BSL1[7:0] and BSL1[15:8] defines a selected band. There are 16 bands in total, within a 64 bits bus, and lower nibble (BSL1[3:0]) selects band for the lower counter within the block CNT_BLOCK0 while upper nibble(BSL1[7:4]) selects band for higher counter within the block CNT_BLOCK0. The same applies for BLS1[15:8]. Both nibbles can have any four-bit value and the counters will produce meaningful results.

In 8-bits mode of operation, there are only eight bands within the 64-bits data bus. Therefore, BSL1[7:0] selects a band for CNT_BLOCK0 and BSL1[15:8] selects band for

CNT_BLOCK1 block. An eight-bit register can have 256 values. In this case, only eight values will enable the counters to produce valid results. These values are:

10h selects first eight bits: data_in[7:0] , data band 0.

32h selects next eight bits: data_in[15:8] , data band 1.

54h selects next eight bits: data_in[23:16] , data band 2.

76h selects next eight bits: data_in[31:24] , data band 3.

98h selects next eight bits: data_in[39:32] , data band 4.

BAh selects next eight bits: data_in[47:40] , data band 5.

DCh selects next eight bits: data_in[55:48] , data band 6.

FEh selects last eight bits: data_in[63:56] , data band 7.

Address	**15:8**	**7:0**	**Access**	**Reset**
0x25	BSL2[15:8]	BSL2[7:0]	R/W	0x0000

Table 7-42 Band Selection 2 – BSL2 register

Everything said for the BSL1[7:0] and BSL1[15:8] applies for BSL2[7:0] and BSL2[15:8], except they control CNT_BLOCK2 and CNT_BLOCK3 blocks respectively.

Address	**15:8**	**7:0**	**Access**	**Reset**
0x26	BSL3[15:8]	BSL3[7:0]	R/W	0x0000

Table 7-43 Band Selection 3 – BSL3 register

Everything said for the BSL1[7:0] and BSL1[15:8] applies for BSL3[7:0] and BSL3[15:8], except they control CNT_BLOCK4 and CNT_BLOCK5 blocks respectively.

Address	15:8	7:0	Access	Reset
0x27	BSL7	BSL6	R/W	0x0000

Table 7-44 Band Selection 4 – BSL4 register

Everything said for the BSL1[7:0] and BSL1[15:8] applies for BSL4[7:0] and BSL4[15:8], except they control CNT_BLOCK6 and CNT_BLOCK7 blocks respectively.

7.2.29 State Selection registers – SSL1, SSL2, SSL3 and SSL4

These registers are used to select the states to be counted for 4-bits and 8-bits.

Address	15:8	7:0	Access	Reset
0x28	SSL1[15:8]	SSL1[7:0]	R/W	0x0000

Table 7-45 State Selection 1 – SSL1 register

This register is used in 4-bits and 8-bits mode of operation. SSL1[7:0] controls counters within CNT_BLOCK0 and SSL1[15:8] controls counters within CNT_BLOCK1 block.

In 4-bits mode value of SSL1[3:0] sets the 4-bit count state for the lower counter within CNT_BLOCK0 and SSL1[7:4] sets a 4-bit state for the higher counter within the same block. The same is true for the SSL1[15:8] except that this part controls CNT_BLOCK1 block.

In 8-bits mode both nibbles of SSL1[7:0] select a 8-bit state for the lower counter within CNT_BLOCK0, while SSL1[15:8] selects an 8-bit state for lower counter within CNT_BLOCK1. Higher counters within the two blocks in this mode are controlled by 8SSL1 register.

Address	15:8	7:0	Access	Reset
0x29	SSL2[15:8]	SSL2[7:0]	R/W	0x0000

Table 7-46 State Selection 2 – SSL2 register

This register, SSL2, controls counters within CNT_BLOCK2 and CNT_BLOCK3 in the same way as SSL1 controls counters within CNT_BLOCK0 and CNT_BLOCK1.

Address	15:8	7:0	Access	Reset
0x2A	SSL3[15:8]	SSL3[7:0]	R/W	0x0000

Table 7-47 State Selection 3 – SSL3 register

This register, SSL3, controls counters within CNT_BLOCK4 and CNT_BLOCK5 in the same way as SSL1 controls counters within CNT_BLOCK0 and CNT_BLOCK1.

Address	15:8	7:0	Access	Reset
0x2B	SSL4[15:8]	SSL4[7:0]	R/W	0x0000

Table 7-48 State Selection 4 – SSL4 register

This register, SSL4, controls counters within CNT_BLOCK6 and CNT_BLOCK7 in the same way as SSL1 controls counters within CNT_BLOCK0 and CNT_BLOCK1.

7.2.30 Eight bit mode State Selection – 8SSL1, 8SSL2, 8SSL3 and 8SSL4

These registers are used to select states to be counted in 8-bits mode only.

Address	15:8	7:0	Access	Reset
0x2C	8SSL1[15:8]	8SSL1[7:0]	R/W	0x0000

Table 7-49 eight-bit mode State Selection 1 – 8SSL1 register

8SSL1[7:0] selects a count state for higher counter within CNT_BLOCK0 while 8SSL1[15:8] does the same within CNT_BLOCK1.

Address	15:8	7:0	Access	Reset
0x2D	8SSL2[15:8]	8SSL2[7:0]	R/W	0x0000

Table 7-50 eight-bit mode State Selection 2 – 8SSL2 register

8SSL2[7:0] selects a count state for higher counter within CNT_BLOCK2 while 8SSL2[15:8] does the same within CNT_BLOCK3

Address	15:8	7:0	Access	Reset
0x2E	8SSL3[15:8]	8SSL3[7:0]	R/W	0x0000

Table 7-51 eight-bit mode State Selection 3 – 8SSL3 register

8SSL3[7:0] selects a count state for higher counter within CNT_BLOCK4 while 8SSL3[15:8] does the same within CNT_BLOCK5

Address	15:8	7:0	Access	Reset
0x2F	8SSL4[15:8]	8SSL4[7:0]	R/W	0x0000

Table 7-52 eight-bit mode State Selection 4 – 8SSL4 register

8SSL4[7:0] selects a count state for higher counter within CNT_BLOCK6 while 8SSL4[15:8] does the same within CNT_BLOCK7.

7.2.31 State Counters registers

There are 16 state counters in the design. The counters are coupled as lower and higher counter within a counter block, Figure 6-8. Since the counters are 22 bits wide, two 16 bits register are used for each counter. The following tables describe counters within CNT_BLOCK0. The rest of the counters behave in the same fashion as the described ones, only the addresses are different, and will not be described.

Address	15:7	5:0	Access	Reset
0x30	Unused	SCLB0_6	R	0x0000

Table 7-53 State Counter Lower Block0 top 6 bits – SCLB0_6 register

Address	15:0	Access	Reset
0x31	SCLB0_16	R	0x0000

Table 7-54 State Counter Lower Block0 lower 16 bits – SCLB0_16 register

The values of these registers change on system tick, each 10ms. To obtain a correct counter value both registers should be read within the same 10ms time interval.

Lower Counter Value within the CNT_BLOCK0 = unsigned {SCLB0_6, SCLB0_16}.

Address	15:7	5:0	Access	Reset
0x32	Unused	SCHB0_6	R	0x0000

Table 7-55 State Counter Higher Block0 top 6 bits – SCHB0_6 register

Address	15:0	Access	Reset
0x33	SCLB0_16	R	0x0000

Table 7-56 State Counter Higher Block0 lower 16 bits – SCHB0_16 register

The values of these registers change on system tick, each 10ms. To obtain a correct counter value both registers should be read within the same 10ms time interval.

Higher Counter Value within the CNT_BLOCK0 = unsigned {SCHB0_6, SCHB0_16}.

Example 1:

The counter SCLB0 should count state 55h within the third band within data ‘b’ bus.

The counter SCHB0 should count state AA within the third band within data ‘b’ bus.

For both counters, SCLB0 and SCHB0, the band and the data bus have to be the same. One counter block, CNT_BLOCKX, in 8-bit mode can monitor only one band. First thing to do is to enable the counters and define the mode and the data bus. This is achieved by writing 0007h to address 0Eh, SCC register. Bit 0, LSB, enables counting, bit 1 selects 8-bits mode of operation and bit 2 selects data ‘b’ bus. Next thing is selecting the band number three. This is achieved by writing xx76h to address 24h, BSL1[7:0] band selection register. The third band in 8-bits mode of operation is defined as data_in[31:24]. The last thing to do is to select the states to be monitored. For lower counter, SCLB0, write xx55h to address 28h, SSL1 register. For higher counter, SCHB0, write xxAAh to address 2Ch, 8SSL1 register.

Example 2:

The counter SCLB3 should count state 5h within the band 0 within data ‘a’ bus.

The counter SCHB3 should count state Ah within the band 14 within data ‘a’ bus.

This is 4-bits mode of operation. As in the previous example, the first thing to do is to enable the counters, define the mode of operation and select the data bus. This is done by writing 0001h to address 0Eh, SCC register. Bit 0, LSB, enables counting, bit 1 selects 4-bits mode of operation and bit 2 selects data ‘a’ bus. Band selecting in this is done thru the BSL2[15:8]. In the 4-bits mode BSL2[11:8] selects band for lower counter within CNT_BLOCK3 and BSL2[15:12] selects band for the higher counter within the same block. Band 0, data_in[3:0], is selected by 0h; Band 1, data_in[7:4] is selected by 1h; Band 2, data_in[11:8] is selected by 2h; Band 3, data_in[15:12] is selected by 3h….. and Band 15, data_in[63:60], is selected by Fh.

Writing E0xxh to location 25h will select the requested data bands. In the 4-bits mode of operation, state selection is achieved thru the SSL group of registers; 8SSL group of registers is ignored. Register SSL2[15:8] selects states for monitoring. Value SSL2[15:12] sets the state for higher counter within the block while SSL2[11:0] sets the state for lower counter within the block. Therefore, writing A5xxh to the address location 29h will do the job. The ’x’ within ‘A5xxh’ means doesn’t care.

7.2.32 Test Port Registers –TPORT0-TPORT3

The value in these registers decide what signals appear on the test ports.

Address	15:8	7:0	Access	Reset
0x50	reserved	signal to test port 0	R/W	0x0000
0x51	reserved	signal to test port 1	R/W	0x0000
0x52	reserved	signal to test port 2	R/W	0x0000
0x53	reserved	signal to test port 3	R/W	0x0000

Table 7-57 Test Port Signal Select Registers

The assignment of test signals is TBD.

7.2.33 Noise Diode ON Counters– NDONH and NDONL

Address	15:6	5:0	Access	Reset
0x54	Unused	NDONH	R	0x0000

Table 7-58 Noise Diode ON Counter High – NDONH register

This register represents the six MS bits of the ON counter. The ON counter is the number of 256MHz clock cycles that the noise diode was ON during the last tick interval.

Address	15:0	Access	Reset
0x55	NDONL	R	0x0000

Table 7-59 Noise Diode ON Counter Low – NDONL register

The register is LS sixteen bits of the ON counter.

7.2.34 Noise Diode OFF Counters– NDOFH and NDOFL

Address	15:6	5:0	Access	Reset
0x56	Unused	NDOFH	R	0x0000

Table 7-60 Noise Diode OFF Counter High – NDOFH register

This register is the six MS bits of the OFF counter. The OFF counter is the number of 256MHz clock cycles that the noise diode was OFF during the last tick interval.

Address	15:0	Access	Reset
0x57	NDOFL	R	0x0000

Table 7-61 Noise Diode OFF Counter Low – NDOFL register

The register represents lower sixteen bits of the ON counter.

7.2.35 Wideband Test Signal Control Registers – TCNTRLA/B

These registers control the two wideband test signal generators, one for each base band. This data generator is useful if the FORM is not present.

Address	15:10	9	8	7	6:4	3:0	Access	Reset
0x58	R	ND	VT	TT	NBIT	NBND	R/W	0x0000
0x59	R	ND	VT	TT	NBIT	NBND	R/W	0x0000

Table 7-62 Wideband Test Signal Control – TCNTRLA/B register

NBND – the number of bands per baseband - 1 (0, 1, 3, 7, 15).

NBIT – the number of bits per sample -1 (0 to 7)

TT – Test Type 0 => random, 1 => delta function with tones every 51.2 MHz.

ND – If TT = 0 then 0 => random (normal) and 1 => switches between large and small values at a 10 Hz rate with an OFF to ON transition at the PPS. If TT = 1 ND has no effect.

VT – Valid Type 0 => always valid, 1 => one sample is invalid at the tick

R – reserved

7.2.36 Wideband Test Signal Seed Registers – TSEEDA/B

These registers allow the random data for each base band to be different.

Address	15:0	Access	Reset
0x5A	TSEEDA	R/W	0x1357
0x5B	TSEEDB	R/W	0x1357

Table 7-63 Wideband Test Signal Control – TCNTRL register

TSEED is used as the seed value for the random signal generators.

7.2.37 Clock Phase Shift Control Register – CPSCTLD (test only)

This register controls clock phase shifting. It is used to determine the correct data edge and its range.

Address	15:4	3	2	1	0	Access	Reset
0x5C	R	INCR	NABL	OVFL	DONE	R/W	0x0000

Table 7-64 Clock Phase Shift Control – CPSCTLD register

DONE – 1 indicates that the phase shift is complete (RO)

OVFL – 1 indicates that the phase shifter has over flowed or under flowed (RO)

NABL – 1 means shift one phase delta (must return to zero to shift again)

INCR – 1 => increment, 0 => decrement

R – reserved

7.2.38 Clock Phase Shift Control Register – CPSCTLS (test only)

This register controls clock phase shifting. It is used to determine the correct system edge and its range.

Address	5:4	3	2	1	0	Access	Reset
0x5D	MATCH	INCR	NABL	OVFL	DONE	R/W	0x0000

Table 7-65 Clock Phase Shift Control – CPSCTLS register

DONE – 1 indicates that the phase shift is complete (RO)

OVFL – 1 indicates that the phase shifter has over flowed or under flowed (RO)

NABL – 1 means shift one phase delta (must return to zero to shift again)

INCR – 1 => increment, 0 => decrement

MATCH[4] – 1 means that the system tick clocked with both + and – edges match

MATCH[5] – 1 means that the chosen output leads the not chosen one.

7.3 FORM Output Connector

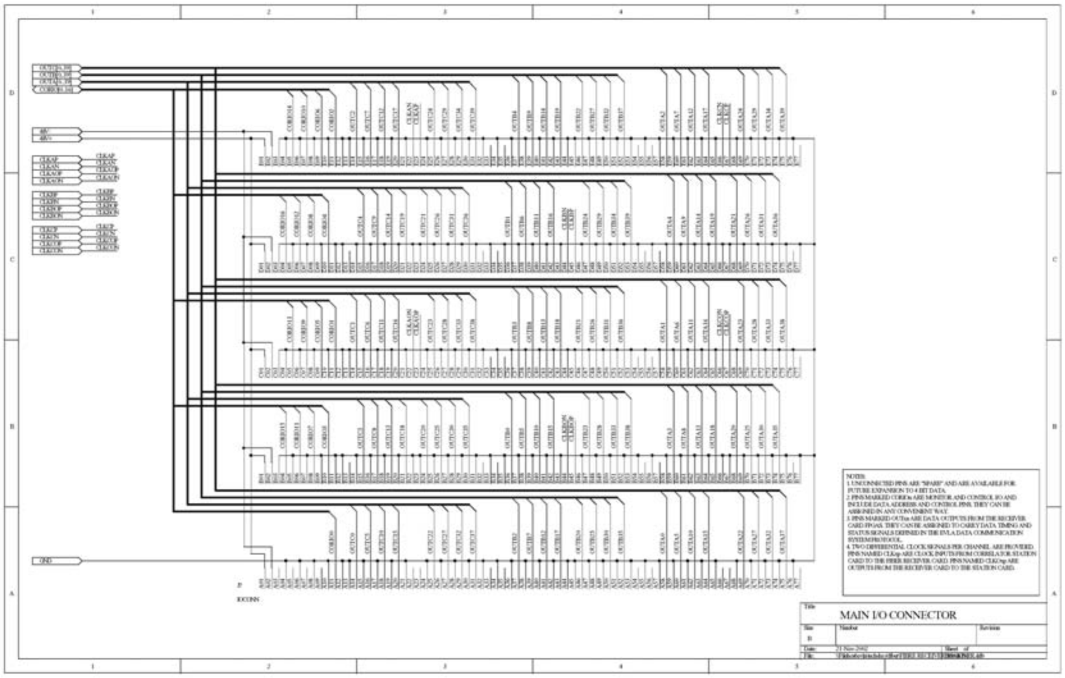

NOTES:
1. UNCONNECTED PINS ARE "SPARE" AND ARE AVAILABLE FOR FUTURE EXPANSION TO 4 BIT DATA.
2. PINS MARKED CORIOn ARE MONITOR AND CONTROL I/O AND INCLUDE DATA ADDRESS AND CONTROL PINS. THEY CAN BE ASSIGNED IN ANY CONVENIENT WAY.
3. PINS MARKED OUTxn ARE DATA OUTPUTS FROM THE RECEIVER CARD FPGAS. THEY CAN BE ASSIGNED TO CARRY DATA, TIMING AND STATUS SIGNALS DEFINED IN THE EVLA DATA COMMUNICATION SYSTEM PROTOCOL.
4. TWO DIFFERENTIAL CLOCK SIGNALS PER CHANNEL ARE PROVIDED. PINS NAMED CLKxp ARE CLOCK INPUTS FROM CORRELATOR STATION CARD TO THE FIBER RECEIVER CARD. PINS NAMED CLKOxp ARE OUTPUTS FROM THE RECEIVER CARD TO THE STATION CARD.
Title
MAIN I/O CONNECTOR
Size
B
Number
Revision
Date: 21-Nov-2002
Sheet of
File:

Figure 7-1 FORM Output Connector

Connector is 5 rows by 77 columns 2mm HM (3 110 pin modules + 1 55 pin module): Hirose from DigiKey

OUTA [39:0] One of three bits (32 data + 8 info)

OUTB [39:0] One of three bits (32 data + 8 info)

OUTC [39:0] One of three bits (32 data + 8 info)

SPARE [34:0] We could connect all these up

CORIO [16:0] “MCB”

CLK A/B/C I [LVDS] input clocks (64 MHz)

CLK A/B/C O [LVDS] output clocks (128 MHz)

48 VDC [+/-] Power

8 Pinouts, Pin Locations and Programming Notes

8.1 Pinouts by signal name

Note: UNUSED and NC pins have been removed.

```
Release 10.1.03 - par K.39 (nt)
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Tue Jun 22 22:07:42 2010

INPUT FILE:       input_top_map.ncd
OUTPUT FILE:      input_top_pad.txt
PART TYPE:        xc4vlx40
SPEED GRADE:      -10
PACKAGE:          ff1148

+-----------------------------------------------------------------------------------------+
|Pin       |Signal Name   |Pin Usage|Pin Name            |Direction  |IO Standard |IO Bank|
+-----------------------------------------------------------------------------------------+
|E9        |ATIME_A       |IOB      |IO_L19N_6           |INPUT      |HSTL_I_DCI  |6      |
|M8        |ATIME_B       |IOB      |IO_L15N_10          |INPUT      |HSTL_I_DCI  |10     |
|AG7       |ATIME_C       |IOB      |IO_L31N_12          |INPUT      |HSTL_I_DCI  |12     |
|C12       |data_a[0]     |IOB      |IO_L1N_6            |INPUT      |HSTL_I_DCI  |6      |
|D12       |data_a[1]     |IOB      |IO_L1P_6            |INPUT      |HSTL_I_DCI  |6      |
|D10       |data_a[10]    |IOB      |IO_L7N_6            |INPUT      |HSTL_I_DCI  |6      |
|F10       |data_a[11]    |IOB      |IO_L6P_6            |INPUT      |HSTL_I_DCI  |6      |
|G10       |data_a[12]    |IOB      |IO_L6N_6            |INPUT      |HSTL_I_DCI  |6      |
|H10       |data_a[13]    |IOB      |IO_L8P_CC_LC_6      |INPUT      |HSTL_I_DCI  |6      |
|C9        |data_a[14]    |IOB      |IO_L4P_6            |INPUT      |HSTL_I_DCI  |6      |
|D9        |data_a[15]    |IOB      |IO_L19P_6           |INPUT      |HSTL_I_DCI  |6      |
|B8        |data_a[16]    |IOB      |IO_L10N_6           |INPUT      |HSTL_I_DCI  |6      |
|G8        |data_a[17]    |IOB      |IO_L16N_6           |INPUT      |HSTL_I_DCI  |6      |
|H8        |data_a[18]    |IOB      |IO_L31P_6           |INPUT      |HSTL_I_DCI  |6      |
|B7        |data_a[19]    |IOB      |IO_L14P_6           |INPUT      |HSTL_I_DCI  |6      |
|A11       |data_a[2]     |IOB      |IO_L3P_6            |INPUT      |HSTL_I_DCI  |6      |
|C7        |data_a[20]    |IOB      |IO_L14N_6           |INPUT      |HSTL_I_DCI  |6      |
|D7        |data_a[21]    |IOB      |IO_L18P_6           |INPUT      |HSTL_I_DCI  |6      |
|G7        |data_a[22]    |IOB      |IO_L28P_6           |INPUT      |HSTL_I_DCI  |6      |
|H7        |data_a[23]    |IOB      |IO_L31N_6           |INPUT      |HSTL_I_DCI  |6      |
|A6        |data_a[24]    |IOB      |IO_L12P_6           |INPUT      |HSTL_I_DCI  |6      |
|D6        |data_a[25]    |IOB      |IO_L18N_6           |INPUT      |HSTL_I_DCI  |6      |
|E6        |data_a[26]    |IOB      |IO_L26P_6           |INPUT      |HSTL_I_DCI  |6      |
|F6        |data_a[27]    |IOB      |IO_L26N_6           |INPUT      |HSTL_I_DCI  |6      |
|J6        |data_a[28]    |IOB      |IO_L10P_10          |INPUT      |HSTL_I_DCI  |10     |
|A5        |data_a[29]    |IOB      |IO_L22P_6           |INPUT      |HSTL_I_DCI  |6      |
|B11       |data_a[3]     |IOB      |IO_L3N_6            |INPUT      |HSTL_I_DCI  |6      |
|B5        |data_a[30]    |IOB      |IO_L22N_6           |INPUT      |HSTL_I_DCI  |6      |
|D5        |data_a[31]    |IOB      |IO_L27N_6           |INPUT      |HSTL_I_DCI  |6      |
|D11       |data_a[4]     |IOB      |IO_L7P_6            |INPUT      |HSTL_I_DCI  |6      |
|E11       |data_a[5]     |IOB      |IO_L11P_6           |INPUT      |HSTL_I_DCI  |6      |
|F11       |data_a[6]     |IOB      |IO_L11N_6           |INPUT      |HSTL_I_DCI  |6      |
|A10       |data_a[7]     |IOB      |IO_L15P_6           |INPUT      |HSTL_I_DCI  |6      |
|B10       |data_a[8]     |IOB      |IO_L2P_6            |INPUT      |HSTL_I_DCI  |6      |
|C10       |data_a[9]     |IOB      |IO_L2N_6            |INPUT      |HSTL_I_DCI  |6      |
|C2        |data_b[0]     |IOB      |IO_L7P_10           |INPUT      |HSTL_I_DCI  |10     |
|D2        |data_b[1]     |IOB      |IO_L7N_10           |INPUT      |HSTL_I_DCI  |10     |
|H2        |data_b[10]    |IOB      |IO_L19N_10          |INPUT      |HSTL_I_DCI  |10     |
|J4        |data_b[11]    |IOB      |IO_L18P_10          |INPUT      |HSTL_I_DCI  |10     |
|K6        |data_b[12]    |IOB      |IO_L16P_10          |INPUT      |HSTL_I_DCI  |10     |
|K4        |data_b[13]    |IOB      |IO_L18N_10          |INPUT      |HSTL_I_DCI  |10     |
|K2        |data_b[14]    |IOB      |IO_L26P_10          |INPUT      |HSTL_I_DCI  |10     |
|L8        |data_b[15]    |IOB      |IO_L15P_10          |INPUT      |HSTL_I_DCI  |10     |
|L6        |data_b[16]    |IOB      |IO_L16N_10          |INPUT      |HSTL_I_DCI  |10     |
|L5        |data_b[17]    |IOB      |IO_L22P_10          |INPUT      |HSTL_I_DCI  |10     |
|L4        |data_b[18]    |IOB      |IO_L22N_10          |INPUT      |HSTL_I_DCI  |10     |
|L3        |data_b[19]    |IOB      |IO_L25N_CC_LC_10    |INPUT      |HSTL_I_DCI  |10     |
|E2        |data_b[2]     |IOB      |IO_L9N_CC_LC_10     |INPUT      |HSTL_I_DCI  |10     |
|L1        |data_b[20]    |IOB      |IO_L29P_10          |INPUT      |HSTL_I_DCI  |10     |
|M6        |data_b[21]    |IOB      |IO_L27P_10          |INPUT      |HSTL_I_DCI  |10     |
|M3        |data_b[22]    |IOB      |IO_L28P_10          |INPUT      |HSTL_I_DCI  |10     |
|M1        |data_b[23]    |IOB      |IO_L29N_10          |INPUT      |HSTL_I_DCI  |10     |
|M10       |data_b[24]    |IOB      |IO_L4P_10           |INPUT      |HSTL_I_DCI  |10     |
|N10       |data_b[25]    |IOB      |IO_L12P_10          |INPUT      |HSTL_I_DCI  |10     |
|P10       |data_b[26]    |IOB      |IO_L20P_10          |INPUT      |HSTL_I_DCI  |10     |
|R9        |data_b[27]    |IOB      |IO_L32N_10          |INPUT      |HSTL_I_DCI  |10     |
|N7        |data_b[28]    |IOB      |IO_L21N_10          |INPUT      |HSTL_I_DCI  |10     |
|P7        |data_b[29]    |IOB      |IO_L31P_10          |INPUT      |HSTL_I_DCI  |10     |
|G3        |data_b[3]     |IOB      |IO_L14P_10          |INPUT      |HSTL_I_DCI  |10     |
|P6        |data_b[30]    |IOB      |IO_L31N_10          |INPUT      |HSTL_I_DCI  |10     |
|P11       |data_b[31]    |IOB      |IO_L13N_10          |INPUT      |HSTL_I_DCI  |10     |
|H3        |data_b[4]     |IOB      |IO_L19P_10          |INPUT      |HSTL_I_DCI  |10     |
|D1        |data_b[5]     |IOB      |IO_L8P_CC_LC_10     |INPUT      |HSTL_I_DCI  |10     |
|E1        |data_b[6]     |IOB      |IO_L8N_CC_LC_10     |INPUT      |HSTL_I_DCI  |10     |
|F1        |data_b[7]     |IOB      |IO_L17P_10          |INPUT      |HSTL_I_DCI  |10     |
|G2        |data_b[8]     |IOB      |IO_L14N_10          |INPUT      |HSTL_I_DCI  |10     |
|G1        |data_b[9]     |IOB      |IO_L17N_10          |INPUT      |HSTL_I_DCI  |10     |
|AA8       |data_c[0]     |IOB      |IO_L8N_CC_LC_12     |INPUT      |HSTL_I_DCI  |12     |
|AB10      |data_c[1]     |IOB      |IO_L25N_CC_LC_12    |INPUT      |HSTL_I_DCI  |12     |
|AF8       |data_c[10]    |IOB      |IO_L27P_12          |INPUT      |HSTL_I_DCI  |12     |
|AG8       |data_c[11]    |IOB      |IO_L31P_12          |INPUT      |HSTL_I_DCI  |12     |
|AD7       |data_c[12]    |IOB      |IO_L24N_CC_LC_12    |INPUT      |HSTL_I_DCI  |12     |
|AE7       |data_c[13]    |IOB      |IO_L24P_CC_LC_12    |INPUT      |HSTL_I_DCI  |12     |
|AD6       |data_c[14]    |IOB      |IO_L11P_12          |INPUT      |HSTL_I_DCI  |12     |
|AE6       |data_c[15]    |IOB      |IO_L19N_12          |INPUT      |HSTL_I_DCI  |12     |
|AD5       |data_c[16]    |IOB      |IO_L11N_12          |INPUT      |HSTL_I_DCI  |12     |
|AH5       |data_c[17]    |IOB      |IO_L28P_12          |INPUT      |HSTL_I_DCI  |12     |
|AD4       |data_c[18]    |IOB      |IO_L14N_12          |INPUT      |HSTL_I_DCI  |12     |
|AC3       |data_c[19]    |IOB      |IO_L2P_12           |INPUT      |HSTL_I_DCI  |12     |
|AC10      |data_c[2]     |IOB      |IO_L25P_CC_LC_12    |INPUT      |HSTL_I_DCI  |12     |
|AE3       |data_c[20]    |IOB      |IO_L10P_12          |INPUT      |HSTL_I_DCI  |12     |
|AF3       |data_c[21]    |IOB      |IO_L18N_12          |INPUT      |HSTL_I_DCI  |12     |
|AG3       |data_c[22]    |IOB      |IO_L18P_12          |INPUT      |HSTL_I_DCI  |12     |
|AH3       |data_c[23]    |IOB      |IO_L15P_12          |INPUT      |HSTL_I_DCI  |12     |
|AK3       |data_c[24]    |IOB      |IO_L26P_12          |INPUT      |HSTL_I_DCI  |12     |
|AL1       |data_c[25]    |IOB      |IO_L21P_12          |INPUT      |HSTL_I_DCI  |12     |
|AM3       |data_c[26]    |IOB      |IO_L32P_12          |INPUT      |HSTL_I_DCI  |12     |
|AC2       |data_c[27]    |IOB      |IO_L2N_12           |INPUT      |HSTL_I_DCI  |12     |
|AD2       |data_c[28]    |IOB      |IO_L4P_12           |INPUT      |HSTL_I_DCI  |12     |
|AE2       |data_c[29]    |IOB      |IO_L10N_12          |INPUT      |HSTL_I_DCI  |12     |
|AC9       |data_c[3]     |IOB      |IO_L17P_12          |INPUT      |HSTL_I_DCI  |12     |
|AG2       |data_c[30]    |IOB      |IO_L16P_12          |INPUT      |HSTL_I_DCI  |12     |
|AK1       |data_c[31]    |IOB      |IO_L21N_12          |INPUT      |HSTL_I_DCI  |12     |
|AC8       |data_c[4]     |IOB      |IO_L17N_12          |INPUT      |HSTL_I_DCI  |12     |
|AB6       |data_c[5]     |IOB      |IO_L1P_12           |INPUT      |HSTL_I_DCI  |12     |
|AC7       |data_c[6]     |IOB      |IO_L12P_12          |INPUT      |HSTL_I_DCI  |12     |
|AB5       |data_c[7]     |IOB      |IO_L1N_12           |INPUT      |HSTL_I_DCI  |12     |
|AC5       |data_c[8]     |IOB      |IO_L6P_12           |INPUT      |HSTL_I_DCI  |12     |
|AE8       |data_c[9]     |IOB      |IO_L27N_12          |INPUT      |HSTL_I_DCI  |12     |
|A29       |data_VSI0[0]  |IOB      |IO_L14N_5           |INPUT      |HSTL_III_DCI|5      |
|A28       |data_VSI0[1]  |IOB      |IO_L14P_5           |INPUT      |HSTL_III_DCI|5      |
|B28       |data_VSI0[10] |IOB      |IO_L25P_CC_LC_5     |INPUT      |HSTL_III_DCI|5      |
|B27       |data_VSI0[11] |IOB      |IO_L8P_CC_LC_5      |INPUT      |HSTL_III_DCI|5      |
|B26       |data_VSI0[12] |IOB      |IO_L2N_5            |INPUT      |HSTL_III_DCI|5      |
|B25       |data_VSI0[13] |IOB      |IO_L15P_5           |INPUT      |HSTL_III_DCI|5      |
|C34       |data_VSI0[14] |IOB      |IO_L7N_9            |INPUT      |HSTL_III_DCI|9      |
|C33       |data_VSI0[15] |IOB      |IO_L7P_9            |INPUT      |HSTL_III_DCI|9      |
|C32       |data_VSI0[16] |IOB      |IO_L2P_9            |INPUT      |HSTL_III_DCI|9      |
|C29       |data_VSI0[17] |IOB      |IO_L20P_5           |INPUT      |HSTL_III_DCI|5      |
|C28       |data_VSI0[18] |IOB      |IO_L25N_CC_LC_5     |INPUT      |HSTL_III_DCI|5      |
|C27       |data_VSI0[19] |IOB      |IO_L8N_CC_LC_5      |INPUT      |HSTL_III_DCI|5      |
|A26       |data_VSI0[2]  |IOB      |IO_L2P_5            |INPUT      |HSTL_III_DCI|5      |
|C25       |data_VSI0[20] |IOB      |IO_L15N_5           |INPUT      |HSTL_III_DCI|5      |
|D34       |data_VSI0[21] |IOB      |IO_L8P_CC_LC_9      |INPUT      |HSTL_III_DCI|9      |
|D32       |data_VSI0[22] |IOB      |IO_L2N_9            |INPUT      |HSTL_III_DCI|9      |
|D31       |data_VSI0[23] |IOB      |IO_L26N_5           |INPUT      |HSTL_III_DCI|5      |
|D30       |data_VSI0[24] |IOB      |IO_L26P_5           |INPUT      |HSTL_III_DCI|5      |
|D29       |data_VSI0[25] |IOB      |IO_L29P_5           |INPUT      |HSTL_III_DCI|5      |
|D27       |data_VSI0[26] |IOB      |IO_L12P_5           |INPUT      |HSTL_III_DCI|5      |
|E34       |data_VSI0[27] |IOB      |IO_L8N_CC_LC_9      |INPUT      |HSTL_III_DCI|9      |
|E33       |data_VSI0[28] |IOB      |IO_L11N_9           |INPUT      |HSTL_III_DCI|9      |
|E32       |data_VSI0[29] |IOB      |IO_L11P_9           |INPUT      |HSTL_III_DCI|9      |
|A25       |data_VSI0[3]  |IOB      |IO_L3N_5            |INPUT      |HSTL_III_DCI|5      |
|E31       |data_VSI0[30] |IOB      |IO_L32P_5           |INPUT      |HSTL_III_DCI|5      |
|E29       |data_VSI0[31] |IOB      |IO_L29N_5           |INPUT      |HSTL_III_DCI|5      |
|A24       |data_VSI0[4]  |IOB      |IO_L3P_5            |INPUT      |HSTL_III_DCI|5      |
|A23       |data_VSI0[5]  |IOB      |IO_L1N_5            |INPUT      |HSTL_III_DCI|5      |
|B33       |data_VSI0[6]  |IOB      |IO_L31N_5           |INPUT      |HSTL_III_DCI|5      |
|B32       |data_VSI0[7]  |IOB      |IO_L31P_5           |INPUT      |HSTL_III_DCI|5      |
|B31       |data_VSI0[8]  |IOB      |IO_L24N_CC_LC_5     |INPUT      |HSTL_III_DCI|5      |
|B30       |data_VSI0[9]  |IOB      |IO_L18N_5           |INPUT      |HSTL_III_DCI|5      |
|G33       |data_VSI1[0]  |IOB      |IO_L16N_9           |INPUT      |HSTL_III_DCI|9      |
|G32       |data_VSI1[1]  |IOB      |IO_L16P_9           |INPUT      |HSTL_III_DCI|9      |
|J30       |data_VSI1[10] |IOB      |IO_L10N_9           |INPUT      |HSTL_III_DCI|9      |
|J29       |data_VSI1[11] |IOB      |IO_L10P_9           |INPUT      |HSTL_III_DCI|9      |
|J27       |data_VSI1[12] |IOB      |IO_L3P_9            |INPUT      |HSTL_III_DCI|9      |
|K34       |data_VSI1[13] |IOB      |IO_L29N_9           |INPUT      |HSTL_III_DCI|9      |
|K33       |data_VSI1[14] |IOB      |IO_L26N_9           |INPUT      |HSTL_III_DCI|9      |
|K32       |data_VSI1[15] |IOB      |IO_L26P_9           |INPUT      |HSTL_III_DCI|9      |
|K29       |data_VSI1[16] |IOB      |IO_L15N_9           |INPUT      |HSTL_III_DCI|9      |
|K28       |data_VSI1[17] |IOB      |IO_L15P_9           |INPUT      |HSTL_III_DCI|9      |
|K27       |data_VSI1[18] |IOB      |IO_L3N_9            |INPUT      |HSTL_III_DCI|9      |
|L34       |data_VSI1[19] |IOB      |IO_L31N_9           |INPUT      |HSTL_III_DCI|9      |
|G31       |data_VSI1[2]  |IOB      |IO_L9N_CC_LC_9      |INPUT      |HSTL_III_DCI|9      |
|L33       |data_VSI1[20] |IOB      |IO_L31P_9           |INPUT      |HSTL_III_DCI|9      |
|L31       |data_VSI1[21] |IOB      |IO_L24N_CC_LC_9     |INPUT      |HSTL_III_DCI|9      |
|L30       |data_VSI1[22] |IOB      |IO_L24P_CC_LC_9     |INPUT      |HSTL_III_DCI|9      |
|L29       |data_VSI1[23] |IOB      |IO_L18N_9           |INPUT      |HSTL_III_DCI|9      |
|L28       |data_VSI1[24] |IOB      |IO_L18P_9           |INPUT      |HSTL_III_DCI|9      |
|M33       |data_VSI1[25] |IOB      |IO_L32N_9           |INPUT      |HSTL_III_DCI|9      |
|M32       |data_VSI1[26] |IOB      |IO_L32P_9           |INPUT      |HSTL_III_DCI|9      |
|M30       |data_VSI1[27] |IOB      |IO_L28P_9           |INPUT      |HSTL_III_DCI|9      |
|N30       |data_VSI1[28] |IOB      |IO_L30N_9           |INPUT      |HSTL_III_DCI|9      |
|N29       |data_VSI1[29] |IOB      |IO_L30P_9           |INPUT      |HSTL_III_DCI|9      |
|G30       |data_VSI1[3]  |IOB      |IO_L9P_CC_LC_9      |INPUT      |HSTL_III_DCI|9      |
|P27       |data_VSI1[30] |IOB      |IO_L27N_9           |INPUT      |HSTL_III_DCI|9      |
|N27       |data_VSI1[31] |IOB      |IO_L27P_9           |INPUT      |HSTL_III_DCI|9      |
|H33       |data_VSI1[4]  |IOB      |IO_L22P_9           |INPUT      |HSTL_III_DCI|9      |
|H32       |data_VSI1[5]  |IOB      |IO_L20P_9           |INPUT      |HSTL_III_DCI|9      |
|H30       |data_VSI1[6]  |IOB      |IO_L6N_9            |INPUT      |HSTL_III_DCI|9      |
|H29       |data_VSI1[7]  |IOB      |IO_L6P_9            |INPUT      |HSTL_III_DCI|9      |
|H28       |data_VSI1[8]  |IOB      |IO_L1N_9            |INPUT      |HSTL_III_DCI|9      |
|J34       |data_VSI1[9]  |IOB      |IO_L29P_9           |INPUT      |HSTL_III_DCI|9      |
|A30       |dpps_VSI0     |IOB      |IO_L18P_5           |INPUT      |HSTL_III_DCI|5      |
|H34       |dpps_VSI1     |IOB      |IO_L22N_9           |INPUT      |HSTL_III_DCI|9      |
|A31       |dtick_VSI0    |IOB      |IO_L24P_CC_LC_5     |INPUT      |HSTL_III_DCI|5      |
|F34       |dtick_VSI1    |IOB      |IO_L14N_9           |INPUT      |HSTL_III_DCI|9      |
|B12       |DTIME_A       |IOB      |IO_L9N_CC_LC_6      |INPUT      |HSTL_I_DCI  |6      |
|B2        |DTIME_B       |IOB      |IO_L30N_6           |INPUT      |HSTL_I_DCI  |6      |
|AB12      |DTIME_C       |IOB      |IO_L29N_12          |INPUT      |HSTL_I_DCI  |12     |
|C5        |dval_a        |IOB      |IO_L27P_6           |INPUT      |HSTL_I_DCI  |6      |
|P12       |dval_b        |IOB      |IO_L13P_10          |INPUT      |HSTL_I_DCI  |10     |
|AJ2       |dval_c        |IOB      |IO_L22P_12          |INPUT      |HSTL_I_DCI  |12     |
|C24       |dval_VSI0     |IOB      |IO_L5N_5            |INPUT      |HSTL_III_DCI|5      |
|K26       |dval_VSI1     |IOB      |IO_L16N_5           |INPUT      |HSTL_III_DCI|5      |
|E14       |fe_hstl[0]    |IOB      |IO_L29P_6           |OUTPUT     |LVCMOS15    |6      |
|A13       |fe_hstl[1]    |IOB      |IO_L17N_6           |OUTPUT     |LVCMOS15    |6      |
|F5        |fe_hstl[10]   |IOB      |IO_L2P_10           |OUTPUT     |LVCMOS15    |10     |
|J5        |fe_hstl[11]   |IOB      |IO_L10N_10          |OUTPUT     |LVCMOS15    |10     |
|G5        |fe_hstl[12]   |IOB      |IO_L2N_10           |OUTPUT     |LVCMOS15    |10     |
|A4        |fe_hstl[13]   |IOB      |IO_L20P_6           |OUTPUT     |LVCMOS15    |6      |
|E4        |fe_hstl[14]   |IOB      |IO_L3N_10           |OUTPUT     |LVCMOS15    |10      |
|E3        |fe_hstl[15]   |IOB      |IO_L9P_CC_LC_10     |OUTPUT     |LVCMOS15    |10      |
|C4        |fe_hstl[16]   |IOB      |IO_L1P_10           |OUTPUT     |LVCMOS15    |10      |
|B3        |fe_hstl[17]   |IOB      |IO_L30P_6           |OUTPUT     |LVCMOS15    |6       |
|F4        |fe_hstl[18]   |IOB      |IO_L6P_10           |OUTPUT     |LVCMOS15    |10      |
|F3        |fe_hstl[19]   |IOB      |IO_L6N_10           |OUTPUT     |LVCMOS15    |10      |
|D14       |fe_hstl[2]    |IOB      |IO_L29N_6           |OUTPUT     |LVCMOS15    |6       |
|D4        |fe_hstl[20]   |IOB      |IO_L3P_10           |OUTPUT     |LVCMOS15    |10      |
|C3        |fe_hstl[21]   |IOB      |IO_L1N_10           |OUTPUT     |LVCMOS15    |10      |
|H4        |fe_hstl[22]   |IOB      |IO_L11N_10          |OUTPUT     |LVCMOS15    |10      |
|N12       |fe_hstl[23]   |IOB      |IO_L5N_10           |OUTPUT     |LVCMOS15    |10      |
|R11       |fe_hstl[24]   |IOB      |IO_L24P_CC_LC_10    |OUTPUT     |LVCMOS15    |10      |
|P5        |fe_hstl[25]   |IOB      |IO_L30N_10          |OUTPUT     |LVCMOS15    |10      |
|T11       |fe_hstl[26]   |IOB      |IO_L24N_CC_LC_10    |OUTPUT     |LVCMOS15    |10      |
|N5        |fe_hstl[27]   |IOB      |IO_L30P_10          |OUTPUT     |LVCMOS15    |10      |
|T10       |fe_hstl[28]   |IOB      |IO_L32P_10          |OUTPUT     |LVCMOS15    |10      |
|Y12       |fe_hstl[29]   |IOB      |IO_L9N_CC_LC_12     |OUTPUT     |LVCMOS15    |12      |
|C13       |fe_hstl[3]    |IOB      |IO_L25N_CC_LC_6     |OUTPUT     |LVCMOS15    |6       |
|AA9       |fe_hstl[30]   |IOB      |IO_L8P_CC_LC_12     |OUTPUT     |LVCMOS15    |12      |
|Y14       |fe_hstl[31]   |IOB      |IO_L5P_12           |OUTPUT     |LVCMOS15    |12      |
|AA13      |fe_hstl[32]   |IOB      |IO_L5N_12           |OUTPUT     |LVCMOS15    |12      |
|Y11       |fe_hstl[33]   |IOB      |IO_L3P_12           |OUTPUT     |LVCMOS15    |12      |
|AB13      |fe_hstl[34]   |IOB      |IO_L29P_12          |OUTPUT     |LVCMOS15    |12      |
|Y13       |fe_hstl[35]   |IOB      |IO_L9P_CC_LC_12     |OUTPUT     |LVCMOS15    |12      |
|AA11      |fe_hstl[36]   |IOB      |IO_L3N_12           |OUTPUT     |LVCMOS15    |12      |
|AA15      |fe_hstl[37]   |IOB      |IO_L13N_12          |OUTPUT     |LVCMOS15    |12      |
|AH2       |fe_hstl[38]   |IOB      |IO_L15N_12          |OUTPUT     |LVCMOS15    |12      |
|AF1       |fe_hstl[39]   |IOB      |IO_L7P_12           |OUTPUT     |LVCMOS15    |12      |
|C14       |fe_hstl[4]    |IOB      |IO_L25P_CC_LC_6     |OUTPUT     |LVCMOS15    |6       |
|AM1       |fe_hstl[40]   |IOB      |IO_L30N_12          |OUTPUT     |LVCMOS15    |12      |
|AG1       |fe_hstl[41]   |IOB      |IO_L16N_12          |OUTPUT     |LVCMOS15    |12      |
|AE1       |fe_hstl[42]   |IOB      |IO_L7N_12           |OUTPUT     |LVCMOS15    |12      |
|AJ1       |fe_hstl[43]   |IOB      |IO_L22N_12          |OUTPUT     |LVCMOS15    |12      |
|E12       |fe_hstl[5]    |IOB      |IO_L21N_6           |OUTPUT     |LVCMOS15    |6       |
|A14       |fe_hstl[6]    |IOB      |IO_L17P_6           |OUTPUT     |LVCMOS15    |6       |
|B13       |fe_hstl[7]    |IOB      |IO_L9P_CC_LC_6      |OUTPUT     |LVCMOS15    |6       |
|E13       |fe_hstl[8]    |IOB      |IO_L21P_6           |OUTPUT     |LVCMOS15    |6       |
|H5        |fe_hstl[9]    |IOB      |IO_L11P_10          |OUTPUT     |LVCMOS15    |10      |
|A9        |fom_clk_a     |IOB      |IO_L15N_6           |OUTPUT     |HSTL_I_DCI  |6       |
|K1        |fom_clk_b     |IOB      |IO_L26N_10          |OUTPUT     |HSTL_I_DCI  |10      |
|AC4       |fom_clk_c     |IOB      |IO_L6N_12           |OUTPUT     |HSTL_I_DCI  |12      |
|A8        |fom_tick_a    |IOB      |IO_L10P_6           |OUTPUT     |HSTL_I_DCI  |6       |
|M7        |fom_tick_b    |IOB      |IO_L21P_10          |OUTPUT     |HSTL_I_DCI  |10      |
|AF6       |fom_tick_c    |IOB      |IO_L19P_12          |OUTPUT     |HSTL_I_DCI  |12      |
|AL20      |mcb_addr_p[0] |IOB      |IO_L19N_LC_2        |INPUT      |LVCMOS25*   |2       |
|AJ20      |mcb_addr_p[1] |IOB      |IO_L19P_LC_2        |INPUT      |LVCMOS25*   |2       |
|AJ21      |mcb_addr_p[2] |IOB      |IO_L1N_D14_CC_LC_2  |INPUT      |LVCMOS25*   |2       |
|AJ22      |mcb_addr_p[3] |IOB      |IO_L1P_D15_CC_LC_2  |INPUT      |LVCMOS25*   |2       |
|AH20      |mcb_addr_p[4] |IOB      |IO_L21N_LC_2        |INPUT      |LVCMOS25*   |2       |
|AH22      |mcb_addr_p[5] |IOB      |IO_L3N_D10_LC_2     |INPUT      |LVCMOS25*   |2       |
|AG20      |mcb_addr_p[6] |IOB      |IO_L21P_LC_2        |INPUT      |LVCMOS25*   |2       |
|AG22      |mcb_addr_p[7] |IOB      |IO_L3P_D11_LC_2     |INPUT      |LVCMOS25*   |2       |
|AM20      |mcb_clk_p     |IOB      |IO_L13P_GC_LC_2     |INPUT      |LVCMOS25*   |2       |
|AM15      |mcb_cs_p      |IOB      |IO_L18P_LC_2        |INPUT      |LVCMOS25*   |2       |
|AL14      |mcb_data_p[0] |IOB      |IO_L4P_D9_LC_2      |BIDIR      |LVCMOS25*   |2       |
|AL15      |mcb_data_p[1] |IOB      |IO_L18N_LC_2        |BIDIR      |LVCMOS25*   |2       |
|AD16      |mcb_data_p[10]|IOB      |IO_L10P_GC_LC_2     |BIDIR      |LVCMOS25*   |2       |
|AD17      |mcb_data_p[11]|IOB      |IO_L12P_GC_LC_2     |BIDIR      |LVCMOS25*   |2       |
|AC15      |mcb_data_p[12]|IOB      |IO_L2P_D13_LC_2     |BIDIR      |LVCMOS25*   |2       |
|AC17      |mcb_data_p[13]|IOB      |IO_L12N_GC_VREF_LC_2|BIDIR      |LVCMOS25*   |2       |
|AB15      |mcb_data_p[14]|IOB      |IO_L2N_D12_LC_2     |BIDIR      |LVCMOS25*   |2       |
|AB16      |mcb_data_p[15]|IOB      |IO_L14N_GC_LC_2     |BIDIR      |LVCMOS25*   |2       |
|AL16      |mcb_data_p[2] |IOB      |IO_L24P_CC_LC_2     |BIDIR      |LVCMOS25*   |2       |
|AK14      |mcb_data_p[3] |IOB      |IO_L4N_D8_VREF_LC_2 |BIDIR      |LVCMOS25*   |2       |
|AK16      |mcb_data_p[4] |IOB      |IO_L24N_CC_LC_2     |BIDIR      |LVCMOS25*   |2       |
|AJ14      |mcb_data_p[5] |IOB      |IO_L20N_VREF_LC_2   |BIDIR      |LVCMOS25*   |2       |
|AJ15      |mcb_data_p[6] |IOB      |IO_L20P_LC_2        |BIDIR      |LVCMOS25*   |2       |
|AH14      |mcb_data_p[7] |IOB      |IO_L22N_LC_2        |BIDIR      |LVCMOS25*   |2       |
|AG15      |mcb_data_p[8] |IOB      |IO_L22P_LC_2        |BIDIR      |LVCMOS25*   |2      |
|AF15      |mcb_data_p[9] |IOB      |IO_L10N_GC_LC_2     |BIDIR      |LVCMOS25*   |2      |
|AL19      |mcb_rw_p      |IOB      |IO_L13N_GC_LC_2     |INPUT      |LVCMOS25*   |2      |
|AK4       |odata_100PPS_a|IOB      |IO_L2P_8            |OUTPUT     |HSTL_III    |8      |
|AP26      |odata_100PPS_b|IOB      |IO_L15N_7           |OUTPUT     |HSTL_III    |7      |
|AP24      |odata_a[0]    |IOB      |IO_L29P_SM4_7       |OUTPUT     |HSTL_III    |7      |
|AP25      |odata_a[1]    |IOB      |IO_L15P_7           |OUTPUT     |HSTL_III    |7      |
|AP21      |odata_a[10]   |IOB      |IO_L17P_7           |OUTPUT     |HSTL_III    |7      |
|AK22      |odata_a[11]   |IOB      |IO_L13P_7           |OUTPUT     |HSTL_III    |7      |
|AL21      |odata_a[12]   |IOB      |IO_L5N_7            |OUTPUT     |HSTL_III    |7      |
|AM21      |odata_a[13]   |IOB      |IO_L9P_CC_LC_7      |OUTPUT     |HSTL_III    |7      |
|AP14      |odata_a[14]   |IOB      |IO_L5N_8            |OUTPUT     |HSTL_III    |8      |
|AK21      |odata_a[15]   |IOB      |IO_L5P_7            |OUTPUT     |HSTL_III    |7      |
|AN13      |odata_a[16]   |IOB      |IO_L13N_8           |OUTPUT     |HSTL_III    |8      |
|AN14      |odata_a[17]   |IOB      |IO_L5P_8            |OUTPUT     |HSTL_III    |8      |
|AL13      |odata_a[18]   |IOB      |IO_L9N_CC_LC_8      |OUTPUT     |HSTL_III    |8      |
|AM13      |odata_a[19]   |IOB      |IO_L13P_8           |OUTPUT     |HSTL_III    |8      |
|AN23      |odata_a[2]    |IOB      |IO_L27N_SM5_7       |OUTPUT     |HSTL_III    |7      |
|AP12      |odata_a[20]   |IOB      |IO_L31N_8           |OUTPUT     |HSTL_III    |8      |
|AK13      |odata_a[21]   |IOB      |IO_L9P_CC_LC_8      |OUTPUT     |HSTL_III    |8      |
|AN12      |odata_a[22]   |IOB      |IO_L31P_8           |OUTPUT     |HSTL_III    |8      |
|AP11      |odata_a[23]   |IOB      |IO_L29P_8           |OUTPUT     |HSTL_III    |8      |
|AK12      |odata_a[24]   |IOB      |IO_L21N_8           |OUTPUT     |HSTL_III    |8      |
|AM12      |odata_a[25]   |IOB      |IO_L27P_8           |OUTPUT     |HSTL_III    |8      |
|AL11      |odata_a[26]   |IOB      |IO_L25P_CC_LC_8     |OUTPUT     |HSTL_III    |8      |
|AM11      |odata_a[27]   |IOB      |IO_L27N_8           |OUTPUT     |HSTL_III    |8      |
|AH12      |odata_a[28]   |IOB      |IO_L17P_8           |OUTPUT     |HSTL_III    |8      |
|AJ12      |odata_a[29]   |IOB      |IO_L21P_8           |OUTPUT     |HSTL_III    |8      |
|AN24      |odata_a[3]    |IOB      |IO_L29N_SM4_7       |OUTPUT     |HSTL_III    |7      |
|AP10      |odata_a[30]   |IOB      |IO_L29N_8           |OUTPUT     |HSTL_III    |8      |
|AG11      |odata_a[31]   |IOB      |IO_L17N_8           |OUTPUT     |HSTL_III    |8      |
|AM10      |odata_a[32]   |IOB      |IO_L19N_8           |OUTPUT     |HSTL_III    |8      |
|AN10      |odata_a[33]   |IOB      |IO_L19P_8           |OUTPUT     |HSTL_III    |8      |
|AP9       |odata_a[34]   |IOB      |IO_L32P_8           |OUTPUT     |HSTL_III    |8      |
|AL10      |odata_a[35]   |IOB      |IO_L25N_CC_LC_8     |OUTPUT     |HSTL_III    |8       |
|AL9       |odata_a[36]   |IOB      |IO_L28P_8           |OUTPUT     |HSTL_III    |8       |
|AN9       |odata_a[37]   |IOB      |IO_L32N_8           |OUTPUT     |HSTL_III    |8       |
|AJ9       |odata_a[38]   |IOB      |IO_L15N_8           |OUTPUT     |HSTL_III    |8       |
|AJ10      |odata_a[39]   |IOB      |IO_L15P_8           |OUTPUT     |HSTL_III    |8       |
|AL23      |odata_a[4]    |IOB      |IO_L31P_SM2_7       |OUTPUT     |HSTL_III    |7       |
|AG10      |odata_a[40]   |IOB      |IO_L30N_8           |OUTPUT     |HSTL_III    |8       |
|AH10      |odata_a[41]   |IOB      |IO_L30P_8           |OUTPUT     |HSTL_III    |8       |
|AP7       |odata_a[42]   |IOB      |IO_L24P_CC_LC_8     |OUTPUT     |HSTL_III    |8       |
|AN8       |odata_a[43]   |IOB      |IO_L22P_8           |OUTPUT     |HSTL_III    |8       |
|AM8       |odata_a[44]   |IOB      |IO_L22N_8           |OUTPUT     |HSTL_III    |8       |
|AN7       |odata_a[45]   |IOB      |IO_L18P_8           |OUTPUT     |HSTL_III    |8       |
|AL8       |odata_a[46]   |IOB      |IO_L11P_8           |OUTPUT     |HSTL_III    |8       |
|AM7       |odata_a[47]   |IOB      |IO_L18N_8           |OUTPUT     |HSTL_III    |8       |
|AH8       |odata_a[48]   |IOB      |IO_L12P_8           |OUTPUT     |HSTL_III    |8       |
|AK8       |odata_a[49]   |IOB      |IO_L11N_8           |OUTPUT     |HSTL_III    |8       |
|AM23      |odata_a[5]    |IOB      |IO_L31N_SM2_7       |OUTPUT     |HSTL_III    |7       |
|AJ7       |odata_a[50]   |IOB      |IO_L7N_8            |OUTPUT     |HSTL_III    |8       |
|AK7       |odata_a[51]   |IOB      |IO_L7P_8            |OUTPUT     |HSTL_III    |8       |
|AP5       |odata_a[52]   |IOB      |IO_L16P_8           |OUTPUT     |HSTL_III    |8       |
|AP6       |odata_a[53]   |IOB      |IO_L24N_CC_LC_8     |OUTPUT     |HSTL_III    |8       |
|AN5       |odata_a[54]   |IOB      |IO_L16N_8           |OUTPUT     |HSTL_III    |8       |
|AP4       |odata_a[55]   |IOB      |IO_L3P_8            |OUTPUT     |HSTL_III    |8       |
|AL6       |odata_a[56]   |IOB      |IO_L10P_8           |OUTPUT     |HSTL_III    |8       |
|AM6       |odata_a[57]   |IOB      |IO_L14P_8           |OUTPUT     |HSTL_III    |8       |
|AJ6       |odata_a[58]   |IOB      |IO_L6P_8            |OUTPUT     |HSTL_III    |8       |
|AK6       |odata_a[59]   |IOB      |IO_L10N_8           |OUTPUT     |HSTL_III    |8       |
|AP22      |odata_a[6]    |IOB      |IO_L17N_7           |OUTPUT     |HSTL_III    |7       |
|AN4       |odata_a[60]   |IOB      |IO_L3N_8            |OUTPUT     |HSTL_III    |8       |
|AN3       |odata_a[61]   |IOB      |IO_L8P_CC_LC_8      |OUTPUT     |HSTL_III    |8       |
|AL5       |odata_a[62]   |IOB      |IO_L1P_8            |OUTPUT     |HSTL_III    |8       |
|AM5       |odata_a[63]   |IOB      |IO_L14N_8           |OUTPUT     |HSTL_III    |8       |
|AK23      |odata_a[7]    |IOB      |IO_L13N_7           |OUTPUT     |HSTL_III    |7       |
|AM22      |odata_a[8]    |IOB      |IO_L9N_CC_LC_7      |OUTPUT     |HSTL_III    |7       |
|AN22      |odata_a[9]    |IOB      |IO_L27P_SM5_7       |OUTPUT     |HSTL_III    |7       |
|AK34      |odata_b[0]    |IOB      |IO_L26N_11          |OUTPUT     |HSTL_III    |11      |
|AL34      |odata_b[1]    |IOB      |IO_L30N_11          |OUTPUT     |HSTL_III    |11      |
|AL33      |odata_b[10]   |IOB      |IO_L30P_11          |OUTPUT     |HSTL_III    |11      |
|AM33      |odata_b[11]   |IOB      |IO_L27N_11          |OUTPUT     |HSTL_III    |11      |
|AG32      |odata_b[12]   |IOB      |IO_L13P_11          |OUTPUT     |HSTL_III    |11      |
|AK33      |odata_b[13]   |IOB      |IO_L26P_11          |OUTPUT     |HSTL_III    |11      |
|AF33      |odata_b[14]   |IOB      |IO_L14P_11          |OUTPUT     |HSTL_III    |11      |
|AG31      |odata_b[15]   |IOB      |IO_L21N_11          |OUTPUT     |HSTL_III    |11      |
|AC33      |odata_b[16]   |IOB      |IO_L6N_11           |OUTPUT     |HSTL_III    |11      |
|AE33      |odata_b[17]   |IOB      |IO_L5P_11           |OUTPUT     |HSTL_III    |11      |
|AM32      |odata_b[18]   |IOB      |IO_L27P_11          |OUTPUT     |HSTL_III    |11      |
|AN32      |odata_b[19]   |IOB      |IO_L4P_7            |OUTPUT     |HSTL_III    |7       |
|AH34      |odata_b[2]    |IOB      |IO_L18N_11          |OUTPUT     |HSTL_III    |11      |
|AH32      |odata_b[20]   |IOB      |IO_L22P_11          |OUTPUT     |HSTL_III    |11      |
|AK32      |odata_b[21]   |IOB      |IO_L25N_CC_LC_11    |OUTPUT     |HSTL_III    |11      |
|AE32      |odata_b[22]   |IOB      |IO_L10P_11          |OUTPUT     |HSTL_III    |11      |
|AF31      |odata_b[23]   |IOB      |IO_L16P_11          |OUTPUT     |HSTL_III    |11      |
|AC32      |odata_b[24]   |IOB      |IO_L6P_11           |OUTPUT     |HSTL_III    |11      |
|AD32      |odata_b[25]   |IOB      |IO_L10N_11          |OUTPUT     |HSTL_III    |11      |
|AP31      |odata_b[26]   |IOB      |IO_L12P_7           |OUTPUT     |HSTL_III    |7       |
|AE31      |odata_b[27]   |IOB      |IO_L16N_11          |OUTPUT     |HSTL_III    |11      |
|AL31      |odata_b[28]   |IOB      |IO_L31N_11          |OUTPUT     |HSTL_III    |11      |
|AM31      |odata_b[29]   |IOB      |IO_L31P_11          |OUTPUT     |HSTL_III    |11      |
|AJ34      |odata_b[3]    |IOB      |IO_L18P_11          |OUTPUT     |HSTL_III    |11      |
|AJ31      |odata_b[30]   |IOB      |IO_L28P_11          |OUTPUT     |HSTL_III    |11      |
|AK31      |odata_b[31]   |IOB      |IO_L25P_CC_LC_11    |OUTPUT     |HSTL_III    |11      |
|AP30      |odata_b[32]   |IOB      |IO_L7P_7            |OUTPUT     |HSTL_III    |7       |
|AG30      |odata_b[33]   |IOB      |IO_L21P_11          |OUTPUT     |HSTL_III    |11      |
|AM30      |odata_b[34]   |IOB      |IO_L10P_7           |OUTPUT     |HSTL_III    |7       |
|AN30      |odata_b[35]   |IOB      |IO_L7N_7            |OUTPUT     |HSTL_III    |7       |
|AJ30      |odata_b[36]   |IOB      |IO_L32P_11          |OUTPUT     |HSTL_III    |11      |
|AL30      |odata_b[37]   |IOB      |IO_L10N_7           |OUTPUT     |HSTL_III    |7       |
|AH29      |odata_b[38]   |IOB      |IO_L6N_7            |OUTPUT     |HSTL_III    |7       |
|AH30      |odata_b[39]   |IOB      |IO_L32N_11           |OUTPUT     |HSTL_III    |11      |
|AG33      |odata_b[4]    |IOB      |IO_L13N_11           |OUTPUT     |HSTL_III    |11      |
|AN29      |odata_b[40]   |IOB      |IO_L18N_7            |OUTPUT     |HSTL_III    |7       |
|AP29      |odata_b[41]   |IOB      |IO_L18P_7            |OUTPUT     |HSTL_III    |7       |
|AM28      |odata_b[42]   |IOB      |IO_L24N_CC_LC_7      |OUTPUT     |HSTL_III    |7       |
|AN28      |odata_b[43]   |IOB      |IO_L24P_CC_LC_7      |OUTPUT     |HSTL_III    |7       |
|AK29      |odata_b[44]   |IOB      |IO_L1P_7             |OUTPUT     |HSTL_III    |7       |
|AL29      |odata_b[45]   |IOB      |IO_L14N_7            |OUTPUT     |HSTL_III    |7       |
|AH28      |odata_b[46]   |IOB      |IO_L6P_7             |OUTPUT     |HSTL_III    |7       |
|AJ29      |odata_b[47]   |IOB      |IO_L1N_7             |OUTPUT     |HSTL_III    |7       |
|AM27      |odata_b[48]   |IOB      |IO_L30N_SM3_7        |OUTPUT     |HSTL_III    |7       |
|AN27      |odata_b[49]   |IOB      |IO_L11N_7            |OUTPUT     |HSTL_III    |7       |
|AH33      |odata_b[5]    |IOB      |IO_L22N_11           |OUTPUT     |HSTL_III    |11      |
|AK27      |odata_b[50]   |IOB      |IO_L20P_7            |OUTPUT     |HSTL_III    |7       |
|AL28      |odata_b[51]   |IOB      |IO_L14P_7            |OUTPUT     |HSTL_III    |7       |
|AM26      |odata_b[52]   |IOB      |IO_L30P_SM3_7        |OUTPUT     |HSTL_III    |7       |
|AP27      |odata_b[53]   |IOB      |IO_L11P_7            |OUTPUT     |HSTL_III    |7       |
|AK26      |odata_b[54]   |IOB      |IO_L26N_SM6_7        |OUTPUT     |HSTL_III    |7       |
|AL26      |odata_b[55]   |IOB      |IO_L26P_SM6_7        |OUTPUT     |HSTL_III    |7       |
|AH27      |odata_b[56]   |IOB      |IO_L16N_7            |OUTPUT     |HSTL_III    |7       |
|AJ27      |odata_b[57]   |IOB      |IO_L16P_7            |OUTPUT     |HSTL_III    |7       |
|AL25      |odata_b[58]   |IOB      |IO_L25N_CC_SM7_LC_7  |OUTPUT     |HSTL_III    |7       |
|AM25      |odata_b[59]   |IOB      |IO_L32N_SM1_7        |OUTPUT     |HSTL_III    |7       |
|AE34      |odata_b[6]    |IOB      |IO_L5N_11            |OUTPUT     |HSTL_III    |11      |
|AL24      |odata_b[60]   |IOB      |IO_L25P_CC_SM7_LC_7  |OUTPUT     |HSTL_III    |7       |
|AK24      |odata_b[61]   |IOB      |IO_L19P_7            |OUTPUT     |HSTL_III    |7       |
|AG25      |odata_b[62]   |IOB      |IO_L22P_7            |OUTPUT     |HSTL_III    |7       |
|AJ25      |odata_b[63]   |IOB      |IO_L28P_7            |OUTPUT     |HSTL_III    |7       |
|AF34      |odata_b[7]    |IOB      |IO_L14N_11           |OUTPUT     |HSTL_III    |11      |
|AC34      |odata_b[8]    |IOB      |IO_L8N_CC_LC_11      |OUTPUT     |HSTL_III    |11      |
|AD34      |odata_b[9]    |IOB      |IO_L8P_CC_LC_11      |OUTPUT     |HSTL_III    |11      |
|AJ4       |odata_nd_a    |IOB      |IO_L2N_8             |OUTPUT     |HSTL_III    |8       |
|AF24      |odata_nd_b    |IOB      |IO_L21N_7            |OUTPUT     |HSTL_III    |7       |
|AL4       |odata_PPS_a   |IOB      |IO_L1N_8             |OUTPUT     |HSTL_III    |8       |
|AJ24      |odata_PPS_b   |IOB      |IO_L19N_7           |OUTPUT     |HSTL_III    |7       |
|AJ5       |odata_val_a   |IOB      |IO_L6N_8            |OUTPUT     |HSTL_III    |8       |
|AG23      |odata_val_b   |IOB      |IO_L21P_7           |OUTPUT     |HSTL_III    |7       |
|AD21      |otest[0]      |IOB      |IO_L17P_LC_2        |OUTPUT     |LVCMOS25*   |2       |
|AD20      |otest[1]      |IOB      |IO_L17N_LC_2        |OUTPUT     |LVCMOS25*   |2       |
|AD19      |otest[2]      |IOB      |IO_L23P_VRN_LC_2    |OUTPUT     |LVCMOS25*   |2       |
|AE19      |otest[3]      |IOB      |IO_L23N_VRP_LC_2    |OUTPUT     |LVCMOS25*   |2       |
|K8        |res_pll_a     |IOB      |IO_L32P_6           |OUTPUT     |HSTL_I_DCI  |6       |
|K3        |res_pll_b     |IOB      |IO_L25P_CC_LC_10    |OUTPUT     |HSTL_I_DCI  |10      |
|AE4       |res_pll_c     |IOB      |IO_L14P_12          |OUTPUT     |HSTL_I_DCI  |12      |
|AB18      |reset_p       |IOB      |IO_L9N_GC_CC_LC_2   |INPUT      |LVCMOS25*   |2       |
|AP20      |sclk_N        |LOWCAPIOB|IO_L11N_GC_LC_2     |INPUT      |LVDS_25     |2       |
|AN20      |sclk_P        |LOWCAPIOB|IO_L11P_GC_LC_2     |INPUT      |LVDS_25     |2       |
|E18       |spare_in_a    |IOB      |IO_L4P_GC_LC_3      |INPUT      |HSTL_I_DCI  |3       |
|E16       |spare_in_b    |IOB      |IO_L6P_GC_LC_3      |INPUT      |HSTL_I_DCI  |3       |
|G17       |spare_in_c    |IOB      |IO_L8P_GC_LC_3      |INPUT      |HSTL_I_DCI  |3       |
|F26       |spare_out_a   |IOB      |IO_L6N_5            |OUTPUT     |HSTL_III    |5       |
|F25       |spare_out_b   |IOB      |IO_L6P_5            |OUTPUT     |HSTL_III    |5       |
|AF18      |spare_VSI0    |IOB      |IO_L1P_GC_LC_4      |INPUT      |HSTL_III_DCI|4       |
|AE17      |spare_VSI1    |IOB      |IO_L6P_GC_LC_4      |INPUT      |HSTL_III_DCI|4       |
|AM18      |spps_N        |LOWCAPIOB|IO_L15N_GC_LC_2     |INPUT      |LVDS_25     |2       |
|AL18      |spps_P        |LOWCAPIOB|IO_L15P_GC_LC_2     |INPUT      |LVDS_25     |2       |
|AM16      |stick_N       |LOWCAPIOB|IO_L16N_GC_LC_2     |INPUT      |LVDS_25     |2       |
|AM17      |stick_P       |LOWCAPIOB|IO_L16P_GC_LC_2     |INPUT      |LVDS_25     |2       |
+-----------------------------------------------------------------------------------------+
```

Table 8-1 Pinout by Signal Name

8.2 FPGA Pinouts by pin number

Note: UNUSED and NC pins have been removed.

```
Release 10.1.03 - par K.39 (nt)
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Tue Jun 22 22:07:42 2010

INPUT FILE:       input_top_map.ncd
OUTPUT FILE:      input_top_pad.txt
PART TYPE:        xc4vlx40
SPEED GRADE:      -10
PACKAGE:          ff1148

+-----------------------------------------------------------------------------------------+
|Pin       |Signal Name   |Pin Usage|Pin Name            |Direction  |IO Standard |IO Bank|
+-----------------------------------------------------------------------------------------+
|A10       |data_a[7]     |IOB      |IO_L15P_6           |INPUT      |HSTL_I_DCI  |6      |
|A11       |data_a[2]     |IOB      |IO_L3P_6            |INPUT      |HSTL_I_DCI  |6      |
|A12       |              |         |VCCO_6              |           |            |6      |
|A13       |fe_hstl[1]    |IOB      |IO_L17N_6           |OUTPUT     |LVCMOS15    |6      |
|A14       |fe_hstl[6]    |IOB      |IO_L17P_6           |OUTPUT     |LVCMOS15    |6      |
|A19       |              |         |GND                 |           |            |       |
|A2        |              |         |VCCO_6              |           |            |6      |
|A22       |              |         |VCCO_5              |           |            |5      |
|A23       |data_VSI0[5]  |IOB      |IO_L1N_5            |INPUT      |HSTL_III_DCI|5      |
|A24       |data_VSI0[4]  |IOB      |IO_L3P_5            |INPUT      |HSTL_III_DCI|5      |
|A25       |data_VSI0[3]  |IOB      |IO_L3N_5            |INPUT      |HSTL_III_DCI|5      |
|A26       |data_VSI0[2]  |IOB      |IO_L2P_5            |INPUT      |HSTL_III_DCI|5      |
|A27       |              |         |GND                 |           |            |       |
|A28       |data_VSI0[1]  |IOB      |IO_L14P_5           |INPUT      |HSTL_III_DCI|5      |
|A29       |data_VSI0[0]  |IOB      |IO_L14N_5           |INPUT      |HSTL_III_DCI|5      |
|A30       |dpps_VSI0     |IOB      |IO_L18P_5           |INPUT      |HSTL_III_DCI|5      |
|A31       |dtick_VSI0    |IOB      |IO_L24P_CC_LC_5     |INPUT      |HSTL_III_DCI|5      |
|A32       |              |         |VCCO_5              |           |            |5      |
|A33       |              |         |GND                 |           |            |       |
|A4        |fe_hstl[13]   |IOB      |IO_L20P_6           |OUTPUT     |LVCMOS15    |6      |
|A5        |data_a[29]    |IOB      |IO_L22P_6           |INPUT      |HSTL_I_DCI  |6      |
|A6        |data_a[24]    |IOB      |IO_L12P_6           |INPUT      |HSTL_I_DCI  |6      |
|A7        |              |         |GND                 |           |            |       |
|A8        |fom_tick_a    |IOB      |IO_L10P_6           |OUTPUT     |HSTL_I_DCI  |6      |
|A9        |fom_clk_a     |IOB      |IO_L15N_6           |OUTPUT     |HSTL_I_DCI  |6      |
|AA10      |              |         |VCCAUX              |           |            |       |
|AA11      |fe_hstl[36]   |IOB      |IO_L3N_12           |OUTPUT     |LVCMOS15    |12     |
|AA12      |              |         |VCCO_12             |           |            |12     |
|AA13      |fe_hstl[32]   |IOB      |IO_L5N_12           |OUTPUT     |LVCMOS15    |12     |
|AA15      |fe_hstl[37]   |IOB      |IO_L13N_12          |OUTPUT     |LVCMOS15    |12     |
|AA16      |              |         |VCCINT              |           |            |       |
|AA17      |              |         |GND                 |           |            |       |
|AA18      |              |         |VCCINT              |           |            |       |
|AA19      |              |         |GND                 |           |            |       |
|AA20      |              |         |VCCINT              |           |            |       |
|AA22      |              |         |VCCO_11             |           |            |11     |
|AA27      |              |         |GND                 |           |            |       |
|AA7       |              |         |GND                 |           |            |       |
|AA8       |data_c[0]     |IOB      |IO_L8N_CC_LC_12     |INPUT      |HSTL_I_DCI  |12     |
|AA9       |fe_hstl[30]   |IOB      |IO_L8P_CC_LC_12     |OUTPUT     |LVCMOS15    |12     |
|AB10      |data_c[1]     |IOB      |IO_L25N_CC_LC_12    |INPUT      |HSTL_I_DCI  |12     |
|AB11      |              |         |VCCINT              |           |            |       |
|AB12      |DTIME_C       |IOB      |IO_L29N_12          |INPUT      |HSTL_I_DCI  |12     |
|AB13      |fe_hstl[34]   |IOB      |IO_L29P_12          |OUTPUT     |LVCMOS15    |12     |
|AB14      |              |         |GND                 |           |            |       |
|AB15      |mcb_data_p[14]|IOB      |IO_L2N_D12_LC_2     |BIDIR      |LVCMOS25*   |2      |
|AB16      |mcb_data_p[15]|IOB      |IO_L14N_GC_LC_2     |BIDIR      |LVCMOS25*   |2      |
|AB18      |reset_p       |IOB      |IO_L9N_GC_CC_LC_2   |INPUT      |LVCMOS25*   |2      |
|AB19      |              |         |VCCO_2              |           |            |2      |
|AB20      |              |         |GND                 |           |            |       |
|AB21      |              |         |VCCINT              |           |            |       |
|AB24      |              |         |GND                 |           |            |       |
|AB27      |              |         |VCCAUX              |           |            |       |
|AB29      |              |         |VCCO_11             |           |            |11     |
|AB34      |              |         |GND                 |           |            |       |
|AB4       |              |         |GND                 |           |            |       |
|AB5       |data_c[7]     |IOB      |IO_L1N_12           |INPUT      |HSTL_I_DCI  |12     |
|AB6       |data_c[5]     |IOB      |IO_L1P_12           |INPUT      |HSTL_I_DCI  |12     |
|AB7       |              |         |VCCINT              |           |            |       |
|AB9       |              |         |VCCO_12             |           |            |12     |
|AC1       |              |         |GND                 |           |            |       |
|AC10      |data_c[2]     |IOB      |IO_L25P_CC_LC_12    |INPUT      |HSTL_I_DCI  |12     |
|AC11      |              |         |GND                 |           |            |       |
|AC12      |              |         |VCCINT              |           |            |       |
|AC13      |              |         |GND                 |           |            |       |
|AC14      |              |         |VCCINT              |           |            |       |
|AC15      |mcb_data_p[12]|IOB      |IO_L2P_D13_LC_2     |BIDIR      |LVCMOS25*   |2      |
|AC16      |              |         |VCCO_2              |           |            |2      |
|AC17      |mcb_data_p[13]|IOB      |IO_L12N_GC_VREF_LC_2|BIDIR      |LVCMOS25*   |2      |
|AC18      |              |         |VCCINT              |           |            |       |
|AC2       |data_c[27]    |IOB      |IO_L2N_12           |INPUT      |HSTL_I_DCI  |12     |
|AC20      |              |         |VCCINT              |           |            |       |
|AC21      |              |         |GND                 |           |            |       |
|AC22      |              |         |VCCINT              |           |            |       |
|AC23      |              |         |GND                 |           |            |       |
|AC24      |              |         |VCCAUX              |           |            |       |
|AC26      |              |         |VCCO_11             |           |            |11     |
|AC3       |data_c[19]    |IOB      |IO_L2P_12           |INPUT      |HSTL_I_DCI  |12     |
|AC31      |              |         |GND                 |           |            |       |
|AC32      |odata_b[24]   |IOB      |IO_L6P_11           |OUTPUT     |HSTL_III    |11     |
|AC33      |odata_b[16]   |IOB      |IO_L6N_11           |OUTPUT     |HSTL_III    |11     |
|AC34      |odata_b[8]    |IOB      |IO_L8N_CC_LC_11     |OUTPUT     |HSTL_III    |11     |
|AC4       |fom_clk_c     |IOB      |IO_L6N_12           |OUTPUT     |HSTL_I_DCI  |12     |
|AC5       |data_c[8]     |IOB      |IO_L6P_12           |INPUT      |HSTL_I_DCI  |12     |
|AC6       |              |         |VCCO_12             |           |            |12     |
|AC7       |data_c[6]     |IOB      |IO_L12P_12          |INPUT      |HSTL_I_DCI  |12     |
|AC8       |data_c[4]     |IOB      |IO_L17N_12          |INPUT      |HSTL_I_DCI  |12     |
|AC9       |data_c[3]     |IOB      |IO_L17P_12          |INPUT      |HSTL_I_DCI  |12     |
|AD11      |              |         |VCCAUX              |           |            |       |
|AD12      |              |         |GND                 |           |            |       |
|AD13      |              |         |VCCINT              |           |            |       |
|AD14      |              |         |GND                 |           |            |       |
|AD15      |              |         |VCCINT              |           |            |       |
|AD16      |mcb_data_p[10]|IOB      |IO_L10P_GC_LC_2     |BIDIR      |LVCMOS25*   |2      |
|AD17      |mcb_data_p[11]|IOB      |IO_L12P_GC_LC_2     |BIDIR      |LVCMOS25*   |2      |
|AD18      |              |         |GND                 |           |            |       |
|AD19      |otest[2]      |IOB      |IO_L23P_VRN_LC_2    |OUTPUT     |LVCMOS25*   |2      |
|AD2       |data_c[28]    |IOB      |IO_L4P_12           |INPUT      |HSTL_I_DCI  |12     |
|AD20      |otest[1]      |IOB      |IO_L17N_LC_2        |OUTPUT     |LVCMOS25*   |2      |
|AD21      |otest[0]      |IOB      |IO_L17P_LC_2        |OUTPUT     |LVCMOS25*   |2      |
|AD22      |              |         |GND                 |           |            |       |
|AD23      |              |         |VCCINT              |           |            |       |
|AD24      |              |         |GND                 |           |            |       |
|AD25      |              |         |VCCINT              |           |            |       |
|AD28      |              |         |GND                 |           |            |       |
|AD3       |              |         |VCCO_12             |           |            |12     |
|AD32      |odata_b[25]   |IOB      |IO_L10N_11          |OUTPUT     |HSTL_III    |11     |
|AD33      |              |         |VCCO_11             |           |            |11     |
|AD34      |odata_b[9]    |IOB      |IO_L8P_CC_LC_11     |OUTPUT     |HSTL_III    |11     |
|AD4       |data_c[18]    |IOB      |IO_L14N_12          |INPUT      |HSTL_I_DCI  |12     |
|AD5       |data_c[16]    |IOB      |IO_L11N_12          |INPUT      |HSTL_I_DCI  |12     |
|AD6       |data_c[14]    |IOB      |IO_L11P_12          |INPUT      |HSTL_I_DCI  |12     |
|AD7       |data_c[12]    |IOB      |IO_L24N_CC_LC_12    |INPUT      |HSTL_I_DCI  |12     |
|AD8       |              |         |GND                 |           |            |       |
|AE1       |fe_hstl[42]   |IOB      |IO_L7N_12           |OUTPUT     |LVCMOS15    |12     |
|AE10      |              |         |VCCO_8              |           |            |8      |
|AE12      |              |         |VCCINT              |           |            |       |
|AE13      |              |         |GND                 |           |            |       |
|AE14      |              |         |VCCINT              |           |            |       |
|AE15      |              |         |GND                 |           |            |       |
|AE17      |spare_VSI1    |IOB      |IO_L6P_GC_LC_4      |INPUT      |HSTL_III_DCI|4      |
|AE19      |otest[3]      |IOB      |IO_L23N_VRP_LC_2    |OUTPUT     |LVCMOS25*   |2      |
|AE2       |data_c[29]    |IOB      |IO_L10N_12          |INPUT      |HSTL_I_DCI  |12     |
|AE20      |              |         |VCCO_2              |           |            |2      |
|AE22      |              |         |VCCINT              |           |            |       |
|AE23      |              |         |GND                 |           |            |       |
|AE24      |              |         |VCCINT              |           |            |       |
|AE25      |              |         |GND                 |           |            |       |
|AE28      |              |         |VCCINT              |           |            |       |
|AE3       |data_c[20]    |IOB      |IO_L10P_12          |INPUT      |HSTL_I_DCI  |12     |
|AE30      |              |         |VCCO_11             |           |            |11     |
|AE31      |odata_b[27]   |IOB      |IO_L16N_11          |OUTPUT     |HSTL_III    |11     |
|AE32      |odata_b[22]   |IOB      |IO_L10P_11          |OUTPUT     |HSTL_III    |11     |
|AE33      |odata_b[17]   |IOB      |IO_L5P_11           |OUTPUT     |HSTL_III    |11     |
|AE34      |odata_b[6]    |IOB      |IO_L5N_11           |OUTPUT     |HSTL_III    |11     |
|AE4       |res_pll_c     |IOB      |IO_L14P_12          |OUTPUT     |HSTL_I_DCI  |12     |
|AE5       |              |         |GND                 |           |            |       |
|AE6       |data_c[15]    |IOB      |IO_L19N_12          |INPUT      |HSTL_I_DCI  |12     |
|AE7       |data_c[13]    |IOB      |IO_L24P_CC_LC_12    |INPUT      |HSTL_I_DCI  |12     |
|AE8       |data_c[9]     |IOB      |IO_L27N_12          |INPUT      |HSTL_I_DCI  |12     |
|AF1       |fe_hstl[39]   |IOB      |IO_L7P_12           |OUTPUT     |LVCMOS15    |12     |
|AF12      |              |         |GND                 |           |            |       |
|AF13      |              |         |VCCINT              |           |            |       |
|AF15      |mcb_data_p[9] |IOB      |IO_L10N_GC_LC_2     |BIDIR      |LVCMOS25*   |2      |
|AF17      |              |         |VCCO_4              |           |            |4      |
|AF18      |spare_VSI0    |IOB      |IO_L1P_GC_LC_4      |INPUT      |HSTL_III_DCI|4      |
|AF19      |              |         |VCCINT              |           |            |       |
|AF2       |              |         |GND                 |           |            |       |
|AF22      |              |         |GND                 |           |            |       |
|AF23      |              |         |VCCINT              |           |            |       |
|AF24      |odata_nd_b    |IOB      |IO_L21N_7           |OUTPUT     |HSTL_III    |7      |
|AF25      |              |         |VCCAUX              |           |            |       |
|AF27      |              |         |VCCO_7              |           |            |7      |
|AF3       |data_c[21]    |IOB      |IO_L18N_12          |INPUT      |HSTL_I_DCI  |12     |
|AF31      |odata_b[23]   |IOB      |IO_L16P_11          |OUTPUT     |HSTL_III    |11     |
|AF32      |              |         |GND                 |           |            |       |
|AF33      |odata_b[14]   |IOB      |IO_L14P_11          |OUTPUT     |HSTL_III    |11     |
|AF34      |odata_b[7]    |IOB      |IO_L14N_11          |OUTPUT     |HSTL_III    |11     |
|AF6       |fom_tick_c    |IOB      |IO_L19P_12          |OUTPUT     |HSTL_I_DCI  |12     |
|AF7       |              |         |VCCO_12             |           |            |12     |
|AF8       |data_c[10]    |IOB      |IO_L27P_12          |INPUT      |HSTL_I_DCI  |12     |
|AF9       |              |         |VCCINT              |           |            |       |
|AG1       |fe_hstl[41]   |IOB      |IO_L16N_12          |OUTPUT     |LVCMOS15    |12     |
|AG10      |odata_a[40]   |IOB      |IO_L30N_8           |OUTPUT     |HSTL_III    |8      |
|AG11      |odata_a[31]   |IOB      |IO_L17N_8           |OUTPUT     |HSTL_III    |8      |
|AG12      |              |         |VCCAUX              |           |            |       |
|AG14      |              |         |VCCO_2              |           |            |2      |
|AG15      |mcb_data_p[8] |IOB      |IO_L22P_LC_2        |BIDIR      |LVCMOS25*   |2      |
|AG19      |              |         |GND                 |           |            |       |
|AG2       |data_c[30]    |IOB      |IO_L16P_12          |INPUT      |HSTL_I_DCI  |12     |
|AG20      |mcb_addr_p[6] |IOB      |IO_L21P_LC_2        |INPUT      |LVCMOS25*   |2      |
|AG22      |mcb_addr_p[7] |IOB      |IO_L3P_D11_LC_2     |INPUT      |LVCMOS25*   |2      |
|AG23      |odata_val_b   |IOB      |IO_L21P_7           |OUTPUT     |HSTL_III    |7      |
|AG24      |              |         |VCCO_7              |           |            |7      |
|AG25      |odata_b[62]   |IOB      |IO_L22P_7           |OUTPUT     |HSTL_III    |7      |
|AG29      |              |         |GND                 |           |            |       |
|AG3       |data_c[22]    |IOB      |IO_L18P_12          |INPUT      |HSTL_I_DCI  |12     |
|AG30      |odata_b[33]   |IOB      |IO_L21P_11          |OUTPUT     |HSTL_III    |11     |
|AG31      |odata_b[15]   |IOB      |IO_L21N_11          |OUTPUT     |HSTL_III    |11     |
|AG32      |odata_b[12]   |IOB      |IO_L13P_11          |OUTPUT     |HSTL_III    |11     |
|AG33      |odata_b[4]    |IOB      |IO_L13N_11          |OUTPUT     |HSTL_III    |11     |
|AG34      |              |         |VCCO_11             |           |            |11     |
|AG4       |              |         |VCCO_12             |           |            |12     |
|AG7       |ATIME_C       |IOB      |IO_L31N_12          |INPUT      |HSTL_I_DCI  |12     |
|AG8       |data_c[11]    |IOB      |IO_L31P_12          |INPUT      |HSTL_I_DCI  |12     |
|AG9       |              |         |GND                 |           |            |       |
|AH1       |              |         |VCCO_12             |           |            |12     |
|AH10      |odata_a[41]   |IOB      |IO_L30P_8           |OUTPUT     |HSTL_III    |8      |
|AH11      |              |         |VCCO_8              |           |            |8      |
|AH12      |odata_a[28]   |IOB      |IO_L17P_8           |OUTPUT     |HSTL_III    |8      |
|AH13      |              |         |VCCINT              |           |            |       |
|AH14      |mcb_data_p[7] |IOB      |IO_L22N_LC_2        |BIDIR      |LVCMOS25*   |2      |
|AH15      |              |         |VCCINT              |           |            |       |
|AH16      |              |         |GND                 |           |            |       |
|AH2       |fe_hstl[38]   |IOB      |IO_L15N_12          |OUTPUT     |LVCMOS15    |12     |
|AH20      |mcb_addr_p[4] |IOB      |IO_L21N_LC_2        |INPUT      |LVCMOS25*   |2      |
|AH21      |              |         |VCCO_2              |           |            |2      |
|AH22      |mcb_addr_p[5] |IOB      |IO_L3N_D10_LC_2     |INPUT      |LVCMOS25*   |2      |
|AH26      |              |         |GND                 |           |            |       |
|AH27      |odata_b[56]   |IOB      |IO_L16N_7           |OUTPUT     |HSTL_III    |7      |
|AH28      |odata_b[46]   |IOB      |IO_L6P_7            |OUTPUT     |HSTL_III    |7      |
|AH29      |odata_b[38]   |IOB      |IO_L6N_7            |OUTPUT     |HSTL_III    |7      |
|AH3       |data_c[23]    |IOB      |IO_L15P_12          |INPUT      |HSTL_I_DCI  |12     |
|AH30      |odata_b[39]   |IOB      |IO_L32N_11          |OUTPUT     |HSTL_III    |11     |
|AH31      |              |         |VCCO_11             |           |            |11     |
|AH32      |odata_b[20]   |IOB      |IO_L22P_11          |OUTPUT     |HSTL_III    |11     |
|AH33      |odata_b[5]    |IOB      |IO_L22N_11          |OUTPUT     |HSTL_III    |11     |
|AH34      |odata_b[2]    |IOB      |IO_L18N_11          |OUTPUT     |HSTL_III    |11     |
|AH5       |data_c[17]    |IOB      |IO_L28P_12          |INPUT      |HSTL_I_DCI  |12     |
|AH6       |              |         |GND                 |           |            |       |
|AH8       |odata_a[48]   |IOB      |IO_L12P_8           |OUTPUT     |HSTL_III    |8      |
|AH9       |              |         |VCCAUX              |           |            |       |
|AJ1       |fe_hstl[43]   |IOB      |IO_L22N_12          |OUTPUT     |LVCMOS15    |12     |
|AJ10      |odata_a[39]   |IOB      |IO_L15P_8           |OUTPUT     |HSTL_III    |8      |
|AJ12      |odata_a[29]   |IOB      |IO_L21P_8           |OUTPUT     |HSTL_III    |8      |
|AJ13      |              |         |GND                 |           |            |       |
|AJ14      |mcb_data_p[5] |IOB      |IO_L20N_VREF_LC_2   |BIDIR      |LVCMOS25*   |2      |
|AJ15      |mcb_data_p[6] |IOB      |IO_L20P_LC_2        |BIDIR      |LVCMOS25*   |2      |
|AJ16      |              |         |VCCAUX              |           |            |       |
|AJ18      |              |         |VCCO_4              |           |            |4      |
|AJ2       |dval_c        |IOB      |IO_L22P_12          |INPUT      |HSTL_I_DCI  |12     |
|AJ20      |mcb_addr_p[1] |IOB      |IO_L19P_LC_2        |INPUT      |LVCMOS25*   |2      |
|AJ21      |mcb_addr_p[2] |IOB      |IO_L1N_D14_CC_LC_2  |INPUT      |LVCMOS25*   |2      |
|AJ22      |mcb_addr_p[3] |IOB      |IO_L1P_D15_CC_LC_2  |INPUT      |LVCMOS25*   |2      |
|AJ23      |              |         |GND                 |           |            |       |
|AJ24      |odata_PPS_b   |IOB      |IO_L19N_7           |OUTPUT     |HSTL_III    |7      |
|AJ25      |odata_b[63]   |IOB      |IO_L28P_7           |OUTPUT     |HSTL_III    |7      |
|AJ26      |              |         |VCCAUX              |           |            |       |
|AJ27      |odata_b[57]   |IOB      |IO_L16P_7           |OUTPUT     |HSTL_III    |7      |
|AJ28      |              |         |VCCO_7              |           |            |7      |
|AJ29      |odata_b[47]   |IOB      |IO_L1N_7            |OUTPUT     |HSTL_III    |7      |
|AJ3       |              |         |GND                 |           |            |       |
|AJ30      |odata_b[36]   |IOB      |IO_L32P_11          |OUTPUT     |HSTL_III    |11     |
|AJ31      |odata_b[30]   |IOB      |IO_L28P_11          |OUTPUT     |HSTL_III    |11     |
|AJ33      |              |         |GND                 |           |            |       |
|AJ34      |odata_b[3]    |IOB      |IO_L18P_11          |OUTPUT     |HSTL_III    |11     |
|AJ4       |odata_nd_a    |IOB      |IO_L2N_8            |OUTPUT     |HSTL_III    |8      |
|AJ5       |odata_val_a   |IOB      |IO_L6N_8            |OUTPUT     |HSTL_III    |8      |
|AJ6       |odata_a[58]   |IOB      |IO_L6P_8            |OUTPUT     |HSTL_III    |8      |
|AJ7       |odata_a[50]   |IOB      |IO_L7N_8            |OUTPUT     |HSTL_III    |8      |
|AJ8       |              |         |VCCO_8              |           |            |8      |
|AJ9       |odata_a[38]   |IOB      |IO_L15N_8           |OUTPUT     |HSTL_III    |8      |
|AK1       |data_c[31]    |IOB      |IO_L21N_12          |INPUT      |HSTL_I_DCI  |12     |
|AK10      |              |         |GND                 |           |            |       |
|AK12      |odata_a[24]   |IOB      |IO_L21N_8           |OUTPUT     |HSTL_III    |8      |
|AK13      |odata_a[21]   |IOB      |IO_L9P_CC_LC_8      |OUTPUT     |HSTL_III    |8      |
|AK14      |mcb_data_p[3] |IOB      |IO_L4N_D8_VREF_LC_2 |BIDIR      |LVCMOS25*   |2      |
|AK15      |              |         |VCCO_2              |           |            |2      |
|AK16      |mcb_data_p[4] |IOB      |IO_L24N_CC_LC_2     |BIDIR      |LVCMOS25*   |2      |
|AK20      |              |         |GND                 |           |            |       |
|AK21      |odata_a[15]   |IOB      |IO_L5P_7            |OUTPUT     |HSTL_III    |7      |
|AK22      |odata_a[11]   |IOB      |IO_L13P_7           |OUTPUT     |HSTL_III    |7      |
|AK23      |odata_a[7]    |IOB      |IO_L13N_7           |OUTPUT     |HSTL_III    |7       |
|AK24      |odata_b[61]   |IOB      |IO_L19P_7           |OUTPUT     |HSTL_III    |7       |
|AK25      |              |         |VCCO_7              |           |            |7       |
|AK26      |odata_b[54]   |IOB      |IO_L26N_SM6_7       |OUTPUT     |HSTL_III    |7       |
|AK27      |odata_b[50]   |IOB      |IO_L20P_7           |OUTPUT     |HSTL_III    |7       |
|AK29      |odata_b[44]   |IOB      |IO_L1P_7            |OUTPUT     |HSTL_III    |7       |
|AK3       |data_c[24]    |IOB      |IO_L26P_12          |INPUT      |HSTL_I_DCI  |12      |
|AK30      |              |         |GND                 |           |            |        |
|AK31      |odata_b[31]   |IOB      |IO_L25P_CC_LC_11    |OUTPUT     |HSTL_III    |11      |
|AK32      |odata_b[21]   |IOB      |IO_L25N_CC_LC_11    |OUTPUT     |HSTL_III    |11      |
|AK33      |odata_b[13]   |IOB      |IO_L26P_11          |OUTPUT     |HSTL_III    |11      |
|AK34      |odata_b[0]    |IOB      |IO_L26N_11          |OUTPUT     |HSTL_III    |11      |
|AK4       |odata_100PPS_a|IOB      |IO_L2P_8            |OUTPUT     |HSTL_III    |8       |
|AK5       |              |         |VCCO_8              |           |            |8       |
|AK6       |odata_a[59]   |IOB      |IO_L10N_8           |OUTPUT     |HSTL_III    |8       |
|AK7       |odata_a[51]   |IOB      |IO_L7P_8            |OUTPUT     |HSTL_III    |8       |
|AK8       |odata_a[49]   |IOB      |IO_L11N_8           |OUTPUT     |HSTL_III    |8       |
|AL1       |data_c[25]    |IOB      |IO_L21P_12          |INPUT      |HSTL_I_DCI  |12      |
|AL10      |odata_a[35]   |IOB      |IO_L25N_CC_LC_8     |OUTPUT     |HSTL_III    |8       |
|AL11      |odata_a[26]   |IOB      |IO_L25P_CC_LC_8     |OUTPUT     |HSTL_III    |8       |
|AL12      |              |         |VCCO_8              |           |            |8       |
|AL13      |odata_a[18]   |IOB      |IO_L9N_CC_LC_8      |OUTPUT     |HSTL_III    |8       |
|AL14      |mcb_data_p[0] |IOB      |IO_L4P_D9_LC_2      |BIDIR      |LVCMOS25*   |2       |
|AL15      |mcb_data_p[1] |IOB      |IO_L18N_LC_2        |BIDIR      |LVCMOS25*   |2       |
|AL16      |mcb_data_p[2] |IOB      |IO_L24P_CC_LC_2     |BIDIR      |LVCMOS25*   |2       |
|AL17      |              |         |GND                 |           |            |        |
|AL18      |spps_P        |LOWCAPIOB|IO_L15P_GC_LC_2     |INPUT      |LVDS_25     |2       |
|AL19      |mcb_rw_p      |IOB      |IO_L13N_GC_LC_2     |INPUT      |LVCMOS25*   |2       |
|AL2       |              |         |VCCO_12             |           |            |12      |
|AL20      |mcb_addr_p[0] |IOB      |IO_L19N_LC_2        |INPUT      |LVCMOS25*   |2       |
|AL21      |odata_a[12]   |IOB      |IO_L5N_7            |OUTPUT     |HSTL_III    |7       |
|AL22      |              |         |VCCO_7              |           |            |7       |
|AL23      |odata_a[4]    |IOB      |IO_L31P_SM2_7       |OUTPUT     |HSTL_III    |7       |
|AL24      |odata_b[60]   |IOB      |IO_L25P_CC_SM7_LC_7 |OUTPUT     |HSTL_III    |7       |
|AL25      |odata_b[58]   |IOB      |IO_L25N_CC_SM7_LC_7 |OUTPUT     |HSTL_III    |7      |
|AL26      |odata_b[55]   |IOB      |IO_L26P_SM6_7       |OUTPUT     |HSTL_III    |7      |
|AL27      |              |         |GND                 |           |            |       |
|AL28      |odata_b[51]   |IOB      |IO_L14P_7           |OUTPUT     |HSTL_III    |7      |
|AL29      |odata_b[45]   |IOB      |IO_L14N_7           |OUTPUT     |HSTL_III    |7      |
|AL30      |odata_b[37]   |IOB      |IO_L10N_7           |OUTPUT     |HSTL_III    |7      |
|AL31      |odata_b[28]   |IOB      |IO_L31N_11          |OUTPUT     |HSTL_III    |11     |
|AL32      |              |         |VCCO_11             |           |            |11     |
|AL33      |odata_b[10]   |IOB      |IO_L30P_11          |OUTPUT     |HSTL_III    |11     |
|AL34      |odata_b[1]    |IOB      |IO_L30N_11          |OUTPUT     |HSTL_III    |11     |
|AL4       |odata_PPS_a   |IOB      |IO_L1N_8            |OUTPUT     |HSTL_III    |8      |
|AL5       |odata_a[62]   |IOB      |IO_L1P_8            |OUTPUT     |HSTL_III    |8      |
|AL6       |odata_a[56]   |IOB      |IO_L10P_8           |OUTPUT     |HSTL_III    |8      |
|AL7       |              |         |GND                 |           |            |       |
|AL8       |odata_a[46]   |IOB      |IO_L11P_8           |OUTPUT     |HSTL_III    |8      |
|AL9       |odata_a[36]   |IOB      |IO_L28P_8           |OUTPUT     |HSTL_III    |8      |
|AM1       |fe_hstl[40]   |IOB      |IO_L30N_12          |OUTPUT     |LVCMOS15    |12     |
|AM10      |odata_a[32]   |IOB      |IO_L19N_8           |OUTPUT     |HSTL_III    |8      |
|AM11      |odata_a[27]   |IOB      |IO_L27N_8           |OUTPUT     |HSTL_III    |8      |
|AM12      |odata_a[25]   |IOB      |IO_L27P_8           |OUTPUT     |HSTL_III    |8      |
|AM13      |odata_a[19]   |IOB      |IO_L13P_8           |OUTPUT     |HSTL_III    |8      |
|AM14      |              |         |GND                 |           |            |       |
|AM15      |mcb_cs_p      |IOB      |IO_L18P_LC_2        |INPUT      |LVCMOS25*   |2      |
|AM16      |stick_N       |LOWCAPIOB|IO_L16N_GC_LC_2     |INPUT      |LVDS_25     |2      |
|AM17      |stick_P       |LOWCAPIOB|IO_L16P_GC_LC_2     |INPUT      |LVDS_25     |2      |
|AM18      |spps_N        |LOWCAPIOB|IO_L15N_GC_LC_2     |INPUT      |LVDS_25     |2      |
|AM19      |              |         |VCCO_2              |           |            |2      |
|AM20      |mcb_clk_p     |IOB      |IO_L13P_GC_LC_2     |INPUT      |LVCMOS25*   |2      |
|AM21      |odata_a[13]   |IOB      |IO_L9P_CC_LC_7      |OUTPUT     |HSTL_III    |7      |
|AM22      |odata_a[8]    |IOB      |IO_L9N_CC_LC_7      |OUTPUT     |HSTL_III    |7      |
|AM23      |odata_a[5]    |IOB      |IO_L31N_SM2_7       |OUTPUT     |HSTL_III    |7      |
|AM24      |              |         |GND                 |           |            |       |
|AM25      |odata_b[59]   |IOB      |IO_L32N_SM1_7       |OUTPUT     |HSTL_III    |7      |
|AM26      |odata_b[52]   |IOB      |IO_L30P_SM3_7       |OUTPUT     |HSTL_III    |7      |
|AM27      |odata_b[48]   |IOB      |IO_L30N_SM3_7       |OUTPUT     |HSTL_III    |7      |
|AM28      |odata_b[42]   |IOB      |IO_L24N_CC_LC_7     |OUTPUT     |HSTL_III    |7      |
|AM29      |              |         |VCCO_7              |           |            |7      |
|AM3       |data_c[26]    |IOB      |IO_L32P_12          |INPUT      |HSTL_I_DCI  |12     |
|AM30      |odata_b[34]   |IOB      |IO_L10P_7           |OUTPUT     |HSTL_III    |7      |
|AM31      |odata_b[29]   |IOB      |IO_L31P_11          |OUTPUT     |HSTL_III    |11     |
|AM32      |odata_b[18]   |IOB      |IO_L27P_11          |OUTPUT     |HSTL_III    |11     |
|AM33      |odata_b[11]   |IOB      |IO_L27N_11          |OUTPUT     |HSTL_III    |11     |
|AM34      |              |         |GND                 |           |            |       |
|AM4       |              |         |GND                 |           |            |       |
|AM5       |odata_a[63]   |IOB      |IO_L14N_8           |OUTPUT     |HSTL_III    |8      |
|AM6       |odata_a[57]   |IOB      |IO_L14P_8           |OUTPUT     |HSTL_III    |8      |
|AM7       |odata_a[47]   |IOB      |IO_L18N_8           |OUTPUT     |HSTL_III    |8      |
|AM8       |odata_a[44]   |IOB      |IO_L22N_8           |OUTPUT     |HSTL_III    |8      |
|AM9       |              |         |VCCO_8              |           |            |8      |
|AN1       |              |         |GND                 |           |            |       |
|AN10      |odata_a[33]   |IOB      |IO_L19P_8           |OUTPUT     |HSTL_III    |8      |
|AN11      |              |         |GND                 |           |            |       |
|AN12      |odata_a[22]   |IOB      |IO_L31P_8           |OUTPUT     |HSTL_III    |8      |
|AN13      |odata_a[16]   |IOB      |IO_L13N_8           |OUTPUT     |HSTL_III    |8      |
|AN14      |odata_a[17]   |IOB      |IO_L5P_8            |OUTPUT     |HSTL_III    |8      |
|AN16      |              |         |VCCO_2              |           |            |2      |
|AN17      |              |         |VREFN_SM            |           |            |       |
|AN18      |              |         |VREFP_SM            |           |            |       |
|AN19      |              |         |AVSS_SM             |           |            |       |
|AN20      |sclk_P        |LOWCAPIOB|IO_L11P_GC_LC_2     |INPUT      |LVDS_25     |2      |
|AN21      |              |         |GND                 |           |            |       |
|AN22      |odata_a[9]    |IOB      |IO_L27P_SM5_7       |OUTPUT     |HSTL_III    |7      |
|AN23      |odata_a[2]    |IOB      |IO_L27N_SM5_7       |OUTPUT     |HSTL_III    |7      |
|AN24      |odata_a[3]    |IOB      |IO_L29N_SM4_7       |OUTPUT     |HSTL_III    |7      |
|AN26      |              |         |VCCO_7              |           |            |7      |
|AN27      |odata_b[49]   |IOB      |IO_L11N_7           |OUTPUT     |HSTL_III    |7      |
|AN28      |odata_b[43]   |IOB      |IO_L24P_CC_LC_7     |OUTPUT     |HSTL_III    |7      |
|AN29      |odata_b[40]   |IOB      |IO_L18N_7           |OUTPUT     |HSTL_III    |7      |
|AN3       |odata_a[61]   |IOB      |IO_L8P_CC_LC_8      |OUTPUT     |HSTL_III    |8      |
|AN30      |odata_b[35]   |IOB      |IO_L7N_7            |OUTPUT     |HSTL_III    |7      |
|AN31      |              |         |GND                 |           |            |       |
|AN32      |odata_b[19]   |IOB      |IO_L4P_7            |OUTPUT     |HSTL_III    |7      |
|AN34      |              |         |GND                 |           |            |       |
|AN4       |odata_a[60]   |IOB      |IO_L3N_8            |OUTPUT     |HSTL_III    |8      |
|AN5       |odata_a[54]   |IOB      |IO_L16N_8           |OUTPUT     |HSTL_III    |8      |
|AN6       |              |         |VCCO_8              |           |            |8      |
|AN7       |odata_a[45]   |IOB      |IO_L18P_8           |OUTPUT     |HSTL_III    |8      |
|AN8       |odata_a[43]   |IOB      |IO_L22P_8           |OUTPUT     |HSTL_III    |8      |
|AN9       |odata_a[37]   |IOB      |IO_L32N_8           |OUTPUT     |HSTL_III    |8      |
|AP10      |odata_a[30]   |IOB      |IO_L29N_8           |OUTPUT     |HSTL_III    |8      |
|AP11      |odata_a[23]   |IOB      |IO_L29P_8           |OUTPUT     |HSTL_III    |8      |
|AP12      |odata_a[20]   |IOB      |IO_L31N_8           |OUTPUT     |HSTL_III    |8      |
|AP13      |              |         |VCCO_8              |           |            |8      |
|AP14      |odata_a[14]   |IOB      |IO_L5N_8            |OUTPUT     |HSTL_III    |8      |
|AP16      |              |         |GND                 |           |            |       |
|AP19      |              |         |AVDD_SM             |           |            |       |
|AP2       |              |         |GND                 |           |            |       |
|AP20      |sclk_N        |LOWCAPIOB|IO_L11N_GC_LC_2     |INPUT      |LVDS_25     |2      |
|AP21      |odata_a[10]   |IOB      |IO_L17P_7           |OUTPUT     |HSTL_III    |7      |
|AP22      |odata_a[6]    |IOB      |IO_L17N_7           |OUTPUT     |HSTL_III    |7      |
|AP23      |              |         |VCCO_7              |           |            |7      |
|AP24      |odata_a[0]    |IOB      |IO_L29P_SM4_7       |OUTPUT     |HSTL_III    |7      |
|AP25      |odata_a[1]    |IOB      |IO_L15P_7           |OUTPUT     |HSTL_III    |7      |
|AP26      |odata_100PPS_b|IOB      |IO_L15N_7           |OUTPUT     |HSTL_III    |7      |
|AP27      |odata_b[53]   |IOB      |IO_L11P_7           |OUTPUT     |HSTL_III    |7      |
|AP28      |              |         |GND                 |           |            |       |
|AP29      |odata_b[41]   |IOB      |IO_L18P_7           |OUTPUT     |HSTL_III    |7      |
|AP3       |              |         |VCCO_8              |           |            |8      |
|AP30      |odata_b[32]   |IOB      |IO_L7P_7            |OUTPUT     |HSTL_III    |7      |
|AP31      |odata_b[26]   |IOB      |IO_L12P_7           |OUTPUT     |HSTL_III    |7      |
|AP33      |              |         |VCCO_7              |           |            |7      |
|AP4       |odata_a[55]   |IOB      |IO_L3P_8            |OUTPUT     |HSTL_III    |8      |
|AP5       |odata_a[52]   |IOB      |IO_L16P_8           |OUTPUT     |HSTL_III    |8      |
|AP6       |odata_a[53]   |IOB      |IO_L24N_CC_LC_8     |OUTPUT     |HSTL_III    |8      |
|AP7       |odata_a[42]   |IOB      |IO_L24P_CC_LC_8     |OUTPUT     |HSTL_III    |8      |
|AP8       |              |         |GND                 |           |            |       |
|AP9       |odata_a[34]   |IOB      |IO_L32P_8           |OUTPUT     |HSTL_III    |8      |
|B1        |              |         |GND                 |           |            |       |
|B10       |data_a[8]     |IOB      |IO_L2P_6            |INPUT      |HSTL_I_DCI  |6      |
|B11       |data_a[3]     |IOB      |IO_L3N_6            |INPUT      |HSTL_I_DCI  |6      |
|B12       |DTIME_A       |IOB      |IO_L9N_CC_LC_6      |INPUT      |HSTL_I_DCI  |6      |
|B13       |fe_hstl[7]    |IOB      |IO_L9P_CC_LC_6      |OUTPUT     |LVCMOS15    |6      |
|B14       |              |         |GND                 |           |            |       |
|B19       |              |         |VCCO_1              |           |            |1      |
|B2        |DTIME_B       |IOB      |IO_L30N_6           |INPUT      |HSTL_I_DCI  |6      |
|B24       |              |         |GND                 |           |            |       |
|B25       |data_VSI0[13] |IOB      |IO_L15P_5           |INPUT      |HSTL_III_DCI|5      |
|B26       |data_VSI0[12] |IOB      |IO_L2N_5            |INPUT      |HSTL_III_DCI|5      |
|B27       |data_VSI0[11] |IOB      |IO_L8P_CC_LC_5      |INPUT      |HSTL_III_DCI|5      |
|B28       |data_VSI0[10] |IOB      |IO_L25P_CC_LC_5     |INPUT      |HSTL_III_DCI|5      |
|B29       |              |         |VCCO_5              |           |            |5      |
|B3        |fe_hstl[17]   |IOB      |IO_L30P_6           |OUTPUT     |LVCMOS15    |6      |
|B30       |data_VSI0[9]  |IOB      |IO_L18N_5           |INPUT      |HSTL_III_DCI|5      |
|B31       |data_VSI0[8]  |IOB      |IO_L24N_CC_LC_5     |INPUT      |HSTL_III_DCI|5      |
|B32       |data_VSI0[7]  |IOB      |IO_L31P_5           |INPUT      |HSTL_III_DCI|5      |
|B33       |data_VSI0[6]  |IOB      |IO_L31N_5           |INPUT      |HSTL_III_DCI|5      |
|B34       |              |         |GND                 |           |            |       |
|B4        |              |         |GND                 |           |            |       |
|B5        |data_a[30]    |IOB      |IO_L22N_6           |INPUT      |HSTL_I_DCI  |6      |
|B7        |data_a[19]    |IOB      |IO_L14P_6           |INPUT      |HSTL_I_DCI  |6      |
|B8        |data_a[16]    |IOB      |IO_L10N_6           |INPUT      |HSTL_I_DCI  |6      |
|B9        |              |         |VCCO_6              |           |            |6      |
|C1        |              |         |GND                 |           |            |       |
|C10       |data_a[9]     |IOB      |IO_L2N_6            |INPUT      |HSTL_I_DCI  |6      |
|C11       |              |         |GND                 |           |            |       |
|C12       |data_a[0]     |IOB      |IO_L1N_6            |INPUT      |HSTL_I_DCI  |6      |
|C13       |fe_hstl[3]    |IOB      |IO_L25N_CC_LC_6     |OUTPUT     |LVCMOS15    |6      |
|C14       |fe_hstl[4]    |IOB      |IO_L25P_CC_LC_6     |OUTPUT     |LVCMOS15    |6      |
|C16       |              |         |VCCO_1              |           |            |1      |
|C2        |data_b[0]     |IOB      |IO_L7P_10           |INPUT      |HSTL_I_DCI  |10     |
|C21       |              |         |GND                 |           |            |       |
|C24       |dval_VSI0     |IOB      |IO_L5N_5            |INPUT      |HSTL_III_DCI|5      |
|C25       |data_VSI0[20] |IOB      |IO_L15N_5           |INPUT      |HSTL_III_DCI|5      |
|C26       |              |         |VCCO_5              |           |            |5      |
|C27       |data_VSI0[19] |IOB      |IO_L8N_CC_LC_5      |INPUT      |HSTL_III_DCI|5      |
|C28       |data_VSI0[18] |IOB      |IO_L25N_CC_LC_5     |INPUT      |HSTL_III_DCI|5      |
|C29       |data_VSI0[17] |IOB      |IO_L20P_5           |INPUT      |HSTL_III_DCI|5      |
|C3        |fe_hstl[21]   |IOB      |IO_L1N_10           |OUTPUT     |LVCMOS15    |10     |
|C31       |              |         |GND                 |           |            |       |
|C32       |data_VSI0[16] |IOB      |IO_L2P_9            |INPUT      |HSTL_III_DCI|9      |
|C33       |data_VSI0[15] |IOB      |IO_L7P_9            |INPUT      |HSTL_III_DCI|9      |
|C34       |data_VSI0[14] |IOB      |IO_L7N_9            |INPUT      |HSTL_III_DCI|9      |
|C4        |fe_hstl[16]   |IOB      |IO_L1P_10           |OUTPUT     |LVCMOS15    |10     |
|C5        |dval_a        |IOB      |IO_L27P_6           |INPUT      |HSTL_I_DCI  |6      |
|C6        |              |         |VCCO_6              |           |            |6      |
|C7        |data_a[20]    |IOB      |IO_L14N_6           |INPUT      |HSTL_I_DCI  |6      |
|C9        |data_a[14]    |IOB      |IO_L4P_6            |INPUT      |HSTL_I_DCI  |6      |
|D1        |data_b[5]     |IOB      |IO_L8P_CC_LC_10     |INPUT      |HSTL_I_DCI  |10     |
|D10       |data_a[10]    |IOB      |IO_L7N_6            |INPUT      |HSTL_I_DCI  |6      |
|D11       |data_a[4]     |IOB      |IO_L7P_6            |INPUT      |HSTL_I_DCI  |6      |
|D12       |data_a[1]     |IOB      |IO_L1P_6            |INPUT      |HSTL_I_DCI  |6      |
|D13       |              |         |VCCO_6              |           |            |6      |
|D14       |fe_hstl[2]    |IOB      |IO_L29N_6           |OUTPUT     |LVCMOS15    |6      |
|D15       |              |         |TDP_0               |           |            |       |
|D18       |              |         |GND                 |           |            |       |
|D2        |data_b[1]     |IOB      |IO_L7N_10           |INPUT      |HSTL_I_DCI  |10     |
|D23       |              |         |VCCO_5              |           |            |5      |
|D27       |data_VSI0[26] |IOB      |IO_L12P_5           |INPUT      |HSTL_III_DCI|5      |
|D28       |              |         |GND                 |           |            |       |
|D29       |data_VSI0[25] |IOB      |IO_L29P_5           |INPUT      |HSTL_III_DCI|5      |
|D3        |              |         |VCCO_10             |           |            |10     |
|D30       |data_VSI0[24] |IOB      |IO_L26P_5           |INPUT      |HSTL_III_DCI|5      |
|D31       |data_VSI0[23] |IOB      |IO_L26N_5           |INPUT      |HSTL_III_DCI|5      |
|D32       |data_VSI0[22] |IOB      |IO_L2N_9            |INPUT      |HSTL_III_DCI|9      |
|D33       |              |         |VCCO_9              |           |            |9      |
|D34       |data_VSI0[21] |IOB      |IO_L8P_CC_LC_9      |INPUT      |HSTL_III_DCI|9      |
|D4        |fe_hstl[20]   |IOB      |IO_L3P_10           |OUTPUT     |LVCMOS15    |10     |
|D5        |data_a[31]    |IOB      |IO_L27N_6           |INPUT      |HSTL_I_DCI  |6      |
|D6        |data_a[25]    |IOB      |IO_L18N_6           |INPUT      |HSTL_I_DCI  |6      |
|D7        |data_a[21]    |IOB      |IO_L18P_6           |INPUT      |HSTL_I_DCI  |6      |
|D8        |              |         |GND                 |           |            |       |
|D9        |data_a[15]    |IOB      |IO_L19P_6           |INPUT      |HSTL_I_DCI  |6      |
|E1        |data_b[6]     |IOB      |IO_L8N_CC_LC_10     |INPUT      |HSTL_I_DCI  |10     |
|E10       |              |         |VCCO_6              |           |            |6      |
|E11       |data_a[5]     |IOB      |IO_L11P_6           |INPUT      |HSTL_I_DCI  |6      |
|E12       |fe_hstl[5]    |IOB      |IO_L21N_6           |OUTPUT     |LVCMOS15    |6      |
|E13       |fe_hstl[8]    |IOB      |IO_L21P_6           |OUTPUT     |LVCMOS15    |6      |
|E14       |fe_hstl[0]    |IOB      |IO_L29P_6           |OUTPUT     |LVCMOS15    |6      |
|E15       |              |         |GND                 |           |            |       |
|E16       |spare_in_b    |IOB      |IO_L6P_GC_LC_3      |INPUT      |HSTL_I_DCI  |3      |
|E18       |spare_in_a    |IOB      |IO_L4P_GC_LC_3      |INPUT      |HSTL_I_DCI  |3      |
|E2        |data_b[2]     |IOB      |IO_L9N_CC_LC_10     |INPUT      |HSTL_I_DCI  |10     |
|E20       |              |         |VCCO_1              |           |            |1      |
|E25       |              |         |GND                 |           |            |       |
|E29       |data_VSI0[31] |IOB      |IO_L29N_5           |INPUT      |HSTL_III_DCI|5      |
|E3        |fe_hstl[15]   |IOB      |IO_L9P_CC_LC_10     |OUTPUT     |LVCMOS15    |10     |
|E30       |              |         |VCCO_5              |           |            |5      |
|E31       |data_VSI0[30] |IOB      |IO_L32P_5           |INPUT      |HSTL_III_DCI|5      |
|E32       |data_VSI0[29] |IOB      |IO_L11P_9           |INPUT      |HSTL_III_DCI|9      |
|E33       |data_VSI0[28] |IOB      |IO_L11N_9           |INPUT      |HSTL_III_DCI|9      |
|E34       |data_VSI0[27] |IOB      |IO_L8N_CC_LC_9      |INPUT      |HSTL_III_DCI|9      |
|E4        |fe_hstl[14]   |IOB      |IO_L3N_10           |OUTPUT     |LVCMOS15    |10     |
|E5        |              |         |GND                 |           |            |       |
|E6        |data_a[26]    |IOB      |IO_L26P_6           |INPUT      |HSTL_I_DCI  |6      |
|E9        |ATIME_A       |IOB      |IO_L19N_6           |INPUT      |HSTL_I_DCI  |6      |
|F1        |data_b[7]     |IOB      |IO_L17P_10          |INPUT      |HSTL_I_DCI  |10     |
|F10       |data_a[11]    |IOB      |IO_L6P_6            |INPUT      |HSTL_I_DCI  |6      |
|F11       |data_a[6]     |IOB      |IO_L11N_6           |INPUT      |HSTL_I_DCI  |6      |
|F12       |              |         |GND                 |           |            |       |
|F15       |              |         |TDN_0               |           |            |       |
|F17       |              |         |VCCO_3              |           |            |3      |
|F19       |              |         |VCCAUX              |           |            |       |
|F2        |              |         |GND                 |           |            |       |
|F22       |              |         |GND                 |           |            |       |
|F25       |spare_out_b   |IOB      |IO_L6P_5            |OUTPUT     |HSTL_III    |5      |
|F26       |spare_out_a   |IOB      |IO_L6N_5            |OUTPUT     |HSTL_III    |5      |
|F27       |              |         |VCCO_5              |           |            |5      |
|F3        |fe_hstl[19]   |IOB      |IO_L6N_10           |OUTPUT     |LVCMOS15    |10     |
|F32       |              |         |GND                 |           |            |       |
|F34       |dtick_VSI1    |IOB      |IO_L14N_9           |INPUT      |HSTL_III_DCI|9      |
|F4        |fe_hstl[18]   |IOB      |IO_L6P_10           |OUTPUT     |LVCMOS15    |10     |
|F5        |fe_hstl[10]   |IOB      |IO_L2P_10           |OUTPUT     |LVCMOS15    |10     |
|F6        |data_a[27]    |IOB      |IO_L26N_6           |INPUT      |HSTL_I_DCI  |6      |
|F7        |              |         |VCCO_6              |           |            |6      |
|F9        |              |         |VCCAUX              |           |            |       |
|G1        |data_b[9]     |IOB      |IO_L17N_10          |INPUT      |HSTL_I_DCI  |10     |
|G10       |data_a[12]    |IOB      |IO_L6N_6            |INPUT      |HSTL_I_DCI  |6      |
|G14       |              |         |VCCO_1              |           |            |1      |
|G17       |spare_in_c    |IOB      |IO_L8P_GC_LC_3      |INPUT      |HSTL_I_DCI  |3      |
|G19       |              |         |GND                 |           |            |       |
|G2        |data_b[8]     |IOB      |IO_L14N_10          |INPUT      |HSTL_I_DCI  |10     |
|G20       |              |         |VCCINT              |           |            |       |
|G22       |              |         |VCCINT              |           |            |       |
|G24       |              |         |VCCO_5              |           |            |5      |
|G26       |              |         |VCCAUX              |           |            |       |
|G29       |              |         |GND                 |           |            |       |
|G3        |data_b[3]     |IOB      |IO_L14P_10          |INPUT      |HSTL_I_DCI  |10     |
|G30       |data_VSI1[3]  |IOB      |IO_L9P_CC_LC_9      |INPUT      |HSTL_III_DCI|9      |
|G31       |data_VSI1[2]  |IOB      |IO_L9N_CC_LC_9      |INPUT      |HSTL_III_DCI|9      |
|G32       |data_VSI1[1]  |IOB      |IO_L16P_9           |INPUT      |HSTL_III_DCI|9      |
|G33       |data_VSI1[0]  |IOB      |IO_L16N_9           |INPUT      |HSTL_III_DCI|9      |
|G34       |              |         |VCCO_9              |           |            |9      |
|G4        |              |         |VCCO_10             |           |            |10     |
|G5        |fe_hstl[12]   |IOB      |IO_L2N_10           |OUTPUT     |LVCMOS15    |10     |
|G7        |data_a[22]    |IOB      |IO_L28P_6           |INPUT      |HSTL_I_DCI  |6      |
|G8        |data_a[17]    |IOB      |IO_L16N_6           |INPUT      |HSTL_I_DCI  |6      |
|G9        |              |         |GND                 |           |            |       |
|H1        |              |         |VCCO_10             |           |            |10     |
|H10       |data_a[13]    |IOB      |IO_L8P_CC_LC_6      |INPUT      |HSTL_I_DCI  |6      |
|H11       |              |         |VCCO_6              |           |            |6      |
|H16       |              |         |GND                 |           |            |       |
|H2        |data_b[10]    |IOB      |IO_L19N_10          |INPUT      |HSTL_I_DCI  |10     |
|H21       |              |         |VCCO_1              |           |            |1      |
|H23       |              |         |VCCAUX              |           |            |       |
|H26       |              |         |GND                 |           |            |       |
|H28       |data_VSI1[8]  |IOB      |IO_L1N_9            |INPUT      |HSTL_III_DCI|9      |
|H29       |data_VSI1[7]  |IOB      |IO_L6P_9            |INPUT      |HSTL_III_DCI|9      |
|H3        |data_b[4]     |IOB      |IO_L19P_10          |INPUT      |HSTL_I_DCI  |10     |
|H30       |data_VSI1[6]  |IOB      |IO_L6N_9            |INPUT      |HSTL_III_DCI|9      |
|H31       |              |         |VCCO_9              |           |            |9      |
|H32       |data_VSI1[5]  |IOB      |IO_L20P_9           |INPUT      |HSTL_III_DCI|9      |
|H33       |data_VSI1[4]  |IOB      |IO_L22P_9           |INPUT      |HSTL_III_DCI|9      |
|H34       |dpps_VSI1     |IOB      |IO_L22N_9           |INPUT      |HSTL_III_DCI|9      |
|H4        |fe_hstl[22]   |IOB      |IO_L11N_10          |OUTPUT     |LVCMOS15    |10     |
|H5        |fe_hstl[9]    |IOB      |IO_L11P_10          |OUTPUT     |LVCMOS15    |10     |
|H6        |              |         |GND                 |           |            |       |
|H7        |data_a[23]    |IOB      |IO_L31N_6           |INPUT      |HSTL_I_DCI  |6      |
|H8        |data_a[18]    |IOB      |IO_L31P_6           |INPUT      |HSTL_I_DCI  |6      |
|J10       |              |         |VCCAUX              |           |            |       |
|J12       |              |         |VCCINT              |           |            |       |
|J13       |              |         |GND                 |           |            |       |
|J16       |              |         |VCCINT              |           |            |       |
|J18       |              |         |VCCO_3              |           |            |3      |
|J22       |              |         |VCCINT              |           |            |       |
|J23       |              |         |GND                 |           |            |       |
|J26       |              |         |VCCINT              |           |            |       |
|J27       |data_VSI1[12] |IOB      |IO_L3P_9            |INPUT      |HSTL_III_DCI|9      |
|J28       |              |         |VCCO_9              |           |            |9      |
|J29       |data_VSI1[11] |IOB      |IO_L10P_9           |INPUT      |HSTL_III_DCI|9      |
|J3        |              |         |GND                 |           |            |       |
|J30       |data_VSI1[10] |IOB      |IO_L10N_9           |INPUT      |HSTL_III_DCI|9      |
|J33       |              |         |GND                 |           |            |       |
|J34       |data_VSI1[9]  |IOB      |IO_L29P_9           |INPUT      |HSTL_III_DCI|9      |
|J4        |data_b[11]    |IOB      |IO_L18P_10          |INPUT      |HSTL_I_DCI  |10     |
|J5        |fe_hstl[11]   |IOB      |IO_L10N_10          |OUTPUT     |LVCMOS15    |10     |
|J6        |data_a[28]    |IOB      |IO_L10P_10          |INPUT      |HSTL_I_DCI  |10     |
|J8        |              |         |VCCO_6              |           |            |6      |
|K1        |fom_clk_b     |IOB      |IO_L26N_10          |OUTPUT     |HSTL_I_DCI  |10     |
|K10       |              |         |GND                 |           |            |       |
|K11       |              |         |VCCINT              |           |            |       |
|K12       |              |         |GND                 |           |            |       |
|K13       |              |         |VCCINT              |           |            |       |
|K15       |              |         |VCCO_1              |           |            |1      |
|K2        |data_b[14]    |IOB      |IO_L26P_10          |INPUT      |HSTL_I_DCI  |10     |
|K20       |              |         |GND                 |           |            |       |
|K21       |              |         |VCCINT              |           |            |       |
|K22       |              |         |GND                 |           |            |       |
|K23       |              |         |VCCINT              |           |            |       |
|K25       |              |         |VCCO_5              |           |            |5      |
|K26       |dval_VSI1     |IOB      |IO_L16N_5           |INPUT      |HSTL_III_DCI|5      |
|K27       |data_VSI1[18] |IOB      |IO_L3N_9            |INPUT      |HSTL_III_DCI|9      |
|K28       |data_VSI1[17] |IOB      |IO_L15P_9           |INPUT      |HSTL_III_DCI|9      |
|K29       |data_VSI1[16] |IOB      |IO_L15N_9           |INPUT      |HSTL_III_DCI|9      |
|K3        |res_pll_b     |IOB      |IO_L25P_CC_LC_10    |OUTPUT     |HSTL_I_DCI  |10     |
|K30       |              |         |GND                 |           |            |       |
|K32       |data_VSI1[15] |IOB      |IO_L26P_9           |INPUT      |HSTL_III_DCI|9      |
|K33       |data_VSI1[14] |IOB      |IO_L26N_9           |INPUT      |HSTL_III_DCI|9      |
|K34       |data_VSI1[13] |IOB      |IO_L29N_9           |INPUT      |HSTL_III_DCI|9      |
|K4        |data_b[13]    |IOB      |IO_L18N_10          |INPUT      |HSTL_I_DCI  |10     |
|K5        |              |         |VCCO_10             |           |            |10     |
|K6        |data_b[12]    |IOB      |IO_L16P_10          |INPUT      |HSTL_I_DCI  |10     |
|K7        |              |         |VCCINT              |           |            |       |
|K8        |res_pll_a     |IOB      |IO_L32P_6           |OUTPUT     |HSTL_I_DCI  |6      |
|L1        |data_b[20]    |IOB      |IO_L29P_10          |INPUT      |HSTL_I_DCI  |10     |
|L10       |              |         |VCCINT              |           |            |       |
|L11       |              |         |GND                 |           |            |       |
|L12       |              |         |VCCINT              |           |            |       |
|L13       |              |         |GND                 |           |            |       |
|L17       |              |         |GND                 |           |            |       |
|L2        |              |         |VCCO_10             |           |            |10     |
|L20       |              |         |VCCINT              |           |            |       |
|L21       |              |         |GND                 |           |            |       |
|L22       |              |         |VCCINT              |           |            |       |
|L23       |              |         |GND                 |           |            |       |
|L24       |              |         |VCCAUX              |           |            |       |
|L27       |              |         |GND                 |           |            |       |
|L28       |data_VSI1[24] |IOB      |IO_L18P_9           |INPUT      |HSTL_III_DCI|9      |
|L29       |data_VSI1[23] |IOB      |IO_L18N_9           |INPUT      |HSTL_III_DCI|9      |
|L3        |data_b[19]    |IOB      |IO_L25N_CC_LC_10    |INPUT      |HSTL_I_DCI  |10     |
|L30       |data_VSI1[22] |IOB      |IO_L24P_CC_LC_9     |INPUT      |HSTL_III_DCI|9      |
|L31       |data_VSI1[21] |IOB      |IO_L24N_CC_LC_9     |INPUT      |HSTL_III_DCI|9      |
|L32       |              |         |VCCO_9              |           |            |9      |
|L33       |data_VSI1[20] |IOB      |IO_L31P_9           |INPUT      |HSTL_III_DCI|9      |
|L34       |data_VSI1[19] |IOB      |IO_L31N_9           |INPUT      |HSTL_III_DCI|9      |
|L4        |data_b[18]    |IOB      |IO_L22N_10          |INPUT      |HSTL_I_DCI  |10     |
|L5        |data_b[17]    |IOB      |IO_L22P_10          |INPUT      |HSTL_I_DCI  |10     |
|L6        |data_b[16]    |IOB      |IO_L16N_10          |INPUT      |HSTL_I_DCI  |10     |
|L7        |              |         |GND                 |           |            |       |
|L8        |data_b[15]    |IOB      |IO_L15P_10          |INPUT      |HSTL_I_DCI  |10     |
|M1        |data_b[23]    |IOB      |IO_L29N_10          |INPUT      |HSTL_I_DCI  |10     |
|M10       |data_b[24]    |IOB      |IO_L4P_10           |INPUT      |HSTL_I_DCI  |10      |
|M11       |              |         |VCCAUX              |           |            |        |
|M12       |              |         |GND                 |           |            |        |
|M13       |              |         |VCCINT              |           |            |        |
|M14       |              |         |GND                 |           |            |        |
|M15       |              |         |VCCINT              |           |            |        |
|M19       |              |         |VCCO_1              |           |            |1       |
|M21       |              |         |VCCINT              |           |            |        |
|M22       |              |         |GND                 |           |            |        |
|M23       |              |         |VCCINT              |           |            |        |
|M24       |              |         |GND                 |           |            |        |
|M29       |              |         |VCCO_9              |           |            |9       |
|M3        |data_b[22]    |IOB      |IO_L28P_10          |INPUT      |HSTL_I_DCI  |10      |
|M30       |data_VSI1[27] |IOB      |IO_L28P_9           |INPUT      |HSTL_III_DCI|9       |
|M32       |data_VSI1[26] |IOB      |IO_L32P_9           |INPUT      |HSTL_III_DCI|9       |
|M33       |data_VSI1[25] |IOB      |IO_L32N_9           |INPUT      |HSTL_III_DCI|9       |
|M34       |              |         |GND                 |           |            |        |
|M4        |              |         |GND                 |           |            |        |
|M6        |data_b[21]    |IOB      |IO_L27P_10          |INPUT      |HSTL_I_DCI  |10      |
|M7        |fom_tick_b    |IOB      |IO_L21P_10          |OUTPUT     |HSTL_I_DCI  |10      |
|M8        |ATIME_B       |IOB      |IO_L15N_10          |INPUT      |HSTL_I_DCI  |10      |
|M9        |              |         |VCCO_10             |           |            |10      |
|N1        |              |         |GND                 |           |            |        |
|N10       |data_b[25]    |IOB      |IO_L12P_10          |INPUT      |HSTL_I_DCI  |10      |
|N11       |              |         |GND                 |           |            |        |
|N12       |fe_hstl[23]   |IOB      |IO_L5N_10           |OUTPUT     |LVCMOS15    |10      |
|N14       |              |         |VCCINT              |           |            |        |
|N16       |              |         |VCCO_1              |           |            |1       |
|N21       |              |         |GND                 |           |            |        |
|N24       |              |         |VCCINT              |           |            |        |
|N26       |              |         |VCCO_9              |           |            |9       |
|N27       |data_VSI1[31] |IOB      |IO_L27P_9           |INPUT      |HSTL_III_DCI|9       |
|N28       |              |         |VCCINT              |           |            |        |
|N29       |data_VSI1[29] |IOB      |IO_L30P_9           |INPUT      |HSTL_III_DCI|9       |
|N30       |data_VSI1[28] |IOB      |IO_L30N_9           |INPUT      |HSTL_III_DCI|9      |
|N31       |              |         |GND                 |           |            |       |
|N5        |fe_hstl[27]   |IOB      |IO_L30P_10          |OUTPUT     |LVCMOS15    |10     |
|N6        |              |         |VCCO_10             |           |            |10     |
|N7        |data_b[28]    |IOB      |IO_L21N_10          |INPUT      |HSTL_I_DCI  |10     |
|N8        |              |         |VCCAUX              |           |            |       |
|P10       |data_b[26]    |IOB      |IO_L20P_10          |INPUT      |HSTL_I_DCI  |10     |
|P11       |data_b[31]    |IOB      |IO_L13N_10          |INPUT      |HSTL_I_DCI  |10     |
|P12       |dval_b        |IOB      |IO_L13P_10          |INPUT      |HSTL_I_DCI  |10     |
|P13       |              |         |VCCO_10             |           |            |10     |
|P15       |              |         |VCCINT              |           |            |       |
|P16       |              |         |GND                 |           |            |       |
|P17       |              |         |VCCINT              |           |            |       |
|P18       |              |         |GND                 |           |            |       |
|P19       |              |         |VCCINT              |           |            |       |
|P23       |              |         |VCCO_9              |           |            |9      |
|P25       |              |         |VCCAUX              |           |            |       |
|P27       |data_VSI1[30] |IOB      |IO_L27N_9           |INPUT      |HSTL_III_DCI|9      |
|P28       |              |         |GND                 |           |            |       |
|P5        |fe_hstl[25]   |IOB      |IO_L30N_10          |OUTPUT     |LVCMOS15    |10     |
|P6        |data_b[30]    |IOB      |IO_L31N_10          |INPUT      |HSTL_I_DCI  |10     |
|P7        |data_b[29]    |IOB      |IO_L31P_10          |INPUT      |HSTL_I_DCI  |10     |
|P8        |              |         |GND                 |           |            |       |
|R10       |              |         |VCCO_10             |           |            |10     |
|R11       |fe_hstl[24]   |IOB      |IO_L24P_CC_LC_10    |OUTPUT     |LVCMOS15    |10     |
|R12       |              |         |VCCINT              |           |            |       |
|R13       |              |         |GND                 |           |            |       |
|R14       |              |         |VCCINT              |           |            |       |
|R15       |              |         |GND                 |           |            |       |
|R16       |              |         |VCCINT              |           |            |       |
|R17       |              |         |CCLK_0              |           |            |       |
|R18       |              |         |VCCAUX              |           |            |       |
|R20       |              |         |VCCO_9              |           |            |9      |
|R25       |              |         |GND                 |           |            |       |
|R5        |              |         |GND                 |           |            |       |
|R9        |data_b[27]    |IOB      |IO_L32N_10          |INPUT      |HSTL_I_DCI  |10     |
|T10       |fe_hstl[28]   |IOB      |IO_L32P_10          |OUTPUT     |LVCMOS15    |10     |
|T11       |fe_hstl[26]   |IOB      |IO_L24N_CC_LC_10    |OUTPUT     |LVCMOS15    |10     |
|T12       |              |         |GND                 |           |            |       |
|T13       |              |         |VCCINT              |           |            |       |
|T14       |              |         |GND                 |           |            |       |
|T15       |              |         |VCCINT              |           |            |       |
|T16       |              |         |D_IN_0              |           |            |       |
|T17       |              |         |VCCO_0              |           |            |0      |
|T18       |              |         |HSWAPEN_0           |           |            |       |
|T19       |              |         |VCCINT              |           |            |       |
|T2        |              |         |GND                 |           |            |       |
|T20       |              |         |GND                 |           |            |       |
|T21       |              |         |VCCINT              |           |            |       |
|T22       |              |         |GND                 |           |            |       |
|T32       |              |         |GND                 |           |            |       |
|T9        |              |         |VCCAUX              |           |            |       |
|U13       |              |         |RDWR_B_0            |           |            |       |
|U14       |              |         |VCCO_0              |           |            |0      |
|U15       |              |         |DONE_0              |           |            |       |
|U16       |              |         |VCCAUX              |           |            |       |
|U17       |              |         |CS_B_0              |           |            |       |
|U18       |              |         |VCCINT              |           |            |       |
|U19       |              |         |GND                 |           |            |       |
|U20       |              |         |VCCINT              |           |            |       |
|U21       |              |         |INIT_0              |           |            |       |
|U22       |              |         |PROGRAM_B_0         |           |            |       |
|U29       |              |         |GND                 |           |            |       |
|U9        |              |         |GND                 |           |            |       |
|V13       |              |         |TMS_0               |           |            |       |
|V14       |              |         |TCK_0               |           |            |       |
|V15       |              |         |VCCINT              |           |            |       |
|V16       |              |         |GND                 |           |            |       |
|V17       |              |         |VCCINT              |           |            |       |
|V18       |              |         |TDO_0               |           |            |       |
|V19       |              |         |VCCAUX              |           |            |       |
|V20       |              |         |M2_0                |           |            |       |
|V21       |              |         |VCCO_0              |           |            |0      |
|V22       |              |         |VBATT_0             |           |            |       |
|V26       |              |         |GND                 |           |            |       |
|V6        |              |         |GND                 |           |            |       |
|W13       |              |         |GND                 |           |            |       |
|W14       |              |         |VCCINT              |           |            |       |
|W15       |              |         |GND                 |           |            |       |
|W16       |              |         |VCCINT              |           |            |       |
|W17       |              |         |TDI_0               |           |            |       |
|W18       |              |         |VCCO_0              |           |            |0      |
|W19       |              |         |M1_0                |           |            |       |
|W20       |              |         |M0_0                |           |            |       |
|W21       |              |         |PWRDWN_B_0          |           |            |       |
|W22       |              |         |VCCINT              |           |            |       |
|W23       |              |         |GND                 |           |            |       |
|W26       |              |         |VCCAUX              |           |            |       |
|W3        |              |         |GND                 |           |            |       |
|W33       |              |         |GND                 |           |            |       |
|Y10       |              |         |GND                 |           |            |       |
|Y11       |fe_hstl[33]   |IOB      |IO_L3P_12           |OUTPUT     |LVCMOS15    |12     |
|Y12       |fe_hstl[29]   |IOB      |IO_L9N_CC_LC_12     |OUTPUT     |LVCMOS15    |12     |
|Y13       |fe_hstl[35]   |IOB      |IO_L9P_CC_LC_12     |OUTPUT     |LVCMOS15    |12     |
|Y14       |fe_hstl[31]   |IOB      |IO_L5P_12           |OUTPUT     |LVCMOS15    |12     |
|Y15       |              |         |VCCO_12             |           |            |12     |
|Y17       |              |         |VCCAUX              |           |            |       |
|Y18       |              |         |DOUT_BUSY_0         |           |            |       |
|Y19       |              |         |VCCINT              |           |            |       |
|Y20       |              |         |GND                 |           |            |       |
|Y21       |              |         |VCCINT              |           |            |       |
|Y22       |              |         |GND                 |           |            |       |
```
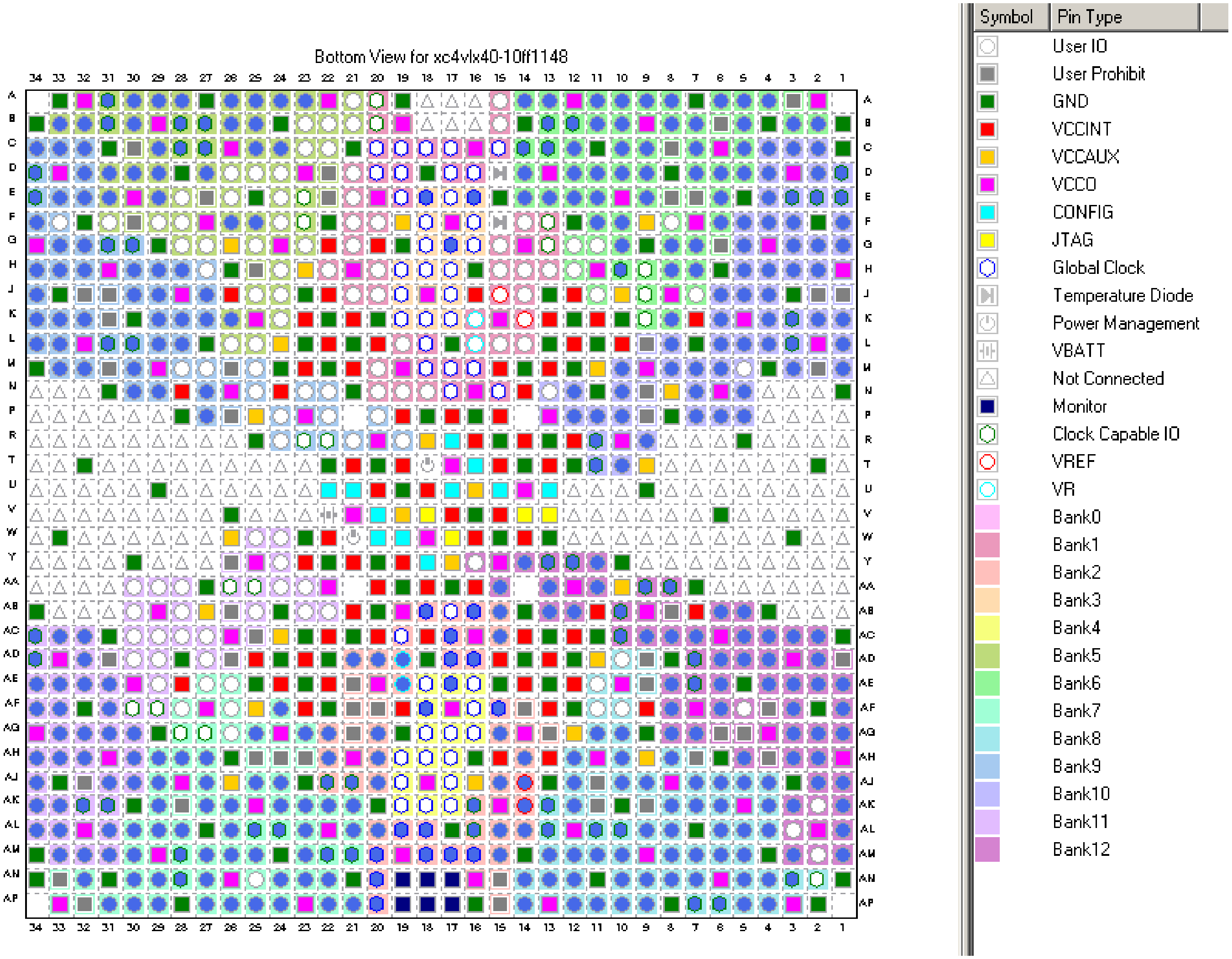

Y23			VCCINT			
Y25			VCCO_11			11
Y30			GND			

Table 8-2 Pinout by Pin Number

8.3 Xilinx XC4VLX40-10FF1148-CS2 Package Drawing


Bottom View for xc4vlx40-10ff1148
34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
A B C D E F G H J K L M N P R T U V W Y AA AB AC AD AE AF AG AH AJ AK AL AM AN AP

Symbol	Pin Type
○	User IO
■	User Prohibit
🟩	GND
🟥	VCCINT
🟧	VCCAUX
🟪	VCCO
🟦	CONFIG
🟨	JTAG
⬡	Global Clock
⧓	Temperature Diode
⏻	Power Management
⊪	VBATT
△	Not Connected
■	Monitor
⬡	Clock Capable IO
○	VREF
○	VR
▨	Bank0
▨	Bank1
▨	Bank2
▨	Bank3
▨	Bank4
▨	Bank5
▨	Bank6
▨	Bank7
▨	Bank8
▨	Bank9
▨	Bank10
▨	Bank11
▨	Bank12

Figure 8-1 Pin Locations

8.4 Programming Notes

All FPGAs on the Station Board are programmed through their 8-bit wide configuration port. The Station Board CMIB software requires the Binary (.bin) output file to program the Xilinx FPGAs. This is set by selecting “Properties…” from the “Process” pull-down menu in the Xilinx ISE software. Select the “General Options” and check “Create Binary Configuration File”.

9 References

Brent Carlson, “Refined EVLA WIDAR Correlator Architecture”, NRC-EVLA Memo# 014, October 2, 2001.

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