REQUIREMENTS AND FUNCTIONAL SPECIFICATION

Station Board MCB Fanout FPGA

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Revision: 1.5

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List of Abbreviations and Acronyms

CFG	Configuration FPGA
CMIB	Correlator Module Interface Board
DMA	Delay Module A.
DMB	Delay Module B.
FORM	Fiber Optic Receiver Module.
IC	Input Chip
MCB	Monitor and Control Bus or MCB FPGA.
MSB	Most Significant Bit.
OUTA	Output A FPGA.
OUTB	Output B FPGA.
PCMC	PC Mezzanine Card.
TC	Timing Chip.
UA	Filter FPGA within group A.
UB	Filter FPGA within group B.
VSIA	VSI A FPGA.
VSIB	VSI B FPGA.
WBC	Wide Band Correlator FPGA.

1 Revision History

Revision	Date	Changes/Notes	Author
Draft	March 2004	Initial release for reviewing	Z. Ljusic
1.0	August 2005	Implemented many changes to reflect the current SB design. Changed the name of the document.	Z. Ljusic
1.1	June 2006	Described changes regarding MCB bus grouping imposed by ICX simulation of the routed Station Board.	Z. Ljusic
1.2	March 2007	Split Fanout FPGAs RFS into MCB RFS and CFG RFS	D. Fort
1.3	February 2007	Added a new register at address 04h for controlling Analog MUX.	Z. Ljusic
1.4	March 2008	Modified Analog Mux register to reflect addition of two new temperature sensors on the board. Corrected a few typos.	Z. Ljusic
1.5	01 Apr 2011	Pinouts, etc added.	D. Fort

2 Introduction

This document describes the Station Board MCB Fanout FPGA. As the name says, this device act as a buffer and the logic level shifter between the PCMC and the rest of the chips on the Station Board. The logic utilization is minimal while the pin utilization is maximal.

3 Context

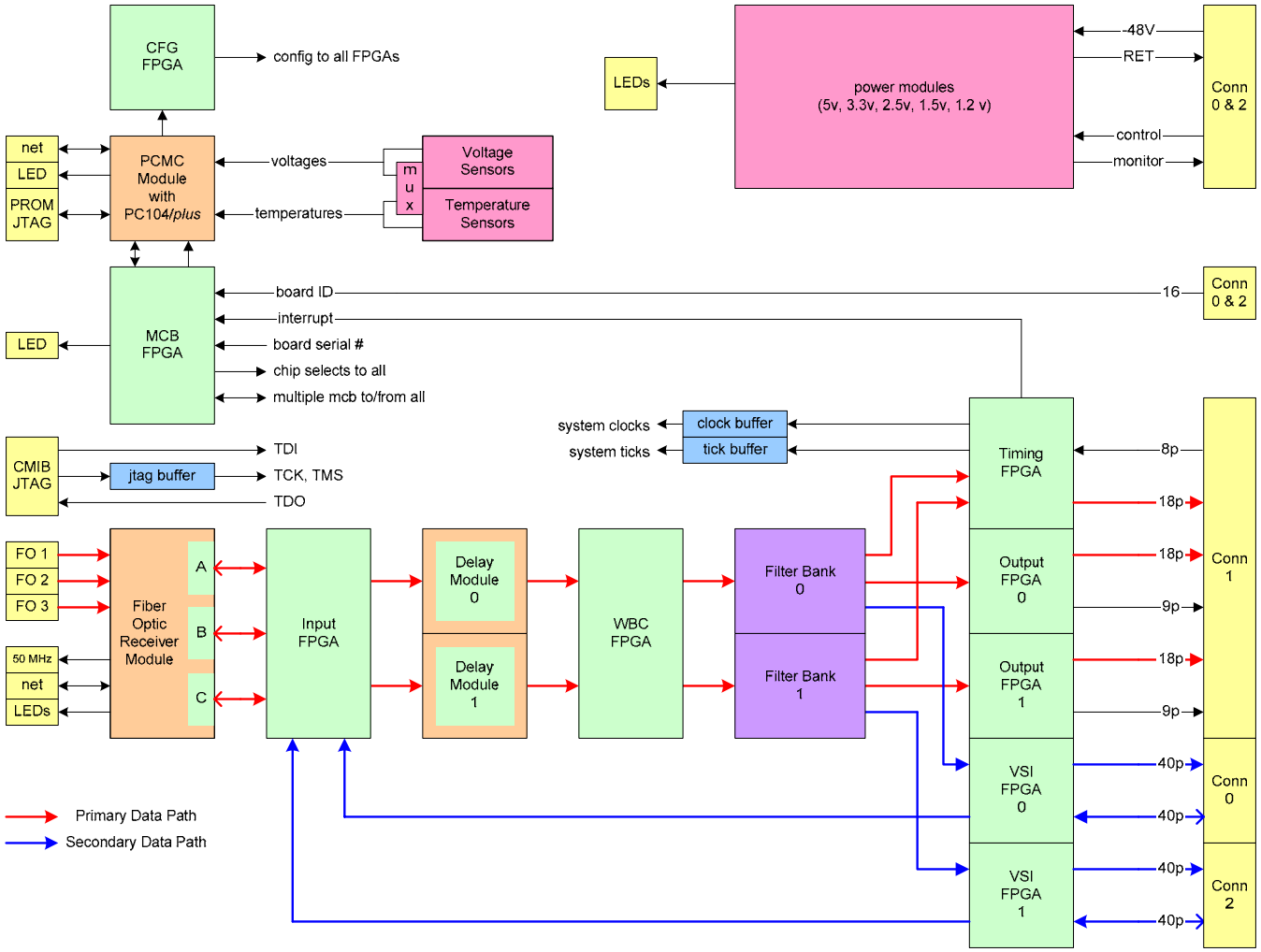

Figure 3-1 Station Board Block Diagram

4 MCB Fanout FPGA

The MCB Fan-out FPGA has two main functions:

1. It fans-out one MCB bus from the PCMC to 47 ICs on the Station Board.

2. It adjusts voltage levels between the PCMC 3.3V FPGA and 3.3V intolerant ICs on the Station Board.

The device selected for the application is Xilinx Virtex-4 series: XC4VSX35-10FF668. The size of the FPGA is dictated by the pin count while the logic usage is minimal. No heat sink is required. The choice of the SX35 is governed by economy since a large number of SX35s are required for the Filter FPGA. According to the simulation and Place and Route done so far the total delay in both direction thru the FPGA is up to 12ns. For timing specification refer to ‘AN25022N0091_MonitorControlSpec_Feb22-05’.

The high-level functional lock diagram of the FPGA is given in the following figure.

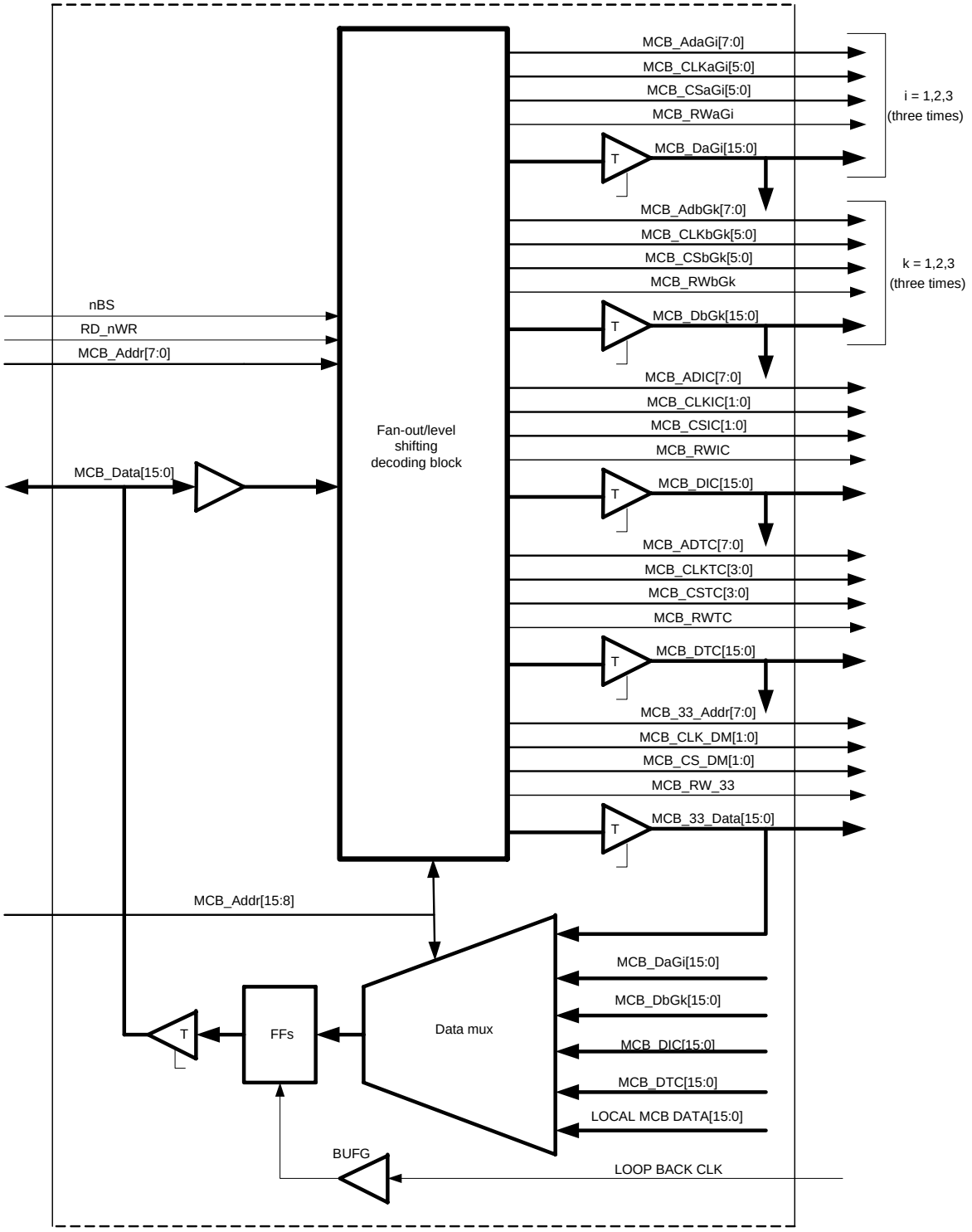

Figure 4-1 MCB Fanout FPGA functional block diagram

The higher address byte, MCB_Addr[15:8] , is used to control the Chip Select ,CS, lines on the board. Each chip has its own unique CS line, which activates the chip when low. Chip groups are formed that share the address and data bus. This concept saves pins and

makes board routing easier. Maximum number of ICs within a group is six. This is a result from signal vision simulation. There are nine MCB groups within the Station Board and only six of them have six ICs on the MCB bus. The rest of the groups are 3 or 4 ICs.

More details are given in the figures that follow.

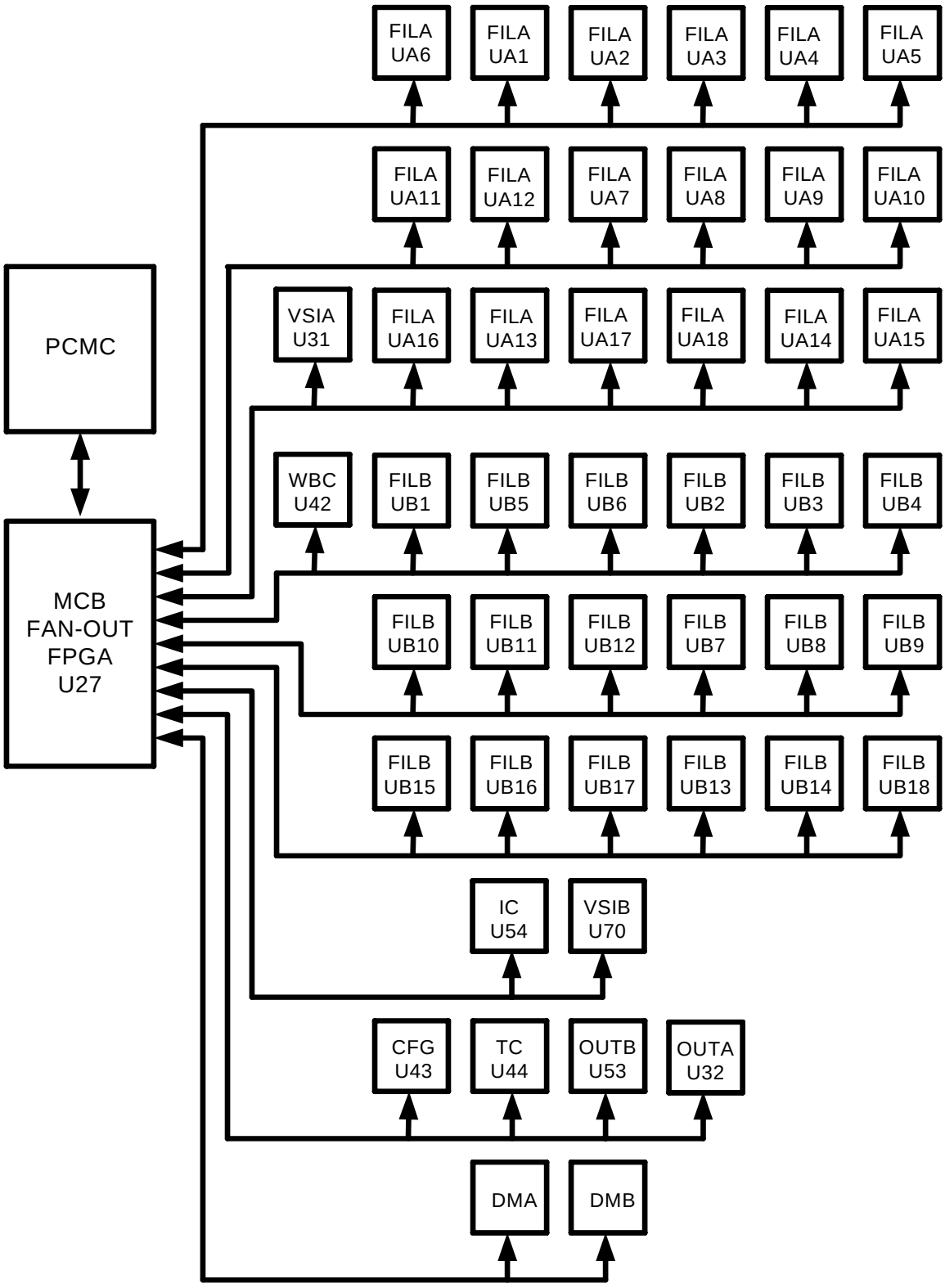

Figure 4-2 Station Board MCB grouping

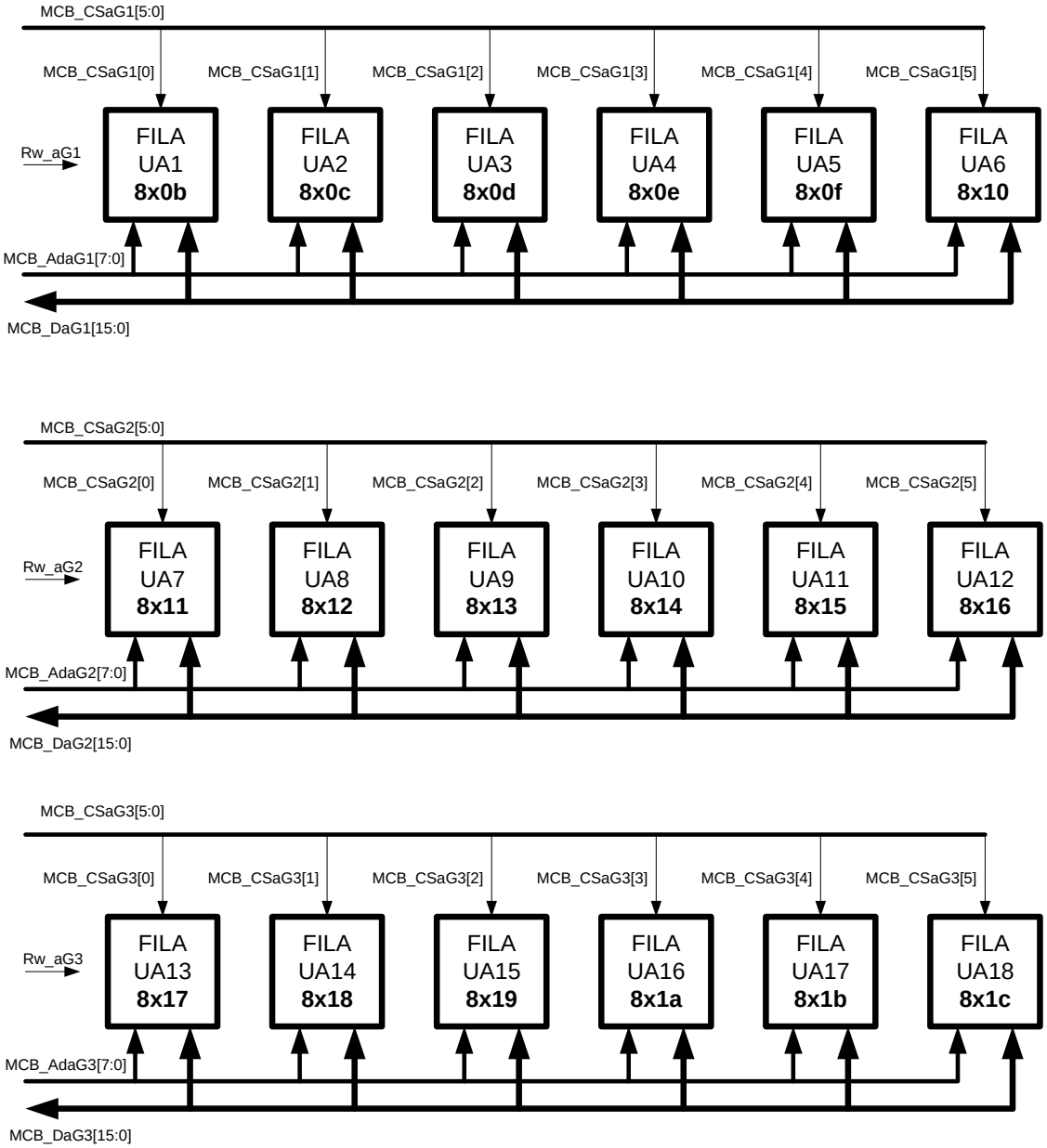

Figure 4-3 MCB groups of six ICs within filter bank A.

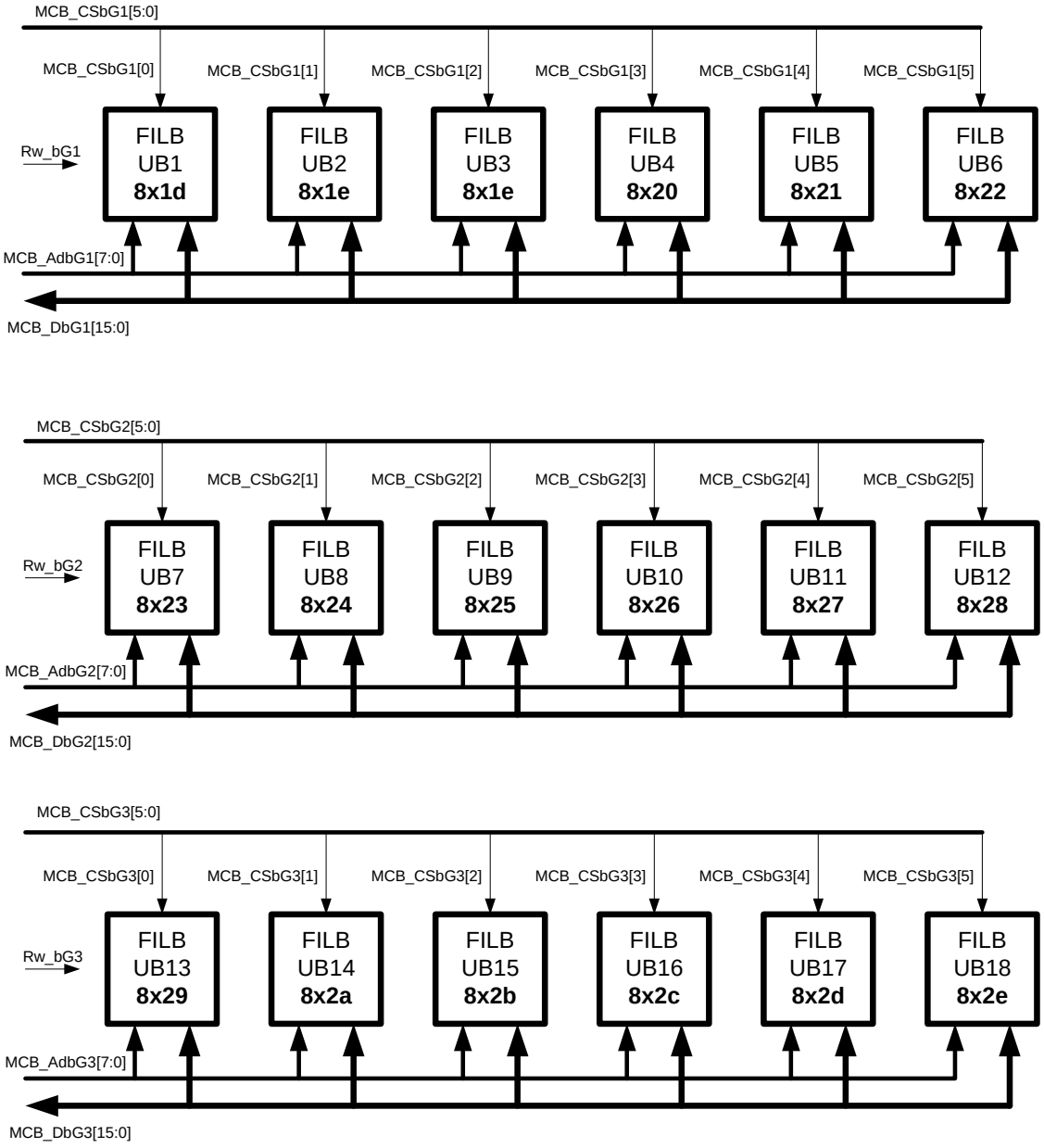

Figure 4-4 MCB groups of six ICs within filter bank B.

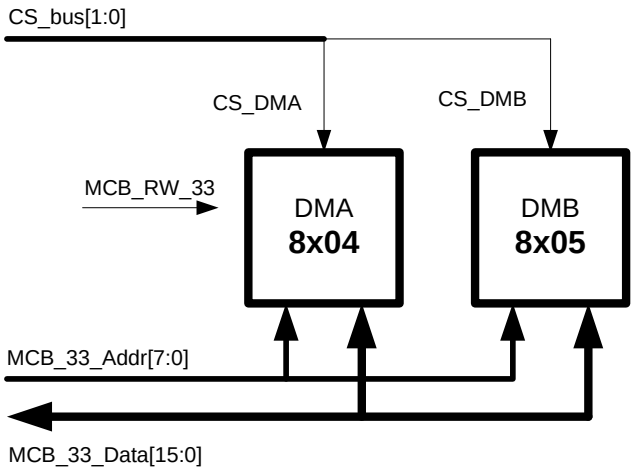

Figure 4-5 Delay Modules 3.3V MCB group

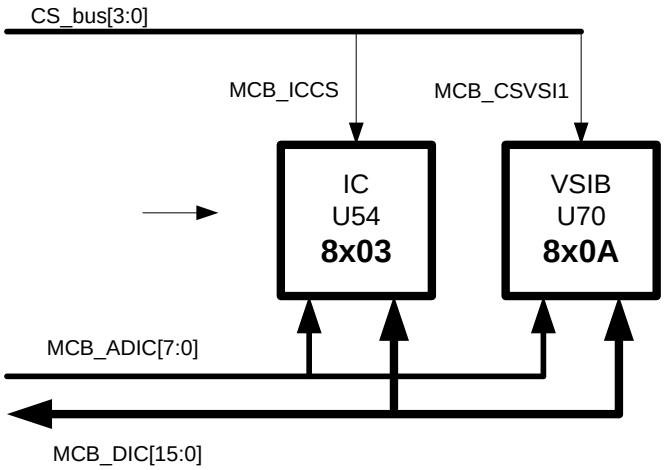

Figure 4-6 WBC Chip and VSIB MCB group

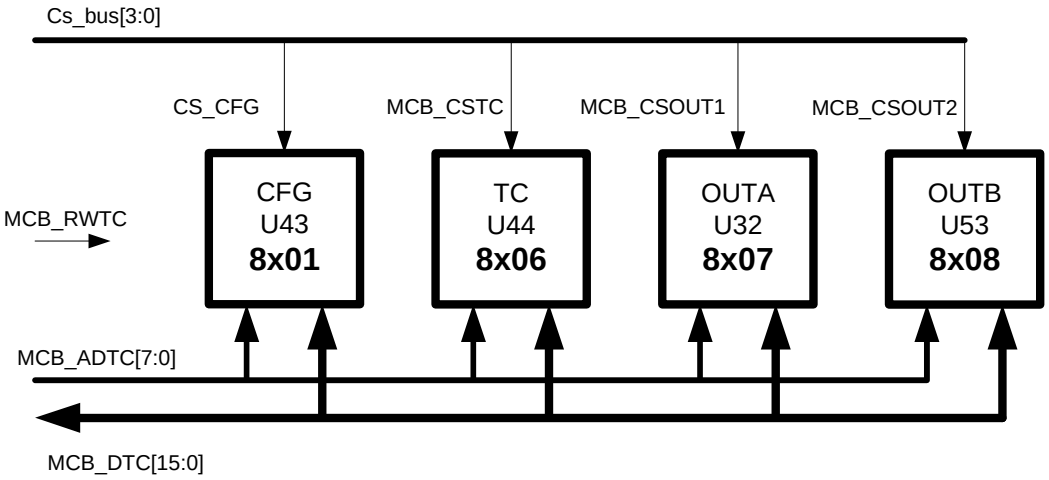

Figure 4-7 Configuration, Timing, Output A and B FPGAs 3.3V MCB group

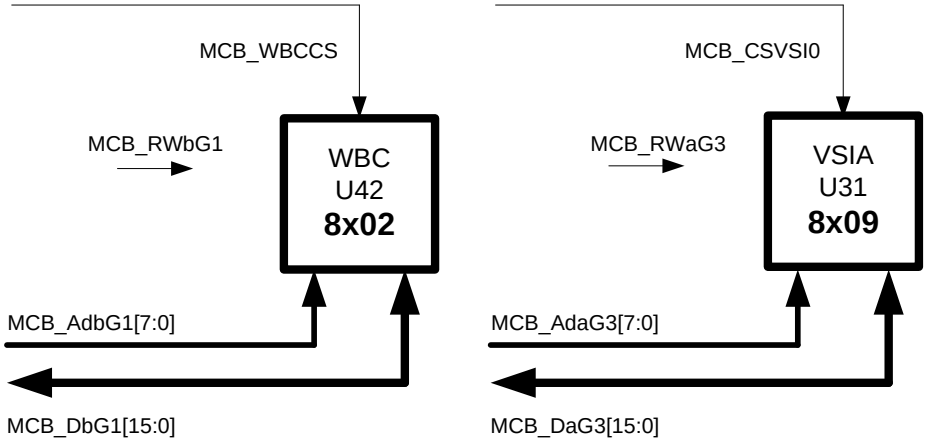

Figure 4-8 WBC and VSIA FPGAs added to MCB filter groups

4.1 MCB Fanout FPGA memory map

The MCB Fan-out FPGA contains four internal registers. This FPGA is selected by the PCMC when higher address byte has **0x00** value.

Address	Mnemonic	Register Name	Access	Reset Value
00h	SBID	Station Board ID (rack, crate, slot)	R	xxxxh
01h	FVR	MCB Fanout FPGA Version/Revision	R	0001h
02h	RBT	MCB Read Back Test register	R/W	0000h
03h	CC	MCB Configurations and Control register	R/W	0000h
04h	AM	Analog Mux register	R/W	001Fh

Table 4-1 MCB Fanout FPGA memory map

4.1.1 Station Board ID register – SBID

Address	15:0	Access	Reset
00h	SBID	R	0001h

Table 4-2 Station Board ID – SBID register

The bits within the register define the rack, crate and slot in which the board resides. The bits come from two of the rear backplanes.

4.1.2 MCB Version/Revision Number register – FVR

Address	15:8	7:4	3:0	Access	Reset
01h	Unused	Version	Revision	R	0001h

Table 4-3 MCB Version/Revision Number – FVR register

This register specifies the FPGA Version/Revision.

The fields within the register are defined as follows:

Version [7:4]: This version number is to be incremented whenever the new FPGA load is incompatible with the previous version from the software standpoint and would require change to the driver. The initial version will be numbered 1(b0001). Version 0 is reserved for prototyping and proof of concept.

Revision [3:0]: This revision number is to be incremented whenever the new FPGA load incorporates new functionality but does not require software upgrades.

4.1.3 MCB Read Back Test register - RB

Address	15:0	Access	Reset
02h	Read Back	R/W	0000h

Table 4-4 MCB Read Back Test – RB register

This is a test register. Writes to this register will have no effect. It simply provides means for communication verification between the FPGA and the MCB. The register keeps its last value until next write to its location. The fields within the register are defined as follows:

Read Back [15:0]: any 16 bits long combination of zeros and ones.

4.1.4 MCB Configurations and Control register - CC

Address	15:3	2:1	0	Access	Reset
03h	Unused	SBST	Unused	R/W	0000h

Table 4-5 MCB Configurations and Control - CC register

The fields within the register are defined as follows:

SBST[2:1]: these two bits indicate status of the Station Board. The bits define a front panel LED color in the following way:

00: LED is off.

01: LED is red.

10: LED is green.

11: Led is orange.

4.1.5 Analog Mux register - AM

Address	6	5	4:0	Access	Reset
04h	nAMUX_WR	nAMUX_ENA	AMUX_ADDR	R/W	001Fh

Table 4-6 Analog Mux – AM register

The fields within the register are defined as follows:

AMUX_ADDR[4:0]: Analog MUX address lines. The MUX output selection is performed according the Table 4-7.

nAMUX_ENA[5]: Enable signal for the Analog MUX output, active low. The bit is defined as follows:

1: MUX output is disabled.

0: MUX output is enabled.

nAMUX_WR[6]: Enable signal for Analog MUX address lines, active low. The bit is defined as follows:

1: Addressing is disabled.

0: Addressing is enabled.

The rest of the bits, [15:7], are unused.

AMUX_ADDR[4:0]	Output	Scaling Factor	Error Range
00000	1V2A higher	((val/256)x2.048)/1	0
00001	1V2A lower	((val/256)x2.048)/1	0
00010	1V2-A1 higher	((val/256)x2.048)/1	0
00011	1V2-A1 lower	((val/256)x2.048)/1	0
00100	1V2-B higher	((val/256)x2.048)/1	0
00101	1V2-B lower	((val/256)x2.048)/1	0

00110	1V2-B1 lower	((val/256)x2.048)/1	0
00111	1V2-B1 higher	((val/256)x2.048)/1	0
01000	1V5 lower	((val/256)x2.048)/1	0
01001	1V5 higher	((val/256)x2.048)/1	0
01010	2V5 lower	((val/256)x2.048)/ 0.5	+/- 2%
01011	2V5 higher	((val/256)x2.048)/ 0.5	+/- 2%
01100	3V3 lower	((val/256)x2.048)/ 0.5	+/- 2%
01101	3V3 higher	((val/256)x2.048)/ 0.5	+/- 2%
01110	F1-48V low conn.	-(((val/256)x2.048)-1)/0.01333	+/- 4%
01111	F2-48V up conn.	-(((val/256)x2.048)-1)/0.01333	+/- 4%
10000	V/T[4]	((val/256)x2.048)/0.02	0
10001	V/T[5]	((val/256)x2.048)/0.02	0
10010	1V2-A2 nominal	((val/256)x2.048)/1	0
10011	1V2-A2 higher	((val/256)x2.048)/1	0
10100	1V2-A2 lower	((val/256)x2.048)/1	0
10101	1V2-B2 nominal	((val/256)x2.048)/1	0
10110	1V2-B2 higher	((val/256)x2.048)/1	0
10111	1V2-B2 lower	((val/256)x2.048)/1	0
11000	T input air	((val/256)x2.048)/0.02	0
11001	T output air	((val/256)x2.048)/0.02	0
11010-11110	Unused		
11111	**V**/T[1]	((val/256)x2.048)/1	0

Table 4-7 Analog MUX output selection table

5 Station Board Memory Space

The following table explains the Station Board addressing. To address any chip on the board eight higher PCMC MCB address bits are used.

MCB Address[15:8]	IC on Station Board
0x00	MCB fan-out FPGA - MCB
0x01	Configuration fan-out FPGA - CFG
0x02	Wide Band Correlator FPGA - WBC
0x03	Input FFGA - IC
0x04	Delay Module A FPGA - DMA
0x05	Delay Module B FPGA - DMB
0x06	Timing FPGA - TC
0x07	Output FPGA A – OUTA
0x08	Output FPGA B – OUTB
0x09	VSIA FPGA
0x0a	VSIB FPGA
0x0b	Filter Bank A - Chip 0
0x0c	Filter Bank A - Chip 1
0x0d	Filter Bank A - Chip 2
0x0e	Filter Bank A - Chip 3
0x0f	Filter Bank A - Chip 4
0x10	Filter Bank A - Chip 5
0x11	Filter Bank A - Chip 6
0x12	Filter Bank A - Chip 7

0x13	Filter Bank A - Chip 8
0x14	Filter Bank A - Chip 9
0x15	Filter Bank A - Chip 10
0x16	Filter Bank A - Chip 11
0x17	Filter Bank A - Chip 12
0x18	Filter Bank A - Chip 13
0x19	Filter Bank A - Chip 14
0x1a	Filter Bank A - Chip 15
0x1b	Filter Bank A - Chip 16
0x1c	Filter Bank A - Chip 17
0x1d	Filter Bank B- Chip 0
0x1e	Filter Bank B- Chip 1
0x1f	Filter Bank B- Chip 2
0x20	Filter Bank B- Chip 3
0x21	Filter Bank B- Chip 4
0x22	Filter Bank B- Chip 5
0x23	Filter Bank B- Chip 6
0x24	Filter Bank B- Chip 7
0x25	Filter Bank B- Chip 8
0x26	Filter Bank B- Chip 9
0x27	Filter Bank B- Chip 10
0x28	Filter Bank B- Chip 11
0x29	Filter Bank B- Chip 12

0x2a	Filter Bank B- Chip 13
0x2b	Filter Bank B- Chip 14
0x2c	Filter Bank B- Chip 15
0x2d	Filter Bank B- Chip 16
0x2e	Filter Bank B- Chip 17

Table 5-1 Station Board Memory Map

6 Pinouts, Pin Locations and Programming Notes

6.1 Pinouts by signal name

Note: UNUSED and NC pins have been removed.

```
Release 10.1.03 - par K.39 (nt)
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Tue Mar 02 16:38:16 2010

INPUT FILE:       vsi_top_map.ncd
OUTPUT FILE:      vsi_top_pad.txt
PART TYPE:        xc4vsx35
SPEED GRADE:      -10
PACKAGE:          ff668
```

Pin	Signal Name	Pin Usage	Pin Name	Direction	IO Standard	IO Bank
W2	clk_G01	IOB	IO_L1P_8	INPUT	HSTL_III_DCI	8
R4	clk_G02	IOB	IO_L20P_10	INPUT	HSTL_III_DCI	10
L8	clk_G03	IOB	IO_L9N_CC_LC_10	INPUT	HSTL_III_DCI	10
G10	clk_G04	IOB	IO_L9P_CC_LC_6	INPUT	HSTL_III_DCI	6
C7	clk_G05	IOB	IO_L11N_6	INPUT	HSTL_III_DCI	6
D2	clk_G06	IOB	IO_L25P_CC_LC_6	INPUT	HSTL_III_DCI	6
M8	clk_G07	IOB	IO_L9P_CC_LC_10	INPUT	HSTL_III_DCI	10
R7	clk_G08	IOB	IO_L25N_CC_LC_10	INPUT	HSTL_III_DCI	10
Y1	clk_G09	IOB	IO_L6N_8	INPUT	HSTL_III_DCI	8
Y6	clk_G10	IOB	IO_L9P_CC_LC_8	INPUT	HSTL_III_DCI	8
U4	clk_G11	IOB	IO_L29N_10	INPUT	HSTL_III_DCI	10

M2	clk_G12	IOB	IO_L11P_10	INPUT	HSTL_III_DCI	10
F3	clk_G13	IOB	IO_L27N_6	INPUT	HSTL_III_DCI	6
C10	clk_G14	IOB	IO_L1N_6	INPUT	HSTL_III_DCI	6
D10	clk_G15	IOB	IO_L1P_6	INPUT	HSTL_III_DCI	6
G2	clk_G16	IOB	IO_L30P_6	INPUT	HSTL_III_DCI	6
P7	clk_G17	IOB	IO_L21P_10	INPUT	HSTL_III_DCI	10
U7	clk_G18	IOB	IO_L31N_10	INPUT	HSTL_III_DCI	10
W7	data_G01<0>	IOB	IO_L3P_8	INPUT	HSTL_III_DCI	8
W6	data_G01<1>	IOB	IO_L5P_8	INPUT	HSTL_III_DCI	8
W5	data_G01<2>	IOB	IO_L5N_8	INPUT	HSTL_III_DCI	8
W4	data_G01<3>	IOB	IO_L4P_8	INPUT	HSTL_III_DCI	8
R2	data_G02<0>	IOB	IO_L22P_10	INPUT	HSTL_III_DCI	10
R1	data_G02<1>	IOB	IO_L22N_10	INPUT	HSTL_III_DCI	10
P2	data_G02<2>	IOB	IO_L16N_10	INPUT	HSTL_III_DCI	10
P3	data_G02<3>	IOB	IO_L16P_10	INPUT	HSTL_III_DCI	10
L7	data_G03<0>	IOB	IO_L5P_10	INPUT	HSTL_III_DCI	10
L6	data_G03<1>	IOB	IO_L5N_10	INPUT	HSTL_III_DCI	10
L3	data_G03<2>	IOB	IO_L8N_CC_LC_10	INPUT	HSTL_III_DCI	10
K7	data_G03<3>	IOB	IO_L3P_10	INPUT	HSTL_III_DCI	10
G9	data_G04<0>	IOB	IO_L9N_CC_LC_6	INPUT	HSTL_III_DCI	6
G8	data_G04<1>	IOB	IO_L10N_6	INPUT	HSTL_III_DCI	6
G7	data_G04<2>	IOB	IO_L19N_6	INPUT	HSTL_III_DCI	6
F7	data_G04<3>	IOB	IO_L19P_6	INPUT	HSTL_III_DCI	6
A9	data_G05<0>	IOB	IO_L13P_6	INPUT	HSTL_III_DCI	6
A8	data_G05<1>	IOB	IO_L3P_6	INPUT	HSTL_III_DCI	6
A7	data_G05<2>	IOB	IO_L3N_6	INPUT	HSTL_III_DCI	6
B7	data_G05<3>	IOB	IO_L11P_6	INPUT	HSTL_III_DCI	6
C5	data_G06<0>	IOB	IO_L12P_6	INPUT	HSTL_III_DCI	6
D4	data_G06<1>	IOB	IO_L16N_6	INPUT	HSTL_III_DCI	6
D3	data_G06<2>	IOB	IO_L22P_6	INPUT	HSTL_III_DCI	6
D1	data_G06<3>	IOB	IO_L25N_CC_LC_6	INPUT	HSTL_III_DCI	6
M6	data_G07<0>	IOB	IO_L13P_10	INPUT	HSTL_III_DCI	10
M5	data_G07<1>	IOB	IO_L13N_10	INPUT	HSTL_III_DCI	10
M4	data_G07<2>	IOB	IO_L12P_10	INPUT	HSTL_III_DCI	10

L4	data_G07<3>	IOB	IO_L8P_CC_LC_10	INPUT	HSTL_III_DCI	10
T8	data_G08<0>	IOB	IO_L31P_10	INPUT	HSTL_III_DCI	10
T7	data_G08<1>	IOB	IO_L27P_10	INPUT	HSTL_III_DCI	10
T6	data_G08<2>	IOB	IO_L27N_10	INPUT	HSTL_III_DCI	10
T4	data_G08<3>	IOB	IO_L26P_10	INPUT	HSTL_III_DCI	10
AA4	data_G09<0>	IOB	IO_L7P_8	INPUT	HSTL_III_DCI	8
AA3	data_G09<1>	IOB	IO_L7N_8	INPUT	HSTL_III_DCI	8
Y4	data_G09<2>	IOB	IO_L8P_CC_LC_8	INPUT	HSTL_III_DCI	8
Y3	data_G09<3>	IOB	IO_L8N_CC_LC_8	INPUT	HSTL_III_DCI	8
AA9	data_G10<0>	IOB	IO_L21P_8	INPUT	HSTL_III_DCI	8
Y9	data_G10<1>	IOB	IO_L21N_8	INPUT	HSTL_III_DCI	8
Y8	data_G10<2>	IOB	IO_L26N_8	INPUT	HSTL_III_DCI	8
AA7	data_G10<3>	IOB	IO_L20P_8	INPUT	HSTL_III_DCI	8
V2	data_G11<0>	IOB	IO_L30P_10	INPUT	HSTL_III_DCI	10
V1	data_G11<1>	IOB	IO_L30N_10	INPUT	HSTL_III_DCI	10
U3	data_G11<2>	IOB	IO_L28P_10	INPUT	HSTL_III_DCI	10
U1	data_G11<3>	IOB	IO_L24P_CC_LC_10	INPUT	HSTL_III_DCI	10
N5	data_G12<0>	IOB	IO_L15P_10	INPUT	HSTL_III_DCI	10
N4	data_G12<1>	IOB	IO_L15N_10	INPUT	HSTL_III_DCI	10
N3	data_G12<2>	IOB	IO_L14P_10	INPUT	HSTL_III_DCI	10
N2	data_G12<3>	IOB	IO_L14N_10	INPUT	HSTL_III_DCI	10
F4	data_G13<0>	IOB	IO_L27P_6	INPUT	HSTL_III_DCI	6
E5	data_G13<1>	IOB	IO_L18N_6	INPUT	HSTL_III_DCI	6
E4	data_G13<2>	IOB	IO_L22N_6	INPUT	HSTL_III_DCI	6
E3	data_G13<3>	IOB	IO_L24P_CC_LC_6	INPUT	HSTL_III_DCI	6
D9	data_G14<0>	IOB	IO_L2P_6	INPUT	HSTL_III_DCI	6
D8	data_G14<1>	IOB	IO_L4P_6	INPUT	HSTL_III_DCI	6
D6	data_G14<2>	IOB	IO_L17N_6	INPUT	HSTL_III_DCI	6
E6	data_G14<3>	IOB	IO_L18P_6	INPUT	HSTL_III_DCI	6
F9	data_G15<0>	IOB	IO_L7N_6	INPUT	HSTL_III_DCI	6
E10	data_G15<1>	IOB	IO_L5N_6	INPUT	HSTL_III_DCI	6
E9	data_G15<2>	IOB	IO_L7P_6	INPUT	HSTL_III_DCI	6
E7	data_G15<3>	IOB	IO_L17P_6	INPUT	HSTL_III_DCI	6
G1	data_G16<0>	IOB	IO_L30N_6	INPUT	HSTL_III_DCI	6

F1	data_G16<1>	IOB	IO_L26N_6	INPUT	HSTL_III_DCI	6
E1	data_G16<2>	IOB	IO_L26P_6	INPUT	HSTL_III_DCI	6
H2	data_G16<3>	IOB	IO_L32P_6	INPUT	HSTL_III_DCI	6
P6	data_G17<0>	IOB	IO_L21N_10	INPUT	HSTL_III_DCI	10
P5	data_G17<1>	IOB	IO_L18P_10	INPUT	HSTL_III_DCI	10
N8	data_G17<2>	IOB	IO_L19N_10	INPUT	HSTL_III_DCI	10
N7	data_G17<3>	IOB	IO_L17P_10	INPUT	HSTL_III_DCI	10
V7	data_G18<0>	IOB	IO_L3N_8	INPUT	HSTL_III_DCI	8
V6	data_G18<1>	IOB	IO_L2P_8	INPUT	HSTL_III_DCI	8
V5	data_G18<2>	IOB	IO_L2N_8	INPUT	HSTL_III_DCI	8
V4	data_G18<3>	IOB	IO_L29P_10	INPUT	HSTL_III_DCI	10
AA13	mcb_addr_p<0>	IOB	IO_L4N_D8_VREF_LC_2	INPUT	LVCMOS25	2
AB13	mcb_addr_p<1>	IOB	IO_L4P_D9_LC_2	INPUT	LVCMOS25	2
AA15	mcb_addr_p<2>	IOB	IO_L3N_D10_LC_2	INPUT	LVCMOS25	2
AA16	mcb_addr_p<3>	IOB	IO_L3P_D11_LC_2	INPUT	LVCMOS25	2
AC11	mcb_addr_p<4>	IOB	IO_L2N_D12_LC_2	INPUT	LVCMOS25	2
AC12	mcb_addr_p<5>	IOB	IO_L2P_D13_LC_2	INPUT	LVCMOS25	2
AB14	mcb_addr_p<6>	IOB	IO_L1N_D14_CC_LC_2	INPUT	LVCMOS25	2
AA14	mcb_addr_p<7>	IOB	IO_L1P_D15_CC_LC_2	INPUT	LVCMOS25	2
AE14	mcb_clk_p	IOB	IO_L5P_GC_LC_4	INPUT	LVCMOS25	4
AE12	mcb_cs_p	IOB	IO_L1N_GC_LC_4	INPUT	LVCMOS25	4
D12	mcb_data_p<0>	IOB	IO_L8N_D16_CC_LC_1	BIDIR	LVCMOS25	1
E13	mcb_data_p<1>	IOB	IO_L8P_D17_CC_LC_1	BIDIR	LVCMOS25	1
F15	mcb_data_p<10>	IOB	IO_L3N_D26_LC_1	BIDIR	LVCMOS25	1
F16	mcb_data_p<11>	IOB	IO_L3P_D27_LC_1	BIDIR	LVCMOS25	1
F11	mcb_data_p<12>	IOB	IO_L2N_D28_LC_1	BIDIR	LVCMOS25	1
F12	mcb_data_p<13>	IOB	IO_L2P_D29_LC_1	BIDIR	LVCMOS25	1
F13	mcb_data_p<14>	IOB	IO_L1N_D30_LC_1	BIDIR	LVCMOS25	1
F14	mcb_data_p<15>	IOB	IO_L1P_D31_LC_1	BIDIR	LVCMOS25	1
C16	mcb_data_p<2>	IOB	IO_L7N_D18_LC_1	BIDIR	LVCMOS25	1
D16	mcb_data_p<3>	IOB	IO_L7P_D19_LC_1	BIDIR	LVCMOS25	1
D11	mcb_data_p<4>	IOB	IO_L6N_D20_LC_1	BIDIR	LVCMOS25	1
C11	mcb_data_p<5>	IOB	IO_L6P_D21_LC_1	BIDIR	LVCMOS25	1
E14	mcb_data_p<6>	IOB	IO_L5N_D22_LC_1	BIDIR	LVCMOS25	1

D15	mcb_data_p<7>	IOB	IO_L5P_D23_LC_1	BIDIR	LVCMOS25	1
D13	mcb_data_p<8>	IOB	IO_L4N_D24_VREF_LC_1	BIDIR	LVCMOS25	1
D14	mcb_data_p<9>	IOB	IO_L4P_D25_LC_1	BIDIR	LVCMOS25	1
AF12	mcb_rw_p	IOB	IO_L1P_GC_LC_4	INPUT	LVCMOS25	4
Y10	odata_100PPS	IOB	IO_L27P_8	OUTPUT	HSTL_III_DCI	8
AD2	odata_clk	IOB	IO_L16P_8	OUTPUT	HSTL_III_DCI	8
AB9	odata_PPS	IOB	IO_L29N_8	OUTPUT	HSTL_III_DCI	8
AF3	odata_val	IOB	IO_L15P_8	OUTPUT	HSTL_III_DCI	8
AA8	odata<0>	IOB	IO_L26P_8	OUTPUT	HSTL_III_DCI	8
AB6	odata<1>	IOB	IO_L24N_CC_LC_8	OUTPUT	HSTL_III_DCI	8
AC4	odata<10>	IOB	IO_L11P_8	OUTPUT	HSTL_III_DCI	8
AC3	odata<11>	IOB	IO_L18N_8	OUTPUT	HSTL_III_DCI	8
AB1	odata<12>	IOB	IO_L10P_8	OUTPUT	HSTL_III_DCI	8
AE9	odata<13>	IOB	IO_L31N_8	OUTPUT	HSTL_III_DCI	8
AC6	odata<14>	IOB	IO_L24P_CC_LC_8	OUTPUT	HSTL_III_DCI	8
AC5	odata<15>	IOB	IO_L13P_8	OUTPUT	HSTL_III_DCI	8
AD4	odata<16>	IOB	IO_L22N_8	OUTPUT	HSTL_III_DCI	8
AD3	odata<17>	IOB	IO_L18P_8	OUTPUT	HSTL_III_DCI	8
AC1	odata<18>	IOB	IO_L14N_8	OUTPUT	HSTL_III_DCI	8
AF9	odata<19>	IOB	IO_L31P_8	OUTPUT	HSTL_III_DCI	8
AB5	odata<2>	IOB	IO_L13N_8	OUTPUT	HSTL_III_DCI	8
AD8	odata<20>	IOB	IO_L32P_8	OUTPUT	HSTL_III_DCI	8
AF7	odata<21>	IOB	IO_L25N_CC_LC_8	OUTPUT	HSTL_III_DCI	8
AE6	odata<22>	IOB	IO_L30P_8	OUTPUT	HSTL_III_DCI	8
AD5	odata<23>	IOB	IO_L22P_8	OUTPUT	HSTL_III_DCI	8
AE4	odata<24>	IOB	IO_L17N_8	OUTPUT	HSTL_III_DCI	8
AE3	odata<25>	IOB	IO_L15N_8	OUTPUT	HSTL_III_DCI	8
AC2	odata<26>	IOB	IO_L14P_8	OUTPUT	HSTL_III_DCI	8
AD1	odata<27>	IOB	IO_L16N_8	OUTPUT	HSTL_III_DCI	8
AF8	odata<28>	IOB	IO_L25P_CC_LC_8	OUTPUT	HSTL_III_DCI	8
AF6	odata<29>	IOB	IO_L19P_8	OUTPUT	HSTL_III_DCI	8
AB4	odata<3>	IOB	IO_L11N_8	OUTPUT	HSTL_III_DCI	8
AF5	odata<30>	IOB	IO_L19N_8	OUTPUT	HSTL_III_DCI	8
AF4	odata<31>	IOB	IO_L17P_8	OUTPUT	HSTL_III_DCI	8

AB3	odata<4>	IOB	IO_L12P_8	OUTPUT	HSTL_III_DCI	8
AA1	odata<5>	IOB	IO_L10N_8	OUTPUT	HSTL_III_DCI	8
AA10	odata<6>	IOB	IO_L27N_8	OUTPUT	HSTL_III_DCI	8
AC9	odata<7>	IOB	IO_L29P_8	OUTPUT	HSTL_III_DCI	8
AC8	odata<8>	IOB	IO_L32N_8	OUTPUT	HSTL_III_DCI	8
AC7	odata<9>	IOB	IO_L28P_8	OUTPUT	HSTL_III_DCI	8
B10	reset_N	IOB	IO_L6N_GC_LC_3	INPUT	LVCMOS25	3
C14	sclk_128_N	LOWCAPIOB	IO_L3N_GC_LC_3	INPUT	LVDS_25	3
C15	sclk_128_P	LOWCAPIOB	IO_L3P_GC_LC_3	INPUT	LVDS_25	3
B14	sys_100PPS_N	IOB	IO_L1N_GC_CC_LC_3	INPUT	LVDS_25	3
B15	sys_100PPS_P	IOB	IO_L1P_GC_CC_LC_3	INPUT	LVDS_25	3
A15	sys_PPS_N	IOB	IO_L5N_GC_LC_3	INPUT	LVDS_25	3
A16	sys_PPS_P	IOB	IO_L5P_GC_LC_3	INPUT	LVDS_25	3
AD26	TC_N<0>	IOBS	IO_L11N_7	OUTPUT	LVDS_25	7
T20	TC_N<1>	IOBS	IO_L30N_9	OUTPUT	LVDS_25	9
AD25	TC_P<0>	IOBM	IO_L11P_7	OUTPUT	LVDS_25	7
T21	TC_P<1>	IOBM	IO_L30P_9	OUTPUT	LVDS_25	9
AF11	test_port<0>	IOB	IO_L4P_GC_LC_4	OUTPUT	LVCMOS25	4
AC17	test_port<1>	IOB	IO_L3N_GC_LC_4	OUTPUT	LVCMOS25	4
AB17	test_port<2>	IOB	IO_L3P_GC_LC_4	OUTPUT	LVCMOS25	4
AB10	test_port<3>	IOB	IO_L2N_GC_LC_4	OUTPUT	LVCMOS25	4
W1	tick_G01	IOB	IO_L1N_8	INPUT	HSTL_III_DCI	8
P4	tick_G02	IOB	IO_L18N_10	INPUT	HSTL_III_DCI	10
K6	tick_G03	IOB	IO_L3N_10	INPUT	HSTL_III_DCI	10
F8	tick_G04	IOB	IO_L10P_6	INPUT	HSTL_III_DCI	6
B9	tick_G05	IOB	IO_L13N_6	INPUT	HSTL_III_DCI	6
C6	tick_G06	IOB	IO_L8N_CC_LC_6	INPUT	HSTL_III_DCI	6
M7	tick_G07	IOB	IO_L17N_10	INPUT	HSTL_III_DCI	10
R8	tick_G08	IOB	IO_L25P_CC_LC_10	INPUT	HSTL_III_DCI	10
Y2	tick_G09	IOB	IO_L6P_8	INPUT	HSTL_III_DCI	8
Y5	tick_G10	IOB	IO_L9N_CC_LC_8	INPUT	HSTL_III_DCI	8
U5	tick_G11	IOB	IO_L32N_10	INPUT	HSTL_III_DCI	10
M1	tick_G12	IOB	IO_L11N_10	INPUT	HSTL_III_DCI	10
G4	tick_G13	IOB	IO_L28P_6	INPUT	HSTL_III_DCI	6

C8	tick_G14	IOB	IO_L2N_6	INPUT	HSTL_III_DCI	6
F10	tick_G15	IOB	IO_L5P_6	INPUT	HSTL_III_DCI	6
H1	tick_G16	IOB	IO_L32N_6	INPUT	HSTL_III_DCI	6
P8	tick_G17	IOB	IO_L19P_10	INPUT	HSTL_III_DCI	10
U6	tick_G18	IOB	IO_L32P_10	INPUT	HSTL_III_DCI	10
M24	VSI_in_N<0>	IOB	IO_L11N_9	INPUT	LVDS_25	9
N24	VSI_in_N<1>	IOB	IO_L15N_9	INPUT	LVDS_25	9
U21	VSI_in_N<10>	IOB	IO_L29N_9	INPUT	LVDS_25	9
T19	VSI_in_N<11>	IOB	IO_L31N_9	INPUT	LVDS_25	9
U24	VSI_in_N<12>	IOB	IO_L28N_VREF_9	INPUT	LVDS_25	9
V25	VSI_in_N<13>	IOB	IO_L32N_9	INPUT	LVDS_25	9
V23	VSI_in_N<14>	IOB	IO_L27N_9	INPUT	LVDS_25	9
V20	VSI_in_N<15>	IOB	IO_L5N_7	INPUT	LVDS_25	7
W26	VSI_in_N<16>	IOB	IO_L2N_7	INPUT	LVDS_25	7
W24	VSI_in_N<17>	IOB	IO_L4N_VREF_7	INPUT	LVDS_25	7
W22	VSI_in_N<18>	IOB	IO_L3N_7	INPUT	LVDS_25	7
Y26	VSI_in_N<19>	IOB	IO_L6N_7	INPUT	LVDS_25	7
N22	VSI_in_N<2>	IOB	IO_L16N_9	INPUT	LVDS_25	9
Y24	VSI_in_N<20>	IOB	IO_L8N_CC_LC_7	INPUT	LVDS_25	7
Y23	VSI_in_N<21>	IOB	IO_L12N_VREF_7	INPUT	LVDS_25	7
Y21	VSI_in_N<22>	IOB	IO_L20N_VREF_7	INPUT	LVDS_25	7
AA26	VSI_in_N<23>	IOB	IO_L10N_7	INPUT	LVDS_25	7
AB25	VSI_in_N<24>	IOB	IO_L7N_7	INPUT	LVDS_25	7
AA23	VSI_in_N<25>	IOB	IO_L14N_7	INPUT	LVDS_25	7
AC26	VSI_in_N<26>	IOB	IO_L9N_CC_LC_7	INPUT	LVDS_25	7
AC24	VSI_in_N<27>	IOB	IO_L16N_7	INPUT	LVDS_25	7
AE24	VSI_in_N<28>	IOB	IO_L22N_7	INPUT	LVDS_25	7
AE23	VSI_in_N<29>	IOB	IO_L19N_7	INPUT	LVDS_25	7
P24	VSI_in_N<3>	IOB	IO_L18N_9	INPUT	LVDS_25	9
AB22	VSI_in_N<30>	IOB	IO_L13N_7	INPUT	LVDS_25	7
AB21	VSI_in_N<31>	IOB	IO_L24N_CC_LC_7	INPUT	LVDS_25	7
AD21	VSI_in_N<32>	IOB	IO_L32N_SM1_7	INPUT	LVDS_25	7
AF22	VSI_in_N<33>	IOB	IO_L30N_SM3_7	INPUT	LVDS_25	7
AC20	VSI_in_N<34>	IOB	IO_L28N_VREF_7	INPUT	LVDS_25	7

W19	VSI_in_N<35>	IOB	IO_L18N_7	INPUT	LVDS_25	7
AF20	VSI_in_N<36>	IOB	IO_L17N_7	INPUT	LVDS_25	7
AC19	VSI_in_N<37>	IOB	IO_L25N_CC_SM7_LC_7	INPUT	LVDS_25	7
AE18	VSI_in_N<38>	IOB	IO_L31N_SM2_7	INPUT	LVDS_25	7
AB18	VSI_in_N<39>	IOB	IO_L29N_SM4_7	INPUT	LVDS_25	7
P22	VSI_in_N<4>	IOB	IO_L19N_9	INPUT	LVDS_25	9
R25	VSI_in_N<5>	IOB	IO_L20N_VREF_9	INPUT	LVDS_25	9
U26	VSI_in_N<6>	IOB	IO_L26N_9	INPUT	LVDS_25	9
R23	VSI_in_N<7>	IOB	IO_L22N_9	INPUT	LVDS_25	9
P19	VSI_in_N<8>	IOB	IO_L21N_9	INPUT	LVDS_25	9
T23	VSI_in_N<9>	IOB	IO_L24N_CC_LC_9	INPUT	LVDS_25	9
M25	VSI_in_P<0>	IOB	IO_L11P_9	INPUT	LVDS_25	9
N25	VSI_in_P<1>	IOB	IO_L15P_9	INPUT	LVDS_25	9
U22	VSI_in_P<10>	IOB	IO_L29P_9	INPUT	LVDS_25	9
U20	VSI_in_P<11>	IOB	IO_L31P_9	INPUT	LVDS_25	9
U25	VSI_in_P<12>	IOB	IO_L28P_9	INPUT	LVDS_25	9
V26	VSI_in_P<13>	IOB	IO_L32P_9	INPUT	LVDS_25	9
U23	VSI_in_P<14>	IOB	IO_L27P_9	INPUT	LVDS_25	9
W20	VSI_in_P<15>	IOB	IO_L5P_7	INPUT	LVDS_25	7
W25	VSI_in_P<16>	IOB	IO_L2P_7	INPUT	LVDS_25	7
W23	VSI_in_P<17>	IOB	IO_L4P_7	INPUT	LVDS_25	7
W21	VSI_in_P<18>	IOB	IO_L3P_7	INPUT	LVDS_25	7
Y25	VSI_in_P<19>	IOB	IO_L6P_7	INPUT	LVDS_25	7
N23	VSI_in_P<2>	IOB	IO_L16P_9	INPUT	LVDS_25	9
AA24	VSI_in_P<20>	IOB	IO_L8P_CC_LC_7	INPUT	LVDS_25	7
Y22	VSI_in_P<21>	IOB	IO_L12P_7	INPUT	LVDS_25	7
Y20	VSI_in_P<22>	IOB	IO_L20P_7	INPUT	LVDS_25	7
AB26	VSI_in_P<23>	IOB	IO_L10P_7	INPUT	LVDS_25	7
AB24	VSI_in_P<24>	IOB	IO_L7P_7	INPUT	LVDS_25	7
AB23	VSI_in_P<25>	IOB	IO_L14P_7	INPUT	LVDS_25	7
AC25	VSI_in_P<26>	IOB	IO_L9P_CC_LC_7	INPUT	LVDS_25	7
AC23	VSI_in_P<27>	IOB	IO_L16P_7	INPUT	LVDS_25	7
AF24	VSI_in_P<28>	IOB	IO_L22P_7	INPUT	LVDS_25	7
AF23	VSI_in_P<29>	IOB	IO_L19P_7	INPUT	LVDS_25	7

P25	VSI_in_P<3>	IOB	IO_L18P_9	INPUT	LVDS_25	9
AC22	VSI_in_P<30>	IOB	IO_L13P_7	INPUT	LVDS_25	7
AC21	VSI_in_P<31>	IOB	IO_L24P_CC_LC_7	INPUT	LVDS_25	7
AE21	VSI_in_P<32>	IOB	IO_L32P_SM1_7	INPUT	LVDS_25	7
AF21	VSI_in_P<33>	IOB	IO_L30P_SM3_7	INPUT	LVDS_25	7
AB20	VSI_in_P<34>	IOB	IO_L28P_7	INPUT	LVDS_25	7
Y19	VSI_in_P<35>	IOB	IO_L18P_7	INPUT	LVDS_25	7
AF19	VSI_in_P<36>	IOB	IO_L17P_7	INPUT	LVDS_25	7
AD19	VSI_in_P<37>	IOB	IO_L25P_CC_SM7_LC_7	INPUT	LVDS_25	7
AF18	VSI_in_P<38>	IOB	IO_L31P_SM2_7	INPUT	LVDS_25	7
AC18	VSI_in_P<39>	IOB	IO_L29P_SM4_7	INPUT	LVDS_25	7
P23	VSI_in_P<4>	IOB	IO_L19P_9	INPUT	LVDS_25	9
R26	VSI_in_P<5>	IOB	IO_L20P_9	INPUT	LVDS_25	9
T26	VSI_in_P<6>	IOB	IO_L26P_9	INPUT	LVDS_25	9
R24	VSI_in_P<7>	IOB	IO_L22P_9	INPUT	LVDS_25	9
P20	VSI_in_P<8>	IOB	IO_L21P_9	INPUT	LVDS_25	9
T24	VSI_in_P<9>	IOB	IO_L24P_CC_LC_9	INPUT	LVDS_25	9
L20	VSI_out_N<0>	IOBS	IO_L6N_9	OUTPUT	LVDS_25	9
D17	VSI_out_N<1>	IOBS	IO_L1N_5	OUTPUT	LVDS_25	5
D19	VSI_out_N<10>	IOBS	IO_L4N_VREF_5	OUTPUT	LVDS_25	5
E20	VSI_out_N<11>	IOBS	IO_L19N_5	OUTPUT	LVDS_25	5
G20	VSI_out_N<12>	IOBS	IO_L22N_5	OUTPUT	LVDS_25	5
C22	VSI_out_N<13>	IOBS	IO_L14N_5	OUTPUT	LVDS_25	5
B21	VSI_out_N<14>	IOBS	IO_L6N_5	OUTPUT	LVDS_25	5
E18	VSI_out_N<15>	IOBS	IO_L11N_5	OUTPUT	LVDS_25	5
G21	VSI_out_N<16>	IOBS	IO_L23N_VRP_5	OUTPUT	LVDS_25	5
H25	VSI_out_N<17>	IOBS	IO_L32N_5	OUTPUT	LVDS_25	5
C23	VSI_out_N<18>	IOBS	IO_L21N_5	OUTPUT	LVDS_25	5
A19	VSI_out_N<19>	IOBS	IO_L13N_5	OUTPUT	LVDS_25	5
F17	VSI_out_N<2>	IOBS	IO_L5N_5	OUTPUT	LVDS_25	5
M20	VSI_out_N<20>	IOBS	IO_L13N_9	OUTPUT	LVDS_25	9
E22	VSI_out_N<21>	IOBS	IO_L18N_5	OUTPUT	LVDS_25	5
A21	VSI_out_N<22>	IOBS	IO_L15N_5	OUTPUT	LVDS_25	5
E24	VSI_out_N<23>	IOBS	IO_L27N_5	OUTPUT	LVDS_25	5

H21	VSI_out_N<24>	IOBS	IO_L26N_5	OUTPUT	LVDS_25	5
C25	VSI_out_N<25>	IOBS	IO_L20N_VREF_5	OUTPUT	LVDS_25	5
G23	VSI_out_N<26>	IOBS	IO_L28N_VREF_5	OUTPUT	LVDS_25	5
H23	VSI_out_N<27>	IOBS	IO_L30N_5	OUTPUT	LVDS_25	5
C24	VSI_out_N<28>	IOBS	IO_L16N_5	OUTPUT	LVDS_25	5
E26	VSI_out_N<29>	IOBS	IO_L29N_5	OUTPUT	LVDS_25	5
N20	VSI_out_N<3>	IOBS	IO_L17N_9	OUTPUT	LVDS_25	9
J22	VSI_out_N<30>	IOBS	IO_L2N_9	OUTPUT	LVDS_25	9
G25	VSI_out_N<31>	IOBS	IO_L31N_5	OUTPUT	LVDS_25	5
J25	VSI_out_N<32>	IOBS	IO_L4N_VREF_9	OUTPUT	LVDS_25	9
J20	VSI_out_N<33>	IOBS	IO_L1N_9	OUTPUT	LVDS_25	9
K21	VSI_out_N<34>	IOBS	IO_L3N_9	OUTPUT	LVDS_25	9
K20	VSI_out_N<35>	IOBS	IO_L5N_9	OUTPUT	LVDS_25	9
L23	VSI_out_N<36>	IOBS	IO_L10N_9	OUTPUT	LVDS_25	9
M26	VSI_out_N<37>	IOBS	IO_L12N_VREF_9	OUTPUT	LVDS_25	9
M22	VSI_out_N<38>	IOBS	IO_L14N_9	OUTPUT	LVDS_25	9
K23	VSI_out_N<39>	IOBS	IO_L7N_9	OUTPUT	LVDS_25	9
A18	VSI_out_N<4>	IOBS	IO_L3N_5	OUTPUT	LVDS_25	5
D18	VSI_out_N<5>	IOBS	IO_L7N_5	OUTPUT	LVDS_25	5
B23	VSI_out_N<6>	IOBS	IO_L10N_5	OUTPUT	LVDS_25	5
F19	VSI_out_N<7>	IOBS	IO_L17N_5	OUTPUT	LVDS_25	5
D21	VSI_out_N<8>	IOBS	IO_L12N_VREF_5	OUTPUT	LVDS_25	5
B20	VSI_out_N<9>	IOBS	IO_L2N_5	OUTPUT	LVDS_25	5
L21	VSI_out_P<0>	IOBM	IO_L6P_9	OUTPUT	LVDS_25	9
C17	VSI_out_P<1>	IOBM	IO_L1P_5	OUTPUT	LVDS_25	5
D20	VSI_out_P<10>	IOBM	IO_L4P_5	OUTPUT	LVDS_25	5
F20	VSI_out_P<11>	IOBM	IO_L19P_5	OUTPUT	LVDS_25	5
H20	VSI_out_P<12>	IOBM	IO_L22P_5	OUTPUT	LVDS_25	5
D22	VSI_out_P<13>	IOBM	IO_L14P_5	OUTPUT	LVDS_25	5
C21	VSI_out_P<14>	IOBM	IO_L6P_5	OUTPUT	LVDS_25	5
F18	VSI_out_P<15>	IOBM	IO_L11P_5	OUTPUT	LVDS_25	5
G22	VSI_out_P<16>	IOBM	IO_L23P_VRN_5	OUTPUT	LVDS_25	5
H26	VSI_out_P<17>	IOBM	IO_L32P_5	OUTPUT	LVDS_25	5
D23	VSI_out_P<18>	IOBM	IO_L21P_5	OUTPUT	LVDS_25	5

A20	VSI_out_P<19>	IOBM	IO_L13P_5	OUTPUT	LVDS_25	5
E17	VSI_out_P<2>	IOBM	IO_L5P_5	OUTPUT	LVDS_25	5
M21	VSI_out_P<20>	IOBM	IO_L13P_9	OUTPUT	LVDS_25	9
E23	VSI_out_P<21>	IOBM	IO_L18P_5	OUTPUT	LVDS_25	5
A22	VSI_out_P<22>	IOBM	IO_L15P_5	OUTPUT	LVDS_25	5
E25	VSI_out_P<23>	IOBM	IO_L27P_5	OUTPUT	LVDS_25	5
H22	VSI_out_P<24>	IOBM	IO_L26P_5	OUTPUT	LVDS_25	5
C26	VSI_out_P<25>	IOBM	IO_L20P_5	OUTPUT	LVDS_25	5
G24	VSI_out_P<26>	IOBM	IO_L28P_5	OUTPUT	LVDS_25	5
H24	VSI_out_P<27>	IOBM	IO_L30P_5	OUTPUT	LVDS_25	5
D24	VSI_out_P<28>	IOBM	IO_L16P_5	OUTPUT	LVDS_25	5
F26	VSI_out_P<29>	IOBM	IO_L29P_5	OUTPUT	LVDS_25	5
N21	VSI_out_P<3>	IOBM	IO_L17P_9	OUTPUT	LVDS_25	9
J23	VSI_out_P<30>	IOBM	IO_L2P_9	OUTPUT	LVDS_25	9
G26	VSI_out_P<31>	IOBM	IO_L31P_5	OUTPUT	LVDS_25	5
J26	VSI_out_P<32>	IOBM	IO_L4P_9	OUTPUT	LVDS_25	9
J21	VSI_out_P<33>	IOBM	IO_L1P_9	OUTPUT	LVDS_25	9
K22	VSI_out_P<34>	IOBM	IO_L3P_9	OUTPUT	LVDS_25	9
L19	VSI_out_P<35>	IOBM	IO_L5P_9	OUTPUT	LVDS_25	9
L24	VSI_out_P<36>	IOBM	IO_L10P_9	OUTPUT	LVDS_25	9
L26	VSI_out_P<37>	IOBM	IO_L12P_9	OUTPUT	LVDS_25	9
M23	VSI_out_P<38>	IOBM	IO_L14P_9	OUTPUT	LVDS_25	9
K24	VSI_out_P<39>	IOBM	IO_L7P_9	OUTPUT	LVDS_25	9
B18	VSI_out_P<4>	IOBM	IO_L3P_5	OUTPUT	LVDS_25	5
C19	VSI_out_P<5>	IOBM	IO_L7P_5	OUTPUT	LVDS_25	5
B24	VSI_out_P<6>	IOBM	IO_L10P_5	OUTPUT	LVDS_25	5
G19	VSI_out_P<7>	IOBM	IO_L17P_5	OUTPUT	LVDS_25	5
E21	VSI_out_P<8>	IOBM	IO_L12P_5	OUTPUT	LVDS_25	5
C20	VSI_out_P<9>	IOBM	IO_L2P_5	OUTPUT	LVDS_25	5

Table 6-1 Pinout by Signal Name

6.2 Pinouts by pin number

Note: UNUSED and NC pins have been removed.

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Release 10.1.03 - par K.39 (nt)
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Tue Mar 02 16:38:16 2010

INPUT FILE:       vsi_top_map.ncd
OUTPUT FILE:      vsi_top_pad.txt
PART TYPE:        xc4vsx35
SPEED GRADE:      -10
PACKAGE:          ff668
```

Pin	Signal Name	Pin Usage	Pin Name	Direction	IO Standard	IO Bank
A13			GND			
A14			GND			
A15	sys_PPS_N	IOB	IO_L5N_GC_LC_3	INPUT	LVDS_25	3
A16	sys_PPS_P	IOB	IO_L5P_GC_LC_3	INPUT	LVDS_25	3
A18	VSI_out_N<4>	IOBS	IO_L3N_5	OUTPUT	LVDS_25	5
A19	VSI_out_N<19>	IOBS	IO_L13N_5	OUTPUT	LVDS_25	5
A2			GND			
A20	VSI_out_P<19>	IOBM	IO_L13P_5	OUTPUT	LVDS_25	5
A21	VSI_out_N<22>	IOBS	IO_L15N_5	OUTPUT	LVDS_25	5
A22	VSI_out_P<22>	IOBM	IO_L15P_5	OUTPUT	LVDS_25	5
A25			GND			
A7	data_G05<2>	IOB	IO_L3N_6	INPUT	HSTL_III_DCI	6
A8	data_G05<1>	IOB	IO_L3P_6	INPUT	HSTL_III_DCI	6
A9	data_G05<0>	IOB	IO_L13P_6	INPUT	HSTL_III_DCI	6

AA1	odata<5>	IOB	IO_L10N_8	OUTPUT	HSTL_III_DCI	8
AA10	odata<6>	IOB	IO_L27N_8	OUTPUT	HSTL_III_DCI	8
AA13	mcb_addr_p<0>	IOB	IO_L4N_D8_VREF_LC_2	INPUT	LVCMOS25	2
AA14	mcb_addr_p<7>	IOB	IO_L1P_D15_CC_LC_2	INPUT	LVCMOS25	2
AA15	mcb_addr_p<2>	IOB	IO_L3N_D10_LC_2	INPUT	LVCMOS25	2
AA16	mcb_addr_p<3>	IOB	IO_L3P_D11_LC_2	INPUT	LVCMOS25	2
AA2			VCCO_8			8
AA21			GND			
AA22			VCCO_7			7
AA23	VSI_in_N<25>	IOB	IO_L14N_7	INPUT	LVDS_25	7
AA24	VSI_in_P<20>	IOB	IO_L8P_CC_LC_7	INPUT	LVDS_25	7
AA25			VCCO_7			7
AA26	VSI_in_N<23>	IOB	IO_L10N_7	INPUT	LVDS_25	7
AA3	data_G09<1>	IOB	IO_L7N_8	INPUT	HSTL_III_DCI	8
AA4	data_G09<0>	IOB	IO_L7P_8	INPUT	HSTL_III_DCI	8
AA5			VCCO_8			8
AA6			GND			
AA7	data_G10<3>	IOB	IO_L20P_8	INPUT	HSTL_III_DCI	8
AA8	odata<0>	IOB	IO_L26P_8	OUTPUT	HSTL_III_DCI	8
AA9	data_G10<0>	IOB	IO_L21P_8	INPUT	HSTL_III_DCI	8
AB1	odata<12>	IOB	IO_L10P_8	OUTPUT	HSTL_III_DCI	8
AB10	test_port<3>	IOB	IO_L2N_GC_LC_4	OUTPUT	LVCMOS25	4
AB11			VCCO_2			2
AB12			GND			
AB13	mcb_addr_p<1>	IOB	IO_L4P_D9_LC_2	INPUT	LVCMOS25	2
AB14	mcb_addr_p<6>	IOB	IO_L1N_D14_CC_LC_2	INPUT	LVCMOS25	2
AB15			GND			
AB16			VCCO_2			2
AB17	test_port<2>	IOB	IO_L3P_GC_LC_4	OUTPUT	LVCMOS25	4
AB18	VSI_in_N<39>	IOB	IO_L29N_SM4_7	INPUT	LVDS_25	7
AB19			VCCO_7			7
AB20	VSI_in_P<34>	IOB	IO_L28P_7	INPUT	LVDS_25	7
AB21	VSI_in_N<31>	IOB	IO_L24N_CC_LC_7	INPUT	LVDS_25	7
AB22	VSI_in_N<30>	IOB	IO_L13N_7	INPUT	LVDS_25	7

AB23	VSI_in_P<25>	IOB	IO_L14P_7	INPUT	LVDS_25	7
AB24	VSI_in_P<24>	IOB	IO_L7P_7	INPUT	LVDS_25	7
AB25	VSI_in_N<24>	IOB	IO_L7N_7	INPUT	LVDS_25	7
AB26	VSI_in_P<23>	IOB	IO_L10P_7	INPUT	LVDS_25	7
AB3	odata<4>	IOB	IO_L12P_8	OUTPUT	HSTL_III_DCI	8
AB4	odata<3>	IOB	IO_L11N_8	OUTPUT	HSTL_III_DCI	8
AB5	odata<2>	IOB	IO_L13N_8	OUTPUT	HSTL_III_DCI	8
AB6	odata<1>	IOB	IO_L24N_CC_LC_8	OUTPUT	HSTL_III_DCI	8
AB8			VCCO_8			8
AB9	odata_PPS	IOB	IO_L29N_8	OUTPUT	HSTL_III_DCI	8
AC1	odata<18>	IOB	IO_L14N_8	OUTPUT	HSTL_III_DCI	8
AC11	mcb_addr_p<4>	IOB	IO_L2N_D12_LC_2	INPUT	LVCMOS25	2
AC12	mcb_addr_p<5>	IOB	IO_L2P_D13_LC_2	INPUT	LVCMOS25	2
AC17	test_port<1>	IOB	IO_L3N_GC_LC_4	OUTPUT	LVCMOS25	4
AC18	VSI_in_P<39>	IOB	IO_L29P_SM4_7	INPUT	LVDS_25	7
AC19	VSI_in_N<37>	IOB	IO_L25N_CC_SM7_LC_7	INPUT	LVDS_25	7
AC2	odata<26>	IOB	IO_L14P_8	OUTPUT	HSTL_III_DCI	8
AC20	VSI_in_N<34>	IOB	IO_L28N_VREF_7	INPUT	LVDS_25	7
AC21	VSI_in_P<31>	IOB	IO_L24P_CC_LC_7	INPUT	LVDS_25	7
AC22	VSI_in_P<30>	IOB	IO_L13P_7	INPUT	LVDS_25	7
AC23	VSI_in_P<27>	IOB	IO_L16P_7	INPUT	LVDS_25	7
AC24	VSI_in_N<27>	IOB	IO_L16N_7	INPUT	LVDS_25	7
AC25	VSI_in_P<26>	IOB	IO_L9P_CC_LC_7	INPUT	LVDS_25	7
AC26	VSI_in_N<26>	IOB	IO_L9N_CC_LC_7	INPUT	LVDS_25	7
AC3	odata<11>	IOB	IO_L18N_8	OUTPUT	HSTL_III_DCI	8
AC4	odata<10>	IOB	IO_L11P_8	OUTPUT	HSTL_III_DCI	8
AC5	odata<15>	IOB	IO_L13P_8	OUTPUT	HSTL_III_DCI	8
AC6	odata<14>	IOB	IO_L24P_CC_LC_8	OUTPUT	HSTL_III_DCI	8
AC7	odata<9>	IOB	IO_L28P_8	OUTPUT	HSTL_III_DCI	8
AC8	odata<8>	IOB	IO_L32N_8	OUTPUT	HSTL_III_DCI	8
AC9	odata<7>	IOB	IO_L29P_8	OUTPUT	HSTL_III_DCI	8
AD1	odata<27>	IOB	IO_L16N_8	OUTPUT	HSTL_III_DCI	8
AD15			VCCO_4			4
AD18			GND			

AD19	VSI_in_P<37>	IOB	IO_L25P_CC_SM7_LC_7	INPUT	LVDS_25	7
AD2	odata_clk	IOB	IO_L16P_8	OUTPUT	HSTL_III_DCI	8
AD21	VSI_in_N<32>	IOB	IO_L32N_SM1_7	INPUT	LVDS_25	7
AD24			GND			
AD25	TC_P<0>	IOBM	IO_L11P_7	OUTPUT	LVDS_25	7
AD26	TC_N<0>	IOBS	IO_L11N_7	OUTPUT	LVDS_25	7
AD3	odata<17>	IOB	IO_L18P_8	OUTPUT	HSTL_III_DCI	8
AD4	odata<16>	IOB	IO_L22N_8	OUTPUT	HSTL_III_DCI	8
AD5	odata<23>	IOB	IO_L22P_8	OUTPUT	HSTL_III_DCI	8
AD8	odata<20>	IOB	IO_L32P_8	OUTPUT	HSTL_III_DCI	8
AD9			GND			
AE1			GND			
AE11			VCCO_4			4
AE12	mcb_cs_p	IOB	IO_L1N_GC_LC_4	INPUT	LVCMOS25	4
AE14	mcb_clk_p	IOB	IO_L5P_GC_LC_4	INPUT	LVCMOS25	4
AE15			VREFN_SM			
AE16			VREFP_SM			
AE17			AVSS_SM			
AE18	VSI_in_N<38>	IOB	IO_L31N_SM2_7	INPUT	LVDS_25	7
AE19			VCCO_7			7
AE2			GND			
AE21	VSI_in_P<32>	IOB	IO_L32P_SM1_7	INPUT	LVDS_25	7
AE22			VCCO_7			7
AE23	VSI_in_N<29>	IOB	IO_L19N_7	INPUT	LVDS_25	7
AE24	VSI_in_N<28>	IOB	IO_L22N_7	INPUT	LVDS_25	7
AE25			GND			
AE26			GND			
AE3	odata<25>	IOB	IO_L15N_8	OUTPUT	HSTL_III_DCI	8
AE4	odata<24>	IOB	IO_L17N_8	OUTPUT	HSTL_III_DCI	8
AE5			VCCO_8			8
AE6	odata<22>	IOB	IO_L30P_8	OUTPUT	HSTL_III_DCI	8
AE8			VCCO_8			8
AE9	odata<13>	IOB	IO_L31N_8	OUTPUT	HSTL_III_DCI	8
AF11	test_port<0>	IOB	IO_L4P_GC_LC_4	OUTPUT	LVCMOS25	4

AF12	mcb_rw_p	IOB	IO_L1P_GC_LC_4	INPUT	LVCMOS25	4
AF13			GND			
AF14			GND			
AF17			AVDD_SM			
AF18	VSI_in_P<38>	IOB	IO_L31P_SM2_7	INPUT	LVDS_25	7
AF19	VSI_in_P<36>	IOB	IO_L17P_7	INPUT	LVDS_25	7
AF2			GND			
AF20	VSI_in_N<36>	IOB	IO_L17N_7	INPUT	LVDS_25	7
AF21	VSI_in_P<33>	IOB	IO_L30P_SM3_7	INPUT	LVDS_25	7
AF22	VSI_in_N<33>	IOB	IO_L30N_SM3_7	INPUT	LVDS_25	7
AF23	VSI_in_P<29>	IOB	IO_L19P_7	INPUT	LVDS_25	7
AF24	VSI_in_P<28>	IOB	IO_L22P_7	INPUT	LVDS_25	7
AF25			GND			
AF3	odata_val	IOB	IO_L15P_8	OUTPUT	HSTL_III_DCI	8
AF4	odata<31>	IOB	IO_L17P_8	OUTPUT	HSTL_III_DCI	8
AF5	odata<30>	IOB	IO_L19N_8	OUTPUT	HSTL_III_DCI	8
AF6	odata<29>	IOB	IO_L19P_8	OUTPUT	HSTL_III_DCI	8
AF7	odata<21>	IOB	IO_L25N_CC_LC_8	OUTPUT	HSTL_III_DCI	8
AF8	odata<28>	IOB	IO_L25P_CC_LC_8	OUTPUT	HSTL_III_DCI	8
AF9	odata<19>	IOB	IO_L31P_8	OUTPUT	HSTL_III_DCI	8
B1			GND			
B10	reset_N	IOB	IO_L6N_GC_LC_3	INPUT	LVCMOS25	3
B11			VCCO_3			3
B14	sys_100PPS_N	IOB	IO_L1N_GC_CC_LC_3	INPUT	LVDS_25	3
B15	sys_100PPS_P	IOB	IO_L1P_GC_CC_LC_3	INPUT	LVDS_25	3
B16			VCCO_3			3
B18	VSI_out_P<4>	IOBM	IO_L3P_5	OUTPUT	LVDS_25	5
B19			VCCO_5			5
B2			GND			
B20	VSI_out_N<9>	IOBS	IO_L2N_5	OUTPUT	LVDS_25	5
B21	VSI_out_N<14>	IOBS	IO_L6N_5	OUTPUT	LVDS_25	5
B22			VCCO_5			5
B23	VSI_out_N<6>	IOBS	IO_L10N_5	OUTPUT	LVDS_25	5
B24	VSI_out_P<6>	IOBM	IO_L10P_5	OUTPUT	LVDS_25	5

B25			GND				
B26			GND				
B5			VCCO_6			6	
B7	data_G05<3>	IOB	IO_L11P_6	INPUT	HSTL_III_DCI	6	
B8			VCCO_6			6	
B9	tick_G05	IOB	IO_L13N_6	INPUT	HSTL_III_DCI	6	
C10	clk_G14	IOB	IO_L1N_6	INPUT	HSTL_III_DCI	6	
C11	mcb_data_p<5>	IOB	IO_L6P_D21_LC_1	BIDIR	LVCMOS25	1	
C14	sclk_128_N	LOWCAPIOB	IO_L3N_GC_LC_3	INPUT	LVDS_25	3	
C15	sclk_128_P	LOWCAPIOB	IO_L3P_GC_LC_3	INPUT	LVDS_25	3	
C16	mcb_data_p<2>	IOB	IO_L7N_D18_LC_1	BIDIR	LVCMOS25	1	
C17	VSI_out_P<1>	IOBM	IO_L1P_5	OUTPUT	LVDS_25	5	
C18			GND				
C19	VSI_out_P<5>	IOBM	IO_L7P_5	OUTPUT	LVDS_25	5	
C20	VSI_out_P<9>	IOBM	IO_L2P_5	OUTPUT	LVDS_25	5	
C21	VSI_out_P<14>	IOBM	IO_L6P_5	OUTPUT	LVDS_25	5	
C22	VSI_out_N<13>	IOBS	IO_L14N_5	OUTPUT	LVDS_25	5	
C23	VSI_out_N<18>	IOBS	IO_L21N_5	OUTPUT	LVDS_25	5	
C24	VSI_out_N<28>	IOBS	IO_L16N_5	OUTPUT	LVDS_25	5	
C25	VSI_out_N<25>	IOBS	IO_L20N_VREF_5	OUTPUT	LVDS_25	5	
C26	VSI_out_P<25>	IOBM	IO_L20P_5	OUTPUT	LVDS_25	5	
C3			GND				
C5	data_G06<0>	IOB	IO_L12P_6	INPUT	HSTL_III_DCI	6	
C6	tick_G06	IOB	IO_L8N_CC_LC_6	INPUT	HSTL_III_DCI	6	
C7	clk_G05	IOB	IO_L11N_6	INPUT	HSTL_III_DCI	6	
C8	tick_G14	IOB	IO_L2N_6	INPUT	HSTL_III_DCI	6	
C9			GND				
D1	data_G06<3>	IOB	IO_L25N_CC_LC_6	INPUT	HSTL_III_DCI	6	
D10	clk_G15	IOB	IO_L1P_6	INPUT	HSTL_III_DCI	6	
D11	mcb_data_p<4>	IOB	IO_L6N_D20_LC_1	BIDIR	LVCMOS25	1	
D12	mcb_data_p<0>	IOB	IO_L8N_D16_CC_LC_1	BIDIR	LVCMOS25	1	
D13	mcb_data_p<8>	IOB	IO_L4N_D24_VREF_LC_1	BIDIR	LVCMOS25	1	
D14	mcb_data_p<9>	IOB	IO_L4P_D25_LC_1	BIDIR	LVCMOS25	1	
D15	mcb_data_p<7>	IOB	IO_L5P_D23_LC_1	BIDIR	LVCMOS25	1	

D16	mcb_data_p<3>	IOB	IO_L7P_D19_LC_1	BIDIR	LVCMOS25	1
D17	VSI_out_N<1>	IOBS	IO_L1N_5	OUTPUT	LVDS_25	5
D18	VSI_out_N<5>	IOBS	IO_L7N_5	OUTPUT	LVDS_25	5
D19	VSI_out_N<10>	IOBS	IO_L4N_VREF_5	OUTPUT	LVDS_25	5
D2	clk_G06	IOB	IO_L25P_CC_LC_6	INPUT	HSTL_III_DCI	6
D20	VSI_out_P<10>	IOBM	IO_L4P_5	OUTPUT	LVDS_25	5
D21	VSI_out_N<8>	IOBS	IO_L12N_VREF_5	OUTPUT	LVDS_25	5
D22	VSI_out_P<13>	IOBM	IO_L14P_5	OUTPUT	LVDS_25	5
D23	VSI_out_P<18>	IOBM	IO_L21P_5	OUTPUT	LVDS_25	5
D24	VSI_out_P<28>	IOBM	IO_L16P_5	OUTPUT	LVDS_25	5
D3	data_G06<2>	IOB	IO_L22P_6	INPUT	HSTL_III_DCI	6
D4	data_G06<1>	IOB	IO_L16N_6	INPUT	HSTL_III_DCI	6
D6	data_G14<2>	IOB	IO_L17N_6	INPUT	HSTL_III_DCI	6
D8	data_G14<1>	IOB	IO_L4P_6	INPUT	HSTL_III_DCI	6
D9	data_G14<0>	IOB	IO_L2P_6	INPUT	HSTL_III_DCI	6
E1	data_G16<2>	IOB	IO_L26P_6	INPUT	HSTL_III_DCI	6
E10	data_G15<1>	IOB	IO_L5N_6	INPUT	HSTL_III_DCI	6
E11			VCCO_1			1
E12			GND			
E13	mcb_data_p<1>	IOB	IO_L8P_D17_CC_LC_1	BIDIR	LVCMOS25	1
E14	mcb_data_p<6>	IOB	IO_L5N_D22_LC_1	BIDIR	LVCMOS25	1
E15			GND			
E16			VCCO_1			1
E17	VSI_out_P<2>	IOBM	IO_L5P_5	OUTPUT	LVDS_25	5
E18	VSI_out_N<15>	IOBS	IO_L11N_5	OUTPUT	LVDS_25	5
E19			VCCO_5			5
E20	VSI_out_N<11>	IOBS	IO_L19N_5	OUTPUT	LVDS_25	5
E21	VSI_out_P<8>	IOBM	IO_L12P_5	OUTPUT	LVDS_25	5
E22	VSI_out_N<21>	IOBS	IO_L18N_5	OUTPUT	LVDS_25	5
E23	VSI_out_P<21>	IOBM	IO_L18P_5	OUTPUT	LVDS_25	5
E24	VSI_out_N<23>	IOBS	IO_L27N_5	OUTPUT	LVDS_25	5
E25	VSI_out_P<23>	IOBM	IO_L27P_5	OUTPUT	LVDS_25	5
E26	VSI_out_N<29>	IOBS	IO_L29N_5	OUTPUT	LVDS_25	5
E3	data_G13<3>	IOB	IO_L24P_CC_LC_6	INPUT	HSTL_III_DCI	6

E4	data_G13<2>	IOB	IO_L22N_6	INPUT	HSTL_III_DCI	6
E5	data_G13<1>	IOB	IO_L18N_6	INPUT	HSTL_III_DCI	6
E6	data_G14<3>	IOB	IO_L18P_6	INPUT	HSTL_III_DCI	6
E7	data_G15<3>	IOB	IO_L17P_6	INPUT	HSTL_III_DCI	6
E8			VCCO_6			6
E9	data_G15<2>	IOB	IO_L7P_6	INPUT	HSTL_III_DCI	6
F1	data_G16<1>	IOB	IO_L26N_6	INPUT	HSTL_III_DCI	6
F10	tick_G15	IOB	IO_L5P_6	INPUT	HSTL_III_DCI	6
F11	mcb_data_p<12>	IOB	IO_L2N_D28_LC_1	BIDIR	LVCMOS25	1
F12	mcb_data_p<13>	IOB	IO_L2P_D29_LC_1	BIDIR	LVCMOS25	1
F13	mcb_data_p<14>	IOB	IO_L1N_D30_LC_1	BIDIR	LVCMOS25	1
F14	mcb_data_p<15>	IOB	IO_L1P_D31_LC_1	BIDIR	LVCMOS25	1
F15	mcb_data_p<10>	IOB	IO_L3N_D26_LC_1	BIDIR	LVCMOS25	1
F16	mcb_data_p<11>	IOB	IO_L3P_D27_LC_1	BIDIR	LVCMOS25	1
F17	VSI_out_N<2>	IOBS	IO_L5N_5	OUTPUT	LVDS_25	5
F18	VSI_out_P<15>	IOBM	IO_L11P_5	OUTPUT	LVDS_25	5
F19	VSI_out_N<7>	IOBS	IO_L17N_5	OUTPUT	LVDS_25	5
F2			VCCO_6			6
F20	VSI_out_P<11>	IOBM	IO_L19P_5	OUTPUT	LVDS_25	5
F21			GND			
F22			VCCO_5			5
F25			VCCO_5			5
F26	VSI_out_P<29>	IOBM	IO_L29P_5	OUTPUT	LVDS_25	5
F3	clk_G13	IOB	IO_L27N_6	INPUT	HSTL_III_DCI	6
F4	data_G13<0>	IOB	IO_L27P_6	INPUT	HSTL_III_DCI	6
F5			VCCO_6			6
F6			GND			
F7	data_G04<3>	IOB	IO_L19P_6	INPUT	HSTL_III_DCI	6
F8	tick_G04	IOB	IO_L10P_6	INPUT	HSTL_III_DCI	6
F9	data_G15<0>	IOB	IO_L7N_6	INPUT	HSTL_III_DCI	6
G1	data_G16<0>	IOB	IO_L30N_6	INPUT	HSTL_III_DCI	6
G10	clk_G04	IOB	IO_L9P_CC_LC_6	INPUT	HSTL_III_DCI	6
G11			CS_B_0			
G12			D_IN_0			

G13			TDN_0				
G14			CCLK_0				
G15			INIT_0				
G16			HSWAPEN_0				
G19	VSI_out_P<7>	IOBM	IO_L17P_5	OUTPUT	LVDS_25	5
G2	clk_G16	IOB	IO_L30P_6	INPUT	HSTL_III_DCI	6
G20	VSI_out_N<12>	IOBS	IO_L22N_5	OUTPUT	LVDS_25	5
G21	VSI_out_N<16>	IOBS	IO_L23N_VRP_5	OUTPUT	LVDS_25	5
G22	VSI_out_P<16>	IOBM	IO_L23P_VRN_5	OUTPUT	LVDS_25	5
G23	VSI_out_N<26>	IOBS	IO_L28N_VREF_5	OUTPUT	LVDS_25	5
G24	VSI_out_P<26>	IOBM	IO_L28P_5	OUTPUT	LVDS_25	5
G25	VSI_out_N<31>	IOBS	IO_L31N_5	OUTPUT	LVDS_25	5
G26	VSI_out_P<31>	IOBM	IO_L31P_5	OUTPUT	LVDS_25	5
G4	tick_G13	IOB	IO_L28P_6	INPUT	HSTL_III_DCI	6
G7	data_G04<2>	IOB	IO_L19N_6	INPUT	HSTL_III_DCI	6
G8	data_G04<1>	IOB	IO_L10N_6	INPUT	HSTL_III_DCI	6
G9	data_G04<0>	IOB	IO_L9N_CC_LC_6	INPUT	HSTL_III_DCI	6
H1	tick_G16	IOB	IO_L32N_6	INPUT	HSTL_III_DCI	6
H10			VCCO_6			6
H11			VCCAUX			
H12			RDWR_B_0			
H13			TDP_0			
H14			DONE_0			
H15			PROGRAM_B_0			
H16			VCCAUX			
H17			VCCAUX			
H18			VCCO_5			5
H19			VCCO_5			5
H2	data_G16<3>	IOB	IO_L32P_6	INPUT	HSTL_III_DCI	6
H20	VSI_out_P<12>	IOBM	IO_L22P_5	OUTPUT	LVDS_25	5
H21	VSI_out_N<24>	IOBS	IO_L26N_5	OUTPUT	LVDS_25	5
H22	VSI_out_P<24>	IOBM	IO_L26P_5	OUTPUT	LVDS_25	5
H23	VSI_out_N<27>	IOBS	IO_L30N_5	OUTPUT	LVDS_25	5
H24	VSI_out_P<27>	IOBM	IO_L30P_5	OUTPUT	LVDS_25	5

H25	VSI_out_N<17>	IOBS	IO_L32N_5	OUTPUT	LVDS_25	5
H26	VSI_out_P<17>	IOBM	IO_L32P_5	OUTPUT	LVDS_25	5
H9			VCCO_6			6
J10			VCCINT			
J11			VCCINT			
J12			VCCAUX			
J13			GND			
J14			GND			
J15			VCCO_0			0
J16			VCCINT			
J17			VCCINT			
J19			VCCO_5			5
J20	VSI_out_N<33>	IOBS	IO_L1N_9	OUTPUT	LVDS_25	9
J21	VSI_out_P<33>	IOBM	IO_L1P_9	OUTPUT	LVDS_25	9
J22	VSI_out_N<30>	IOBS	IO_L2N_9	OUTPUT	LVDS_25	9
J23	VSI_out_P<30>	IOBM	IO_L2P_9	OUTPUT	LVDS_25	9
J24			GND			
J25	VSI_out_N<32>	IOBS	IO_L4N_VREF_9	OUTPUT	LVDS_25	9
J26	VSI_out_P<32>	IOBM	IO_L4P_9	OUTPUT	LVDS_25	9
J3			GND			
J8			VCCO_6			6
K10			VCCINT			
K11			GND			
K12			GND			
K13			GND			
K14			GND			
K15			GND			
K16			GND			
K17			VCCINT			
K18			VCCINT			
K19			VCCO_9			9
K20	VSI_out_N<35>	IOBS	IO_L5N_9	OUTPUT	LVDS_25	9
K21	VSI_out_N<34>	IOBS	IO_L3N_9	OUTPUT	LVDS_25	9
K22	VSI_out_P<34>	IOBM	IO_L3P_9	OUTPUT	LVDS_25	9

K23	VSI_out_N<39>	IOBS	IO_L7N_9	OUTPUT	LVDS_25	9
K24	VSI_out_P<39>	IOBM	IO_L7P_9	OUTPUT	LVDS_25	9
K6	tick_G03	IOB	IO_L3N_10	INPUT	HSTL_III_DCI	10
K7	data_G03<3>	IOB	IO_L3P_10	INPUT	HSTL_III_DCI	10
K8			VCCO_10			10
K9			VCCINT			
L10			VCCINT			
L11			VCCINT			
L12			GND			
L13			GND			
L14			GND			
L15			GND			
L16			VCCINT			
L17			VCCINT			
L18			VCCINT			
L19	VSI_out_P<35>	IOBM	IO_L5P_9	OUTPUT	LVDS_25	9
L2			VCCO_10			10
L20	VSI_out_N<0>	IOBS	IO_L6N_9	OUTPUT	LVDS_25	9
L21	VSI_out_P<0>	IOBM	IO_L6P_9	OUTPUT	LVDS_25	9
L22			VCCO_9			9
L23	VSI_out_N<36>	IOBS	IO_L10N_9	OUTPUT	LVDS_25	9
L24	VSI_out_P<36>	IOBM	IO_L10P_9	OUTPUT	LVDS_25	9
L25			VCCO_9			9
L26	VSI_out_P<37>	IOBM	IO_L12P_9	OUTPUT	LVDS_25	9
L3	data_G03<2>	IOB	IO_L8N_CC_LC_10	INPUT	HSTL_III_DCI	10
L4	data_G07<3>	IOB	IO_L8P_CC_LC_10	INPUT	HSTL_III_DCI	10
L5			VCCO_10			10
L6	data_G03<1>	IOB	IO_L5N_10	INPUT	HSTL_III_DCI	10
L7	data_G03<0>	IOB	IO_L5P_10	INPUT	HSTL_III_DCI	10
L8	clk_G03	IOB	IO_L9N_CC_LC_10	INPUT	HSTL_III_DCI	10
L9			VCCINT			
M1	tick_G12	IOB	IO_L11N_10	INPUT	HSTL_III_DCI	10
M10			GND			
M11			GND			

M12			VCCINT				
M13			GND				
M14			GND				
M15			VCCINT				
M16			GND				
M17			GND				
M18			VCCO_9			9	
M2	clk_G12	IOB	IO_L11P_10	INPUT	HSTL_III_DCI	10	
M20	VSI_out_N<20>	IOBS	IO_L13N_9	OUTPUT	LVDS_25	9	
M21	VSI_out_P<20>	IOBM	IO_L13P_9	OUTPUT	LVDS_25	9	
M22	VSI_out_N<38>	IOBS	IO_L14N_9	OUTPUT	LVDS_25	9	
M23	VSI_out_P<38>	IOBM	IO_L14P_9	OUTPUT	LVDS_25	9	
M24	VSI_in_N<0>	IOB	IO_L11N_9	INPUT	LVDS_25	9	
M25	VSI_in_P<0>	IOB	IO_L11P_9	INPUT	LVDS_25	9	
M26	VSI_out_N<37>	IOBS	IO_L12N_VREF_9	OUTPUT	LVDS_25	9	
M4	data_G07<2>	IOB	IO_L12P_10	INPUT	HSTL_III_DCI	10	
M5	data_G07<1>	IOB	IO_L13N_10	INPUT	HSTL_III_DCI	10	
M6	data_G07<0>	IOB	IO_L13P_10	INPUT	HSTL_III_DCI	10	
M7	tick_G07	IOB	IO_L17N_10	INPUT	HSTL_III_DCI	10	
M8	clk_G07	IOB	IO_L9P_CC_LC_10	INPUT	HSTL_III_DCI	10	
M9			VCCAUX				
N1			VCCO_10			10	
N10			GND				
N11			GND				
N12			GND				
N13			GND				
N14			GND				
N15			GND				
N16			GND				
N17			GND				
N18			VCCAUX				
N2	data_G12<3>	IOB	IO_L14N_10	INPUT	HSTL_III_DCI	10	
N20	VSI_out_N<3>	IOBS	IO_L17N_9	OUTPUT	LVDS_25	9	
N21	VSI_out_P<3>	IOBM	IO_L17P_9	OUTPUT	LVDS_25	9	

N22	VSI_in_N<2>	IOB	IO_L16N_9	INPUT	LVDS_25	9
N23	VSI_in_P<2>	IOB	IO_L16P_9	INPUT	LVDS_25	9
N24	VSI_in_N<1>	IOB	IO_L15N_9	INPUT	LVDS_25	9
N25	VSI_in_P<1>	IOB	IO_L15P_9	INPUT	LVDS_25	9
N26			GND			
N3	data_G12<2>	IOB	IO_L14P_10	INPUT	HSTL_III_DCI	10
N4	data_G12<1>	IOB	IO_L15N_10	INPUT	HSTL_III_DCI	10
N5	data_G12<0>	IOB	IO_L15P_10	INPUT	HSTL_III_DCI	10
N6			GND			
N7	data_G17<3>	IOB	IO_L17P_10	INPUT	HSTL_III_DCI	10
N8	data_G17<2>	IOB	IO_L19N_10	INPUT	HSTL_III_DCI	10
N9			VCCAUX			
P1			GND			
P10			GND			
P11			GND			
P12			GND			
P13			GND			
P14			GND			
P15			GND			
P16			GND			
P17			GND			
P18			VCCAUX			
P19	VSI_in_N<8>	IOB	IO_L21N_9	INPUT	LVDS_25	9
P2	data_G02<2>	IOB	IO_L16N_10	INPUT	HSTL_III_DCI	10
P20	VSI_in_P<8>	IOB	IO_L21P_9	INPUT	LVDS_25	9
P21			GND			
P22	VSI_in_N<4>	IOB	IO_L19N_9	INPUT	LVDS_25	9
P23	VSI_in_P<4>	IOB	IO_L19P_9	INPUT	LVDS_25	9
P24	VSI_in_N<3>	IOB	IO_L18N_9	INPUT	LVDS_25	9
P25	VSI_in_P<3>	IOB	IO_L18P_9	INPUT	LVDS_25	9
P26			VCCO_9			9
P3	data_G02<3>	IOB	IO_L16P_10	INPUT	HSTL_III_DCI	10
P4	tick_G02	IOB	IO_L18N_10	INPUT	HSTL_III_DCI	10
P5	data_G17<1>	IOB	IO_L18P_10	INPUT	HSTL_III_DCI	10

P6	data_G17<0>	IOB	IO_L21N_10	INPUT	HSTL_III_DCI	10
P7	clk_G17	IOB	IO_L21P_10	INPUT	HSTL_III_DCI	10
P8	tick_G17	IOB	IO_L19P_10	INPUT	HSTL_III_DCI	10
P9			VCCAUX			
R1	data_G02<1>	IOB	IO_L22N_10	INPUT	HSTL_III_DCI	10
R10			GND			
R11			GND			
R12			VCCINT			
R13			GND			
R14			GND			
R15			VCCINT			
R16			GND			
R17			GND			
R18			VCCAUX			
R2	data_G02<0>	IOB	IO_L22P_10	INPUT	HSTL_III_DCI	10
R23	VSI_in_N<7>	IOB	IO_L22N_9	INPUT	LVDS_25	9
R24	VSI_in_P<7>	IOB	IO_L22P_9	INPUT	LVDS_25	9
R25	VSI_in_N<5>	IOB	IO_L20N_VREF_9	INPUT	LVDS_25	9
R26	VSI_in_P<5>	IOB	IO_L20P_9	INPUT	LVDS_25	9
R4	clk_G02	IOB	IO_L20P_10	INPUT	HSTL_III_DCI	10
R7	clk_G08	IOB	IO_L25N_CC_LC_10	INPUT	HSTL_III_DCI	10
R8	tick_G08	IOB	IO_L25P_CC_LC_10	INPUT	HSTL_III_DCI	10
R9			VCCO_10			10
T10			VCCINT			
T11			VCCINT			
T12			GND			
T13			GND			
T14			GND			
T15			GND			
T16			VCCINT			
T17			VCCINT			
T18			VCCINT			
T19	VSI_in_N<11>	IOB	IO_L31N_9	INPUT	LVDS_25	9
T2			VCCO_10			10

T20	TC_N<1>	IOBS	IO_L30N_9	OUTPUT	LVDS_25	9
T21	TC_P<1>	IOBM	IO_L30P_9	OUTPUT	LVDS_25	9
T22			VCCO_9			9
T23	VSI_in_N<9>	IOB	IO_L24N_CC_LC_9	INPUT	LVDS_25	9
T24	VSI_in_P<9>	IOB	IO_L24P_CC_LC_9	INPUT	LVDS_25	9
T25			VCCO_9			9
T26	VSI_in_P<6>	IOB	IO_L26P_9	INPUT	LVDS_25	9
T4	data_G08<3>	IOB	IO_L26P_10	INPUT	HSTL_III_DCI	10
T5			VCCO_10			10
T6	data_G08<2>	IOB	IO_L27N_10	INPUT	HSTL_III_DCI	10
T7	data_G08<1>	IOB	IO_L27P_10	INPUT	HSTL_III_DCI	10
T8	data_G08<0>	IOB	IO_L31P_10	INPUT	HSTL_III_DCI	10
T9			VCCINT			
U1	data_G11<3>	IOB	IO_L24P_CC_LC_10	INPUT	HSTL_III_DCI	10
U10			VCCINT			
U11			GND			
U12			GND			
U13			GND			
U14			GND			
U15			GND			
U16			GND			
U17			VCCINT			
U18			VCCINT			
U19			VCCO_9			9
U20	VSI_in_P<11>	IOB	IO_L31P_9	INPUT	LVDS_25	9
U21	VSI_in_N<10>	IOB	IO_L29N_9	INPUT	LVDS_25	9
U22	VSI_in_P<10>	IOB	IO_L29P_9	INPUT	LVDS_25	9
U23	VSI_in_P<14>	IOB	IO_L27P_9	INPUT	LVDS_25	9
U24	VSI_in_N<12>	IOB	IO_L28N_VREF_9	INPUT	LVDS_25	9
U25	VSI_in_P<12>	IOB	IO_L28P_9	INPUT	LVDS_25	9
U26	VSI_in_N<6>	IOB	IO_L26N_9	INPUT	LVDS_25	9
U3	data_G11<2>	IOB	IO_L28P_10	INPUT	HSTL_III_DCI	10
U4	clk_G11	IOB	IO_L29N_10	INPUT	HSTL_III_DCI	10
U5	tick_G11	IOB	IO_L32N_10	INPUT	HSTL_III_DCI	10

U6	tick_G18	IOB	IO_L32P_10	INPUT	HSTL_III_DCI	10
U7	clk_G18	IOB	IO_L31N_10	INPUT	HSTL_III_DCI	10
U8			VCCO_10			10
U9			VCCINT			
V1	data_G11<1>	IOB	IO_L30N_10	INPUT	HSTL_III_DCI	10
V10			VCCINT			
V11			VCCINT			
V12			VCCO_0			0
V13			GND			
V14			GND			
V15			VCCAUX			
V16			VCCINT			
V17			VCCINT			
V19			VCCO_7			7
V2	data_G11<0>	IOB	IO_L30P_10	INPUT	HSTL_III_DCI	10
V20	VSI_in_N<15>	IOB	IO_L5N_7	INPUT	LVDS_25	7
V23	VSI_in_N<14>	IOB	IO_L27N_9	INPUT	LVDS_25	9
V24			GND			
V25	VSI_in_N<13>	IOB	IO_L32N_9	INPUT	LVDS_25	9
V26	VSI_in_P<13>	IOB	IO_L32P_9	INPUT	LVDS_25	9
V3			GND			
V4	data_G18<3>	IOB	IO_L29P_10	INPUT	HSTL_III_DCI	10
V5	data_G18<2>	IOB	IO_L2N_8	INPUT	HSTL_III_DCI	8
V6	data_G18<1>	IOB	IO_L2P_8	INPUT	HSTL_III_DCI	8
V7	data_G18<0>	IOB	IO_L3N_8	INPUT	HSTL_III_DCI	8
V8			VCCO_8			8
W1	tick_G01	IOB	IO_L1N_8	INPUT	HSTL_III_DCI	8
W10			VCCAUX			
W11			VCCAUX			
W12			TCK_0			
W13			PWRDWN_B_0			
W14			M2_0			
W15			M0_0			
W16			VCCAUX			

W17			VCCO_7			7	
W18			VCCO_7			7	
W19	VSI_in_N<35>	IOB	IO_L18N_7	INPUT	LVDS_25	7	
W2	clk_G01	IOB	IO_L1P_8	INPUT	HSTL_III_DCI	8	
W20	VSI_in_P<15>	IOB	IO_L5P_7	INPUT	LVDS_25	7	
W21	VSI_in_P<18>	IOB	IO_L3P_7	INPUT	LVDS_25	7	
W22	VSI_in_N<18>	IOB	IO_L3N_7	INPUT	LVDS_25	7	
W23	VSI_in_P<17>	IOB	IO_L4P_7	INPUT	LVDS_25	7	
W24	VSI_in_N<17>	IOB	IO_L4N_VREF_7	INPUT	LVDS_25	7	
W25	VSI_in_P<16>	IOB	IO_L2P_7	INPUT	LVDS_25	7	
W26	VSI_in_N<16>	IOB	IO_L2N_7	INPUT	LVDS_25	7	
W4	data_G01<3>	IOB	IO_L4P_8	INPUT	HSTL_III_DCI	8	
W5	data_G01<2>	IOB	IO_L5N_8	INPUT	HSTL_III_DCI	8	
W6	data_G01<1>	IOB	IO_L5P_8	INPUT	HSTL_III_DCI	8	
W7	data_G01<0>	IOB	IO_L3P_8	INPUT	HSTL_III_DCI	8	
W8			VCCO_8			8	
W9			VCCO_8			8	
Y1	clk_G09	IOB	IO_L6N_8	INPUT	HSTL_III_DCI	8	
Y10	odata_100PPS	IOB	IO_L27P_8	OUTPUT	HSTL_III_DCI	8	
Y11			TMS_0				
Y12			TDI_0				
Y13			TDO_0				
Y14			DOUT_BUSY_0				
Y15			M1_0				
Y16			VBATT_0				
Y19	VSI_in_P<35>	IOB	IO_L18P_7	INPUT	LVDS_25	7	
Y2	tick_G09	IOB	IO_L6P_8	INPUT	HSTL_III_DCI	8	
Y20	VSI_in_P<22>	IOB	IO_L20P_7	INPUT	LVDS_25	7	
Y21	VSI_in_N<22>	IOB	IO_L20N_VREF_7	INPUT	LVDS_25	7	
Y22	VSI_in_P<21>	IOB	IO_L12P_7	INPUT	LVDS_25	7	
Y23	VSI_in_N<21>	IOB	IO_L12N_VREF_7	INPUT	LVDS_25	7	
Y24	VSI_in_N<20>	IOB	IO_L8N_CC_LC_7	INPUT	LVDS_25	7	
Y25	VSI_in_P<19>	IOB	IO_L6P_7	INPUT	LVDS_25	7	
Y26	VSI_in_N<19>	IOB	IO_L6N_7	INPUT	LVDS_25	7	

Y3	data_G09<3>	IOB	IO_L8N_CC_LC_8	INPUT	HSTL_III_DCI	8
Y4	data_G09<2>	IOB	IO_L8P_CC_LC_8	INPUT	HSTL_III_DCI	8
Y5	tick_G10	IOB	IO_L9N_CC_LC_8	INPUT	HSTL_III_DCI	8
Y6	clk_G10	IOB	IO_L9P_CC_LC_8	INPUT	HSTL_III_DCI	8
Y8	data_G10<2>	IOB	IO_L26N_8	INPUT	HSTL_III_DCI	8
Y9	data_G10<1>	IOB	IO_L21N_8	INPUT	HSTL_III_DCI	8

Table 6-2 Pinout by Pin Number

6.3 Xilinx XC4VSX35-10FF668-CS2 Package Drawing

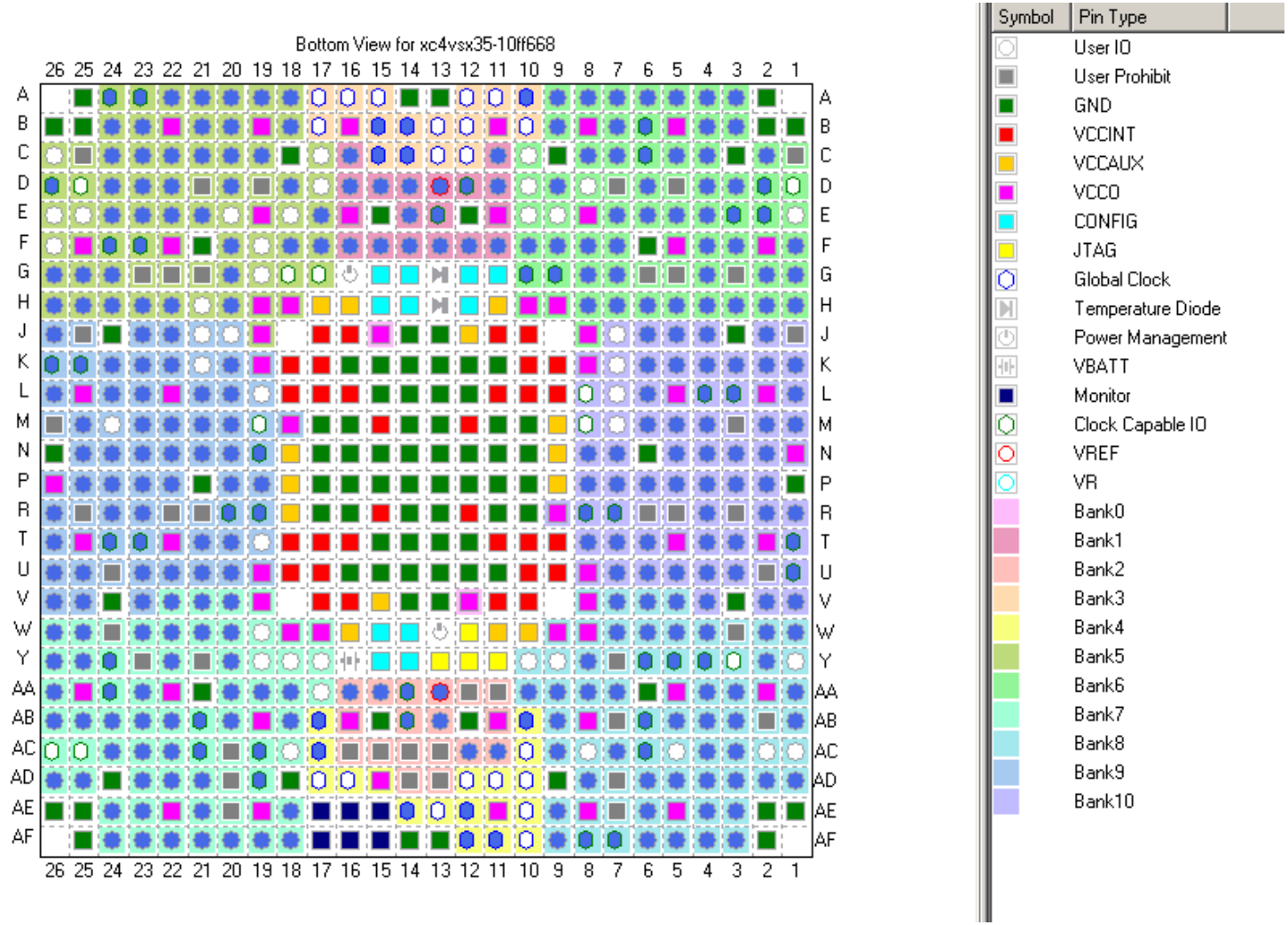

Figure 6-1 Pin Locations

6.4 Programming Notes

All FPGAs on the Station Board are programmed through their 8-bit wide configuration port. The Station Board CMIB software requires the Binary (.bin) output file to program the Xilinx FPGAs. This is set by selecting “Properties…” from the “Process” pull-down menu in the Xilinx ISE software. Select the “General Options” and check “Create Binary Configuration File”.