REQUIREMENTS AND FUNCTIONAL SPECIFICATION

Station Board Configuration FPGA

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Zoran Ljusic, 01 April 2011

National Research Council Canada
Herzberg Institute of Astrophysics
Dominion Radio Astrophysical Observatory

P.O. Box 248, 717 White Lake Rd
Penticton, B.C., Canada
V2A 6J9

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List of Abbreviations and Acronyms

CFG	Configuration FPGA
DMA	Delay Module A.
DMB	Delay Module B.
FORM	Fiber Optic Receiver Module.
IC	Input Chip
MCB	Monitor and Control Bus or MCB FPGA.
MSB	Most Significant Bit.
OUTA	Output A FPGA.
OUTB	Output B FPGA.
PCMC	PC Mezzanine Card.
SB	Station Board.
TC	Timing Chip.
UA	Filter FPGA within group A.
UB	Filter FPGA within group B.
VSIA	VSI A FPGA.
VSIB	VSI B FPGA.
WBC	Wide Band Correlator FPGA.

1 Revision History

Revision	Date	Changes/Notes	Author
Draft	March, 2004	Initial release for reviewing	Z. Ljusic
1.0	August, 2005	Implemented many changes to reflect the current SB design. Changed the name of the document.	Z. Ljusic
1.1	June 2006	Described changes regarding Configuration bus grouping imposed by ICX simulation of the routed Station Board. Added one register (@ 8x09) to the Configuration FPGA that reports status of individual FPGAs DONE signals.	Z. Ljusic
1.2	March 2007	Split Fanout FPGAs RFS into two parts. MCB Fanout RFS Configuration Fanout RFS	D. Fort
1.3	November, 2007	Changed registers at addresses 02h and 0bh.	Z.Ljusic
1.4	June, 2008	Added a register at address 0c.	Z.Ljusic
1.5	01 Apr 2011	Pinouts, etc added.	D. Fort

2 Introduction

This document describes the Station Board Configuration FPGA. This device acts as a buffer and the logic level shifter between the PCMC and the rest of the chips on the Station Board. The logic utilization is minimal while the pin utilization is maximal.

3 Context

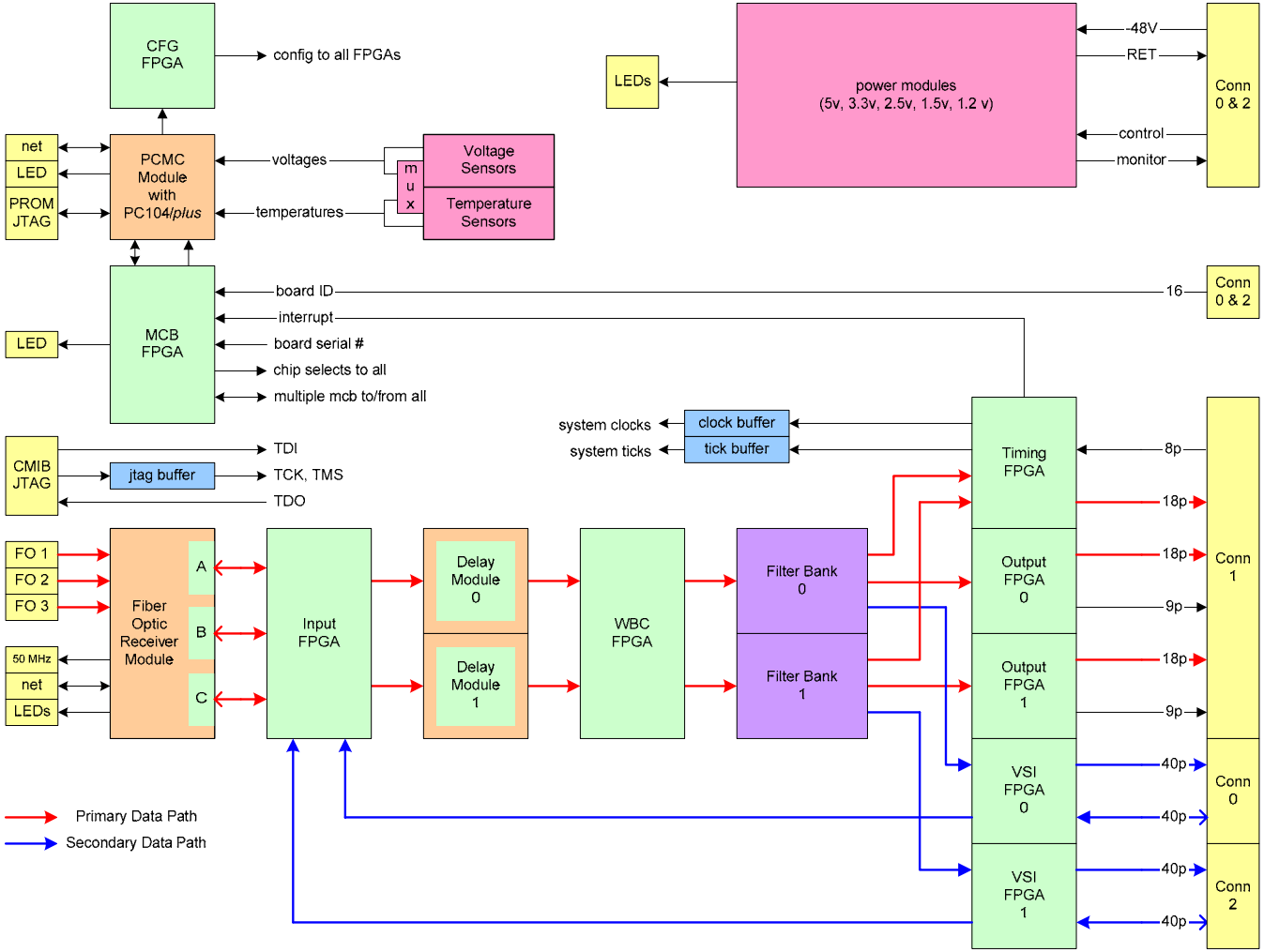

Figure 3-1 Station Board Block Diagram

4 Configuration FPGA

This FPGA serves as an unidirectional buffer and fans out the FPGA configuration bus to all the other FPGAs on the Station Board. It receives configuration data from the PCMC. The interface being used for the purpose is LVTTL 3.3V. The device selected for the application is Xilinx Virtex-4 series: XC4VSX35-10FF668. The size of the FPGA is dictated by the pin count while the logic usage is minimal. No heat sink is required. The choice of the SX35 is governed by economy since a large number of SX35s are required for the Filter FPGA. According to the simulation and Place and Route done so far the total delay in both direction thru the FPGA is up to 12ns.

The high level design of the FPGA is given on the figure below.

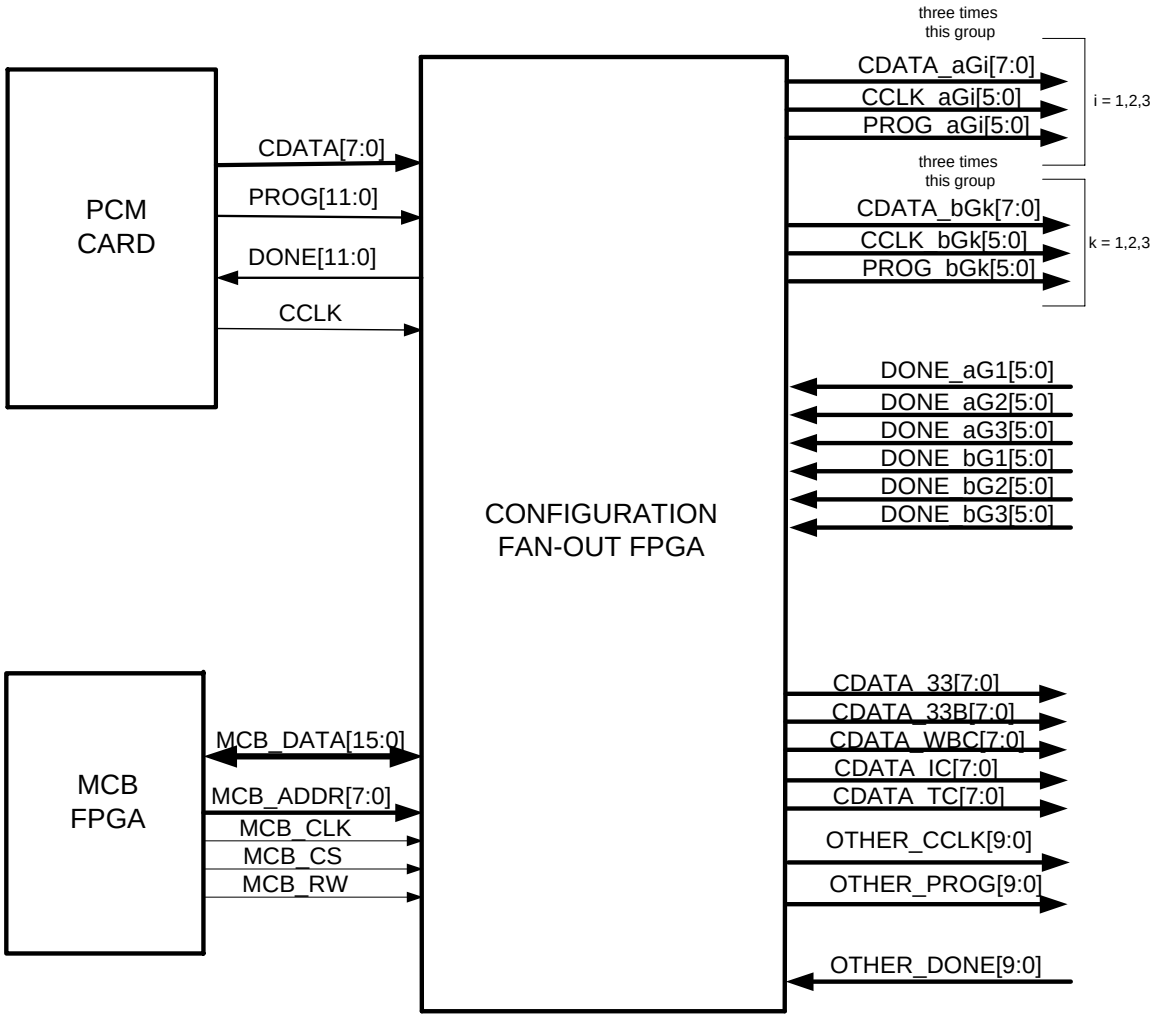

Figure 4-1 Configuration FPGA top-level diagram

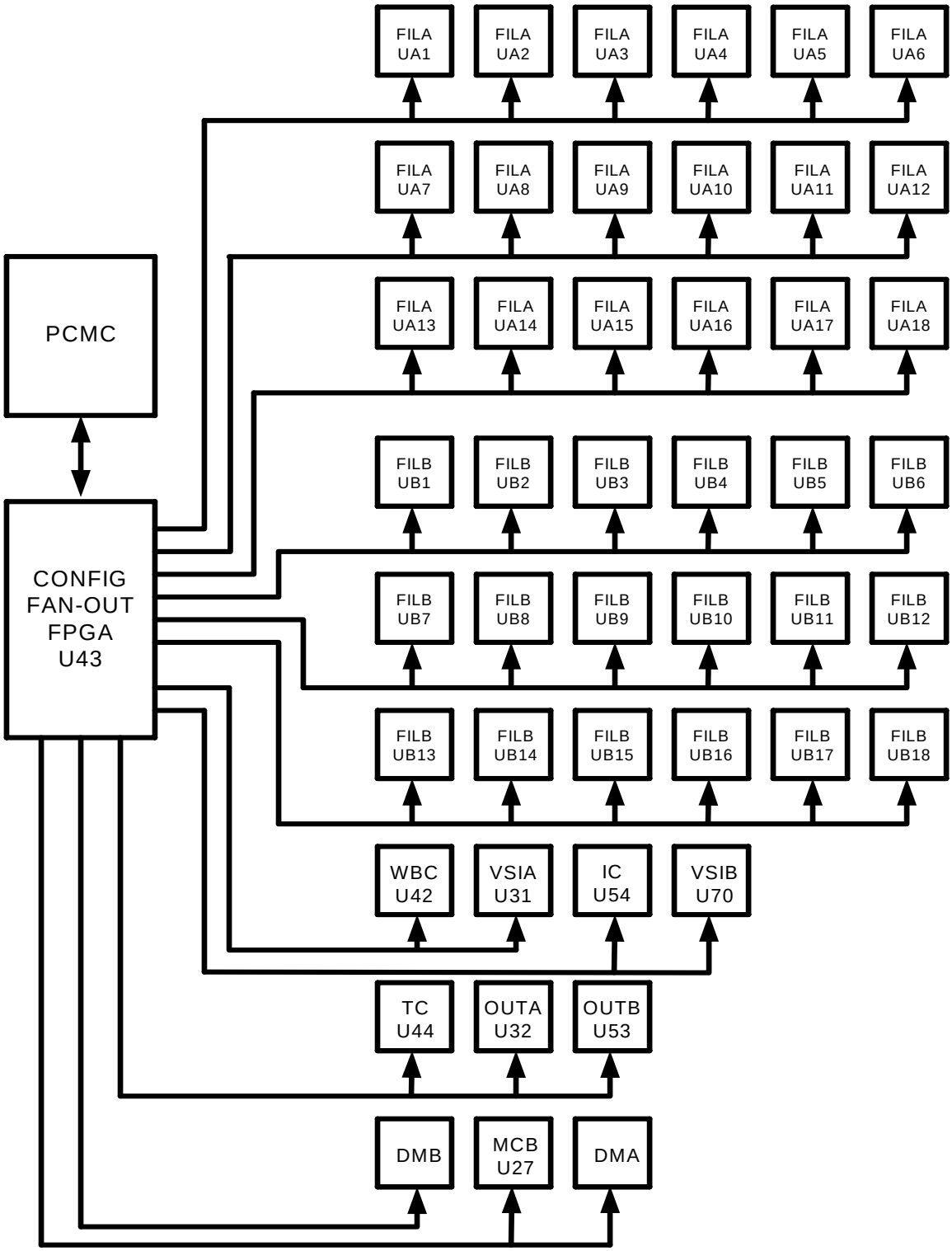

Figure 4-2 Station Board Configuration grouping

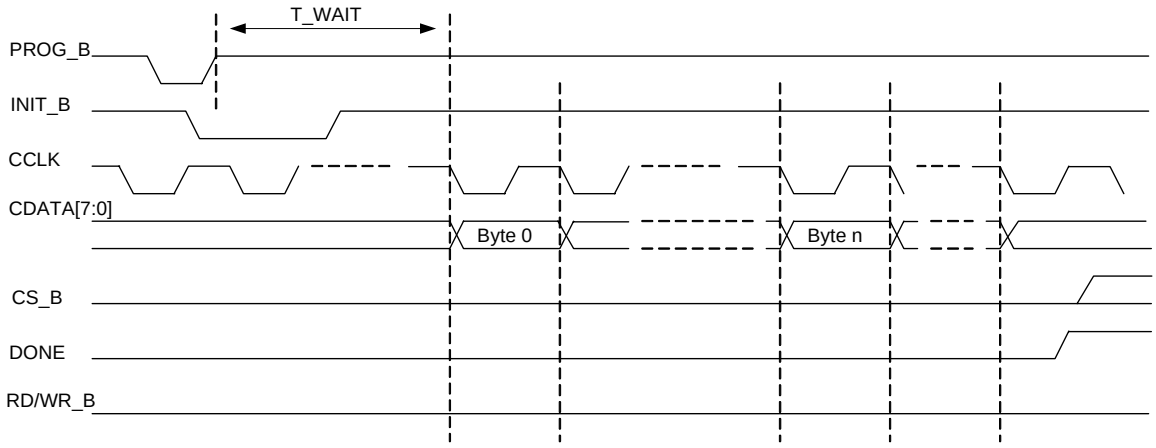

Figure 4-3 Configuration bus timing diagram

PROG_B is used to initiate configuration of a FPGA. This is a point-to-point signal and is pulled-up at target's FPGA pin. A low-to-high transition causes a FPGA to enter the configuration mode. There are 12-bits wide bus of PROG signals coming from the PCM Card to the Configuration fan-out FPGA, there are more FPGAs on the Station Board then PROG lines. Here is the mapping between the lines and the chips on the board:

PROG[0]: Initiates Configuration fan-out FPGA programming.

PROG[1]: Initiates MCB fan-out FPGA programming.

PROG[2]: Initiates Delay Module A ,DMA, FPGA programming.

PROG[3]: Initiates Delay Module B ,DMB, FPGA programming.

PROG[4]: Initiates Input Chip ,IC, FPGA programming.

PROG[5]: Initiates Wide Band Correlator , WBC, FPGA programming.

PROG[6]: Initiates Timing Chip ,TC, FPGA programming.

PROG[7]: Initiates Output Chip A, OUTA, FPGA programming.

PROG[8]: Initiates Output Chip B, OUTB, FPGA programming.

PROG[9]: Initiates VSIA and VSIB FPGAs programming.

PROG[10]: Initiates filter bank A FPGAs programming, all 18.

PROG[11]: Initiates filter bank B FPGAs programming, all 18.

After the MCB fanout FPGA is configured and up and running it can mask individual PROG lines within filters and VSI groups of FPGAs. This provides means for configuring each FPGA on the Station Board separately.

INIT_B: This pin is pulled-up at a target's FPGA. After PROG_B makes its low-to-high transition this pin pulls low indicating that the FPGA is getting ready for configuration. A low-to-high transition indicates that the FPGA is ready to accept configuration bit stream. In our system this feature is not used. The pin is not monitored. Instead there is a waiting period provided. Somewhere within this period of time, T_WAIT, a FPGA has become ready to accept the configuration stream, i.e. low-to-high transition on the INIT_B had happened.

CS_B: This pin is pulled low enabling a FPGA configuration. After the configuration is completed this pin can be set high thru its FPGAs configuration register. The MCB can assert a bit within the register, which prevents the FPGA from being reconfigured. This has two implications: a device cannot enter configuration mode accidentally and the second one is this can be used to enable separate re-programming of any filter chip.

DONE: This signal indicates configuration state of a FPGA. There is a line per chip on the board. There is a pull-up resistor on this pin. After power-up the signal goes low and it changes the state after the FPGA is successfully configured. There is 12-bits wide bus of these signals leaving the Configuration FPGA to the PCM Card. Here is the mapping of the signals:

DONE[0]: Indicates state of Configuration fan-out FPGA.

DONE[1]: Indicates state of MCB fan-out FPGA.

DONE[2]: Indicates state of Delay Module A ,DMA, FPGA.

DONE[3]: Indicates state of Delay Module B ,DMB, FPGA.

DONE[4]: Indicates state of Input Chip ,SBIC, FPGA.

DONE[5]: Indicates state of Wide Band Corelator , WBC, FPGA.

DONE[6]: Indicates state of Timing Chip ,TC, FPGA.

DONE[7]: Indicates state of Output Chip A, SBOCA, FPGA.

DONE[8]: Indicates state of Output Chip B, SBOCB, FPGA.

DONE[9]: Indicates state of VSIA and VSIB FPGAs.

DONE[10]: Indicates state of filter bank A FPGAs , all 18.

DONE [11]: Indicates state of filter bank B FPGAs programming, all 18.

All the DONE signals from a filter bank are summed together and the result is passed to the PCM Card. The same goes for the VSI couple. For purposes of testing and debugging each DONE signal is made available to the MCB thru Configuration FPGA status registers.

RD/WR_B: This signals puts an FPGA into read mode – when high or into write mode – when low. The signal is set to always low state since no reading from the FPGAs is required.

4.1 Configuration FPGA memory map

The memory map of the Configuration fan-out FPGA is given on the figure below.

Address	Mnemonic	Register Name	Access	Reset Value
0x00	FVR	CFG Fan-out FPGA Version/Revision	R	0x0001
0x01	RBT	CFG Read Back Test register	R/W	0x0000
0x02	CC	CFG Configurations and Control register	R/W	0x0000
0x03	CD1	CFG Configuration Disable 1	R/W	0x0000
0x04	CD2	CFG Configuration Disable 2	R/W	0x0000
0x05	DONEA1	CFG DONE signals for Group A 1	R	0x0000
0x06	DONEA2	CFG DONE signals for Group A 2	R	0x0000
0x07	DONEB1	CFG DONE signals for Group B 1	R	0x0000
0x08	DONEB2	CFG DONE signals for Group B 2	R	0x0000
0x09	DONE	CFG individual DONE signals	R	0x0000
0x0a	SBSER	CFG Station Board Serial number	R	0xxxxx
0x0b	PWS	Power Status of the SB power sources	R	0x0000
0x0c	PSE	Power Status Error of the SB power sources	R	0x0000

Table 4-1 CFG FPGA Memory Map

4.1.1 CFG Version/Revision Number register – FVR

Address	15:8	7:4	3:0	Access	Reset
00h	Unused	Version	Revision	R	0001h

Table 4-2 CFG Version/Revision Number – FVR register

This register specifies the FPGA Version/Revision.

The fields within the register are defined as follows:

Version [7:4]: This version number is to be incremented whenever the new FPGA load is incompatible with the previous version from the software standpoint and would require change to the driver. The initial version will be numbered 1(b0001). Version 0 is reserved for prototyping and proof of concept.

Revision [3:0]: This revision number is to be incremented whenever the new FPGA load incorporates new functionality but does not require software upgrades.

4.1.2 CFG Read Back Test register - RB

Address	15:0	Access	Reset
01h	Read Back	R/W	0000h

Table 4-3 CFG Read Back Test – RB register

This is a test register. Writes to this register will have no effect. It simply provides means for communication verification between the FPGA and the MCB. The register keeps its last value until next write to its location.

The fields within the register are defined as follows:

Read Back [15:0]: any 16 bits long combination of zeros and ones.

4.1.3 CFG Configurations and Control register – CC

Address	15:7	6:5	4:3	2:1	0	Access	Reset
02h	Unused	VSIDIS	BDIS	ADIS	U	R/W	0000h

Table 4-4 CFG Configurations and Control - CC register

The fields within the register are defined as follows:

U [0]: Unused, for now.

ADIS[1]: disables programming/reprogramming of filter 16 within bank A – F16A.

1: programming/reprogramming of the chip is disabled.

0: programming/reprogramming of the chip is not disabled.

ADIS[2]: disables programming/reprogramming of filter 17 within bank A – F17A.

1: programming/reprogramming of the chip is disabled.

0: programming/reprogramming of the chip is not disabled.

BDIS[3]: disables programming/reprogramming of filter 16 within bank B – F16B.

1: programming/reprogramming of the chip is disabled.

0: programming/reprogramming of the chip is not disabled.

BDIS[4]: disables reprogramming of filter 17 within bank B – F17B.

1: programming/reprogramming of the chip is disabled.

0: programming/reprogramming of the chip is not disabled.

VSIDIS[5]: disables programming/reprogramming of VSIA chip.

1: programming/reprogramming of the chip is disabled.

0: programming/reprogramming of the chip is not disabled.

VSIDIS[6]: disables programming/reprogramming of VSIB chip.

1: programming/reprogramming of the chip is disabled.

0: programming/reprogramming of the chip is not disabled.

4.1.4 CFG Configuration Disable 1 register - CD1

Address	15:0	Access	Reset
03h	CD1	R/W	0000h

Table 4-5 CFG Configuration Disable 1 – CD1 register

The fields within the register are defined as follows.

CD1[0]: Disables configuration/reconfiguration of the filter 0 within bank A – F0A

1: programming/reprogramming of the chip is disabled.

0: programming/reprogramming of the chip is not disabled.

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CD1[15]: Disables configuration/reconfiguration of the filter 15 within bank A – F15A

1: programming/reprogramming of the chip is disabled.

0: programming/reprogramming of the chip is not disabled.

4.1.5 CFG Configuration Disable 2 register – CD2

Address	15:0	Access	Reset
04h	CD2	R/W	0000h

Table 4-6 CFG Configuration Disable 2 – CD2 register

The fields within the register are defined as follows.

CD2[0]: Disables configuration/reconfiguration of the filter 0 within bank B – F0B

1: programming/reprogramming of the chip is disabled.

0: programming/reprogramming of the chip is not disabled.

.

CD2[15]: Disables configuration/reconfiguration of the filter 15 within bank B – F15B

1: programming/reprogramming of the chip is disabled.

0: programming/reprogramming of the chip is not disabled.

4.1.6 CFG DONE signals for Group A register 1- DONEA1

Address	15:12	11:0	Access	Reset
05h	Unused	DONEA1	R	0000h

Table 4-7 CFG DONE signals for Group A – DONEA1 register

This registers reports programming status of the first 12 filter chips within bank A.

DONEA1[0]: indicates programming status of the filter chip 0 in bank A – F0A.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

.

.

DONEA1[11]: indicates programming status of the filter chip 11 in bank A – F11A.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

4.1.7 CFG DONE signals for Group A register 2- DONEA2

Address	15:6	5:0	Access	Reset
06h	Unused	DONEA2	R	0000h

Table 4-8 CFG DONE signals for Group A – DONEA2 register

This registers reports programming status of the remaining 6 filter chips within bank A.

DONEA2[0]: indicates programming status of the filter chip 12 in bank A – F12A.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

.

DONEA2[5]: indicates programming status of the filter chip 17 in bank A – F17A.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

4.1.8 CFG DONE signals for Group B register 1- DONEB1

Address	15:12	11:0	Access	Reset
07h	Unused	DONEB1	R	0000h

Table 4-9 CFG DONE signals for Group B – DONEB1 register

This registers reports programming status of the first 12 filter chips within bank B.

DONEB1[0]: indicates programming status of the filter chip 0 in bank B – F0B.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

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DONEB1[11]: indicates programming status of the filter chip 11 in bank B – F11B.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

4.1.9 CFG DONE signals for Group B register 2- DONEB2

Address	15:6	5:0	Access	Reset
08h	Unused	DONEA2	R	0000h

Table 4-10 CFG DONE signals for Group B – DONEB2 register

This registers reports programming status of the remaining 6 filter chips within bank B.

DONEB2[0]: indicates programming status of the filter chip 12 in bank B – F12B.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

.

DONEB2[5]: indicates programming status of the filter chip 17 in bank B – F17B.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

4.1.10 CFG individual DONE signals – DONE

Address	5	4	3	2	1	0	Access	Reset
09h	TC	WBC	IC	DMB	DMA	MCB	R	0000h

Table 4-11 CFG individual DONE signals – DONE Register

Address	15:8	9	8	7	6	Access	Reset
09h	Unused	VSIB	VSIA	OUTA	OUTB	R	0000h

Table 4-12 CFG individual DONE signals – DONE Register cont'd

This registers reports programming status of the remaining FPGAs on the board.

MCB[0]: indicates programming status of the MCB fan-out FPGA.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

DMA[1]: indicates programming status of the Delay Module A FPGA.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

DMB[2]: indicates programming status of the Delay Module B FPGA.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

IC[3]: indicates programming status of the Input FPGA.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

WBC[4]: indicates programming status of the WBC FPGA.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

TC[5]: indicates programming status of the Timing FPGA.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

OUTA[6]: indicates programming status of the Output A FPGA.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

OUTB[7]: indicates programming status of the Output B FPGA.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

VSIA[8]: indicates programming status of the VSIA FPGA.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

VSIB[9]: indicates programming status of the VSIB FPGA.

1: the FPGA has been successively programmed.

0: the FPGA is not programmed.

4.1.11 Station Board Serial Number Register - SBSER

Address	15:0	Access	Reset
0ah	Station Board Serial Number	R	xxxxh

Table 4-13 Station Board Serial Numbers – SBSER Register

External wires on the PCB set the value of this register. It is different for each station Board.

4.1.12 CFG Power Status register – PWS

Address	5	4	3	2	1	0	Access	Reset
0bh	S1V2B2	S1V5	S2V5	S3V3	S5V	CE	R	0000h

Table 4-14 CFG Power Status – PWS register

Address	10	9	8	7	6	Access	Reset
0bh	S1V2A	S1V2A1	S1V2A2	S1V2B	S1V2B1	R	0000h

Table 4-15 CFG Power Status – PWS register cont'd

Address	15:11	Access	Reset
0bh	Unused	R	0000h

Table 4-16 CFG Power Status – PWS register cont'd

The fields are defined as follows.

CE[0]: The signal is given to this FPGA by the PCM card and enables programming of other FPGAs on the board.

1: Station Board FPGAs can be programmed.

0: Station Board FPGAs cannot be programmed.

S5V[1]: indicates 5V power source status:

1: the output voltage of the power source is within prescribed range.

0: the output voltage of the power source is not within prescribed range.

S3V3[2]: indicates 3.3V power source status:

1: the output voltage of the power source is within prescribed range.

0: the output voltage of the power source is not within prescribed range.

S2V5[3]: indicates 2.5V power source status:

1: the output voltage of the power source is within prescribed range.

0: the output voltage of the power source is not within prescribed range.

S1V5[4]: indicates 1.5V power source status:

1: the output voltage of the power source is within prescribed range.

0: the output voltage of the power source is not within prescribed range.

S1V2B2[5]: indicates 1.2V B2 power source status:

1: the output voltage of the power source is within prescribed range.

0: the output voltage of the power source is not within prescribed range.

S1V2B1[6]: indicates 1.2V B1 power source status:

1: the output voltage of the power source is within prescribed range.

0: the output voltage of the power source is not within prescribed range.

S1V2B[7]: indicates 1.2V B power source status:

1: the output voltage of the power source is within prescribed range.

0: the output voltage of the power source is not within prescribed range.

S1V2A2[8]: indicates 1.2V A2 power source status:

1: the output voltage of the power source is within prescribed range.

0: the output voltage of the power source is not within prescribed range.

S1V2A1[9]: indicates 1.2V A1 power source status:

1: the output voltage of the power source is within prescribed range.

0: the output voltage of the power source is not within prescribed range.

S1V2A[10]: indicates 1.2V A power source status:

1: the output voltage of the power source is within prescribed range.

0: the output voltage of the power source is not within prescribed range.

4.1.13 Power Status Error register – PSE

This register reports temporary out-of-range condition for all of the power sources on the board. If the source 1V2-B2 drops below certain level this FPGA losses its configuration. The logic here is similar to the data parity error reporting.

Address	5	4	3	2	1	0	Access	Reset
0ch	E1V2B1	E1V2B2	E1V5	E2V5	E3V3	E5	R	0000h

Table 4-17 Power Status Error – PSE register

Address	15:10	9	8	7	6	Access	Reset
0ch	Unused	E1V2A	E1V2A1	E1V2A2	E1V2B	R	0000h

Table 4-18 Power Status Error – PSE register cont'd

The bits are defined as follows:

E5: Out-of-range **Error** on **5V** power source. The bit goes high if the 5V power source status bit goes to zero value, (bit[1] @0x0b). The 5V source could go back to its range, which drives its power status bit back to high logic level. However, this bit, E5 stays high until read. This could be an indication that power source 5V is not working reliably.

1: Power source 5V had gone out-of-range at least once since last read.

0: Power source 5V had not gone out-of-range since the last read.

The rest of the bits are defined in the same manner for its power source.

PROG and DONE Mapping

There are 12 PROG lines coming from the PCMC. Mapping between these lines and the chips on the Station Board is given in the table below. There is the same mapping between the chips and DONE lines as well.

PROG & DONE pair	**IC or Group of ICs on Station Board**
PROG[0] & DONE[0]	CFG
PROG[1] & DONE[1]	MCB
PROG[2] & DONE[2]	DMA
PROG[3] & DONE[3]	DMB
PROG[4] & DONE[4]	IC
PROG[5] & DONE[5]	WBC
PROG[6] & DONE[6]	TC
PROG[7] & DONE[7]	OUTA
PROG[8] & DONE[8]	OUTB
PROG[9] & DONE[9]	VSIA and VSIB
PROG[10] & DONE[10]	Filter Bank A (all of 18 FPGAs)
PROG[11] & DONE[11]	Filter Bank B (all of 18 FPGAs)

Table 4-19 PROG and DONE pairs mapping

5 Pinouts, Pin and Package Notes

5.1 Pinouts by signal name

Note: UNUSED and NC pins have been removed.

```
Release 10.1.03 - par K.39 (nt)
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Mon Jan 05 14:53:14 2009

INPUT FILE:       CFG_top_map.ncd
OUTPUT FILE:      CFG_top_pad.txt
PART TYPE:        xc4vsx35
SPEED GRADE:      -10
PACKAGE:          ff668
```

Pin Number	Signal Name	Pin Usage	Pin Name	Direction	IO Standard	IO Bank
W5	board_id[0]	IOB	IO_L5N_8	INPUT	LVCMOS25	8
W6	board_id[1]	IOB	IO_L5P_8	INPUT	LVCMOS25	8
M6	board_id[10]	IOB	IO_L13P_10	INPUT	LVCMOS25	10
K6	board_id[11]	IOB	IO_L3N_10	INPUT	LVCMOS25	10
L6	board_id[12]	IOB	IO_L5N_10	INPUT	LVCMOS25	10
K4	board_id[13]	IOB	IO_L6N_10	INPUT	LVCMOS25	10
K5	board_id[14]	IOB	IO_L6P_10	INPUT	LVCMOS25	10
K3	board_id[15]	IOB	IO_L7P_10	INPUT	LVCMOS25	10
W7	board_id[2]	IOB	IO_L3P_8	INPUT	LVCMOS25	8
V7	board_id[3]	IOB	IO_L3N_8	INPUT	LVCMOS25	8
R6	board_id[4]	IOB	IO_L23P_VRN_10	INPUT	LVCMOS25	10
P6	board_id[5]	IOB	IO_L21N_10	INPUT	LVCMOS25	10
R7	board_id[6]	IOB	IO_L25N_CC_LC_10	INPUT	LVCMOS25	10

N7	board_id[7]	IOB	IO_L17P_10	INPUT	LVCMOS25	10
M7	board_id[8]	IOB	IO_L17N_10	INPUT	LVCMOS25	10
M5	board_id[9]	IOB	IO_L13N_10	INPUT	LVCMOS25	10
A18	CCLK_aG1_p[0]	IOB	IO_L3N_5	OUTPUT	LVCMOS25	5
A19	CCLK_aG1_p[1]	IOB	IO_L13N_5	OUTPUT	LVCMOS25	5
A20	CCLK_aG1_p[2]	IOB	IO_L13P_5	OUTPUT	LVCMOS25	5
A21	CCLK_aG1_p[3]	IOB	IO_L15N_5	OUTPUT	LVCMOS25	5
A22	CCLK_aG1_p[4]	IOB	IO_L15P_5	OUTPUT	LVCMOS25	5
A23	CCLK_aG1_p[5]	IOB	IO_L8N_CC_LC_5	OUTPUT	LVCMOS25	5
A9	CCLK_aG2_p[0]	IOB	IO_L13P_6	OUTPUT	LVCMOS25	6
A8	CCLK_aG2_p[1]	IOB	IO_L3P_6	OUTPUT	LVCMOS25	6
A7	CCLK_aG2_p[2]	IOB	IO_L3N_6	OUTPUT	LVCMOS25	6
A6	CCLK_aG2_p[3]	IOB	IO_L6P_6	OUTPUT	LVCMOS25	6
A5	CCLK_aG2_p[4]	IOB	IO_L6N_6	OUTPUT	LVCMOS25	6
A4	CCLK_aG2_p[5]	IOB	IO_L15P_6	OUTPUT	LVCMOS25	6
C1	CCLK_aG3_p[0]	IOB	IO_L20N_VREF_6	OUTPUT	LVCMOS25	6
D1	CCLK_aG3_p[1]	IOB	IO_L25N_CC_LC_6	OUTPUT	LVCMOS25	6
E1	CCLK_aG3_p[2]	IOB	IO_L26P_6	OUTPUT	LVCMOS25	6
F1	CCLK_aG3_p[3]	IOB	IO_L26N_6	OUTPUT	LVCMOS25	6
G1	CCLK_aG3_p[4]	IOB	IO_L30N_6	OUTPUT	LVCMOS25	6
H1	CCLK_aG3_p[5]	IOB	IO_L32N_6	OUTPUT	LVCMOS25	6
W1	CCLK_bG1_p[0]	IOB	IO_L1N_8	OUTPUT	LVCMOS25	8
Y1	CCLK_bG1_p[1]	IOB	IO_L6N_8	OUTPUT	LVCMOS25	8
AA1	CCLK_bG1_p[2]	IOB	IO_L10N_8	OUTPUT	LVCMOS25	8
AB1	CCLK_bG1_p[3]	IOB	IO_L10P_8	OUTPUT	LVCMOS25	8
AC1	CCLK_bG1_p[4]	IOB	IO_L14N_8	OUTPUT	LVCMOS25	8
AD1	CCLK_bG1_p[5]	IOB	IO_L16N_8	OUTPUT	LVCMOS25	8
AF3	CCLK_bG2_p[0]	IOB	IO_L15P_8	OUTPUT	LVCMOS25	8
AF4	CCLK_bG2_p[1]	IOB	IO_L17P_8	OUTPUT	LVCMOS25	8
AF5	CCLK_bG2_p[2]	IOB	IO_L19N_8	OUTPUT	LVCMOS25	8
AF6	CCLK_bG2_p[3]	IOB	IO_L19P_8	OUTPUT	LVCMOS25	8
AF7	CCLK_bG2_p[4]	IOB	IO_L25N_CC_LC_8	OUTPUT	LVCMOS25	8
AF8	CCLK_bG2_p[5]	IOB	IO_L25P_CC_LC_8	OUTPUT	LVCMOS25	8
R26	CCLK_bG3_p[0]	IOB	IO_L20P_9	OUTPUT	LVCMOS25	9

T26	CCLK_bG3_p[1]	IOB	IO_L26P_9	OUTPUT	LVCMOS25	9
U26	CCLK_bG3_p[2]	IOB	IO_L26N_9	OUTPUT	LVCMOS25	9
V26	CCLK_bG3_p[3]	IOB	IO_L32P_9	OUTPUT	LVCMOS25	9
U25	CCLK_bG3_p[4]	IOB	IO_L28P_9	OUTPUT	LVCMOS25	9
V25	CCLK_bG3_p[5]	IOB	IO_L32N_9	OUTPUT	LVCMOS25	9
AF22	CCLK_DMA_p	IOB	IO_L30N_SM3_7	TRISTATE	LVTTL	7
AF23	CCLK_DMB_p	IOB	IO_L19P_7	TRISTATE	LVTTL	7
T1	CCLK_IC_p	IOB	IO_L24N_CC_LC_10	TRISTATE	LVCMOS25	10
AA26	CCLK_MCB_p	IOB	IO_L10N_7	TRISTATE	LVTTL	7
A10	CCLK_OUT1_p	IOB	IO_L6P_GC_LC_3	TRISTATE	LVTTL	3
A16	CCLK_OUT2_p	IOB	IO_L5P_GC_LC_3	TRISTATE	LVTTL	3
C13	CCLK_p	IOB	IO_L8P_GC_LC_3	INPUT	LVTTL	3
W26	CCLK_TC_p	IOB	IO_L2N_7	TRISTATE	LVTTL	7
M1	CCLK_VSI0_p	IOB	IO_L11N_10	TRISTATE	LVCMOS25	10
V1	CCLK_VSI1_p	IOB	IO_L30N_10	TRISTATE	LVCMOS25	10
U1	CCLK_WBC_p	IOB	IO_L24P_CC_LC_10	TRISTATE	LVCMOS25	10
AD22	CDATA_33_p[0]	IOB	IO_L15P_7	TRISTATE	LVTTL	7
AD23	CDATA_33_p[1]	IOB	IO_L15N_7	TRISTATE	LVTTL	7
AD25	CDATA_33_p[2]	IOB	IO_L11P_7	TRISTATE	LVTTL	7
AD26	CDATA_33_p[3]	IOB	IO_L11N_7	TRISTATE	LVTTL	7
AC23	CDATA_33_p[4]	IOB	IO_L16P_7	TRISTATE	LVTTL	7
AC24	CDATA_33_p[5]	IOB	IO_L16N_7	TRISTATE	LVTTL	7
AC25	CDATA_33_p[6]	IOB	IO_L9P_CC_LC_7	TRISTATE	LVTTL	7
AC26	CDATA_33_p[7]	IOB	IO_L9N_CC_LC_7	TRISTATE	LVTTL	7
AB21	CDATA_33B_p[0]	IOB	IO_L24N_CC_LC_7	TRISTATE	LVTTL	7
AC21	CDATA_33B_p[1]	IOB	IO_L24P_CC_LC_7	TRISTATE	LVTTL	7
AD20	CDATA_33B_p[2]	IOB	IO_L23N_VRP_7	TRISTATE	LVTTL	7
AE24	CDATA_33B_p[3]	IOB	IO_L22N_7	TRISTATE	LVTTL	7
AF24	CDATA_33B_p[4]	IOB	IO_L22P_7	TRISTATE	LVTTL	7
W19	CDATA_33B_p[5]	IOB	IO_L18N_7	TRISTATE	LVTTL	7
AF19	CDATA_33B_p[6]	IOB	IO_L17P_7	TRISTATE	LVTTL	7
AE18	CDATA_33B_p[7]	IOB	IO_L31N_SM2_7	TRISTATE	LVTTL	7
C17	CDATA_aG1_p[0]	IOB	IO_L1P_5	TRISTATE	LVCMOS25	5
C19	CDATA_aG1_p[1]	IOB	IO_L7P_5	TRISTATE	LVCMOS25	5

C20	CDATA_aG1_p[2]	IOB	IO_L2P_5	TRISTATE	LVCMOS25	5
C21	CDATA_aG1_p[3]	IOB	IO_L6P_5	TRISTATE	LVCMOS25	5
C22	CDATA_aG1_p[4]	IOB	IO_L14N_5	TRISTATE	LVCMOS25	5
C23	CDATA_aG1_p[5]	IOB	IO_L21N_5	TRISTATE	LVCMOS25	5
C24	CDATA_aG1_p[6]	IOB	IO_L16N_5	TRISTATE	LVCMOS25	5
C25	CDATA_aG1_p[7]	IOB	IO_L20N_VREF_5	TRISTATE	LVCMOS25	5
C10	CDATA_aG2_p[0]	IOB	IO_L1N_6	TRISTATE	LVCMOS25	6
C8	CDATA_aG2_p[1]	IOB	IO_L2N_6	TRISTATE	LVCMOS25	6
C7	CDATA_aG2_p[2]	IOB	IO_L11N_6	TRISTATE	LVCMOS25	6
C6	CDATA_aG2_p[3]	IOB	IO_L8N_CC_LC_6	TRISTATE	LVCMOS25	6
C5	CDATA_aG2_p[4]	IOB	IO_L12P_6	TRISTATE	LVCMOS25	6
C4	CDATA_aG2_p[5]	IOB	IO_L16P_6	TRISTATE	LVCMOS25	6
D10	CDATA_aG2_p[6]	IOB	IO_L1P_6	TRISTATE	LVCMOS25	6
D9	CDATA_aG2_p[7]	IOB	IO_L2P_6	TRISTATE	LVCMOS25	6
E3	CDATA_aG3_p[0]	IOB	IO_L24P_CC_LC_6	TRISTATE	LVCMOS25	6
G3	CDATA_aG3_p[1]	IOB	IO_L28N_VREF_6	TRISTATE	LVCMOS25	6
H3	CDATA_aG3_p[2]	IOB	IO_L31N_6	TRISTATE	LVCMOS25	6
E4	CDATA_aG3_p[3]	IOB	IO_L22N_6	TRISTATE	LVCMOS25	6
F4	CDATA_aG3_p[4]	IOB	IO_L27P_6	TRISTATE	LVCMOS25	6
G4	CDATA_aG3_p[5]	IOB	IO_L28P_6	TRISTATE	LVCMOS25	6
H4	CDATA_aG3_p[6]	IOB	IO_L31P_6	TRISTATE	LVCMOS25	6
H5	CDATA_aG3_p[7]	IOB	IO_L29N_6	TRISTATE	LVCMOS25	6
W3	CDATA_bG1_p[0]	IOB	IO_L4N_VREF_8	TRISTATE	LVCMOS25	8
Y3	CDATA_bG1_p[1]	IOB	IO_L8N_CC_LC_8	TRISTATE	LVCMOS25	8
AA3	CDATA_bG1_p[2]	IOB	IO_L7N_8	TRISTATE	LVCMOS25	8
AB3	CDATA_bG1_p[3]	IOB	IO_L12P_8	TRISTATE	LVCMOS25	8
AC3	CDATA_bG1_p[4]	IOB	IO_L18N_8	TRISTATE	LVCMOS25	8
AB4	CDATA_bG1_p[5]	IOB	IO_L11N_8	TRISTATE	LVCMOS25	8
AC4	CDATA_bG1_p[6]	IOB	IO_L11P_8	TRISTATE	LVCMOS25	8
AD4	CDATA_bG1_p[7]	IOB	IO_L22N_8	TRISTATE	LVCMOS25	8
AD5	CDATA_bG2_p[0]	IOB	IO_L22P_8	TRISTATE	LVCMOS25	8
AD6	CDATA_bG2_p[1]	IOB	IO_L30N_8	TRISTATE	LVCMOS25	8
AD7	CDATA_bG2_p[2]	IOB	IO_L23N_VRP_8	TRISTATE	LVCMOS25	8
AD8	CDATA_bG2_p[3]	IOB	IO_L32P_8	TRISTATE	LVCMOS25	8

AC5	CDATA_bG2_p[4]	IOB	IO_L13P_8	TRISTATE	LVCMOS25	8	
AC6	CDATA_bG2_p[5]	IOB	IO_L24P_CC_LC_8	TRISTATE	LVCMOS25	8	
AC7	CDATA_bG2_p[6]	IOB	IO_L28P_8	TRISTATE	LVCMOS25	8	
AC8	CDATA_bG2_p[7]	IOB	IO_L32N_8	TRISTATE	LVCMOS25	8	
L23	CDATA_bG3_p[0]	IOB	IO_L10N_9	TRISTATE	LVCMOS25	9	
M23	CDATA_bG3_p[1]	IOB	IO_L14P_9	TRISTATE	LVCMOS25	9	
N23	CDATA_bG3_p[2]	IOB	IO_L16P_9	TRISTATE	LVCMOS25	9	
P23	CDATA_bG3_p[3]	IOB	IO_L19P_9	TRISTATE	LVCMOS25	9	
R23	CDATA_bG3_p[4]	IOB	IO_L22N_9	TRISTATE	LVCMOS25	9	
T23	CDATA_bG3_p[5]	IOB	IO_L24N_CC_LC_9	TRISTATE	LVCMOS25	9	
U23	CDATA_bG3_p[6]	IOB	IO_L27P_9	TRISTATE	LVCMOS25	9	
V23	CDATA_bG3_p[7]	IOB	IO_L27N_9	TRISTATE	LVCMOS25	9	
J23	CDATA_IC_p[0]	IOB	IO_L2P_9	TRISTATE	LVCMOS25	9	
J22	CDATA_IC_p[1]	IOB	IO_L2N_9	TRISTATE	LVCMOS25	9	
K22	CDATA_IC_p[2]	IOB	IO_L3P_9	TRISTATE	LVCMOS25	9	
K21	CDATA_IC_p[3]	IOB	IO_L3N_9	TRISTATE	LVCMOS25	9	
L19	CDATA_IC_p[4]	IOB	IO_L5P_9	TRISTATE	LVCMOS25	9	
K20	CDATA_IC_p[5]	IOB	IO_L5N_9	TRISTATE	LVCMOS25	9	
L21	CDATA_IC_p[6]	IOB	IO_L6P_9	TRISTATE	LVCMOS25	9	
L20	CDATA_IC_p[7]	IOB	IO_L6N_9	TRISTATE	LVCMOS25	9	
AD13	CDATA_p[0]	IOB	IO_L8N_D0_LC_2	INPUT	LVTTL	2	
AC13	CDATA_p[1]	IOB	IO_L8P_D1_LC_2	INPUT	LVTTL	2	
AC15	CDATA_p[2]	IOB	IO_L7N_D2_LC_2	INPUT	LVTTL	2	
AC16	CDATA_p[3]	IOB	IO_L7P_D3_LC_2	INPUT	LVTTL	2	
AA11	CDATA_p[4]	IOB	IO_L6N_D4_LC_2	INPUT	LVTTL	2	
AA12	CDATA_p[5]	IOB	IO_L6P_D5_LC_2	INPUT	LVTTL	2	
AD14	CDATA_p[6]	IOB	IO_L5N_D6_LC_2	INPUT	LVTTL	2	
AC14	CDATA_p[7]	IOB	IO_L5P_D7_LC_2	INPUT	LVTTL	2	
Y23	CDATA_TC_p[0]	IOB	IO_L12N_VREF_7	TRISTATE	LVTTL	7	
Y24	CDATA_TC_p[1]	IOB	IO_L8N_CC_LC_7	TRISTATE	LVTTL	7	
Y25	CDATA_TC_p[2]	IOB	IO_L6P_7	TRISTATE	LVTTL	7	
Y26	CDATA_TC_p[3]	IOB	IO_L6N_7	TRISTATE	LVTTL	7	
W22	CDATA_TC_p[4]	IOB	IO_L3N_7	TRISTATE	LVTTL	7	
W23	CDATA_TC_p[5]	IOB	IO_L4P_7	TRISTATE	LVTTL	7	

W24	CDATA_TC_p[6]	IOB	IO_L4N_VREF_7	TRISTATE	LVTTL	7
W25	CDATA_TC_p[7]	IOB	IO_L2P_7	TRISTATE	LVTTL	7
R4	CDATA_WBC_p[0]	IOB	IO_L20P_10	TRISTATE	LVCMOS25	10
R3	CDATA_WBC_p[1]	IOB	IO_L20N_VREF_10	TRISTATE	LVCMOS25	10
R2	CDATA_WBC_p[2]	IOB	IO_L22P_10	TRISTATE	LVCMOS25	10
R1	CDATA_WBC_p[3]	IOB	IO_L22N_10	TRISTATE	LVCMOS25	10
P3	CDATA_WBC_p[4]	IOB	IO_L16P_10	TRISTATE	LVCMOS25	10
P2	CDATA_WBC_p[5]	IOB	IO_L16N_10	TRISTATE	LVCMOS25	10
P4	CDATA_WBC_p[6]	IOB	IO_L18N_10	TRISTATE	LVCMOS25	10
P5	CDATA_WBC_p[7]	IOB	IO_L18P_10	TRISTATE	LVCMOS25	10
C15	CHIP_ENA_p	IOB	IO_L3P_GC_LC_3	INPUT	LVTTL	3
D17	DONE_aG1_p[0]	IOB	IO_L1N_5	INPUT	LVCMOS25	5
D18	DONE_aG1_p[1]	IOB	IO_L7N_5	INPUT	LVCMOS25	5
D19	DONE_aG1_p[2]	IOB	IO_L4N_VREF_5	INPUT	LVCMOS25	5
D20	DONE_aG1_p[3]	IOB	IO_L4P_5	INPUT	LVCMOS25	5
D21	DONE_aG1_p[4]	IOB	IO_L12N_VREF_5	INPUT	LVCMOS25	5
D22	DONE_aG1_p[5]	IOB	IO_L14P_5	INPUT	LVCMOS25	5
D8	DONE_aG2_p[0]	IOB	IO_L4P_6	INPUT	LVCMOS25	6
D7	DONE_aG2_p[1]	IOB	IO_L4N_VREF_6	INPUT	LVCMOS25	6
D6	DONE_aG2_p[2]	IOB	IO_L17N_6	INPUT	LVCMOS25	6
D5	DONE_aG2_p[3]	IOB	IO_L12N_VREF_6	INPUT	LVCMOS25	6
D4	DONE_aG2_p[4]	IOB	IO_L16N_6	INPUT	LVCMOS25	6
D3	DONE_aG2_p[5]	IOB	IO_L22P_6	INPUT	LVCMOS25	6
E5	DONE_aG3_p[0]	IOB	IO_L18N_6	INPUT	LVCMOS25	6
G5	DONE_aG3_p[1]	IOB	IO_L23N_VRP_6	INPUT	LVCMOS25	6
E6	DONE_aG3_p[2]	IOB	IO_L18P_6	INPUT	LVCMOS25	6
E7	DONE_aG3_p[3]	IOB	IO_L17P_6	INPUT	LVCMOS25	6
F7	DONE_aG3_p[4]	IOB	IO_L19P_6	INPUT	LVCMOS25	6
G7	DONE_aG3_p[5]	IOB	IO_L19N_6	INPUT	LVCMOS25	6
T4	DONE_bG1_p[0]	IOB	IO_L26P_10	INPUT	LVCMOS25	10
U4	DONE_bG1_p[1]	IOB	IO_L29N_10	INPUT	LVCMOS25	10
V4	DONE_bG1_p[2]	IOB	IO_L29P_10	INPUT	LVCMOS25	10
W4	DONE_bG1_p[3]	IOB	IO_L4P_8	INPUT	LVCMOS25	8
Y4	DONE_bG1_p[4]	IOB	IO_L8P_CC_LC_8	INPUT	LVCMOS25	8

AA4	DONE_bG1_p[5]	IOB	IO_L7P_8	INPUT	LVCMOS25	8
Y5	DONE_bG2_p[0]	IOB	IO_L9N_CC_LC_8	INPUT	LVCMOS25	8
Y6	DONE_bG2_p[1]	IOB	IO_L9P_CC_LC_8	INPUT	LVCMOS25	8
AA7	DONE_bG2_p[2]	IOB	IO_L20P_8	INPUT	LVCMOS25	8
Y7	DONE_bG2_p[3]	IOB	IO_L20N_VREF_8	INPUT	LVCMOS25	8
Y8	DONE_bG2_p[4]	IOB	IO_L26N_8	INPUT	LVCMOS25	8
AA8	DONE_bG2_p[5]	IOB	IO_L26P_8	INPUT	LVCMOS25	8
M22	DONE_bG3_p[0]	IOB	IO_L14N_9	INPUT	LVCMOS25	9
N22	DONE_bG3_p[1]	IOB	IO_L16N_9	INPUT	LVCMOS25	9
P22	DONE_bG3_p[2]	IOB	IO_L19N_9	INPUT	LVCMOS25	9
R22	DONE_bG3_p[3]	IOB	IO_L23P_VRN_9	INPUT	LVCMOS25	9
U22	DONE_bG3_p[4]	IOB	IO_L29P_9	INPUT	LVCMOS25	9
U24	DONE_bG3_p[5]	IOB	IO_L28N_VREF_9	INPUT	LVCMOS25	9
AF20	DONE_DMA_p	IOB	IO_L17N_7	INPUT	LVTTL	7
AE20	DONE_DMB_p	IOB	IO_L23P_VRN_7	INPUT	LVTTL	7
U2	DONE_IC_p	IOB	IO_L28N_VREF_10	INPUT	LVCMOS25	10
AE21	DONE_MCB_p	IOB	IO_L32P_SM1_7	INPUT	LVTTL	7
AB22	DONE_OUT1_p	IOB	IO_L13N_7	INPUT	LVTTL	7
AC22	DONE_OUT2_p	IOB	IO_L13P_7	INPUT	LVTTL	7
Y17	DONE_p[0]	IOB	IO_L27P_SM5_7	OUTPUT	LVTTL	7
Y18	DONE_p[1]	IOB	IO_L21N_7	OUTPUT	LVTTL	7
AB20	DONE_p[10]	IOB	IO_L28P_7	OUTPUT	LVTTL	7
Y19	DONE_p[2]	IOB	IO_L18P_7	OUTPUT	LVTTL	7
Y20	DONE_p[3]	IOB	IO_L20P_7	OUTPUT	LVTTL	7
Y21	DONE_p[4]	IOB	IO_L20N_VREF_7	OUTPUT	LVTTL	7
AA17	DONE_p[5]	IOB	IO_L27N_SM5_7	OUTPUT	LVTTL	7
AA18	DONE_p[6]	IOB	IO_L21P_7	OUTPUT	LVTTL	7
AA19	DONE_p[7]	IOB	IO_L26P_SM6_7	OUTPUT	LVTTL	7
AA20	DONE_p[8]	IOB	IO_L26N_SM6_7	OUTPUT	LVTTL	7
AB18	DONE_p[9]	IOB	IO_L29N_SM4_7	OUTPUT	LVTTL	7
AB23	DONE_TC_p	IOB	IO_L14P_7	INPUT	LVTTL	7
L1	DONE_VSI0_p	IOB	IO_L10P_10	INPUT	LVCMOS25	10
V2	DONE_VSI1_p	IOB	IO_L30P_10	INPUT	LVCMOS25	10
M2	DONE_WBC_p	IOB	IO_L11P_10	INPUT	LVCMOS25	10

AA13	MCB_ADDR_p[0]	IOB	IO_L4N_D8_VREF_LC_2	INPUT	LVTTL	2
AB13	MCB_ADDR_p[1]	IOB	IO_L4P_D9_LC_2	INPUT	LVTTL	2
AA15	MCB_ADDR_p[2]	IOB	IO_L3N_D10_LC_2	INPUT	LVTTL	2
AA16	MCB_ADDR_p[3]	IOB	IO_L3P_D11_LC_2	INPUT	LVTTL	2
AC11	MCB_ADDR_p[4]	IOB	IO_L2N_D12_LC_2	INPUT	LVTTL	2
AC12	MCB_ADDR_p[5]	IOB	IO_L2P_D13_LC_2	INPUT	LVTTL	2
AB14	MCB_ADDR_p[6]	IOB	IO_L1N_D14_CC_LC_2	INPUT	LVTTL	2
AA14	MCB_ADDR_p[7]	IOB	IO_L1P_D15_CC_LC_2	INPUT	LVTTL	2
AE14	MCB_CLK_p	IOB	IO_L5P_GC_LC_4	INPUT	LVTTL	4
AE12	MCB_CS_p	IOB	IO_L1N_GC_LC_4	INPUT	LVTTL	4
D12	MCB_DATA_p[0]	IOB	IO_L8N_D16_CC_LC_1	BIDIR	LVTTL	1
E13	MCB_DATA_p[1]	IOB	IO_L8P_D17_CC_LC_1	BIDIR	LVTTL	1
F15	MCB_DATA_p[10]	IOB	IO_L3N_D26_LC_1	BIDIR	LVTTL	1
F16	MCB_DATA_p[11]	IOB	IO_L3P_D27_LC_1	BIDIR	LVTTL	1
F11	MCB_DATA_p[12]	IOB	IO_L2N_D28_LC_1	BIDIR	LVTTL	1
F12	MCB_DATA_p[13]	IOB	IO_L2P_D29_LC_1	BIDIR	LVTTL	1
F13	MCB_DATA_p[14]	IOB	IO_L1N_D30_LC_1	BIDIR	LVTTL	1
F14	MCB_DATA_p[15]	IOB	IO_L1P_D31_LC_1	BIDIR	LVTTL	1
C16	MCB_DATA_p[2]	IOB	IO_L7N_D18_LC_1	BIDIR	LVTTL	1
D16	MCB_DATA_p[3]	IOB	IO_L7P_D19_LC_1	BIDIR	LVTTL	1
D11	MCB_DATA_p[4]	IOB	IO_L6N_D20_LC_1	BIDIR	LVTTL	1
C11	MCB_DATA_p[5]	IOB	IO_L6P_D21_LC_1	BIDIR	LVTTL	1
E14	MCB_DATA_p[6]	IOB	IO_L5N_D22_LC_1	BIDIR	LVTTL	1
D15	MCB_DATA_p[7]	IOB	IO_L5P_D23_LC_1	BIDIR	LVTTL	1
D13	MCB_DATA_p[8]	IOB	IO_L4N_D24_VREF_LC_1	BIDIR	LVTTL	1
D14	MCB_DATA_p[9]	IOB	IO_L4P_D25_LC_1	BIDIR	LVTTL	1
AF12	MCB_RW_p	IOB	IO_L1P_GC_LC_4	INPUT	LVTTL	4
B13	nPROG_p[0]	IOB	IO_L4P_GC_LC_3	INPUT	LVTTL	3
C14	nPROG_p[1]	IOB	IO_L3N_GC_LC_3	INPUT	LVTTL	3
AD17	nPROG_p[10]	IOB	IO_L7P_GC_VRN_LC_4	INPUT	LVTTL	4
AE10	nPROG_p[2]	IOB	IO_L6P_GC_LC_4	INPUT	LVTTL	4
AD10	nPROG_p[3]	IOB	IO_L6N_GC_LC_4	INPUT	LVTTL	4
B14	nPROG_p[4]	IOB	IO_L1N_GC_CC_LC_3	INPUT	LVTTL	3
A12	nPROG_p[5]	IOB	IO_L2P_GC_VRN_LC_3	INPUT	LVTTL	3

AD11	nPROG_p[6]	IOB	IO_L8N_GC_CC_LC_4	INPUT	LVTTL	4
AD12	nPROG_p[7]	IOB	IO_L8P_GC_CC_LC_4	INPUT	LVTTL	4
AE13	nPROG_p[8]	IOB	IO_L5N_GC_LC_4	INPUT	LVTTL	4
AD16	nPROG_p[9]	IOB	IO_L7N_GC_VRP_LC_4	INPUT	LVTTL	4
B18	PROG_aG1_p[0]	IOB	IO_L3P_5	OUTPUT	LVCMOS25	5
B20	PROG_aG1_p[1]	IOB	IO_L2N_5	OUTPUT	LVCMOS25	5
B21	PROG_aG1_p[2]	IOB	IO_L6N_5	OUTPUT	LVCMOS25	5
B23	PROG_aG1_p[3]	IOB	IO_L10N_5	OUTPUT	LVCMOS25	5
B24	PROG_aG1_p[4]	IOB	IO_L10P_5	OUTPUT	LVCMOS25	5
A24	PROG_aG1_p[5]	IOB	IO_L8P_CC_LC_5	OUTPUT	LVCMOS25	5
B9	PROG_aG2_p[0]	IOB	IO_L13N_6	OUTPUT	LVCMOS25	6
B7	PROG_aG2_p[1]	IOB	IO_L11P_6	OUTPUT	LVCMOS25	6
B6	PROG_aG2_p[2]	IOB	IO_L8P_CC_LC_6	OUTPUT	LVCMOS25	6
B4	PROG_aG2_p[3]	IOB	IO_L15N_6	OUTPUT	LVCMOS25	6
B3	PROG_aG2_p[4]	IOB	IO_L14N_6	OUTPUT	LVCMOS25	6
A3	PROG_aG2_p[5]	IOB	IO_L14P_6	OUTPUT	LVCMOS25	6
C2	PROG_aG3_p[0]	IOB	IO_L20P_6	OUTPUT	LVCMOS25	6
D2	PROG_aG3_p[1]	IOB	IO_L25P_CC_LC_6	OUTPUT	LVCMOS25	6
E2	PROG_aG3_p[2]	IOB	IO_L24N_CC_LC_6	OUTPUT	LVCMOS25	6
F3	PROG_aG3_p[3]	IOB	IO_L27N_6	OUTPUT	LVCMOS25	6
G2	PROG_aG3_p[4]	IOB	IO_L30P_6	OUTPUT	LVCMOS25	6
H2	PROG_aG3_p[5]	IOB	IO_L32P_6	OUTPUT	LVCMOS25	6
W2	PROG_bG1_p[0]	IOB	IO_L1P_8	OUTPUT	LVCMOS25	8
Y2	PROG_bG1_p[1]	IOB	IO_L6P_8	OUTPUT	LVCMOS25	8
AB2	PROG_bG1_p[2]	IOB	IO_L12N_VREF_8	OUTPUT	LVCMOS25	8
AC2	PROG_bG1_p[3]	IOB	IO_L14P_8	OUTPUT	LVCMOS25	8
AD2	PROG_bG1_p[4]	IOB	IO_L16P_8	OUTPUT	LVCMOS25	8
AD3	PROG_bG1_p[5]	IOB	IO_L18P_8	OUTPUT	LVCMOS25	8
AE3	PROG_bG2_p[0]	IOB	IO_L15N_8	OUTPUT	LVCMOS25	8
AE4	PROG_bG2_p[1]	IOB	IO_L17N_8	OUTPUT	LVCMOS25	8
AE6	PROG_bG2_p[2]	IOB	IO_L30P_8	OUTPUT	LVCMOS25	8
AE7	PROG_bG2_p[3]	IOB	IO_L23P_VRN_8	OUTPUT	LVCMOS25	8
AE9	PROG_bG2_p[4]	IOB	IO_L31N_8	OUTPUT	LVCMOS25	8
AF9	PROG_bG2_p[5]	IOB	IO_L31P_8	OUTPUT	LVCMOS25	8

N25	PROG_bG3_p[0]	IOB	IO_L15P_9	OUTPUT	LVCMOS25	9
P25	PROG_bG3_p[1]	IOB	IO_L18P_9	OUTPUT	LVCMOS25	9
R25	PROG_bG3_p[2]	IOB	IO_L20N_VREF_9	OUTPUT	LVCMOS25	9
N24	PROG_bG3_p[3]	IOB	IO_L15N_9	OUTPUT	LVCMOS25	9
P24	PROG_bG3_p[4]	IOB	IO_L18N_9	OUTPUT	LVCMOS25	9
R24	PROG_bG3_p[5]	IOB	IO_L22P_9	OUTPUT	LVCMOS25	9
AF21	PROG_DMA_p	IOB	IO_L30P_SM3_7	OUTPUT	LVTTL	7
AE23	PROG_DMB_p	IOB	IO_L19N_7	OUTPUT	LVTTL	7
N3	PROG_IC_p	IOB	IO_L14P_10	OUTPUT	LVCMOS25	10
AB26	PROG_MCB_p	IOB	IO_L10P_7	OUTPUT	LVTTL	7
AA23	PROG_OUT1_p	IOB	IO_L14N_7	OUTPUT	LVTTL	7
Y22	PROG_OUT2_p	IOB	IO_L12P_7	OUTPUT	LVTTL	7
AB24	PROG_TC_p	IOB	IO_L7P_7	OUTPUT	LVTTL	7
N4	PROG_VSI0_p	IOB	IO_L15N_10	OUTPUT	LVCMOS25	10
N5	PROG_VSI1_p	IOB	IO_L15P_10	OUTPUT	LVCMOS25	10
N2	PROG_WBC_p	IOB	IO_L14N_10	OUTPUT	LVCMOS25	10
B10	RESET_p	IOB	IO_L6N_GC_LC_3	INPUT	LVTTL	3
V21	stat_1V2_A	IOB	IO_L1P_7	INPUT	LVTTL	7
V22	stat_1V2_A1	IOB	IO_L1N_7	INPUT	LVTTL	7
B17	stat_1V2_A2	IOB	IO_L7P_GC_LC_3	INPUT	LVTTL	3
AC20	stat_1V2_B	IOB	IO_L28N_VREF_7	INPUT	LVTTL	7
AC18	stat_1V2_B1	IOB	IO_L29P_SM4_7	INPUT	LVTTL	7
A17	stat_1V2_B2	IOB	IO_L7N_GC_LC_3	INPUT	LVTTL	3
V20	stat_1V5	IOB	IO_L5N_7	INPUT	LVTTL	7
W20	stat_2V5	IOB	IO_L5P_7	INPUT	LVTTL	7
AA24	stat_3V3	IOB	IO_L8P_CC_LC_7	INPUT	LVTTL	7
AB25	stat_5V	IOB	IO_L7N_7	INPUT	LVTTL	7
AF11	test_port[0]	IOB	IO_L4P_GC_LC_4	OUTPUT	LVTTL	4
AC17	test_port[1]	IOB	IO_L3N_GC_LC_4	OUTPUT	LVTTL	4
AB17	test_port[2]	IOB	IO_L3P_GC_LC_4	OUTPUT	LVTTL	4
AB10	test_port[3]	IOB	IO_L2N_GC_LC_4	OUTPUT	LVTTL	4

Table 5-1 Pinout by Signal Name

5.2 Pinouts by Pin Number

Note: UNUSED and NC pins have been removed.

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Release 10.1.03 - par K.39 (nt)
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Mon Jan 05 14:53:14 2009

INPUT FILE:       CFG_top_map.ncd
OUTPUT FILE:      CFG_top_pad.txt
PART TYPE:        xc4vsx35
SPEED GRADE:      -10
PACKAGE:          ff668
```

Pin Number	Signal Name	Pin Usage	Pin Name	Direction	IO Standard	IO Bank
A10	CCLK_OUT1_p	IOB	IO_L6P_GC_LC_3	TRISTATE	LVTTL	3
A12	nPROG_p[5]	IOB	IO_L2P_GC_VRN_LC_3	INPUT	LVTTL	3
A13			GND			
A14			GND			
A16	CCLK_OUT2_p	IOB	IO_L5P_GC_LC_3	TRISTATE	LVTTL	3
A17	stat_1V2_B2	IOB	IO_L7N_GC_LC_3	INPUT	LVTTL	3
A18	CCLK_aG1_p[0]	IOB	IO_L3N_5	OUTPUT	LVCMOS25	5
A19	CCLK_aG1_p[1]	IOB	IO_L13N_5	OUTPUT	LVCMOS25	5
A2			GND			
A20	CCLK_aG1_p[2]	IOB	IO_L13P_5	OUTPUT	LVCMOS25	5
A21	CCLK_aG1_p[3]	IOB	IO_L15N_5	OUTPUT	LVCMOS25	5
A22	CCLK_aG1_p[4]	IOB	IO_L15P_5	OUTPUT	LVCMOS25	5
A23	CCLK_aG1_p[5]	IOB	IO_L8N_CC_LC_5	OUTPUT	LVCMOS25	5
A24	PROG_aG1_p[5]	IOB	IO_L8P_CC_LC_5	OUTPUT	LVCMOS25	5

A25			GND				
A3	PROG_aG2_p[5]	IOB	IO_L14P_6	OUTPUT	LVCMOS25	6	
A4	CCLK_aG2_p[5]	IOB	IO_L15P_6	OUTPUT	LVCMOS25	6	
A5	CCLK_aG2_p[4]	IOB	IO_L6N_6	OUTPUT	LVCMOS25	6	
A6	CCLK_aG2_p[3]	IOB	IO_L6P_6	OUTPUT	LVCMOS25	6	
A7	CCLK_aG2_p[2]	IOB	IO_L3N_6	OUTPUT	LVCMOS25	6	
A8	CCLK_aG2_p[1]	IOB	IO_L3P_6	OUTPUT	LVCMOS25	6	
A9	CCLK_aG2_p[0]	IOB	IO_L13P_6	OUTPUT	LVCMOS25	6	
AA1	CCLK_bG1_p[2]	IOB	IO_L10N_8	OUTPUT	LVCMOS25	8	
AA11	CDATA_p[4]	IOB	IO_L6N_D4_LC_2	INPUT	LVTTL	2	
AA12	CDATA_p[5]	IOB	IO_L6P_D5_LC_2	INPUT	LVTTL	2	
AA13	MCB_ADDR_p[0]	IOB	IO_L4N_D8_VREF_LC_2	INPUT	LVTTL	2	
AA14	MCB_ADDR_p[7]	IOB	IO_L1P_D15_CC_LC_2	INPUT	LVTTL	2	
AA15	MCB_ADDR_p[2]	IOB	IO_L3N_D10_LC_2	INPUT	LVTTL	2	
AA16	MCB_ADDR_p[3]	IOB	IO_L3P_D11_LC_2	INPUT	LVTTL	2	
AA17	DONE_p[5]	IOB	IO_L27N_SM5_7	OUTPUT	LVTTL	7	
AA18	DONE_p[6]	IOB	IO_L21P_7	OUTPUT	LVTTL	7	
AA19	DONE_p[7]	IOB	IO_L26P_SM6_7	OUTPUT	LVTTL	7	
AA2			VCCO_8			8	
AA20	DONE_p[8]	IOB	IO_L26N_SM6_7	OUTPUT	LVTTL	7	
AA21			GND				
AA22			VCCO_7			7	
AA23	PROG_OUT1_p	IOB	IO_L14N_7	OUTPUT	LVTTL	7	
AA24	stat_3V3	IOB	IO_L8P_CC_LC_7	INPUT	LVTTL	7	
AA25			VCCO_7			7	
AA26	CCLK_MCB_p	IOB	IO_L10N_7	TRISTATE	LVTTL	7	
AA3	CDATA_bG1_p[2]	IOB	IO_L7N_8	TRISTATE	LVCMOS25	8	
AA4	DONE_bG1_p[5]	IOB	IO_L7P_8	INPUT	LVCMOS25	8	
AA5			VCCO_8			8	
AA6			GND				
AA7	DONE_bG2_p[2]	IOB	IO_L20P_8	INPUT	LVCMOS25	8	
AA8	DONE_bG2_p[5]	IOB	IO_L26P_8	INPUT	LVCMOS25	8	
AB1	CCLK_bG1_p[3]	IOB	IO_L10P_8	OUTPUT	LVCMOS25	8	
AB10	test_port[3]	IOB	IO_L2N_GC_LC_4	OUTPUT	LVTTL	4	

AB11			VCCO_2			2
AB12			GND			
AB13	MCB_ADDR_p[1]	IOB	IO_L4P_D9_LC_2	INPUT	LVTTL	2
AB14	MCB_ADDR_p[6]	IOB	IO_L1N_D14_CC_LC_2	INPUT	LVTTL	2
AB15			GND			
AB16			VCCO_2			2
AB17	test_port[2]	IOB	IO_L3P_GC_LC_4	OUTPUT	LVTTL	4
AB18	DONE_p[9]	IOB	IO_L29N_SM4_7	OUTPUT	LVTTL	7
AB19			VCCO_7			7
AB2	PROG_bG1_p[2]	IOB	IO_L12N_VREF_8	OUTPUT	LVCMOS25	8
AB20	DONE_p[10]	IOB	IO_L28P_7	OUTPUT	LVTTL	7
AB21	CDATA_33B_p[0]	IOB	IO_L24N_CC_LC_7	TRISTATE	LVTTL	7
AB22	DONE_OUT1_p	IOB	IO_L13N_7	INPUT	LVTTL	7
AB23	DONE_TC_p	IOB	IO_L14P_7	INPUT	LVTTL	7
AB24	PROG_TC_p	IOB	IO_L7P_7	OUTPUT	LVTTL	7
AB25	stat_5V	IOB	IO_L7N_7	INPUT	LVTTL	7
AB26	PROG_MCB_p	IOB	IO_L10P_7	OUTPUT	LVTTL	7
AB3	CDATA_bG1_p[3]	IOB	IO_L12P_8	TRISTATE	LVCMOS25	8
AB4	CDATA_bG1_p[5]	IOB	IO_L11N_8	TRISTATE	LVCMOS25	8
AB8			VCCO_8			8
AC1	CCLK_bG1_p[4]	IOB	IO_L14N_8	OUTPUT	LVCMOS25	8
AC11	MCB_ADDR_p[4]	IOB	IO_L2N_D12_LC_2	INPUT	LVTTL	2
AC12	MCB_ADDR_p[5]	IOB	IO_L2P_D13_LC_2	INPUT	LVTTL	2
AC13	CDATA_p[1]	IOB	IO_L8P_D1_LC_2	INPUT	LVTTL	2
AC14	CDATA_p[7]	IOB	IO_L5P_D7_LC_2	INPUT	LVTTL	2
AC15	CDATA_p[2]	IOB	IO_L7N_D2_LC_2	INPUT	LVTTL	2
AC16	CDATA_p[3]	IOB	IO_L7P_D3_LC_2	INPUT	LVTTL	2
AC17	test_port[1]	IOB	IO_L3N_GC_LC_4	OUTPUT	LVTTL	4
AC18	stat_1V2_B1	IOB	IO_L29P_SM4_7	INPUT	LVTTL	7
AC2	PROG_bG1_p[3]	IOB	IO_L14P_8	OUTPUT	LVCMOS25	8
AC20	stat_1V2_B	IOB	IO_L28N_VREF_7	INPUT	LVTTL	7
AC21	CDATA_33B_p[1]	IOB	IO_L24P_CC_LC_7	TRISTATE	LVTTL	7
AC22	DONE_OUT2_p	IOB	IO_L13P_7	INPUT	LVTTL	7
AC23	CDATA_33_p[4]	IOB	IO_L16P_7	TRISTATE	LVTTL	7

AC24	CDATA_33_p[5]	IOB	IO_L16N_7	TRISTATE	LVTTL	7	
AC25	CDATA_33_p[6]	IOB	IO_L9P_CC_LC_7	TRISTATE	LVTTL	7	
AC26	CDATA_33_p[7]	IOB	IO_L9N_CC_LC_7	TRISTATE	LVTTL	7	
AC3	CDATA_bG1_p[4]	IOB	IO_L18N_8	TRISTATE	LVCMOS25	8	
AC4	CDATA_bG1_p[6]	IOB	IO_L11P_8	TRISTATE	LVCMOS25	8	
AC5	CDATA_bG2_p[4]	IOB	IO_L13P_8	TRISTATE	LVCMOS25	8	
AC6	CDATA_bG2_p[5]	IOB	IO_L24P_CC_LC_8	TRISTATE	LVCMOS25	8	
AC7	CDATA_bG2_p[6]	IOB	IO_L28P_8	TRISTATE	LVCMOS25	8	
AC8	CDATA_bG2_p[7]	IOB	IO_L32N_8	TRISTATE	LVCMOS25	8	
AD1	CCLK_bG1_p[5]	IOB	IO_L16N_8	OUTPUT	LVCMOS25	8	
AD10	nPROG_p[3]	IOB	IO_L6N_GC_LC_4	INPUT	LVTTL	4	
AD11	nPROG_p[6]	IOB	IO_L8N_GC_CC_LC_4	INPUT	LVTTL	4	
AD12	nPROG_p[7]	IOB	IO_L8P_GC_CC_LC_4	INPUT	LVTTL	4	
AD13	CDATA_p[0]	IOB	IO_L8N_D0_LC_2	INPUT	LVTTL	2	
AD14	CDATA_p[6]	IOB	IO_L5N_D6_LC_2	INPUT	LVTTL	2	
AD15			VCCO_4			4	
AD16	nPROG_p[9]	IOB	IO_L7N_GC_VRP_LC_4	INPUT	LVTTL	4	
AD17	nPROG_p[10]	IOB	IO_L7P_GC_VRN_LC_4	INPUT	LVTTL	4	
AD18			GND				
AD2	PROG_bG1_p[4]	IOB	IO_L16P_8	OUTPUT	LVCMOS25	8	
AD20	CDATA_33B_p[2]	IOB	IO_L23N_VRP_7	TRISTATE	LVTTL	7	
AD22	CDATA_33_p[0]	IOB	IO_L15P_7	TRISTATE	LVTTL	7	
AD23	CDATA_33_p[1]	IOB	IO_L15N_7	TRISTATE	LVTTL	7	
AD24			GND				
AD25	CDATA_33_p[2]	IOB	IO_L11P_7	TRISTATE	LVTTL	7	
AD26	CDATA_33_p[3]	IOB	IO_L11N_7	TRISTATE	LVTTL	7	
AD3	PROG_bG1_p[5]	IOB	IO_L18P_8	OUTPUT	LVCMOS25	8	
AD4	CDATA_bG1_p[7]	IOB	IO_L22N_8	TRISTATE	LVCMOS25	8	
AD5	CDATA_bG2_p[0]	IOB	IO_L22P_8	TRISTATE	LVCMOS25	8	
AD6	CDATA_bG2_p[1]	IOB	IO_L30N_8	TRISTATE	LVCMOS25	8	
AD7	CDATA_bG2_p[2]	IOB	IO_L23N_VRP_8	TRISTATE	LVCMOS25	8	
AD8	CDATA_bG2_p[3]	IOB	IO_L32P_8	TRISTATE	LVCMOS25	8	
AD9			GND				
AE1			GND				

AE10	nPROG_p[2]	IOB	IO_L6P_GC_LC_4	INPUT	LVTTL	4
AE11			VCCO_4			4
AE12	MCB_CS_p	IOB	IO_L1N_GC_LC_4	INPUT	LVTTL	4
AE13	nPROG_p[8]	IOB	IO_L5N_GC_LC_4	INPUT	LVTTL	4
AE14	MCB_CLK_p	IOB	IO_L5P_GC_LC_4	INPUT	LVTTL	4
AE15			VREFN_SM			
AE16			VREFP_SM			
AE17			AVSS_SM			
AE18	CDATA_33B_p[7]	IOB	IO_L31N_SM2_7	TRISTATE	LVTTL	7
AE19			VCCO_7			7
AE2			GND			
AE20	DONE_DMB_p	IOB	IO_L23P_VRN_7	INPUT	LVTTL	7
AE21	DONE_MCB_p	IOB	IO_L32P_SM1_7	INPUT	LVTTL	7
AE22			VCCO_7			7
AE23	PROG_DMB_p	IOB	IO_L19N_7	OUTPUT	LVTTL	7
AE24	CDATA_33B_p[3]	IOB	IO_L22N_7	TRISTATE	LVTTL	7
AE25			GND			
AE26			GND			
AE3	PROG_bG2_p[0]	IOB	IO_L15N_8	OUTPUT	LVCMOS25	8
AE4	PROG_bG2_p[1]	IOB	IO_L17N_8	OUTPUT	LVCMOS25	8
AE5			VCCO_8			8
AE6	PROG_bG2_p[2]	IOB	IO_L30P_8	OUTPUT	LVCMOS25	8
AE7	PROG_bG2_p[3]	IOB	IO_L23P_VRN_8	OUTPUT	LVCMOS25	8
AE8			VCCO_8			8
AE9	PROG_bG2_p[4]	IOB	IO_L31N_8	OUTPUT	LVCMOS25	8
AF11	test_port[0]	IOB	IO_L4P_GC_LC_4	OUTPUT	LVTTL	4
AF12	MCB_RW_p	IOB	IO_L1P_GC_LC_4	INPUT	LVTTL	4
AF13			GND			
AF14			GND			
AF17			AVDD_SM			
AF19	CDATA_33B_p[6]	IOB	IO_L17P_7	TRISTATE	LVTTL	7
AF2			GND			
AF20	DONE_DMA_p	IOB	IO_L17N_7	INPUT	LVTTL	7
AF21	PROG_DMA_p	IOB	IO_L30P_SM3_7	OUTPUT	LVTTL	7

AF22	CCLK_DMA_p	IOB	IO_L30N_SM3_7	TRISTATE	LVTTL	7	
AF23	CCLK_DMB_p	IOB	IO_L19P_7	TRISTATE	LVTTL	7	
AF24	CDATA_33B_p[4]	IOB	IO_L22P_7	TRISTATE	LVTTL	7	
AF25			GND				
AF3	CCLK_bG2_p[0]	IOB	IO_L15P_8	OUTPUT	LVCMOS25	8	
AF4	CCLK_bG2_p[1]	IOB	IO_L17P_8	OUTPUT	LVCMOS25	8	
AF5	CCLK_bG2_p[2]	IOB	IO_L19N_8	OUTPUT	LVCMOS25	8	
AF6	CCLK_bG2_p[3]	IOB	IO_L19P_8	OUTPUT	LVCMOS25	8	
AF7	CCLK_bG2_p[4]	IOB	IO_L25N_CC_LC_8	OUTPUT	LVCMOS25	8	
AF8	CCLK_bG2_p[5]	IOB	IO_L25P_CC_LC_8	OUTPUT	LVCMOS25	8	
AF9	PROG_bG2_p[5]	IOB	IO_L31P_8	OUTPUT	LVCMOS25	8	
B1			GND				
B10	RESET_p	IOB	IO_L6N_GC_LC_3	INPUT	LVTTL	3	
B11			VCCO_3			3	
B13	nPROG_p[0]	IOB	IO_L4P_GC_LC_3	INPUT	LVTTL	3	
B14	nPROG_p[4]	IOB	IO_L1N_GC_CC_LC_3	INPUT	LVTTL	3	
B16			VCCO_3			3	
B17	stat_1V2_A2	IOB	IO_L7P_GC_LC_3	INPUT	LVTTL	3	
B18	PROG_aG1_p[0]	IOB	IO_L3P_5	OUTPUT	LVCMOS25	5	
B19			VCCO_5			5	
B2			GND				
B20	PROG_aG1_p[1]	IOB	IO_L2N_5	OUTPUT	LVCMOS25	5	
B21	PROG_aG1_p[2]	IOB	IO_L6N_5	OUTPUT	LVCMOS25	5	
B22			VCCO_5			5	
B23	PROG_aG1_p[3]	IOB	IO_L10N_5	OUTPUT	LVCMOS25	5	
B24	PROG_aG1_p[4]	IOB	IO_L10P_5	OUTPUT	LVCMOS25	5	
B25			GND				
B26			GND				
B3	PROG_aG2_p[4]	IOB	IO_L14N_6	OUTPUT	LVCMOS25	6	
B4	PROG_aG2_p[3]	IOB	IO_L15N_6	OUTPUT	LVCMOS25	6	
B5			VCCO_6			6	
B6	PROG_aG2_p[2]	IOB	IO_L8P_CC_LC_6	OUTPUT	LVCMOS25	6	
B7	PROG_aG2_p[1]	IOB	IO_L11P_6	OUTPUT	LVCMOS25	6	
B8			VCCO_6			6	

B9	PROG_aG2_p[0]	IOB	IO_L13N_6	OUTPUT	LVCMOS25	6
C1	CCLK_aG3_p[0]	IOB	IO_L20N_VREF_6	OUTPUT	LVCMOS25	6
C10	CDATA_aG2_p[0]	IOB	IO_L1N_6	TRISTATE	LVCMOS25	6
C11	MCB_DATA_p[5]	IOB	IO_L6P_D21_LC_1	BIDIR	LVTTL	1
C13	CCLK_p	IOB	IO_L8P_GC_LC_3	INPUT	LVTTL	3
C14	nPROG_p[1]	IOB	IO_L3N_GC_LC_3	INPUT	LVTTL	3
C15	CHIP_ENA_p	IOB	IO_L3P_GC_LC_3	INPUT	LVTTL	3
C16	MCB_DATA_p[2]	IOB	IO_L7N_D18_LC_1	BIDIR	LVTTL	1
C17	CDATA_aG1_p[0]	IOB	IO_L1P_5	TRISTATE	LVCMOS25	5
C18			GND			
C19	CDATA_aG1_p[1]	IOB	IO_L7P_5	TRISTATE	LVCMOS25	5
C2	PROG_aG3_p[0]	IOB	IO_L20P_6	OUTPUT	LVCMOS25	6
C20	CDATA_aG1_p[2]	IOB	IO_L2P_5	TRISTATE	LVCMOS25	5
C21	CDATA_aG1_p[3]	IOB	IO_L6P_5	TRISTATE	LVCMOS25	5
C22	CDATA_aG1_p[4]	IOB	IO_L14N_5	TRISTATE	LVCMOS25	5
C23	CDATA_aG1_p[5]	IOB	IO_L21N_5	TRISTATE	LVCMOS25	5
C24	CDATA_aG1_p[6]	IOB	IO_L16N_5	TRISTATE	LVCMOS25	5
C25	CDATA_aG1_p[7]	IOB	IO_L20N_VREF_5	TRISTATE	LVCMOS25	5
C3			GND			
C4	CDATA_aG2_p[5]	IOB	IO_L16P_6	TRISTATE	LVCMOS25	6
C5	CDATA_aG2_p[4]	IOB	IO_L12P_6	TRISTATE	LVCMOS25	6
C6	CDATA_aG2_p[3]	IOB	IO_L8N_CC_LC_6	TRISTATE	LVCMOS25	6
C7	CDATA_aG2_p[2]	IOB	IO_L11N_6	TRISTATE	LVCMOS25	6
C8	CDATA_aG2_p[1]	IOB	IO_L2N_6	TRISTATE	LVCMOS25	6
C9			GND			
D1	CCLK_aG3_p[1]	IOB	IO_L25N_CC_LC_6	OUTPUT	LVCMOS25	6
D10	CDATA_aG2_p[6]	IOB	IO_L1P_6	TRISTATE	LVCMOS25	6
D11	MCB_DATA_p[4]	IOB	IO_L6N_D20_LC_1	BIDIR	LVTTL	1
D12	MCB_DATA_p[0]	IOB	IO_L8N_D16_CC_LC_1	BIDIR	LVTTL	1
D13	MCB_DATA_p[8]	IOB	IO_L4N_D24_VREF_LC_1	BIDIR	LVTTL	1
D14	MCB_DATA_p[9]	IOB	IO_L4P_D25_LC_1	BIDIR	LVTTL	1
D15	MCB_DATA_p[7]	IOB	IO_L5P_D23_LC_1	BIDIR	LVTTL	1
D16	MCB_DATA_p[3]	IOB	IO_L7P_D19_LC_1	BIDIR	LVTTL	1
D17	DONE_aG1_p[0]	IOB	IO_L1N_5	INPUT	LVCMOS25	5

D18	DONE_aG1_p[1]	IOB	IO_L7N_5	INPUT	LVCMOS25	5
D19	DONE_aG1_p[2]	IOB	IO_L4N_VREF_5	INPUT	LVCMOS25	5
D2	PROG_aG3_p[1]	IOB	IO_L25P_CC_LC_6	OUTPUT	LVCMOS25	6
D20	DONE_aG1_p[3]	IOB	IO_L4P_5	INPUT	LVCMOS25	5
D21	DONE_aG1_p[4]	IOB	IO_L12N_VREF_5	INPUT	LVCMOS25	5
D22	DONE_aG1_p[5]	IOB	IO_L14P_5	INPUT	LVCMOS25	5
D3	DONE_aG2_p[5]	IOB	IO_L22P_6	INPUT	LVCMOS25	6
D4	DONE_aG2_p[4]	IOB	IO_L16N_6	INPUT	LVCMOS25	6
D5	DONE_aG2_p[3]	IOB	IO_L12N_VREF_6	INPUT	LVCMOS25	6
D6	DONE_aG2_p[2]	IOB	IO_L17N_6	INPUT	LVCMOS25	6
D7	DONE_aG2_p[1]	IOB	IO_L4N_VREF_6	INPUT	LVCMOS25	6
D8	DONE_aG2_p[0]	IOB	IO_L4P_6	INPUT	LVCMOS25	6
D9	CDATA_aG2_p[7]	IOB	IO_L2P_6	TRISTATE	LVCMOS25	6
E1	CCLK_aG3_p[2]	IOB	IO_L26P_6	OUTPUT	LVCMOS25	6
E11			VCCO_1			1
E12			GND			
E13	MCB_DATA_p[1]	IOB	IO_L8P_D17_CC_LC_1	BIDIR	LVTTL	1
E14	MCB_DATA_p[6]	IOB	IO_L5N_D22_LC_1	BIDIR	LVTTL	1
E15			GND			
E16			VCCO_1			1
E19			VCCO_5			5
E2	PROG_aG3_p[2]	IOB	IO_L24N_CC_LC_6	OUTPUT	LVCMOS25	6
E3	CDATA_aG3_p[0]	IOB	IO_L24P_CC_LC_6	TRISTATE	LVCMOS25	6
E4	CDATA_aG3_p[3]	IOB	IO_L22N_6	TRISTATE	LVCMOS25	6
E5	DONE_aG3_p[0]	IOB	IO_L18N_6	INPUT	LVCMOS25	6
E6	DONE_aG3_p[2]	IOB	IO_L18P_6	INPUT	LVCMOS25	6
E7	DONE_aG3_p[3]	IOB	IO_L17P_6	INPUT	LVCMOS25	6
E8			VCCO_6			6
F1	CCLK_aG3_p[3]	IOB	IO_L26N_6	OUTPUT	LVCMOS25	6
F11	MCB_DATA_p[12]	IOB	IO_L2N_D28_LC_1	BIDIR	LVTTL	1
F12	MCB_DATA_p[13]	IOB	IO_L2P_D29_LC_1	BIDIR	LVTTL	1
F13	MCB_DATA_p[14]	IOB	IO_L1N_D30_LC_1	BIDIR	LVTTL	1
F14	MCB_DATA_p[15]	IOB	IO_L1P_D31_LC_1	BIDIR	LVTTL	1
F15	MCB_DATA_p[10]	IOB	IO_L3N_D26_LC_1	BIDIR	LVTTL	1

F16	MCB_DATA_p[11]	IOB	IO_L3P_D27_LC_1	BIDIR	LVTTL	1
F2			VCCO_6			6
F21			GND			
F22			VCCO_5			5
F25			VCCO_5			5
F3	PROG_aG3_p[3]	IOB	IO_L27N_6	OUTPUT	LVCMOS25	6
F4	CDATA_aG3_p[4]	IOB	IO_L27P_6	TRISTATE	LVCMOS25	6
F5			VCCO_6			6
F6			GND			
F7	DONE_aG3_p[4]	IOB	IO_L19P_6	INPUT	LVCMOS25	6
G1	CCLK_aG3_p[4]	IOB	IO_L30N_6	OUTPUT	LVCMOS25	6
G11			CS_B_0			
G12			D_IN_0			
G13			TDN_0			
G14			CCLK_0			
G15			INIT_0			
G16			HSWAPEN_0			
G2	PROG_aG3_p[4]	IOB	IO_L30P_6	OUTPUT	LVCMOS25	6
G3	CDATA_aG3_p[1]	IOB	IO_L28N_VREF_6	TRISTATE	LVCMOS25	6
G4	CDATA_aG3_p[5]	IOB	IO_L28P_6	TRISTATE	LVCMOS25	6
G5	DONE_aG3_p[1]	IOB	IO_L23N_VRP_6	INPUT	LVCMOS25	6
G7	DONE_aG3_p[5]	IOB	IO_L19N_6	INPUT	LVCMOS25	6
H1	CCLK_aG3_p[5]	IOB	IO_L32N_6	OUTPUT	LVCMOS25	6
H10			VCCO_6			6
H11			VCCAUX			
H12			RDWR_B_0			
H13			TDP_0			
H14			DONE_0			
H15			PROGRAM_B_0			
H16			VCCAUX			
H17			VCCAUX			
H18			VCCO_5			5
H19			VCCO_5			5
H2	PROG_aG3_p[5]	IOB	IO_L32P_6	OUTPUT	LVCMOS25	6

H3	CDATA_aG3_p[2]	IOB	IO_L31N_6	TRISTATE	LVCMOS25	6
H4	CDATA_aG3_p[6]	IOB	IO_L31P_6	TRISTATE	LVCMOS25	6
H5	CDATA_aG3_p[7]	IOB	IO_L29N_6	TRISTATE	LVCMOS25	6
H9			VCCO_6			6
J10			VCCINT			
J11			VCCINT			
J12			VCCAUX			
J13			GND			
J14			GND			
J15			VCCO_0			0
J16			VCCINT			
J17			VCCINT			
J19			VCCO_5			5
J22	CDATA_IC_p[1]	IOB	IO_L2N_9	TRISTATE	LVCMOS25	9
J23	CDATA_IC_p[0]	IOB	IO_L2P_9	TRISTATE	LVCMOS25	9
J24			GND			
J3			GND			
J8			VCCO_6			6
K10			VCCINT			
K11			GND			
K12			GND			
K13			GND			
K14			GND			
K15			GND			
K16			GND			
K17			VCCINT			
K18			VCCINT			
K19			VCCO_9			9
K20	CDATA_IC_p[5]	IOB	IO_L5N_9	TRISTATE	LVCMOS25	9
K21	CDATA_IC_p[3]	IOB	IO_L3N_9	TRISTATE	LVCMOS25	9
K22	CDATA_IC_p[2]	IOB	IO_L3P_9	TRISTATE	LVCMOS25	9
K3	board_id[15]	IOB	IO_L7P_10	INPUT	LVCMOS25	10
K4	board_id[13]	IOB	IO_L6N_10	INPUT	LVCMOS25	10
K5	board_id[14]	IOB	IO_L6P_10	INPUT	LVCMOS25	10

K6	board_id[11]	IOB	IO_L3N_10	INPUT	LVCMOS25	10
K8			VCCO_10			10
K9			VCCINT			
L1	DONE_VSI0_p	IOB	IO_L10P_10	INPUT	LVCMOS25	10
L10			VCCINT			
L11			VCCINT			
L12			GND			
L13			GND			
L14			GND			
L15			GND			
L16			VCCINT			
L17			VCCINT			
L18			VCCINT			
L19	CDATA_IC_p[4]	IOB	IO_L5P_9	TRISTATE	LVCMOS25	9
L2			VCCO_10			10
L20	CDATA_IC_p[7]	IOB	IO_L6N_9	TRISTATE	LVCMOS25	9
L21	CDATA_IC_p[6]	IOB	IO_L6P_9	TRISTATE	LVCMOS25	9
L22			VCCO_9			9
L23	CDATA_bG3_p[0]	IOB	IO_L10N_9	TRISTATE	LVCMOS25	9
L25			VCCO_9			9
L5			VCCO_10			10
L6	board_id[12]	IOB	IO_L5N_10	INPUT	LVCMOS25	10
L9			VCCINT			
M1	CCLK_VSI0_p	IOB	IO_L11N_10	TRISTATE	LVCMOS25	10
M10			GND			
M11			GND			
M12			VCCINT			
M13			GND			
M14			GND			
M15			VCCINT			
M16			GND			
M17			GND			
M18			VCCO_9			9
M2	DONE_WBC_p	IOB	IO_L11P_10	INPUT	LVCMOS25	10

M22	DONE_bG3_p[0]	IOB	IO_L14N_9	INPUT	LVCMOS25	9	
M23	CDATA_bG3_p[1]	IOB	IO_L14P_9	TRISTATE	LVCMOS25	9	
M5	board_id[9]	IOB	IO_L13N_10	INPUT	LVCMOS25	10	
M6	board_id[10]	IOB	IO_L13P_10	INPUT	LVCMOS25	10	
M7	board_id[8]	IOB	IO_L17N_10	INPUT	LVCMOS25	10	
M9			VCCAUX				
N1			VCCO_10			10	
N10			GND				
N11			GND				
N12			GND				
N13			GND				
N14			GND				
N15			GND				
N16			GND				
N17			GND				
N18			VCCAUX				
N2	PROG_WBC_p	IOB	IO_L14N_10	OUTPUT	LVCMOS25	10	
N22	DONE_bG3_p[1]	IOB	IO_L16N_9	INPUT	LVCMOS25	9	
N23	CDATA_bG3_p[2]	IOB	IO_L16P_9	TRISTATE	LVCMOS25	9	
N24	PROG_bG3_p[3]	IOB	IO_L15N_9	OUTPUT	LVCMOS25	9	
N25	PROG_bG3_p[0]	IOB	IO_L15P_9	OUTPUT	LVCMOS25	9	
N26			GND				
N3	PROG_IC_p	IOB	IO_L14P_10	OUTPUT	LVCMOS25	10	
N4	PROG_VSI0_p	IOB	IO_L15N_10	OUTPUT	LVCMOS25	10	
N5	PROG_VSI1_p	IOB	IO_L15P_10	OUTPUT	LVCMOS25	10	
N6			GND				
N7	board_id[7]	IOB	IO_L17P_10	INPUT	LVCMOS25	10	
N9			VCCAUX				
P1			GND				
P10			GND				
P11			GND				
P12			GND				
P13			GND				
P14			GND				

P15			GND				
P16			GND				
P17			GND				
P18			VCCAUX				
P2	CDATA_WBC_p[5]	IOB	IO_L16N_10	TRISTATE	LVCMOS25	10
P21			GND				
P22	DONE_bG3_p[2]	IOB	IO_L19N_9	INPUT	LVCMOS25	9
P23	CDATA_bG3_p[3]	IOB	IO_L19P_9	TRISTATE	LVCMOS25	9
P24	PROG_bG3_p[4]	IOB	IO_L18N_9	OUTPUT	LVCMOS25	9
P25	PROG_bG3_p[1]	IOB	IO_L18P_9	OUTPUT	LVCMOS25	9
P26			VCCO_9			9
P3	CDATA_WBC_p[4]	IOB	IO_L16P_10	TRISTATE	LVCMOS25	10
P4	CDATA_WBC_p[6]	IOB	IO_L18N_10	TRISTATE	LVCMOS25	10
P5	CDATA_WBC_p[7]	IOB	IO_L18P_10	TRISTATE	LVCMOS25	10
P6	board_id[5]	IOB	IO_L21N_10	INPUT	LVCMOS25	10
P9			VCCAUX			
R1	CDATA_WBC_p[3]	IOB	IO_L22N_10	TRISTATE	LVCMOS25	10
R10			GND			
R11			GND			
R12			VCCINT			
R13			GND			
R14			GND			
R15			VCCINT			
R16			GND			
R17			GND			
R18			VCCAUX			
R2	CDATA_WBC_p[2]	IOB	IO_L22P_10	TRISTATE	LVCMOS25	10
R22	DONE_bG3_p[3]	IOB	IO_L23P_VRN_9	INPUT	LVCMOS25	9
R23	CDATA_bG3_p[4]	IOB	IO_L22N_9	TRISTATE	LVCMOS25	9
R24	PROG_bG3_p[5]	IOB	IO_L22P_9	OUTPUT	LVCMOS25	9
R25	PROG_bG3_p[2]	IOB	IO_L20N_VREF_9	OUTPUT	LVCMOS25	9
R26	CCLK_bG3_p[0]	IOB	IO_L20P_9	OUTPUT	LVCMOS25	9
R3	CDATA_WBC_p[1]	IOB	IO_L20N_VREF_10	TRISTATE	LVCMOS25	10
R4	CDATA_WBC_p[0]	IOB	IO_L20P_10	TRISTATE	LVCMOS25	10

R6	board_id[4]	IOB	IO_L23P_VRN_10	INPUT	LVCMOS25	10
R7	board_id[6]	IOB	IO_L25N_CC_LC_10	INPUT	LVCMOS25	10
R9			VCCO_10			10
T1	CCLK_IC_p	IOB	IO_L24N_CC_LC_10	TRISTATE	LVCMOS25	10
T10			VCCINT			
T11			VCCINT			
T12			GND			
T13			GND			
T14			GND			
T15			GND			
T16			VCCINT			
T17			VCCINT			
T18			VCCINT			
T2			VCCO_10			10
T22			VCCO_9			9
T23	CDATA_bG3_p[5]	IOB	IO_L24N_CC_LC_9	TRISTATE	LVCMOS25	9
T25			VCCO_9			9
T26	CCLK_bG3_p[1]	IOB	IO_L26P_9	OUTPUT	LVCMOS25	9
T4	DONE_bG1_p[0]	IOB	IO_L26P_10	INPUT	LVCMOS25	10
T5			VCCO_10			10
T9			VCCINT			
U1	CCLK_WBC_p	IOB	IO_L24P_CC_LC_10	TRISTATE	LVCMOS25	10
U10			VCCINT			
U11			GND			
U12			GND			
U13			GND			
U14			GND			
U15			GND			
U16			GND			
U17			VCCINT			
U18			VCCINT			
U19			VCCO_9			9
U2	DONE_IC_p	IOB	IO_L28N_VREF_10	INPUT	LVCMOS25	10
U22	DONE_bG3_p[4]	IOB	IO_L29P_9	INPUT	LVCMOS25	9

U23	CDATA_bG3_p[6]	IOB	IO_L27P_9	TRISTATE	LVCMOS25	9
U24	DONE_bG3_p[5]	IOB	IO_L28N_VREF_9	INPUT	LVCMOS25	9
U25	CCLK_bG3_p[4]	IOB	IO_L28P_9	OUTPUT	LVCMOS25	9
U26	CCLK_bG3_p[2]	IOB	IO_L26N_9	OUTPUT	LVCMOS25	9
U4	DONE_bG1_p[1]	IOB	IO_L29N_10	INPUT	LVCMOS25	10
U8			VCCO_10			10
U9			VCCINT			
V1	CCLK_VSI1_p	IOB	IO_L30N_10	TRISTATE	LVCMOS25	10
V10			VCCINT			
V11			VCCINT			
V12			VCCO_0			0
V13			GND			
V14			GND			
V15			VCCAUX			
V16			VCCINT			
V17			VCCINT			
V19			VCCO_7			7
V2	DONE_VSI1_p	IOB	IO_L30P_10	INPUT	LVCMOS25	10
V20	stat_1V5	IOB	IO_L5N_7	INPUT	LVTTL	7
V21	stat_1V2_A	IOB	IO_L1P_7	INPUT	LVTTL	7
V22	stat_1V2_A1	IOB	IO_L1N_7	INPUT	LVTTL	7
V23	CDATA_bG3_p[7]	IOB	IO_L27N_9	TRISTATE	LVCMOS25	9
V24			GND			
V25	CCLK_bG3_p[5]	IOB	IO_L32N_9	OUTPUT	LVCMOS25	9
V26	CCLK_bG3_p[3]	IOB	IO_L32P_9	OUTPUT	LVCMOS25	9
V3			GND			
V4	DONE_bG1_p[2]	IOB	IO_L29P_10	INPUT	LVCMOS25	10
V7	board_id[3]	IOB	IO_L3N_8	INPUT	LVCMOS25	8
V8			VCCO_8			8
W1	CCLK_bG1_p[0]	IOB	IO_L1N_8	OUTPUT	LVCMOS25	8
W10			VCCAUX			
W11			VCCAUX			
W12			TCK_0			
W13			PWRDWN_B_0			

W14			|M2_0				
W15			|M0_0				
W16			|VCCAUX				
W17			|VCCO_7			|7
W18			|VCCO_7			|7
W19	CDATA_33B_p[5]	IOB	IO_L18N_7	TRISTATE	LVTTL	7
W2	PROG_bG1_p[0]	IOB	IO_L1P_8	OUTPUT	LVCMOS25	8
W20	stat_2V5	IOB	IO_L5P_7	INPUT	LVTTL	7
W22	CDATA_TC_p[4]	IOB	IO_L3N_7	TRISTATE	LVTTL	7
W23	CDATA_TC_p[5]	IOB	IO_L4P_7	TRISTATE	LVTTL	7
W24	CDATA_TC_p[6]	IOB	IO_L4N_VREF_7	TRISTATE	LVTTL	7
W25	CDATA_TC_p[7]	IOB	IO_L2P_7	TRISTATE	LVTTL	7
W26	CCLK_TC_p	IOB	IO_L2N_7	TRISTATE	LVTTL	7
W3	CDATA_bG1_p[0]	IOB	IO_L4N_VREF_8	TRISTATE	LVCMOS25	8
W4	DONE_bG1_p[3]	IOB	IO_L4P_8	INPUT	LVCMOS25	8
W5	board_id[0]	IOB	IO_L5N_8	INPUT	LVCMOS25	8
W6	board_id[1]	IOB	IO_L5P_8	INPUT	LVCMOS25	8
W7	board_id[2]	IOB	IO_L3P_8	INPUT	LVCMOS25	8
W8			|VCCO_8			|8
W9			|VCCO_8			|8
Y1	CCLK_bG1_p[1]	IOB	IO_L6N_8	OUTPUT	LVCMOS25	8
Y11			|TMS_0				
Y12			|TDI_0				
Y13			|TDO_0				
Y14			|DOUT_BUSY_0				
Y15			|M1_0				
Y16			|VBATT_0				
Y17	DONE_p[0]	IOB	IO_L27P_SM5_7	OUTPUT	LVTTL	7
Y18	DONE_p[1]	IOB	IO_L21N_7	OUTPUT	LVTTL	7
Y19	DONE_p[2]	IOB	IO_L18P_7	OUTPUT	LVTTL	7
Y2	PROG_bG1_p[1]	IOB	IO_L6P_8	OUTPUT	LVCMOS25	8
Y20	DONE_p[3]	IOB	IO_L20P_7	OUTPUT	LVTTL	7
Y21	DONE_p[4]	IOB	IO_L20N_VREF_7	OUTPUT	LVTTL	7
Y22	PROG_OUT2_p	IOB	IO_L12P_7	OUTPUT	LVTTL	7

Y23	CDATA_TC_p[0]	IOB	IO_L12N_VREF_7	TRISTATE	LVTTL	7
Y24	CDATA_TC_p[1]	IOB	IO_L8N_CC_LC_7	TRISTATE	LVTTL	7
Y25	CDATA_TC_p[2]	IOB	IO_L6P_7	TRISTATE	LVTTL	7
Y26	CDATA_TC_p[3]	IOB	IO_L6N_7	TRISTATE	LVTTL	7
Y3	CDATA_bG1_p[1]	IOB	IO_L8N_CC_LC_8	TRISTATE	LVCMOS25	8
Y4	DONE_bG1_p[4]	IOB	IO_L8P_CC_LC_8	INPUT	LVCMOS25	8
Y5	DONE_bG2_p[0]	IOB	IO_L9N_CC_LC_8	INPUT	LVCMOS25	8
Y6	DONE_bG2_p[1]	IOB	IO_L9P_CC_LC_8	INPUT	LVCMOS25	8
Y7	DONE_bG2_p[3]	IOB	IO_L20N_VREF_8	INPUT	LVCMOS25	8
Y8	DONE_bG2_p[4]	IOB	IO_L26N_8	INPUT	LVCMOS25	8

Table 5-2 Pinout by Pin Number

5.3 Xilinx XC4VSX35-10FF668-CS2 Package Drawing

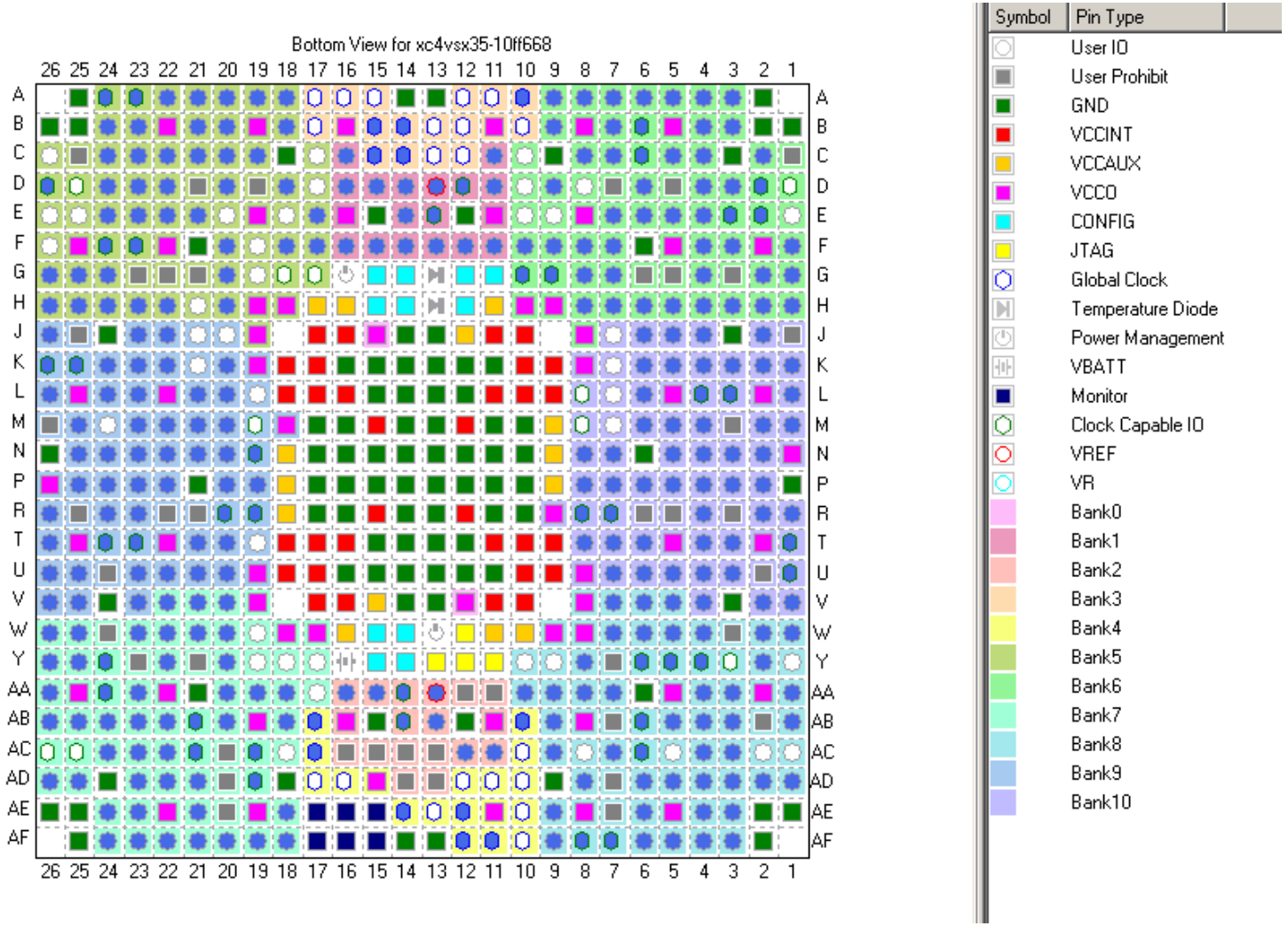

Figure 5-1 Pin Locations

5.4 Programming Notes

All FPGAs on the Station Board are programmed through their 8-bit wide configuration port. The Station Board CMIB software requires the Binary (.bin) output file to program the Xilinx FPGAs. This is set by selecting “Properties…” from the “Process” pull-down menu in the Xilinx ISE software. Select the “General Options” and check “Create Binary Configuration File”.