National Radio Astronomy Observatory
PO Box O
Socorro, NM 87801

Expanded Very Large Array

Title: Correlator Digital Data Input Interface Control Document Document Number: ~~A25000N0002~~ Type: ICD DN: A25025N0000 Authors: M. Revnell	Date: 3 May 2005 Revision: 1.2

Correlator Digital Data Input

Interface Control Document

Interface between EVLA Correlator Station Board and Data Playback and Transmission Systems.

Author: Michael Revnell
Organization: NRAO
Author: David Fort
Organization: DRAO
Author: Zoran Ljusic
Organization: DRAO

Source File Path: /filehost/evla/techdocs/sysintegrt/TecMan Documents/Correlator

Keywords: Correlator input interface, Data Transmission System	
Author Signatures:	Date:
Approved by	Date:
Released by:	Date:

Revision	Date	Author	Sections Affected	Remarks
DRAFT	2/13/2004	Michael Revnell	All	
Revised draft	3/2/2004	Michael Revnell	All	
Revised draft	3/10/2004	Michael Revnell	6, outline drawing	Outline drawing, signal description
Prepare for revision control	3/22/2004	Michael Revnell	All	
Expanded section on 8 bit data format	4/9/2004	Michael Revnell	9	
Missing dimension in outline drawing	4/13/04	Michael Revnell	Fig. 1	
Rename/redefine signal TENSEC	5/3/05	Michael Revnell	6	
Add signal integrity discussion	5/3/05	Michael Revnell	7	
Add signal timing diagram	5/3/05	Michael Revnell	11	

Table of Contents

1. DOCUMENT SCOPE

This document controls the electrical and mechanical interfaces between the EVLA correlator station board inputs and the systems providing data input to the correlator. Examples of such systems include the EVLA real time digital data transmission system and the VLBI playback systems. Functional and performance characteristics of systems on either side of this interface are not specified or controlled by this document.

2. GENERAL DESCRIPTION

The primary digital data input to the EVLA correlator is provided through this interface. All electrical signaling and power connections are through a single 385 pin connector based on the IEC 61076-4-101 standard generally referred to as 2mm Hard Metric Connectors. The mechanical dimensions are based on but not identical to the 6U Eurocard format with the same mechanical outline as a double height VME card.

The correlator station card front panel has a large rectangular cutout to accommodate the front panel of the interface module. Application specific connectors such as optical and network interfaces are part of the interface module. Mechanical support of the interface module is provided by the interface connector, mounting screws on the front panel and standoff mounting holes on the module board.

3. PHYSICAL SPECIFICATIONS

Figure 1 shows the module outline dimensions, mounting hole and interface connector locations. The rectangular volume behind the interface module front panel that is bounded by the module board outline is reserved for interface module components and cooling airflow. Note that the interface connector extends beyond this volume.

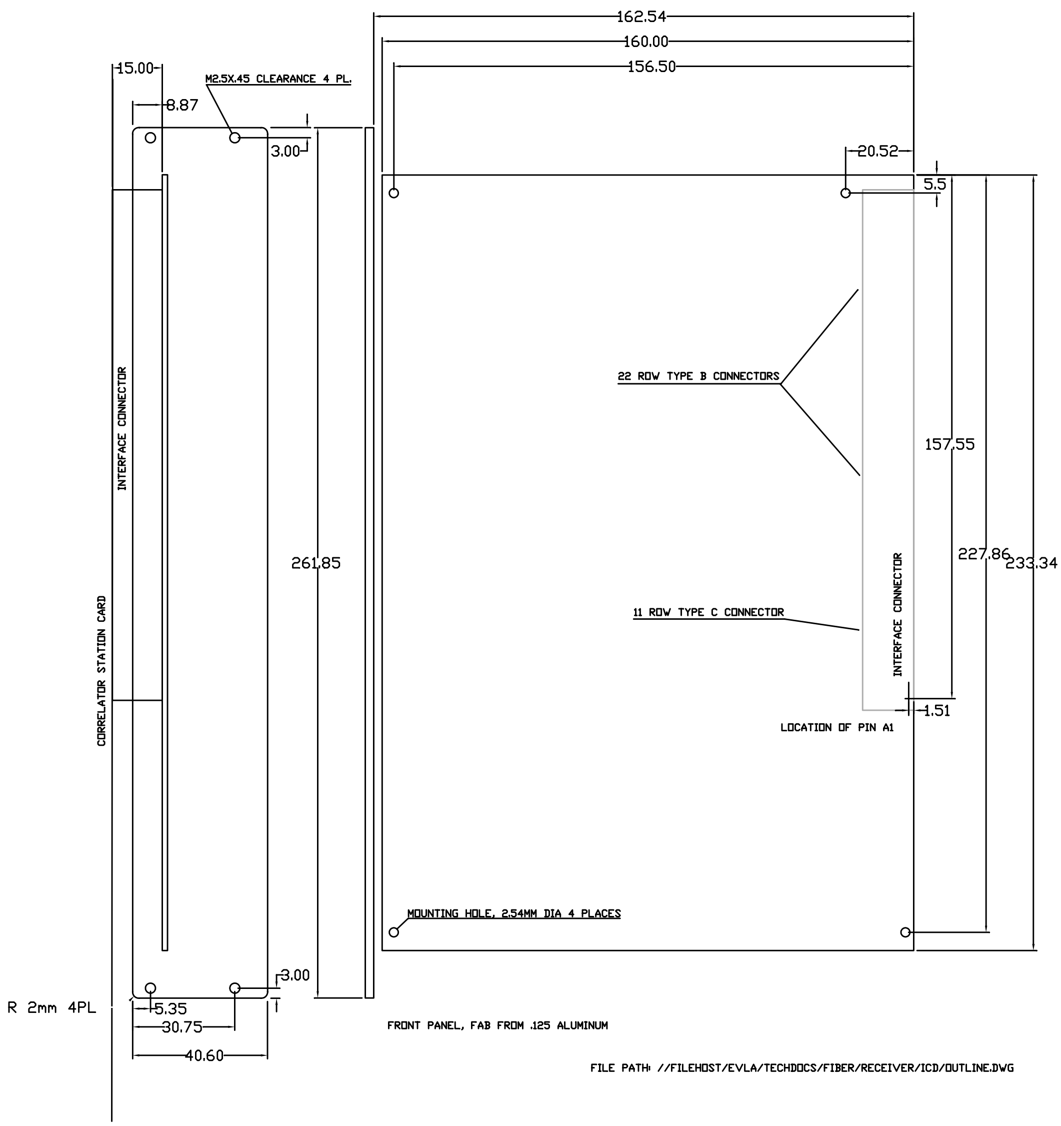


Figure 1. Module dimensions

4. POWER PROVISIONS

The correlator station board provides –48 volts DC through the interface via two rows of pins on the interface connector. The positive lead will be bonded to ground at the battery plant and shall be isolated everywhere else in the system. Maximum power available from the station board is 50 watts. This power system is based on telecom industry standards. The voltage will typically be around 52 volts but may vary considerably at any given time. Interfaces deriving power from this source should be designed accordingly.

5. ELECTRICAL INTERFACE

There are two groups of signal pins identified below as the primary and secondary interfaces. The primary interface is the main high-speed digital data path. The secondary interface is available as either a low speed parallel monitor and control interface or for potential future expansion of the primary interface. The electrical signaling standard of the secondary interface is application dependent.

When used for monitor and control the electrical signaling standard shall be low voltage TTL (LVTTL). When used for expansion of the primary interface the signaling shall be the same as that specified for the primary interface. Signaling protocols for the monitor and control functions are not further defined at this time. This interface is currently unused.

Electrical signaling in the primary interface shall be in accordance with EIA/JDEC standard EIA/JESD8-6 High Speed Transceiver Logic (HSTL) Class I. All signals are single ended and terminated to Vccio/2 at the load ends with 50 ohm impedance

Pin assignments are specified in Section 10. The female connectors are located on the correlator side of the interface.

6. SIGNAL DESCRIPTIONS

Notes on signal names: In this discussion base signal names are in all caps (i.e. RTIME). Signals on the primary interface fall generally into three groups corresponding to three channels in the original DTS receiver module. To identify the channel a character is appended to identify the channel (e.g. RTIMEA). A lowercase ‘c’ (RTIMEc) indicates that the characteristics of all the channels are being addressed. In cases where signals are of a parallel bus nature an identifying number is appended. For example, DATAA15 indicates data line 15 in channel A. Where the characteristics of all data lines are addressed this becomes (DATAcn).

Refer to section 11 for a graphical timing diagram showing signal timing relationships.

Signal RCLOCKc: This signal is the primary reference clock from the correlator station board to the interface module. This is a 64 MHz clock.

Signal RTIMEc: This is the primary timing reference provided by the correlator station board to the interface module. Signal integrity information is also encoded on this signal. Refer to Section 7 for details on the protocol.

Signal RSPAREc: This signal is available for future needs for signaling from the station board to the interface module. All interface modules must connect this signal to logic resources.

Signal DCLOCKc: This is the data clock from the interface module to the station board. Data signals change synchronous with both rising and falling edges of this clock (double data rate signaling). This clock is derived from RCLOCKc and is 128 MHz.

Signal DTIMEc: This signal encodes time and signal integrity information related to data being delivered to the station card. Refer to Section 7 for details on the protocol.

Signal ATIMEc: Carries timing information of data derived from when the data were taken at the antenna. High for one data bit time each 10 milliseconds during the first bit time of a frame. In the last frame before a 1 second boundary this signal will be high for an additional bit time. In the last frame before a 10 second boundary this signal will be high for three bit times. (This signal was redefined and renamed from TENSECc).

Signal DVALIDc: This signal marks data frames containing data considered valid. The minimum resolution of this signal in any application is one period of DCLOCKc. The minimum resolution in a particular application will depend on the characteristics of the data source processed by an interface module.

Signal DSPAREc: This is a spare signal for needs identified in the future for signaling from the interface module to the station board. All interface modules must connect this signal to logic resources.

Signal SPARE: These are spare pins available for signaling requirements in future interface module designs. They need not be physically connected in the interface module. They must be connected on the station board to logic resources.

Signal GND: These are ground reference pins. Grounds are connected in a checkerboard pattern to provide good signal integrity for all signal pins. All ground pins must be connected on the station board and the interface module.

Signal DATAcn: These are the main data signals. These signals change state synchronously with both the rising and falling edges of DCLOCKc.

7. SIGNAL INTEGRITY VERIFICATION

In order to verify the integrity of the data link between the input interface and the correlator station card the interface computes a cyclic redundancy check (CRC) on a selected data bit and passes the computed CRC to the station card for checking.

The station card selects the data bit for the computation and passes the bit number to the interface serially, least significant bit first, on the RTIMEc signal. The bits are transferred at the RCLOCK rate (64MHz) in the 5 bits immediately following the 10 millisecond mark.

The interface logic computes the CRC on the assigned bit during the next data frame. The 4 bit result is transferred on the DTIME line during the following frame. The bits are transferred at the data bit rate which is twice the DCLOCK rate (DDR clocking). They immediately follow the 10 millisecond mark on the DTIME line, least significant bit first.

Data frame timing for integrity checking is independent from data frame timing for the astronomical data.

There is a two frame pipeline delay from when a data line is identified and the CRC data become available for checking.

The CRC generation circuitry used is as defined in RFS Document A25022N0041 PROTOCOL SPECIFICATION, HM Gbps Cable Signaling Specification by Brent Carlson Dated Feb 24, 2005. Published by National Research Council Canada, Herzberg Institute of Astrophysics, Dominion Radio Astrophysical Observatory.

8. DATA FORMAT FOR 3-BIT SAMPLED DATA

The EVLA uses the samplers and digital formatters developed for the ALMA project. Therefore, the data formatting corresponds to the ALMA standard.

The data format is a 3-bit gray code. Table 1 gives the channel outputs corresponding to the digitizer analog input.

Table 1. Channel outputs corresponding to the digitizer analog input

	Channel	**Channel**	**Channel**
Digitizer Input	**A**	**B**	**C**
Most Negative	0	0	0
	0	1	0
	1	1	0
	1	0	0
	1	0	1
	1	1	1

	0	1	1
Most Positive	0	0	1

Data from the oldest samples appear on DATAc31. Similarly data from the newest samples appear on DATAc0.

9. DATA FORMAT FOR 8-BIT SAMPLED DATA

When the EVLA observing system is in 8-bit mode data is carried in channels A and C. Channel B is idle.

Samples are interleaved between channels A and C with older samples in channel A. Four samples appear in each data frame in each channel. Bits DATAc31 through DATAc24 contain the oldest sample bits DATAc7 through DATAc0 the newest. DATAc31 is the most significant bit of the oldest sample. Signal encoding is offset straight binary with hexadecimal 00 representing the most negative digitizer input level.

10. INTERFACE CONNECTOR PIN ASSIGNMENTS.

FILE PATH: //filehost/evla/techdocs/fiber/receiver/icd/WIDARPINOUT.xls

Notes:

1. Signals named “SPARE” with no additional identifiers are available for possible future expansion to 4-bit wide data. They are unconnected in the current deformatter module.

2. Signals named “RCLOCKx” are 64 MHz reference clock from correlator to deformatter.

3. Signals named “RTIMEx” are 10 millisecond reference timing from correlator to deformatter. The fiducial is the rising edge of RCLOCK when this signal is high after it has been low for at least one clock period. Duty cycle is otherwise undefined.

4. Signals named “RSPAREx” are spare signals from correlator to deformatter.

5. Signals named “DSPAREx” are spare signals from deformatter to correlator. They are connected in the current deformatter module.

6. Signals named “DCLOCKx” are 128 MHz doubled data rate clocks associated with DATAx lines. Clock edges are aligned with data signal edges.

7. Signals named “CORIOn” are undefined spares. They are available for potential future expansion of monitor and control transfer or data bit transfer.

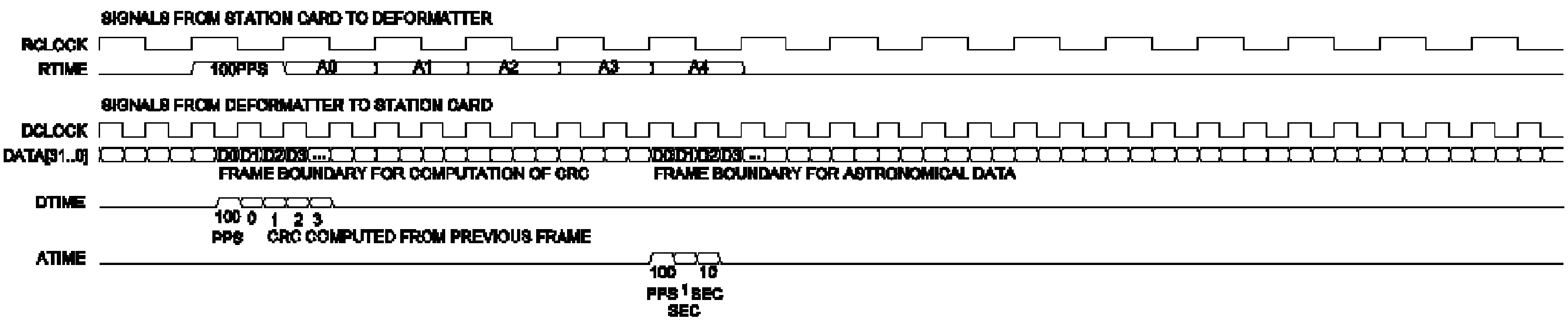
8. To maintain recommended clearances on 48V power supplies the pins marked N/C in rows one and two must have their plating and pads removed from the board.

Column/ Row	A	B	C	D	E
1	48V+	48V+	N/C	48V-	48V-
2	N/C	N/C	N/C	N/C	N/C
3	N/C	GND	GND	GND	GND
4	GND	CORIO15	GND	CORIO16	GND
5	N/C	GND	CORIO13	GND	CORIO14
6	GND	CORIO11	GND	CORIO12	GND
7	N/C	GND	CORIO9	GND	CORIO10
8	GND	CORIO7	GND	CORIO8	GND
9	N/C	GND	CORIO5	GND	CORIO6
10	GND	CORIO3	GND	CORIO4	GND
11	CORIO0	GND	CORIO1	GND	CORIO2
12	GND	SPARE	GND	SPARE	GND
13	SPARE	GND	SPARE	GND	SPARE
14	GND	SPARE	GND	SPARE	GND
15	SPARE	GND	SPARE	GND	DSPAREA0
16	GND	DATAA0	GND	DATAA1	GND
17	DATAA2	GND	DATAA3	GND	DATAA4
18	GND	DATAA5	GND	DATAA6	GND
19	DATAA7	GND	DATAA8	GND	DATAA9
20	GND	DATAA10	GND	DATAA11	GND
21	DATAA12	GND	DATAA13	GND	RCLOCKA
22	GND	DATAA14	GND	DCLOCKA	GND
23	DATAA15	GND	ATIMEA	GND	RTIMEA
24	GND	DATAA16	GND	DTIMEA	GND
25	DATAA17	GND	DATAA18	GND	RSPAREA
26	GND	DATAA19	GND	DATAA20	GND
27	DATAA21	GND	DATAA22	GND	DATAA23
28	GND	DATAA24	GND	DATAA25	GND
29	DATAA26	GND	DATAA27	GND	DATAA28
30	GND	DATAA29	GND	DATAA30	GND
31	SPARE	GND	DVALIDA	GND	DATAA31
32	GND	SPARE	GND	SPARE	GND
33	SPARE	GND	SPARE	GND	SPARE
34	GND	SPARE	GND	SPARE	GND
35	SPARE	GND	SPARE	GND	SPARE
36	GND	SPARE	GND	SPARE	GND
37	SPARE	GND	SPARE	GND	DSPAREB0
38	GND	DATAB0	GND	DATAB1	GND
39	DATAB2	GND	DATAB3	GND	DATAB4
40	GND	DATAB5	GND	DATAB6	GND
41	DATAB7	GND	DATAB8	GND	DATAB9

Column/ Row	A	B	C	D	E
42	GND	DATAB10	GND	DATAB11	GND
43	DATAB12	GND	DATAB13	GND	RCLOCKB
44	GND	DATAB14	GND	DCLOCKB	GND
45	DATAB15	GND	ATIMEB	GND	RTIMEB
46	GND	DATAB16	GND	DTIMEB	GND
47	DATAB17	GND	DATAB18	GND	RSPAREB
48	GND	DATAB19	GND	DATAB20	GND
49	DATAB21	GND	DATAB22	GND	DATAB23
50	GND	DATAB24	GND	DATAB25	GND
51	DATAB26	GND	DATAB27	GND	DATAB28
52	GND	DATAB29	GND	DATAB30	GND
53	SPARE	GND	DVALIDB	GND	DATAB31
54	GND	SPARE	GND	SPARE	GND
55	SPARE	GND	SPARE	GND	SPARE
56	GND	SPARE	GND	SPARE	GND
57	SPARE	GND	SPARE	GND	SPARE
58	GND	SPARE	GND	SPARE	GND
59	SPARE	GND	SPARE	GND	DSPAREC0
60	GND	DATAC0	GND	DATAC1	GND
61	DATAC2	GND	DATAC3	GND	DATAC4
62	GND	DATAC5	GND	DATAC6	GND
63	DATAC7	GND	DATAC8	GND	DATAC9
64	GND	DATAC10	GND	DATAC11	GND
65	DATAC12	GND	DATAC13	GND	RCLOCKC
66	GND	DATAC14	GND	DCLOCKC	GND
67	DATAC15	GND	ATIMEC	GND	RTIMEC
68	GND	DATAC16	GND	DTIMEC	GND
69	DATAC17	GND	DATAC18	GND	RSPAREC
70	GND	DATAC19	GND	DATAC20	GND
71	DATAC21	GND	DATAC22	GND	DATAC23
72	GND	DATAC24	GND	DATAC25	GND
73	DATAC26	GND	DATAC27	GND	DATAC28
74	GND	DATAC29	GND	DATAC30	GND
75	SPARE	GND	DVALIDC	GND	DATAC31
76	GND	SPARE	GND	SPARE	GND
77	SPARE	GND	SPARE	GND	SPARE

11. INTERFACE SIGNAL TIMING DIAGRAM.

FILE PATH: //filehost/evla/techdocs/fiber/receiver/icd/INTERFACETIMING.vsd



FRAME IS DEFINED AS 10 MILLISECONDS OF DATA

RCLOCK IS A 64MHZ REFERENCE CLOCK PROVIDED BY THE STATION CARD TO THE DEFORMATTER

RTIME IS THE TIMING SIGNAL FROM THE STATION CARD TO THE DEFORMATTER. IT IS HIGH DURING THE FIRST RCLOCK CYCLE OF EACH CORRELATOR FRAME TIME. THE TIME MARK IS FOLLOWED BY A 5 BIT WORD LSB FIRST WHICH SPECIFIES A DATA BIT NUMBER TO COMPUTE A CRC FOR.

DCLOCK IS THE 128 MHZ DATA CLOCK FROM THE DEFORMATTER TO THE STATION CARD

DTIME ECHOES BACK THE CORRELATOR TIME. IT IS HIGH DURING THE FIRST BIT TIME OF A CRC DATA FRAME. THE TIME MARK IS FOLLOWED BY A 4 BIT CRC LSB FIRST COMPUTED OVER THE PREVIOUS DATA FRAME FOR THE DAT BIT SPECIFIED BY RTIME TWO FRAMES PREVIOUS. THERE ARE TWO PIPELINE DELAYS FROM WHEN A BIT IS SPECIFIED UNTIL A CRC COMPUTATION BECOMES AVAILABLE FOR A FULL FRAME FOR THE SPECIFIED BIT.

ATIME INDICATES ANTENNA TIME DERIVED FROM THE DATA STREAM FORMATTING INFORMATION. IT IS HIGH FOR ONE BIT TIME IN EACH 10 MS FRAME INDICATING THE START OF DATA. IT IS HIGH FOR AN ADDITIONAL BIT TIME IN FRAMES THAT ARE ONE FRAME BEFORE EACH FRAME STARTING A 1 SECOND INTERVAL. IT IS HIGH AN ADDITIONAL BIT TIME IN FRAMES THAT ARE ONE FRAME BEFORE EACH FRAME STARTING A 10 SECOND INTERVAL.

DATA ARE 32 DATA LINES CARRYING THE ASTRONOMICAL DATA SAMPLES.