TEST AND VERIFICATION PLAN

Station Board

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Revision: 1.0

Dave Fort, 15 April 2006

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List of Abbreviations and Acronyms

CBE	Correlator Back End
CMIB	Correlator Module Interface Board
DLL	Delay Locked Loop
DUT	Device Under Test
ESD	Electro-Static Discharge
EVLA	Expanded Very Large Array
FORM	Fibre Optic Receiver Module
FPGA	Field Programmable Gate Array
IOB	Input Output Buffer
ISR	Interrupt Service Routine
JTAG	Joint Test Action Group (Boundary Scan Architecture)
MHz	Megahertz (10^6 cycles per second)
Ms/s	Mega Samples per Second
MTBF	Mean Time Before Failure
Mw/s	Mega Words per Second
PCB	Printed Circuit Board
PLL	Phase Locked Loop
RFI	Radio Frequency Interference
TCGB	Time Code Generator Board
VLBA	Very Long Baseline Array
VLBI	Very Long Baseline Interferometry
WIDAR	Wideband Interferometric Digital ARchitecture

1 Revision History

Revision	Date	Changes/Notes	Author
0.0	06 Apr 2005	Initial Draft	D. Fort
1.0	15 Apr 2006	Updates	D. Fort

2 Introduction

The testing of the WIDAR correlator may be divided into the following categories.

1. FPGA bit level testing using ModelSim.
2. FPGA functional testing using ModelSim.
3. FPGA post-place-and-route functional testing using ModelSim.
4. Board signal integrity testing using SignalVision.
5. Board post-place-and-route trace delays using TAU.
6. Board post-place-and-route signal integrity testing using ICX.
7. Board interconnect testing using JTAG by the board assembler.
8. Board interconnect testing at DRAO lab using temporary and/or built-in tests.
9. Board functional testing at DRAO using test data.
10. System interconnect testing at DRAO using built-in tests.
11. System functionality at DRAO using simulated data.
12. System testing at the EVLA using real radio sources.

This document describes a plan for steps 8 and 9 above for the prototype Station Board.

The stages in this plan are as follows:

1. Power distribution tests.
2. FPGA configuration tests.
3. CMIB communications tests.
4. Timing distribution tests.
5. Connectivity and Signal Integrity tests.
6. Functionality tests.
7. System Level tests.

3 Overview

The Station Board receives two wide bands and selects 18 narrow bands from each of the wide bands and sends them to the baseline part of the correlator. A simplified block diagram of the Station Board is shown in Figure 3-1. Wide band optical inputs are recovered by the Fibre Optic Receiver Module, re-arranged by the Input FPGA, delayed by the Delay Modules, passed through the WBC FPGA and filtered by the Filter Banks. The narrow band outputs of each Filter Bank are sent to the baseline part of the correlator via an Output FPGA. The Filter Bank also sends the narrow band signals to a VLBI recording system via the VSI FPGA. The narrow band phase error outputs of both filter banks are sent to the baseline part of the correlator via the Timing FPGA. The Input FPGA can also select the wide band input from a VLBI playback system via the VSI FPGAs. The Timing FPGA selects and decodes the external time code and produces the system timing signals and the CMIB interrupt.

The Station Board has been designed so that no external boards are required for testing by providing on-board ability to generate and send time code (replacing TCGB) and to receive and check output data (replacing the Baseline Board) via the backplane connectors. In addition, no optical input signals are necessary, since it is assumed that this part of the Fibre Optic Receiver Module (FORM) has been tested at NRAO. The FORM will be required to produce test patterns and perform the CRC checking scheme common to all the FPGAs on the Station Board.

This document is meant to rather general but detailed enough to enable the prototype test software to be identified. Another document will follow that gives a more detailed description of the tests needed to establish that the Prototype Station Board is functioning correctly. A further document will describe tests with the prototype system in which the Delay Module RAM is loaded with pre-computed data and the output of the Baseline Board is processed and inspected.

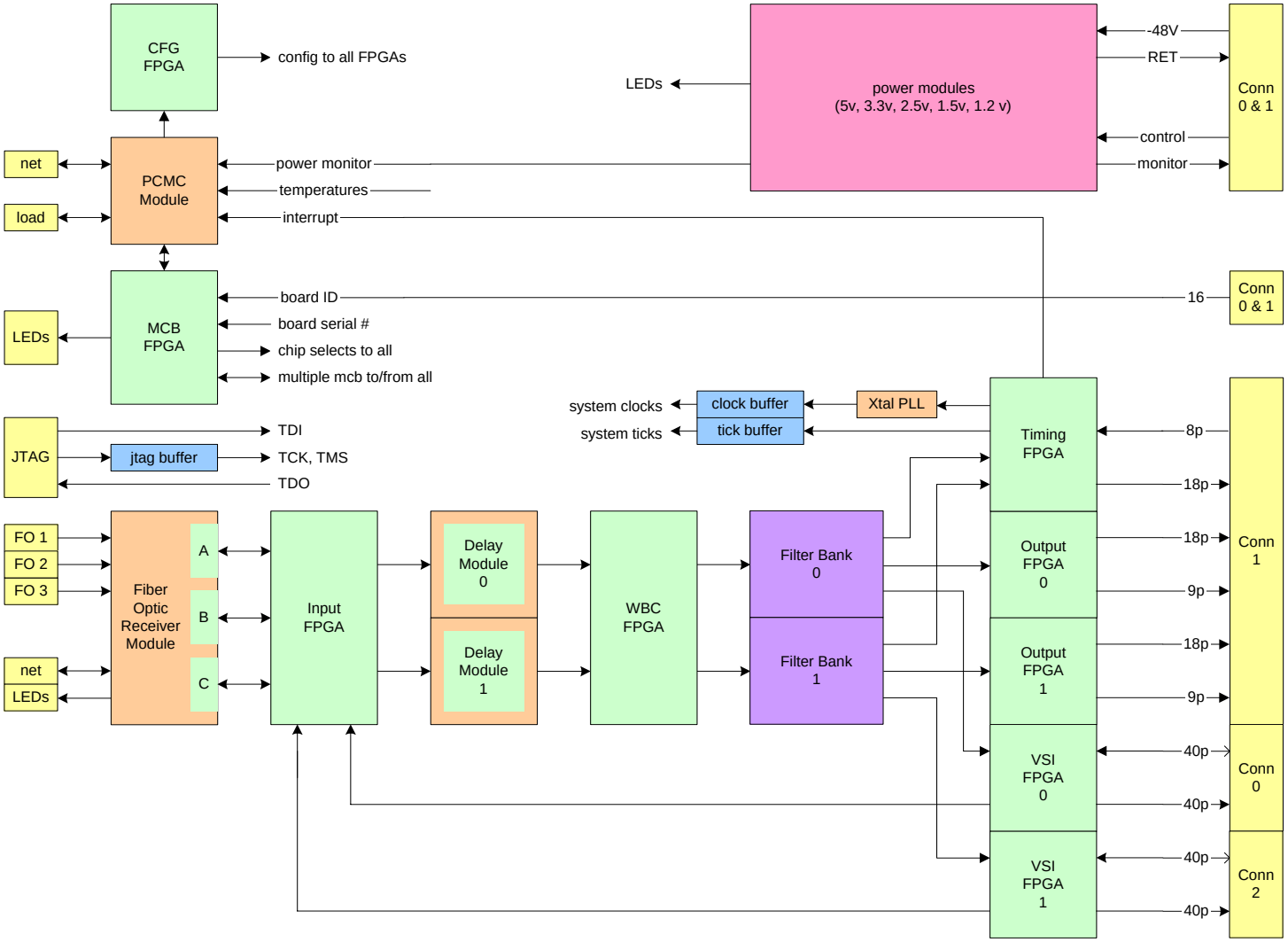

Figure 3-1 Station Board block diagram

4 Test Setup

1. Vertical board holder with air cooling (easy to get at both sides).
2. PCMC has been tested and works.
    a. OS executable on local server
    b. CMIB executable on local server.
    c. PCMC FPGA bit file on local server.
3. FORM has been tested, except for Station Board connections, and works.
    a. Bit files on server (assumed loaded on FORM PC104 boot)
4. Cables have been tested and work.
    a. Time code cable (2 wafers).
    b. Data cable (4 wafers).
5. Three 3U common backplanes.
6. 48 V power supply with cables to connect to at least two 3U backplanes.
7. Oscilloscope
8. Logic analyzer
9. Ethernet switch and four RJ45 cables
10. Fully assembled and JTAG-tested Station Board.
11. Bit files for full versions of all FPGAs.
12. Bit files for test versions of the required set of FPGAs.

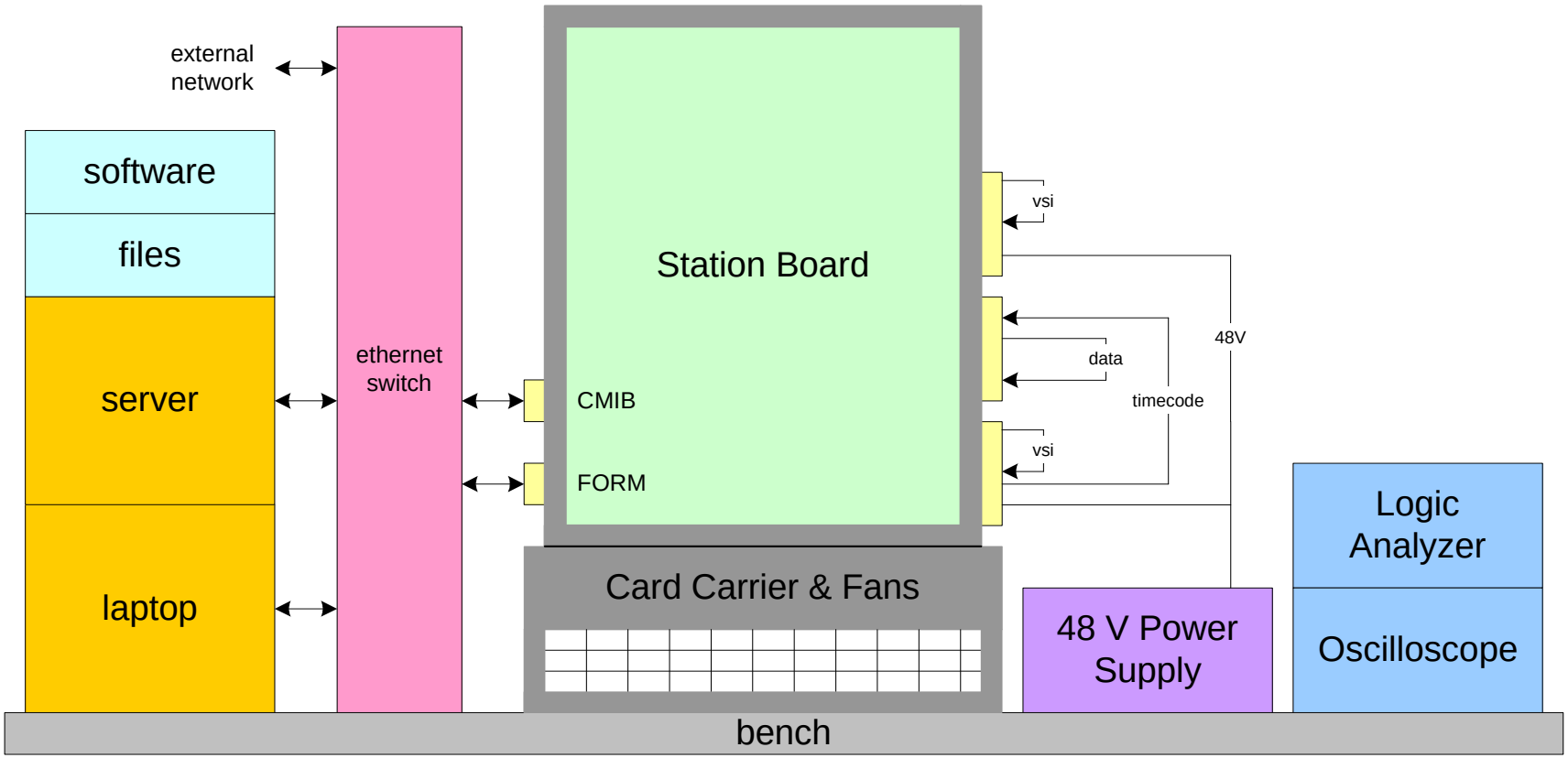

Figure 4-1 Prototype Station Board test setup

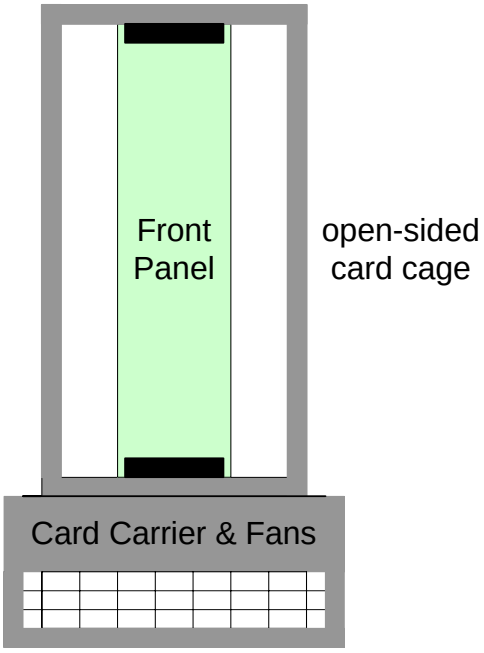

Figure 4-2 Prototype Station Board carrier

5 Test Classification

5.1 Basic

5.1.1 Power Distribution

Tests that all power supplies are functioning, voltages are within range, noise levels are acceptable and LEDs are lit.

5.1.2 Configuration

Tests that all FPGAs can be configured and selectively re-configured.

5.1.3 Communications

Tests that PC104/Plus communication to FPGAs is OK by writing and reading suitable registers on each FPGA. The burst mode should be checked for relevant FPGAs.

5.1.4 System Timing

Tests the generation and distribution of the system 128 MHz clock and the system tick. Check the 64 MHz test clock used for generating the on-board time code.

5.2 Connectivity and Signal Integrity

Tests that all PCB traces are correct and run at speed. After all these tests are successful, the Station Board PCB is deemed to be designed correctly.

5.3 Functional

Tests that the all the FPGAs are functioning as expected one at a time. After all these tests are successful, each FPGA is deemed to be designed correctly and the prototype Station Board is ready for prototype system testing.

5.4 Environmental

Tests that the board works over a range of temperatures and for long periods of time.

5.5 System Level

This kind of testing would check that the Station Board worked properly in conjunction with the TIME Code Generator Board and the Baseline Board. This could develop into a test for newly made or defective boards. After a board has been tested at this level it would be deemed operational.

6 Connectivity and Signal Integrity Tests

These tests are meant to establish that the PCB traces are correct and that they run at speed. Most of the interconnections can be tested using the built-in CRC comparison scheme. The CMIB selects which bit stream to compare in each of two connected FPGAs and compares the 4-bit CRC from each. One FPGA is calculating a CRC on the output bit stream and the other on the same input bit stream. The CRC is calculated between ticks and must be read by the ISR from both FPGAs. The bit stream selected can be changed on every interrupt and hence one bit stream of all input/output pairs can be checked every interrupt. This scheme should be implemented permanently in software. The CRC check does not work properly unless the bit stream being tested is toggling more or less randomly. For this reason, it may be advisable to build in an special output mode in some FPGAs (FORM and Filter FPGA, in particular) that guarantees this type of output. In some cases, the testing would benefit from a simple design just for this testing. The Filter FPGA would benefit the most from such a simple design because any changes to the full design takes a long time to place and route, the FPGA is very full and the software to load lookup tables has to be more advanced.

Some of the signals connected between FPGAs are not part of the CRC checking scheme (PPS, TICK, VALID, NOISE, DERR and DFRM). PPS, TICK and DFRM are checked by using time interval measurements at the input to the FPGA (ISR sets expected period and checks status bit). DERR is checked by using a 4-bit pattern match (ISR checks status bit). NOISE could be checked by a time interval measurement. VALID needs some thinking.

7 Functional Tests

One type of functional test would compare actual measurements integrated over the tick interval with the same values produced from simulations or calculations. Another type of functional test would allow data to be generated/captured by RAM lookup tables/storage for loading/inspection by the CMIB. For some FPGAs there may be simpler tests than these; for example, the actual delay introduced by the Delay Module could be measured directly by the WBC. For this class of tests, data generation would normally take place in the previous FPGA, measurements would be performed in the DUT and data capture in the following FPGA. The CMIB would read the results to verify the correct operation of the DUT. In this type of test, the previous and following FPGAs may be loaded with special logic that generates data and performs measurements respectively while the DUT is loaded with the normal logic. The Output FPGA is capable of recording a sizeable amount of Filter output data which could be used for testing.

8 Environmental

The test setup is placed in the environmental chamber and cycled between -10°C and +40°C and checked for errors using some or all of the tests developed above. Some

testing can be done with relatively rapid temperature changes and the much longer runs (>100 hours) at the two temperature extremes.

9 System Level

The system setup shown below could provide a complete test bed in that it can test a faulty Time Code Generator Board, Station Board, Baseline Board or Fanout Board, one at a time. In addition, the 17th and 18th sub-bands of the Station Boards get tested. The Fibre Optic Receiver Module (FORM) would be tested elsewhere (NRAO) and would provide the data for all system level tests, possibly using special FPGA designs. The On-the-Sky tests at the EVLA site could use a sub-set of this arrangement with only one Time Code Generator Board, one Baseline Board and no Fanout Board.

Eventually, a set of tests could be used during the production of new boards to be sure that all parts of the board function correctly and to help determine the faulty paths/parts if errors are found. The same tests could be used during EVLA operation to help in the repair of faulty boards.

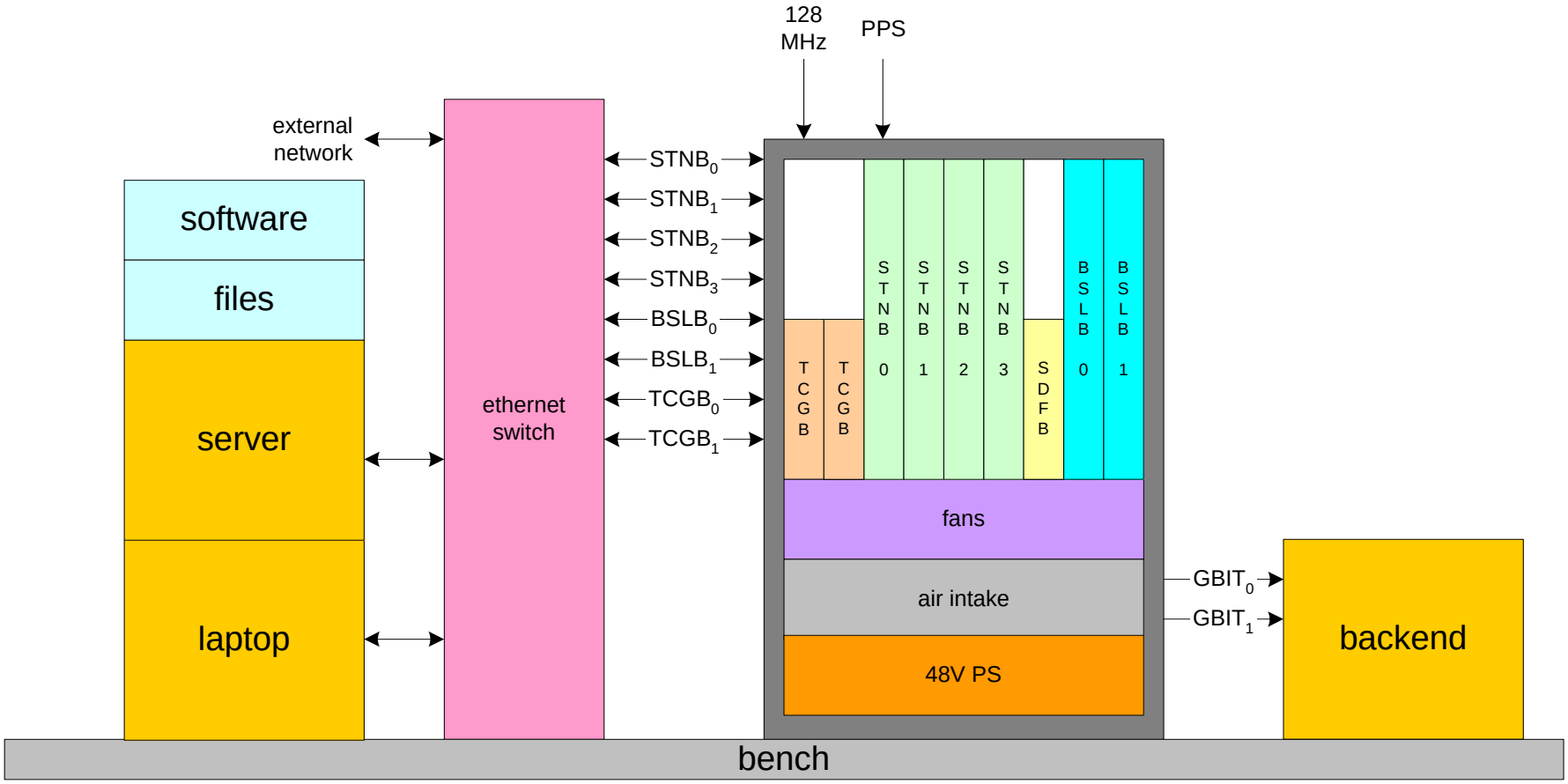

Figure 9-1 Prototype System and Test Bench

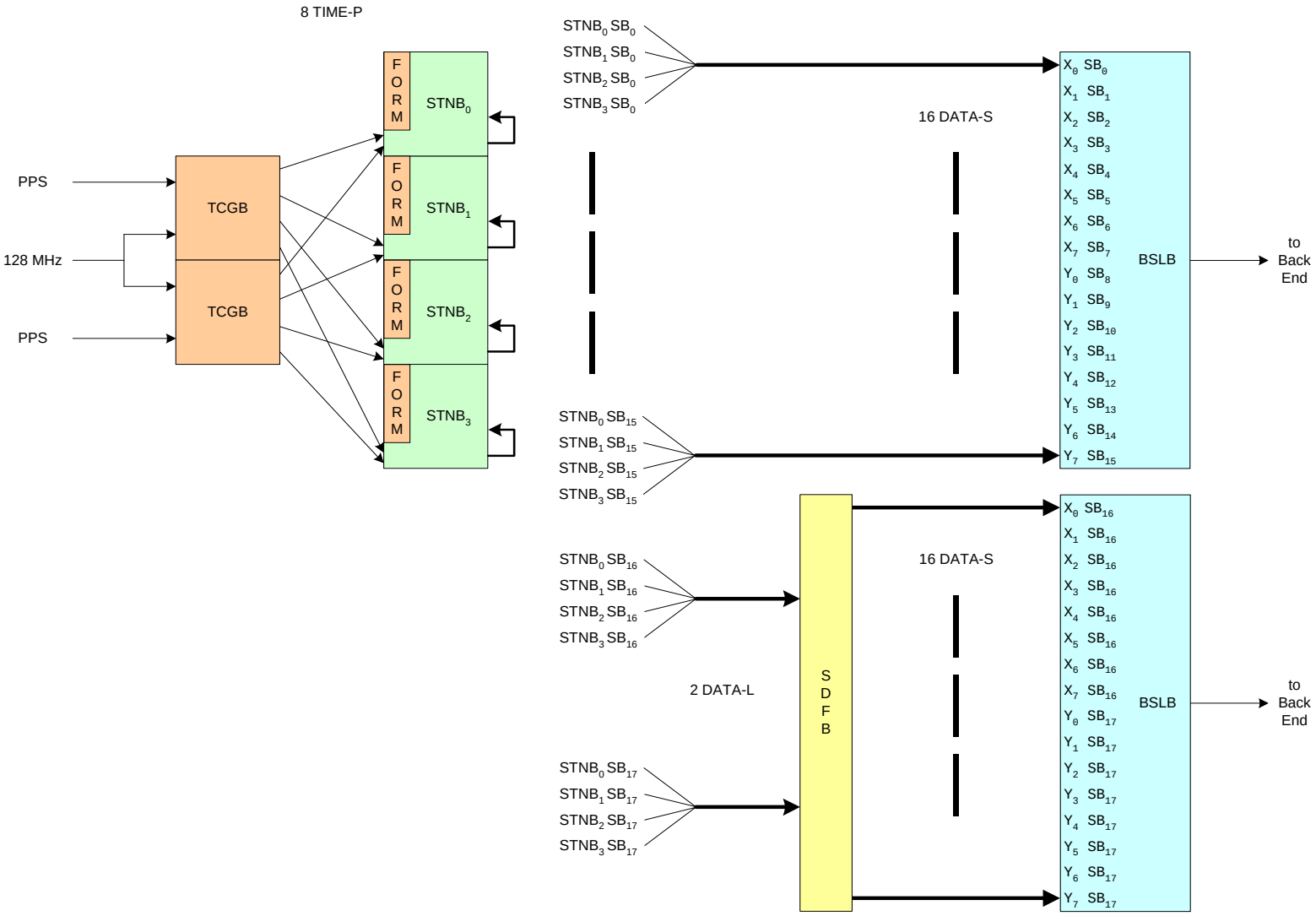

Figure 9-2 Prototype System Interconnections

10 Software Requirements

More or less in time order of being required.

10.1 Initial Testing

PCMC PC104 boots automatically on power-up and reset.

PCMC FPGA boots automatically.

FORM PC104 boots automatically and loads FORM FPGAs.

GUIs for:

1. individual FPGA download of bit files.
2. read value from address and write value to address
3. individual FPGA configurations “open-change-save”

10.2 Interrupt Service Routine

read time from timing FPGA and compare with internal counter.

check status bits, etc and display error conditions.

implement continuous CRC checking scheme with error display.

read selected addresses, double buffer to one second and write to a file.

the ability to add short ad hoc code to the ISR.

10.3 Load lookup tables from files and check

Input FPGA lookup tables

Filter FPGA stage 1 product table

Filter FPGA stages 2, 3 and 4 coefficient tables

Filter FPGA mixer cosine and sine tables

Filter FPGA tone extractor cosine/sine table

Delay Module test data (not needed for a while)

10.4 Models

Models are:

1. Delay Module delay model.
2. Filter FPGA delay model.
3. Filter FPGA mixer phase model.
4. Filter FPGA tone extractor phase model.
5. Output FPGA geometric phase model.
6. DUMPTRIG generation.
7. Pulsar model.

Set simple models manually (no interrupt processing).

Test mode to convert test models and output at interrupt.

Normal mode to convert CALC models and output at interrupt.

10.5 Multiple Read Measurements

The measurements are:

1. Input FPGA state counts.
2. Filter FPGA state counts.
3. Filter FPGA clip counts.
4. Filter FPGA pre-re-quantizer on and off power.
5. Filter FPGA post-re-quantizer power
6. Filter FPGA tone extractor I product sum, Q product sum and valid counts.
7. WBC FPGA output product accumulations and valid counts.
8. Output FPGA radar mode samples.

Store raw/integrated measurements in a file.

10.6 Useful GUI Functions

Display interconnect (CRC, …) errors.

Display FPGA internal errors.

Display WBC wideband lags and bins (spectrum).*

Display Input FPGA state count histograms.*

Display Filter FPGA state count histograms.*

Display Filter FPGA pre-quantizer noise diode on and off power vs time.*

Display Filter FPGA post-quantizer power vs time.*

Display Filter FPGA tone extractor amplitude and phase vs time.*

Display signal path switch settings.

System level error display (board, FPGA, function).

For setting on-the-fly configuration – e.g. Filter FPGA scale factors.

* it is more likely that these are simple buttons starting off-line tasks that read the output file and produce the displays. They would continue to read the file and update each display as more data appeared in the file. When the files already exist, the same programs would be called with a user set ‘sleep’ interval between updates and/or a ‘next’ button to slow down the updates.

11 GUI Screens

The following GUI contains buttons and status indicators for all the FPGAs on the board. Clicking on a particular FPGA opens the next level window for that FPGA.

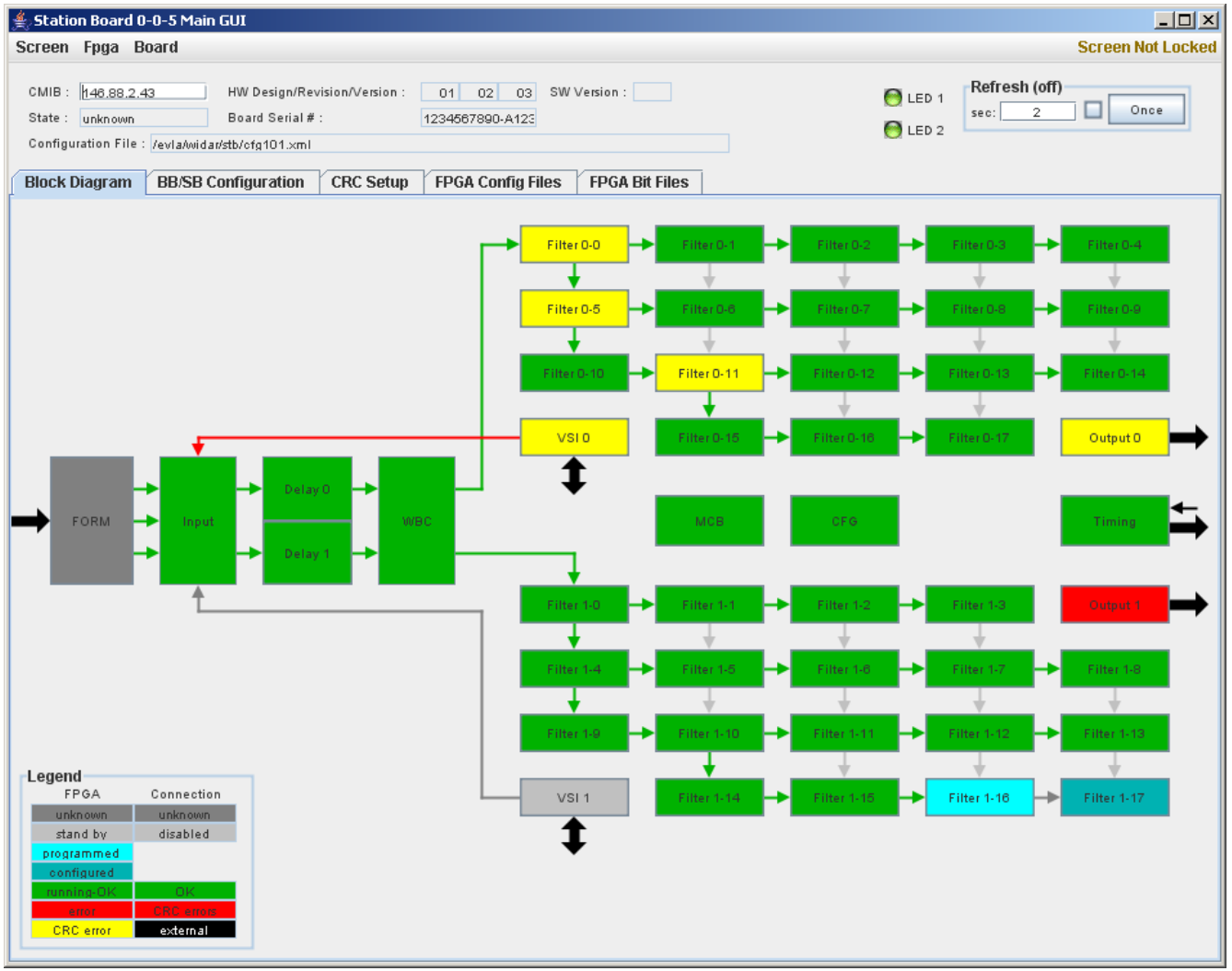

Figure 11-1 Station Board FPGA Level GUI

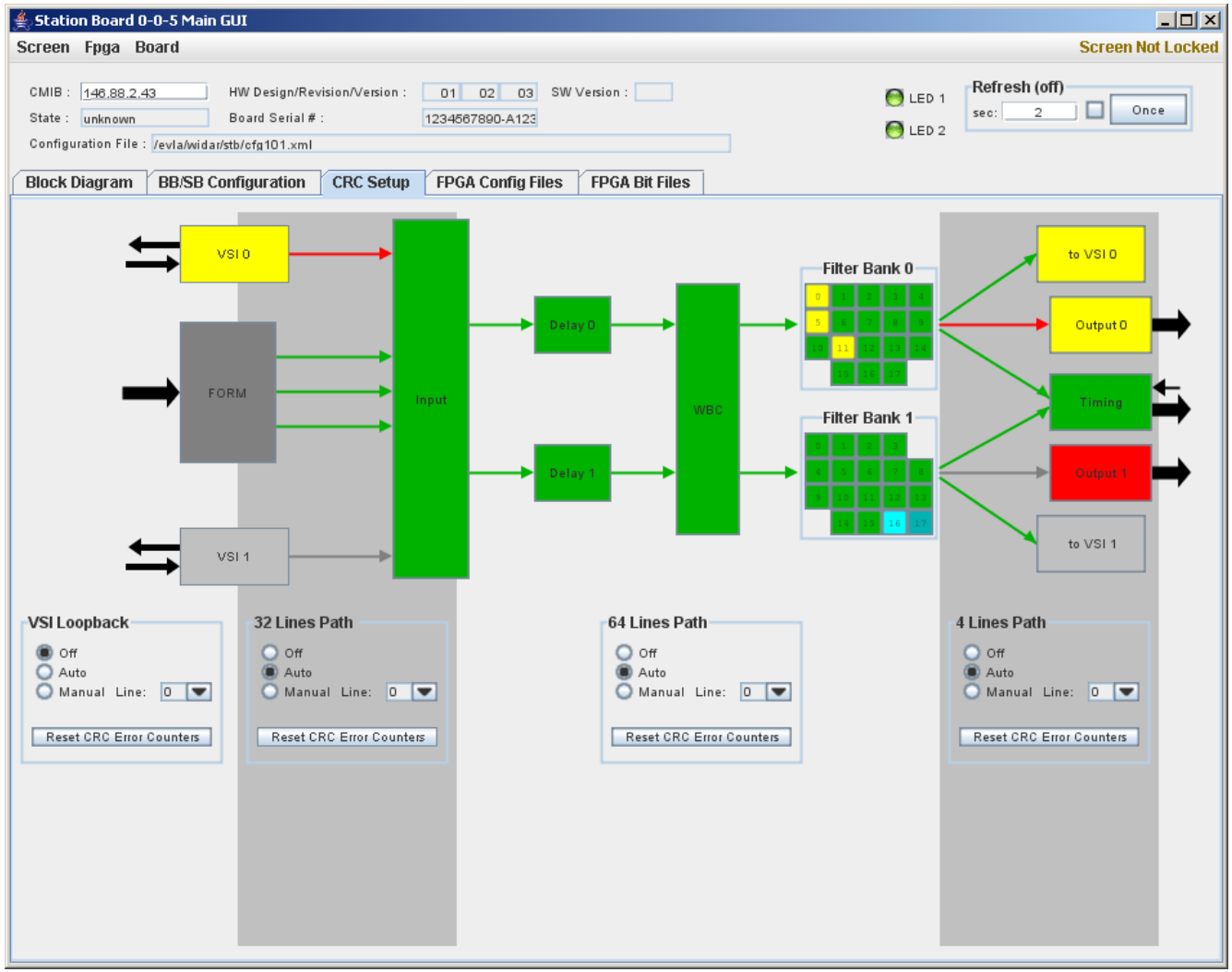

Figure 11-2 CRC Error Display GUI

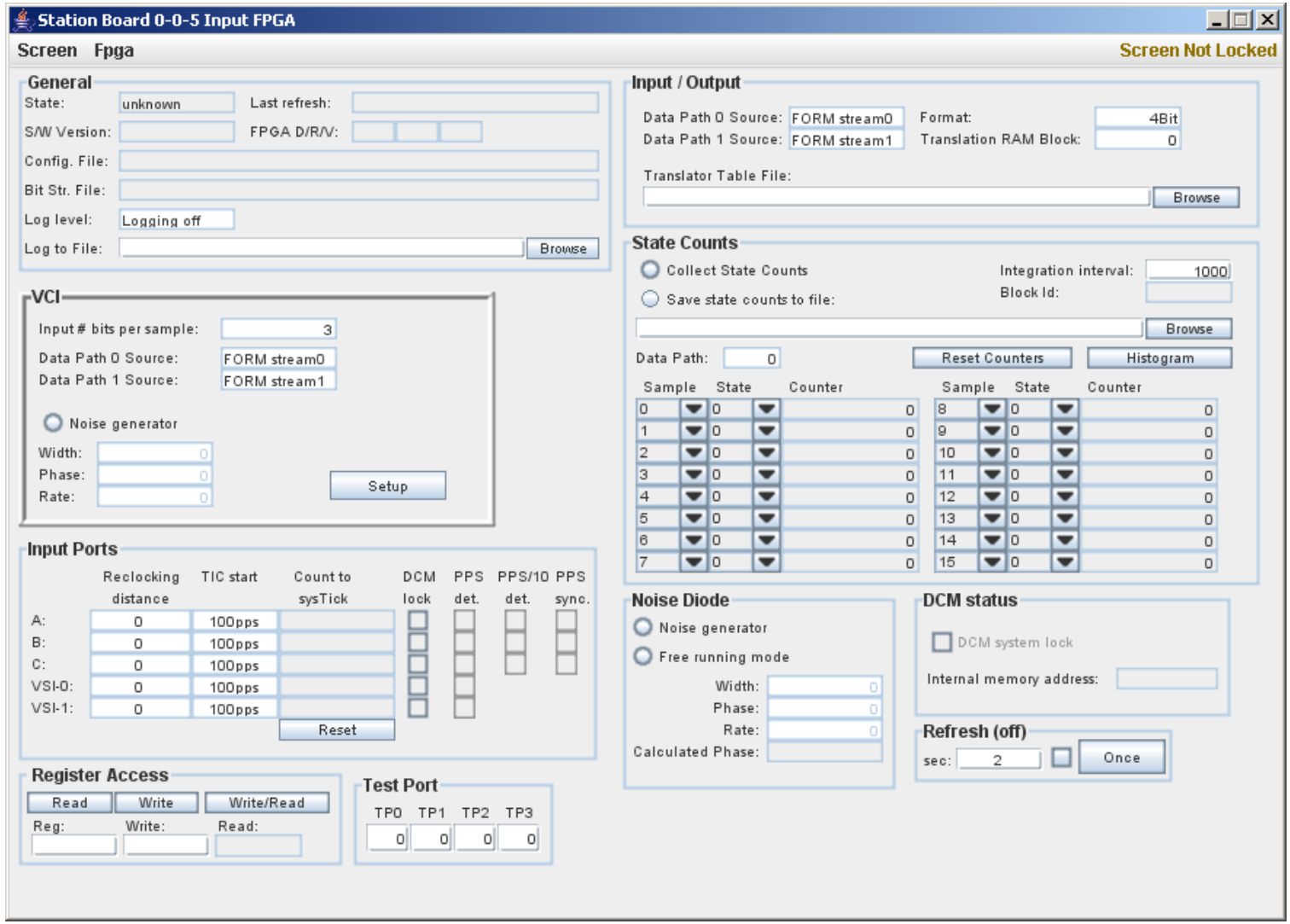

Figure 11-3 Input FPGA GUI

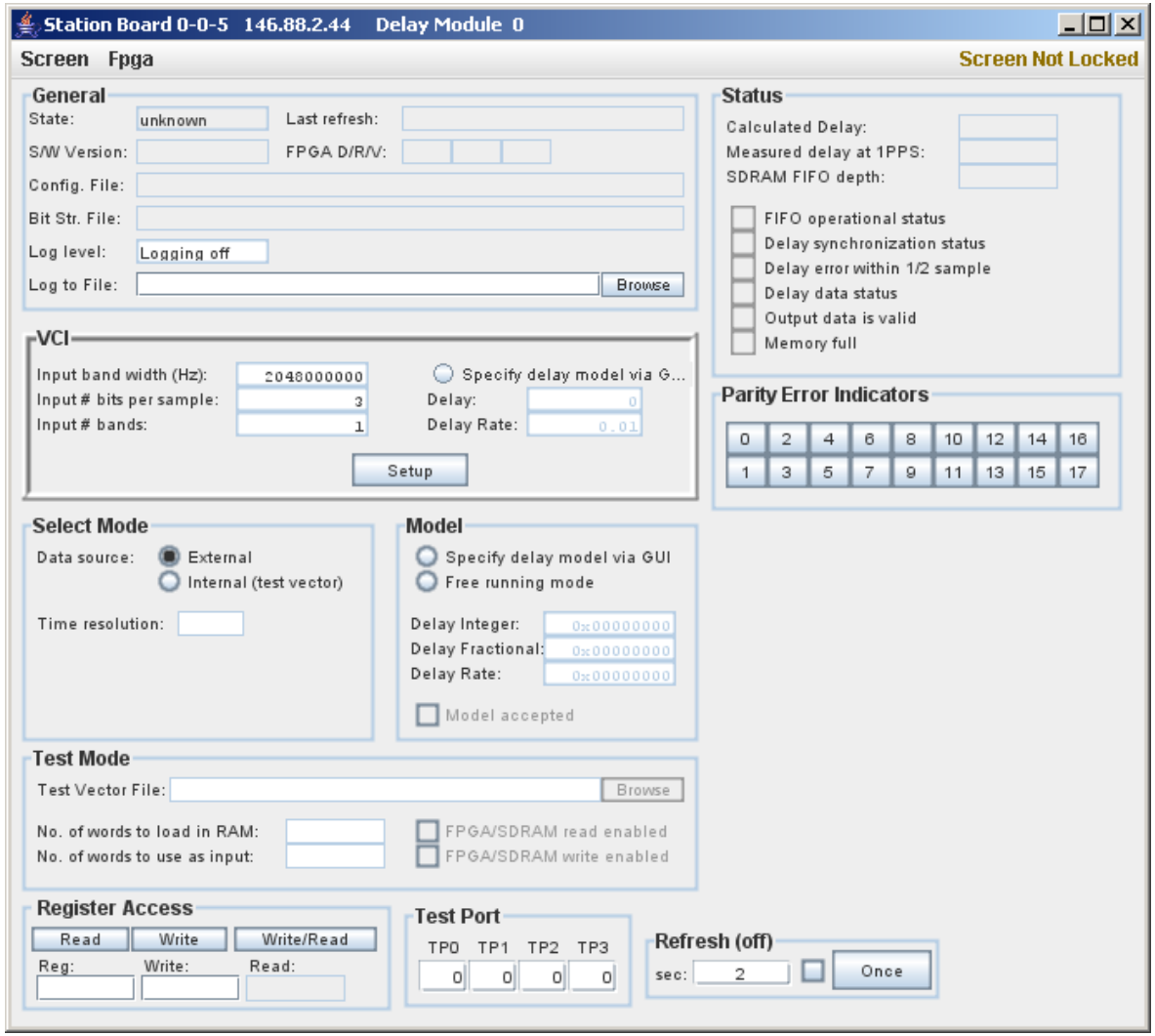

Figure 11-4 Delay Module GUI

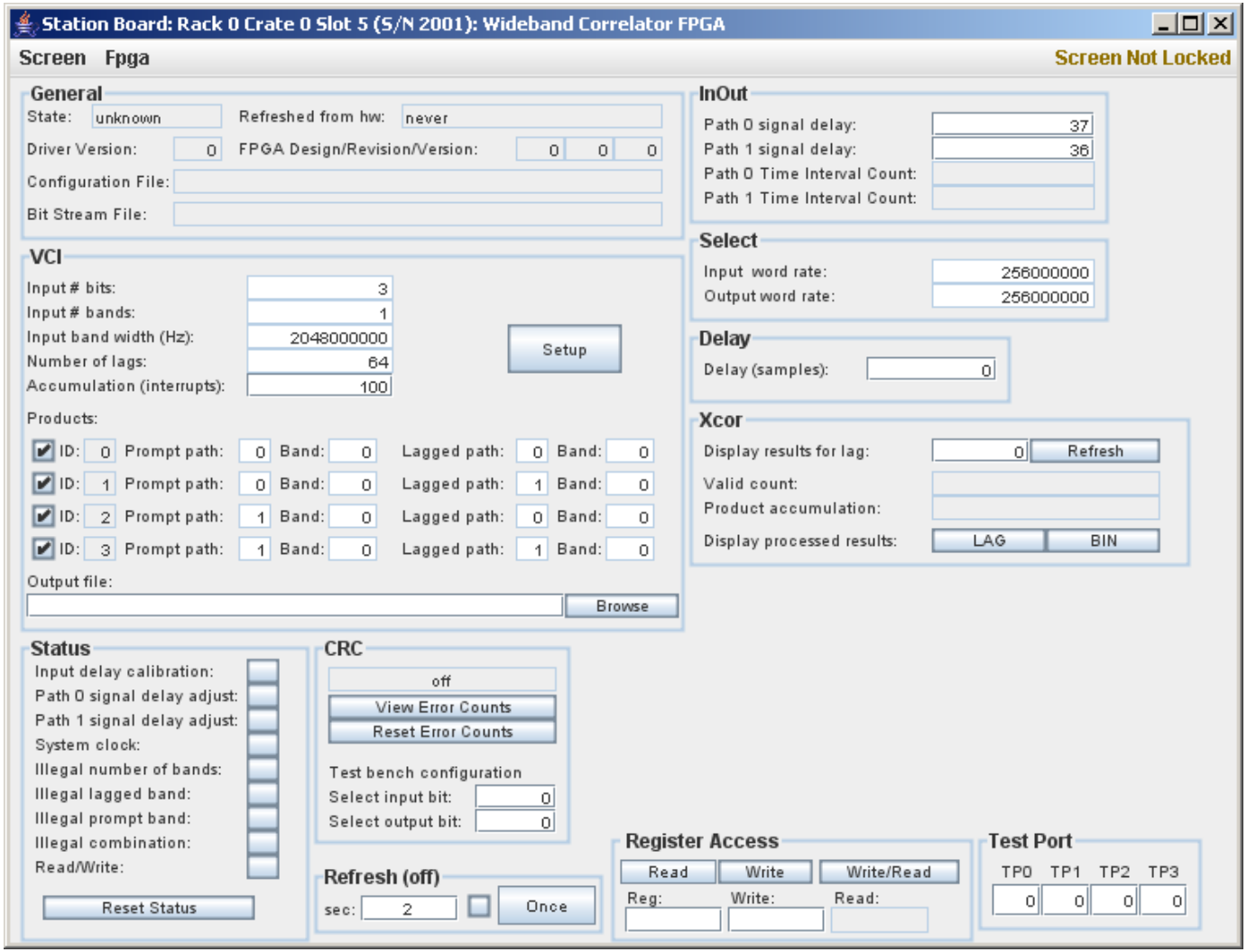

Figure 11-5 WBC FPGA GUI

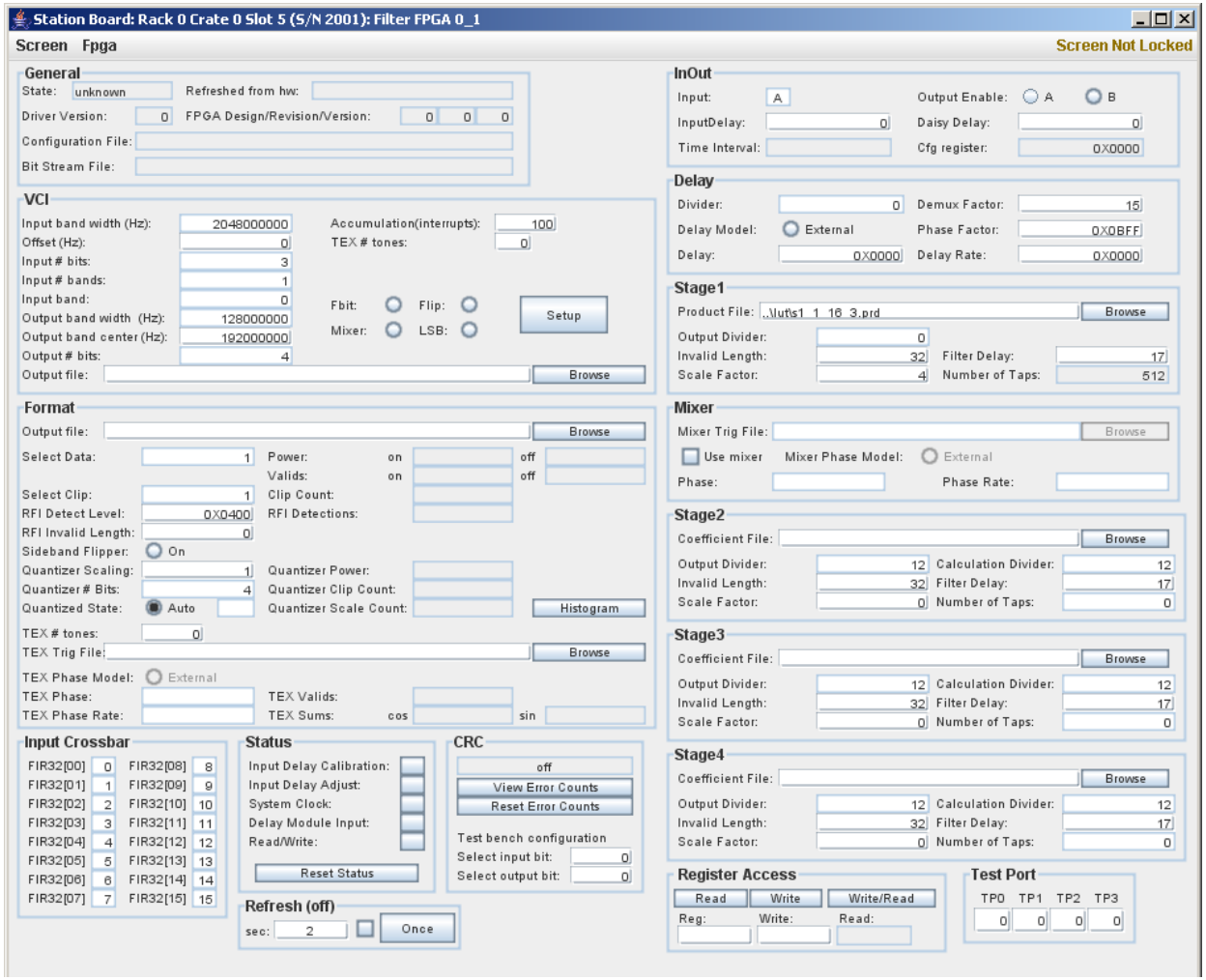

Figure 11-6 Filter FPGA GUI

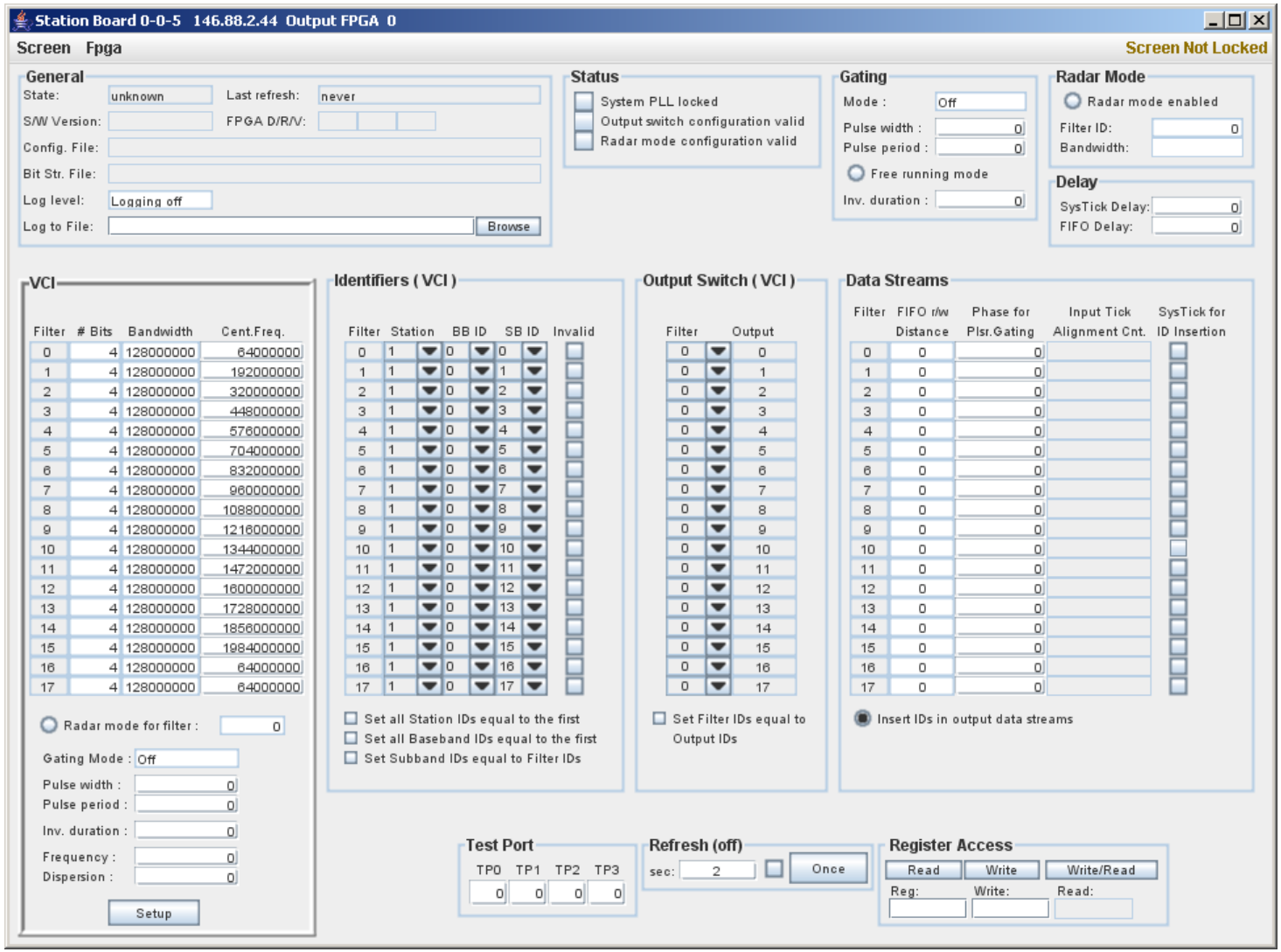

Figure 11-6 Output FPGA GUI

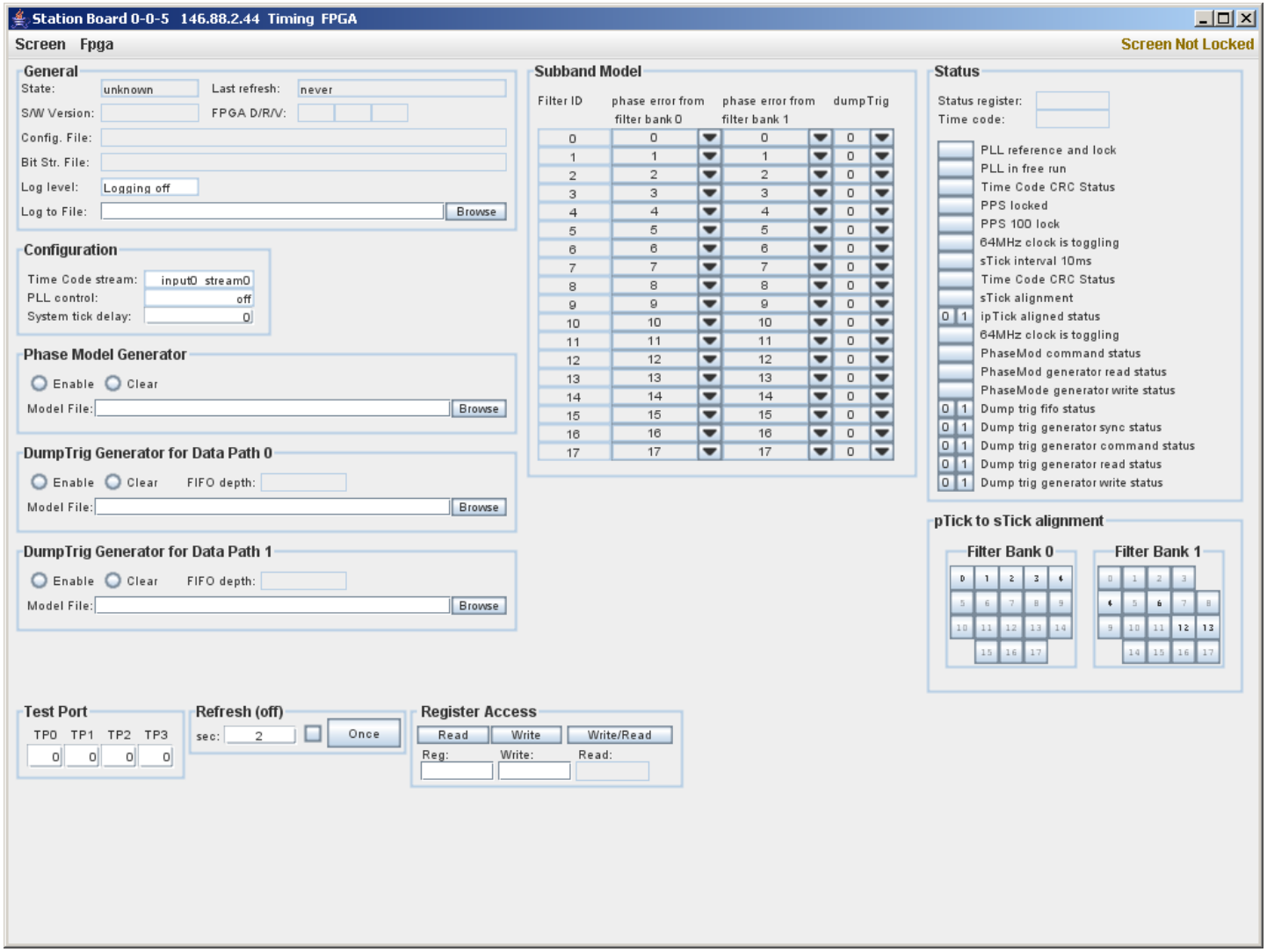

Figure 11-7 Timing FPGA GUI

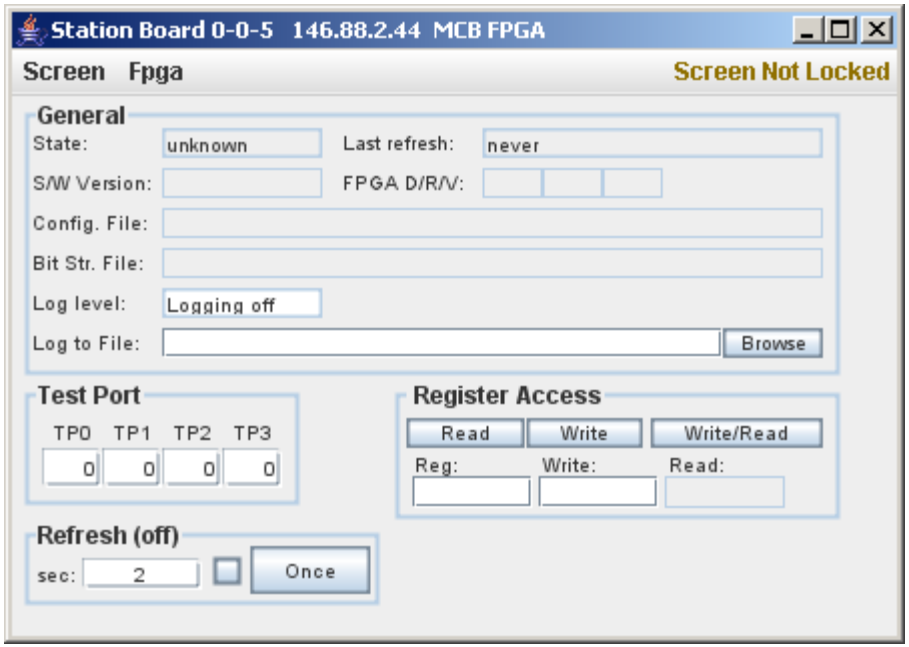

Figure 11-8 MCB FPGA GUI

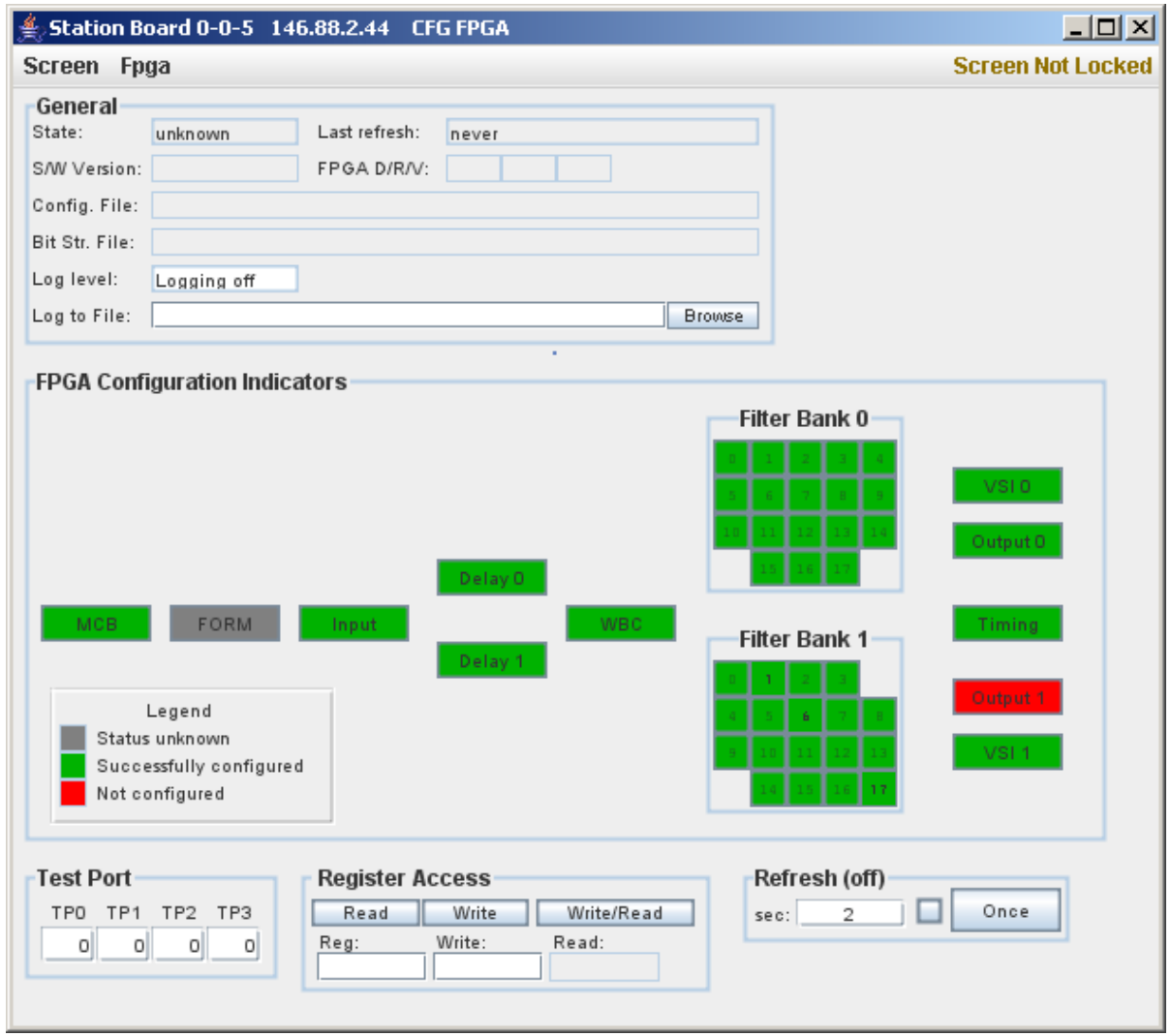

Figure 11-9 CFG FPGA GUI

12 Other Stuff

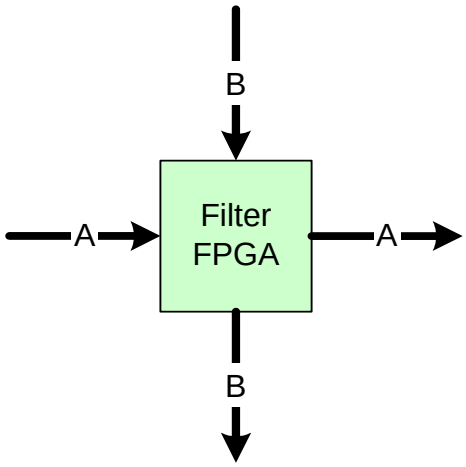

Figure 12-1 Filter I/Os

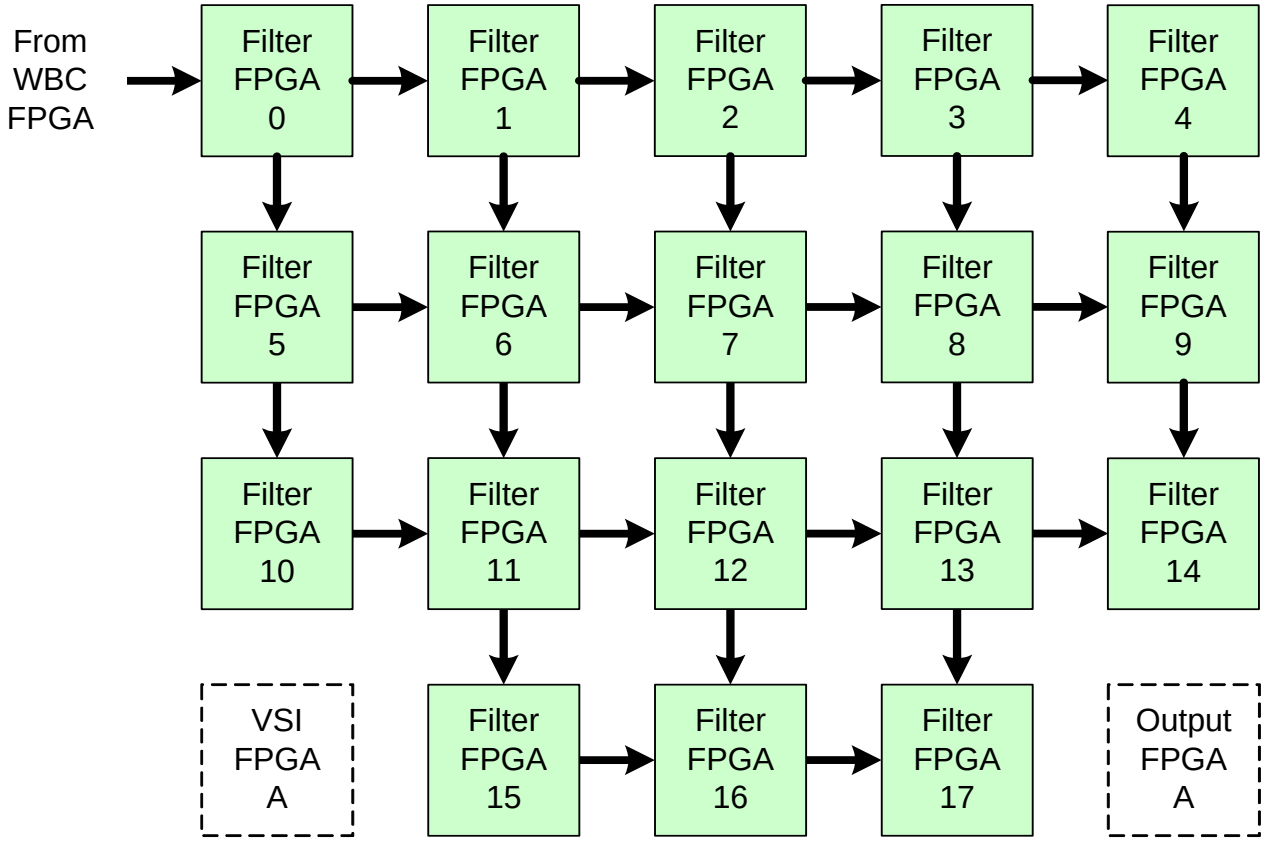

Figure 12-2 Filter Bank A Interconnections

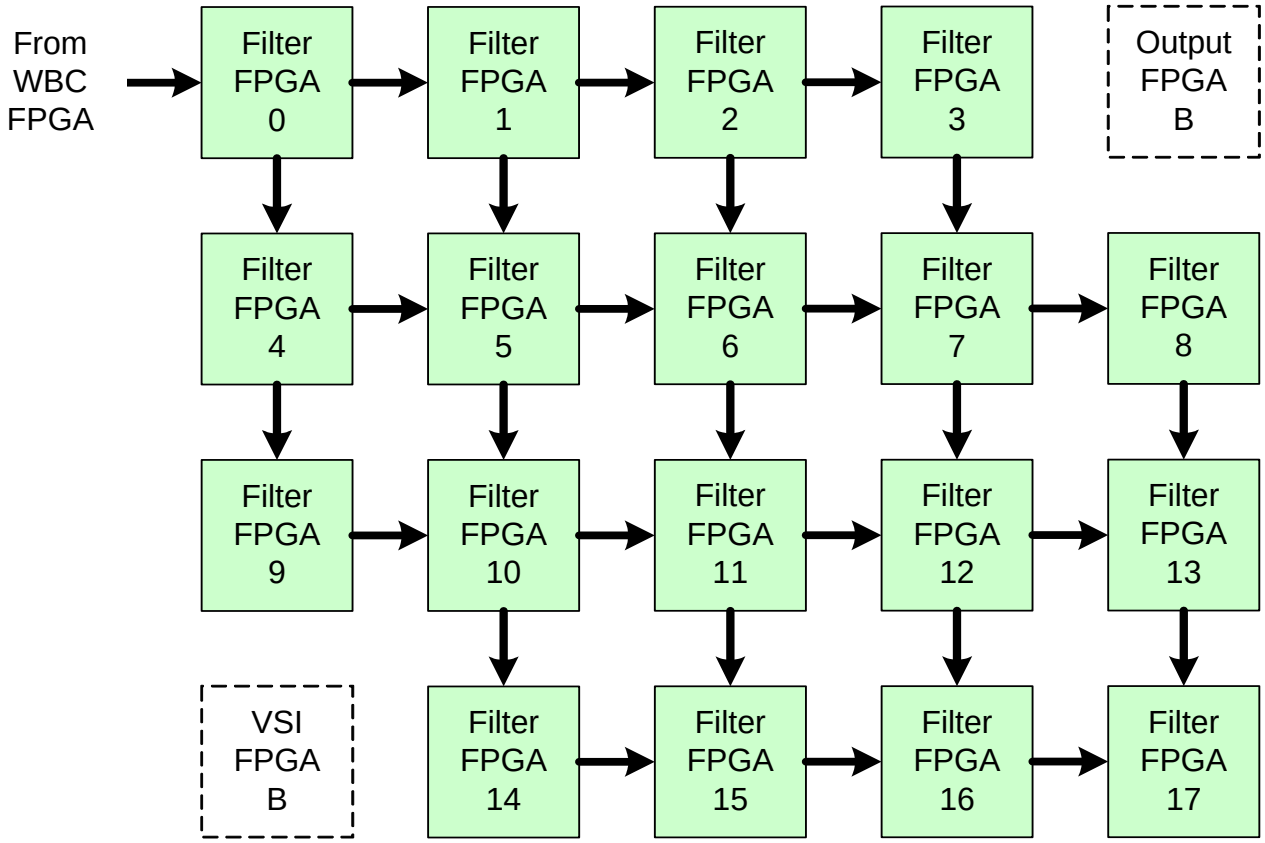

Figure 12-3 Filter Bank B Interconnections

13 References

All information referenced in this document can be found at

Station Board Documents

http://www.drao-ofr.hia-iha.nrc-cnrc.gc.ca/science/widar/private/Station_Board.html