USER MANUAL

EVLA Correlator Station Board

User Manual Document: **A25040N0001**

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D. Fort, 21 June 2011

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List of Abbreviations and Acronyms

BlB	Short for Baseline Board
CBE	Correlator Back End
CFG	short for ConFiGuration FPGA
CMIB	Correlator Module Interface Board
COTS	Commercial Off The Shelf
CPCC	Correlator Power Control Computer
CRC	Cyclic Redundancy Check
eMERLIN	expanded Multi Element Radio Linked Interferometer Network
DLY	short for the FPGA on the DeLaY module
DM	Delay Module
EVLA	Expanded Very Large Array
FIR	Short for Filter FPGA (Finite Impulse Response)
FORM	Fibre Optic Receiver Module
FPGA	Field Programmable Gate Array (NRAO deformatter module)
HM	Hard Metric
JTAG	Joint Test Access Group
INP	short for INPut FPGA
LED	Light Emitting Diode
LSB	Least Significant Bit
LUT	Look Up Table
LVDS	Low Voltage Differential Signaling
MCB	Monitor/Control Bus and MCB FPGA
MCCC	Master Correlator Control Computer
MSB	Most Significant Bit
NMA	New Mexico Array
OUT	short for OUTput FPGA
PCB	Printed Circuit Board
PCMC	PC/104+ Monitor/Control
PLL	Phase-Locked Loop
PPS	Pulse Per Second
RAM	Random Access Memory
RFS	Requirements and Functional Specifications
RMS	Root Mean Square
StB	short for Station Board
TIM	short for Timing FPGA
TPG	Test Pattern Generator
VSI	short for the VLBI Standard Interface FPGA
WBC	short for Wide Band Correlator FPGA
WIDAR	Wideband Digital Architecture
XbB	Crossbar Board
XML	eXtensible Markup Language

1 Revision History

Revision	Date	Changes/Notes	Author
0.0	26 Jun 2009	Initial Draft	D. Fort
1.0	21 Jun 2011	Initial Release	D. Fort

2 Introduction

This document is to provide those who have to maintain and trouble shoot the EVLA Station Board with an overall view of its functionality, external interfaces and other useful information.

The functionality, register sets, pin-outs and pin descriptions for all custom-designed FPGAs on the Station Board are detailed in separate RFS documents. Most of this information will not be repeated here.

FPGA	Mnemonic	Document
Input	INP	A25054N0000
Delay	DLY	A25043N0000
Wide Band Correlator	WBC	A25051N0000
Filter	FIR	A25044N0000
Output	OUT	A25055N0000
Timing	TIM	A25052N0000
VSI	VSI	A25050N0000
Configuration	CFG	A25049N0000
Monitor & Control Bus	MCB	A25053N0000

Table 2-1 Station Board RFS Documents

These documents will be referenced heavily throughout this document and only a relatively simplified description of each device will be provided.

The Station Board (StB for short) is a double-sided surface-mount 12U x 400 mm card containing up to 43 FPGAs on the main board and another 5 FPGAs on mezzanine cards as well as 10 48VDC power supply modules, a PC/104+ CPU mezzanine card and

temperature and voltage monitor circuitry. The completed assembly also includes a monolithic heat sink weighing ~10 lbs over all the hottest (Filter) FPGAs.

The purpose of the StB is to receive data from an antenna, apply independent geometric delay models for each band, divide each band into 18 sub-bands each individually positioned in the main band with independent bandwidths and output the data to the Baseline Boards (via the Crossbar Boards) along with the necessary timing, phase models, fractional phase (from delay) error, Crossbar Board control and Baseline Board dump control information. In addition, a number of functions for calibration and monitoring of the input and output signals are made available to the system software.

Input data can consist of two 2048 MHz bands sampled at 4 bits or two 1024 MHz bands sampled at 8-bits. The fibre optic transmission system and the NRAO-supplied deformatter mezzanine card limit the 8-bit case to one 1024 MHz band but the StB is capable of handling two. Sub-band bandwidths of 128 MHz, 64 MHz, 32 MHz, 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz, 62.5 kHz and 31.25 kHz are selectable.

The board contains a “CMIB stack”, consisting of a COTS PC/104+ (3.5” by 3.5”) embedded CPU card running a real-time Linux OS mated with a PC104 Mezzanine Card (PCMC). This CMIB CPU provides an on-board intelligent monitor and control of the board and communicates with outside world using the XML protocol on Ethernet TCP/IP via and RJ-45 connector currently set for 100 Mb/s. The PCMC, sandwiched between the PC/104+ and the StB motherboard, provides a simple synchronous bus interface to the MCB FPGA which provides address decoding and bus fan-in/fan-out to allow the CPU read/write access to all FPGAs on the board. The design of the FPGAs, data paths and signalling protocols do not require high performance from the CMIB or connections to the board.

The StB power dissipation is 610 W maximum. The board is powered by dual independent -48 VDC inputs, both of which are required. The inputs are each protected with 60 WVDC 1500 W transient absorbers, crow-bar protected with on-board 10 A fuses to prevent voltage spikes from damaging the board’s power supplies. All board power supplies are in sockets and are ¼ brick or 1/8 brick Artesyn DC-DC converters and contain integrated thermal overload and over-current protection. The board contains integral, redundant dead-man thermal=overload protection and will automatically shutdown if the monolithic heat sink temperature exceeds 65 C.

2.1 Acknowledgements

The design, construction, test and deployment of the Station Board has depended on the efforts of many people.

Zoran Ljusic built the schematic, laid out the board, designed several FPGAs and was heavily involved in the board testing (even the first prototype worked well!). Zoran also designed the Delay Module mezzanine card. Heng Zhang did the initial design on the Timing FPGA and was responsible for the PC/104+ mezzanine card. Mike Revnell (NRAO) was responsible for the deformatter mezzanine card. Ralph Webber did the heat sink and front panel design as well as being responsible for the production testing of the 128 (+ spares) boards. Amy Fink kept track of time, budgets, parts, predictions and dealing with the board manufacturer. Pete Pelletier, Shelley Deakin and Dale Basnett were instrumental in the assembly and testing of the production boards. Mark Halman helped with the thermal design aspects of the StB and associated crate and rack. Donna Morgan kept the documentation organized and Josh Fink did the same for parts.

Sonja Vrcic was responsible for the Graphical User Interface to the StB as well as many other aspects of the system software design and implementation. Bruce Rowen (NRAO) was responsible for the real-time software for the PC/104+ which required an understanding of how each FPGA design worked in some detail.

Ken Sowinski (NRAO) along with Michael Rupen (NRAO) did most of the on-site and on-sky testing which resulted in more robust firmware for the FPGAs. Kerry Shores (NRAO) was (and is) responsible for the care and feeding of the StBs after delivery to the VLA site.

There are many others, not mentioned above, who contributed to the success of the StB and consequently to the current good state of the WIDAR correlator.

3 Context

There are two large (12U by 400 mm) boards in the EVLA Correlator system, the Station Board and the Baseline Board. The 128 Station Boards reside in 8 Station Racks and the 128 Baseline Boards reside in 8 Baseline Racks. Both types of racks contain two 12U crates with a 6U crate in between and are cooled by 4 fans at the top of the rack which suck cold air from under the floor, through the crates and out the top, considerably warmer. In the Station Rack, the 6U crate is populated with Crossbar Boards. The main functions of the Station Board are to receive wideband data from the antennas, perform the wideband delays necessary to compensate for earth rotation, divide the wideband data into narrower sub-bands and transmit the sub-band data to the Baseline Boards via the Crossbar Boards. A simplified block diagram of the correlator is shown below.

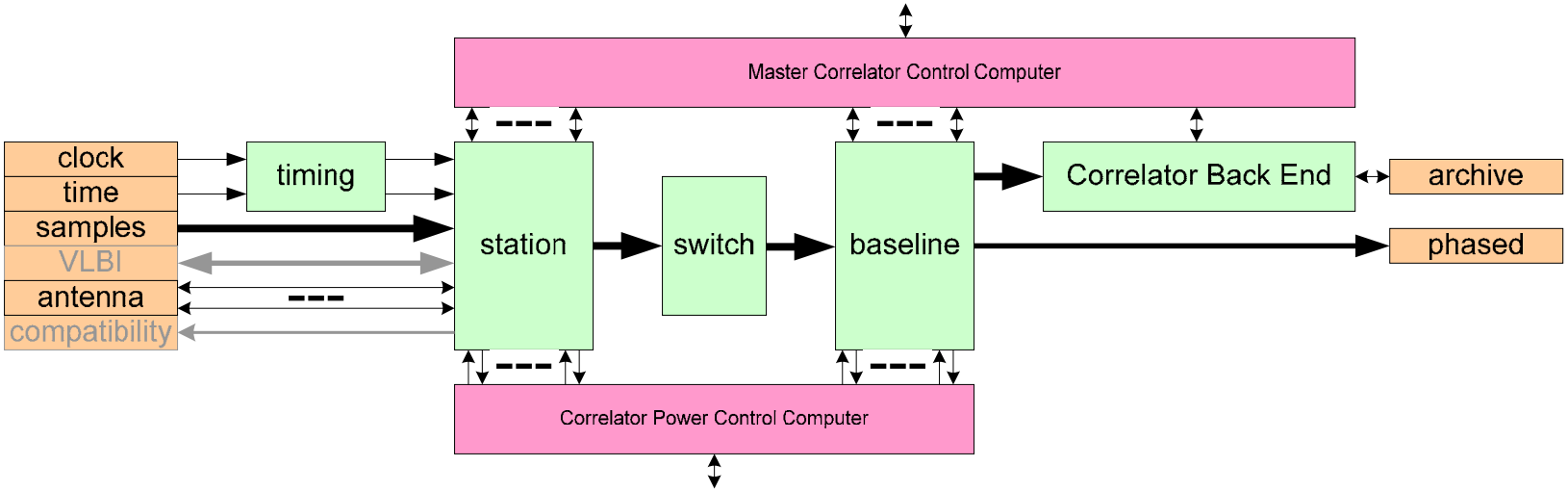


Figure 3-1 Simplified block diagram of the ELVA Correlator

The Station block contains 128 StBs, the Baseline block contains 128 BlBs, the Switch block contains ? XbBs and the Timing block contains ? XbBs. Originally, the WIDAR correlator was to be used to correlate data from the VLBA + NMA and record data from the EVLA (phased) and from the NMA antennas but this function is no longer needed as the VLBA adopted a software correlator and the NMA has not been funded. Only the eMERLIN correlator is has StBs that are populated with the FPGAs necessary for the "VLBI" interface. The "compatibility" outputs of the StBs were used during the transition phase between the old correlator and the WIDAR correlator and provided 50 MHz analog signals.

An input/output diagram of the Station Board is shown below.

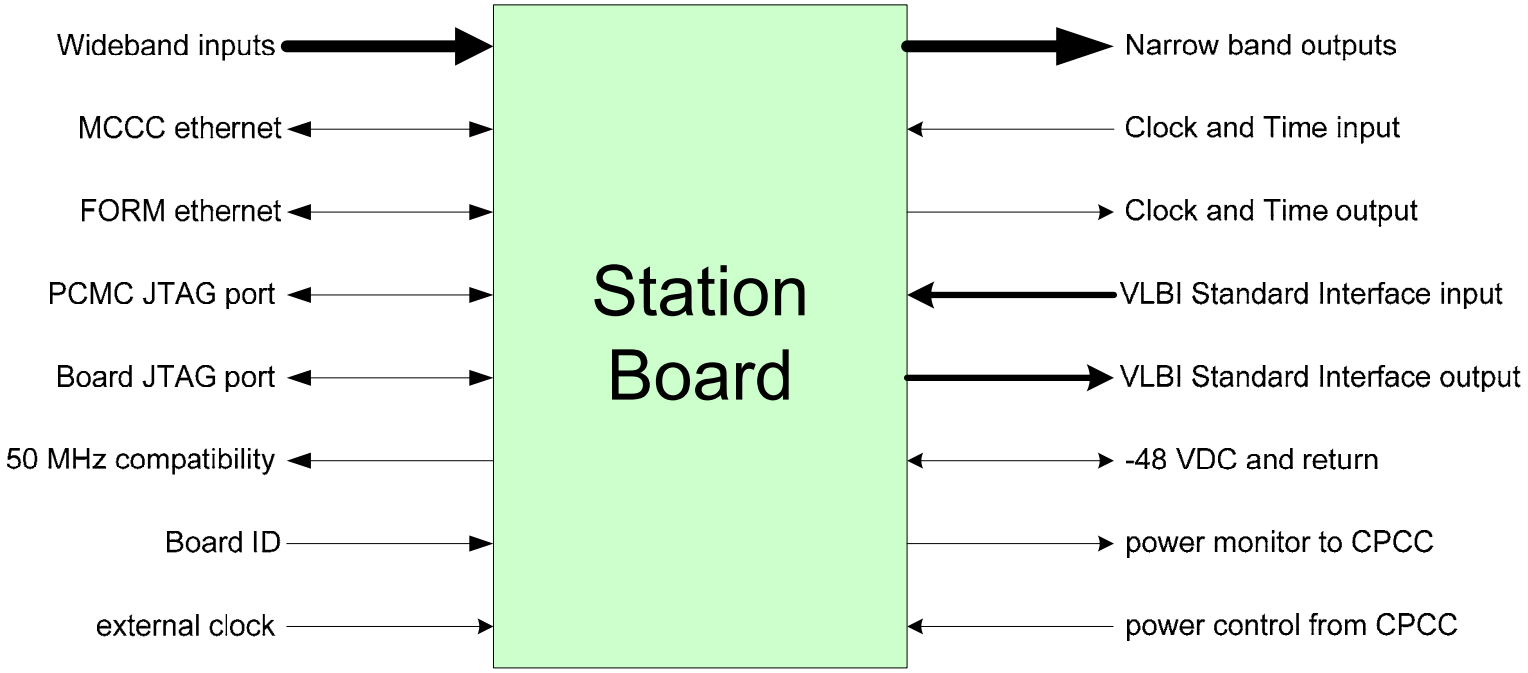


Figure 3-2 Functional I/O diagram of the Station Board

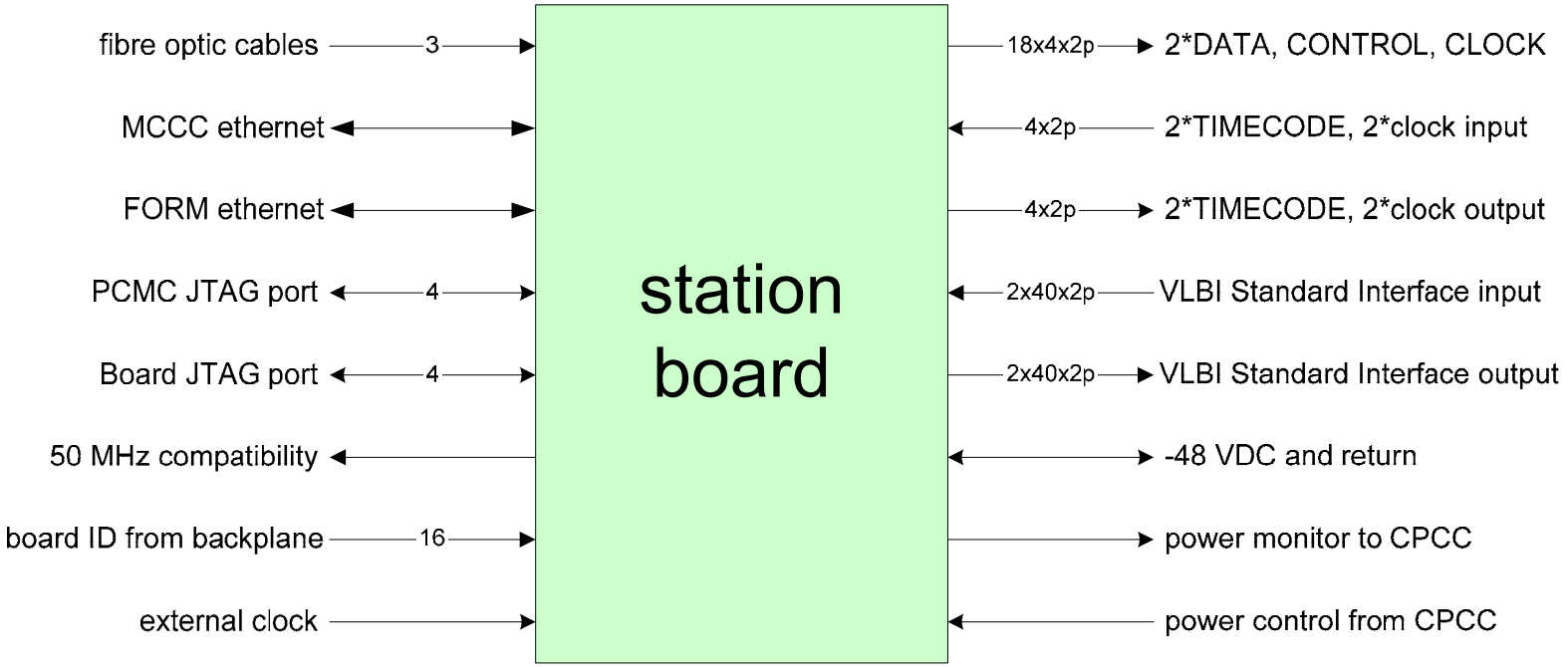


Figure 3-3 Physical I/O diagram of the Station Board

The wideband inputs consist of three optical fibres to the FORM, an NRAO-supplied mezzanine card on the StB (see A25045N0000). There are enough copper connections (two 64-wire buses running at 256 Mb/s per wire) from the FORM to the StB to handle two 2048 MHz bands sampled at 4-bits per sample; however, the FORM would have to be redesigned to use them. The FORM also produced the "compatibility" output used during the transition from the old correlator to the WIDAR correlator. The FORM is controlled by a separate ethernet connection to the antenna control system.

There are two sets of 18 narrow band outputs that appear on the centre HM connector. Only two sets of 16 are connected to the rest of the system. The four spare Filter FPGAs can be used for calibration by making independent measurements anywhere in the baseband.

The PCMC JTAG port can be used to program the FPGA on the PCMC. The board JTAG port was used during production to check that most of the copper connections were correct as the part of the production test procedure.

The "board ID" consists of 16 pins, 8 on each of the outer HM connectors that are hard wired with the location of the board in the system.

"Clock and Time" include a 128 MHz clock input only used during testing and two sets of 128 MHz clock and TIMECODE (see A25022N0043).

4 Overview

A simplified block diagram of the Station Board is shown below. Each Station Board can receive a pair of 2 GHz basebands sampled at 4-bits or a wide variety of other arrangements that total 16 Gb/s as shown in the figure below.

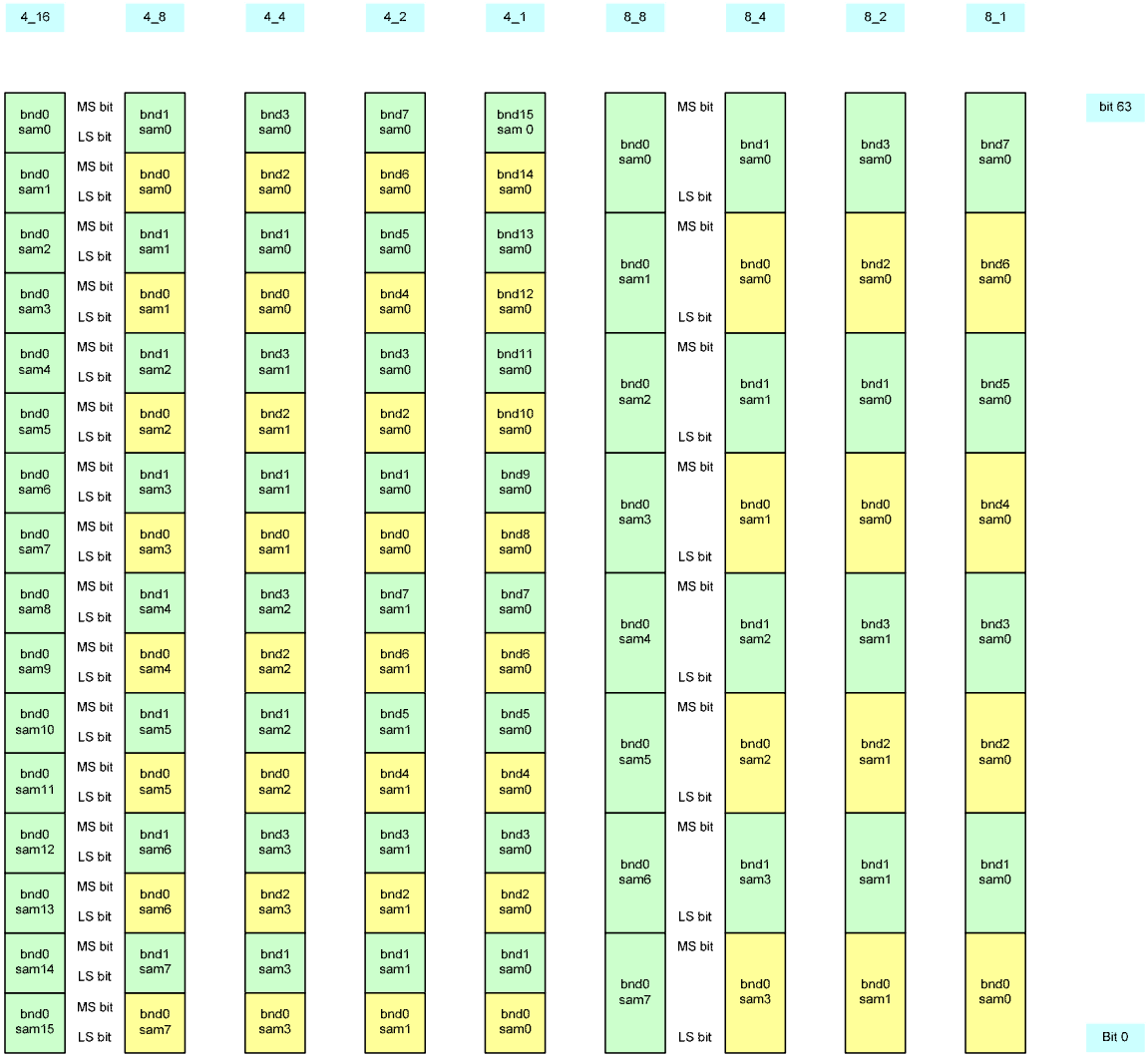


Figure 4-1 Allowed Input Arrangements

The current EVLA fibre optic transmission system and FORM limit the wideband inputs to two 2 GHz basebands sampled at 3-bits or one 1 GHz baseband sampled at 8-bits. When the board is receiving two 2 GHz basebands then they are typically a right and left circularly polarized pair. eMERLIN transmits both polarizations in the 8-bit mode by reducing the bandwidth to 512 MHz (mode 8_4 above).

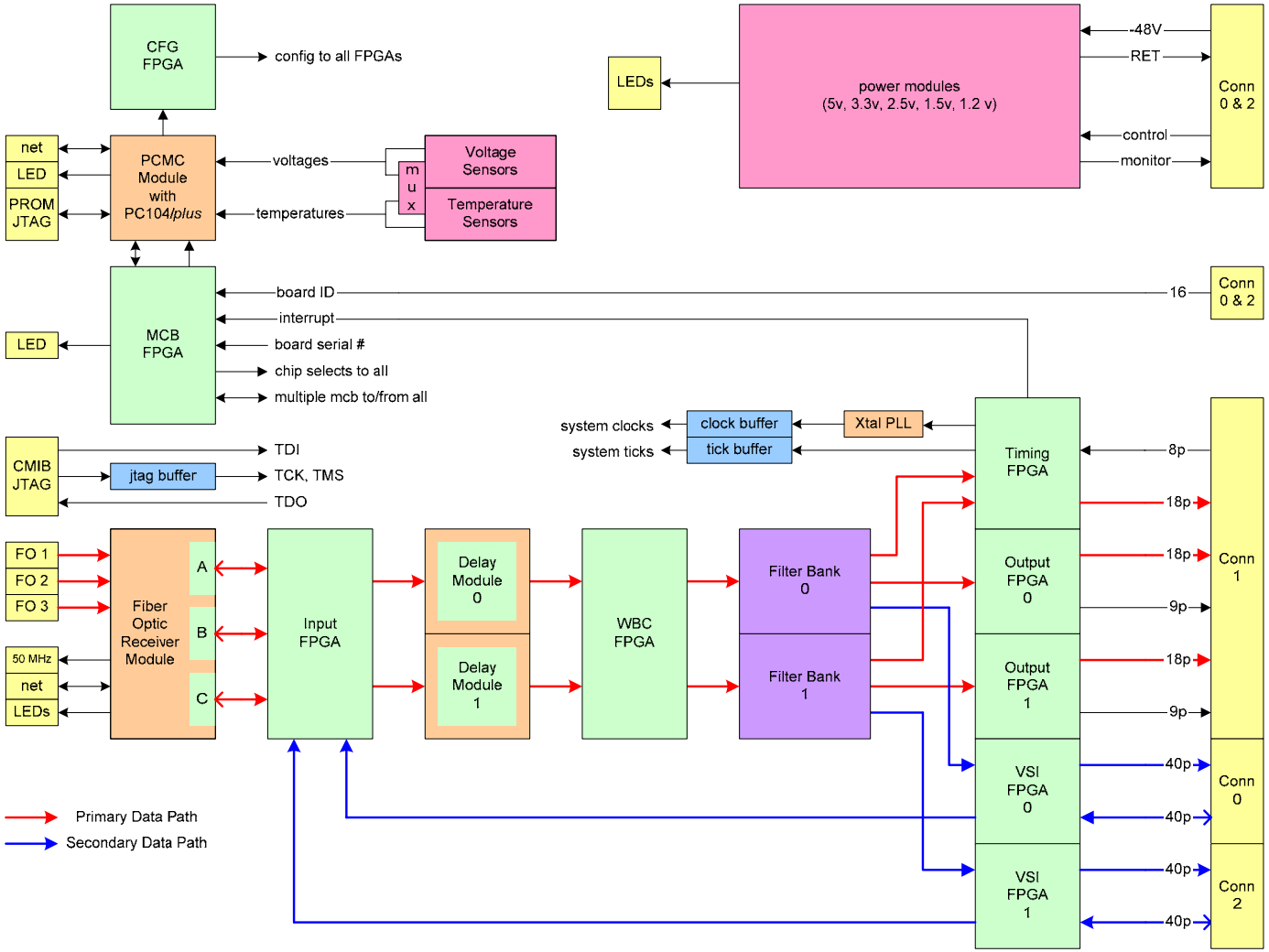


Figure 4-2 Simplified Block Diagram of the Station Board

The data paths are shown in the above figure as red for the primary data path and blue for the secondary data path. Only the primary data path is used by the EVLA. The secondary path is meant to be used by VLBI record/playback units using the VSI. After the FORM does its job of converting the signal from photons to electrons, the data is sent to the Input FPGA as three 32-wire buses running at 256 Mb/s per wire. A "full-up" system would have required 4 optical fibres and four 32-bit buses running from the FORM to the Input FPGA at 256 Mb/s to give two 2048 MHz basebands sampled at 4-bit or two 1024 MHz basebands sampled at 8-bits. The four buses between the FORM and the Input FPGA are present on the StB but only three are used by the FORM. The wideband data presented to the FORM is generally the output of samplers in an antenna and are usually in offset binary – 0 representing the most negative voltage and 0xF (4-bit samples), 7 (3-bit samples) or 0xFF (8-bit samples) representing the most positive voltage. If the RMS voltage into the samplers is sufficiently high, the output samples will be clipped and represented by either the most negative code or the most positive code. One characteristic of these samples is that there is no zero level represented in the code. The Input FPGA chooses whether 3-bit or 8-bit samples are expected and contains lookup tables which allows any code to be converted to any other code. The output of the Input FPGA is two 64-wire buses running at 256 Mb/s per wire. Offset binary was chosen as the way to represent wideband data throughout the StB so that a one to one mapping is normally used (the default) for the INP lookup tables. Conversion to 2's complement would have required another bit in order to maintain precision. This means that the wideband data presented to Delay Module, the Wide Band Correlator FPGA and the Filter FPGAs is 64 bits wide with the samples encoded as offset binary. The Delay Module does not care about the encoding because no arithmetic is done on the samples. The WBC and FIR FPGAs perform arithmetic on the samples and the Verilog code that does this must take into account the encoding. The Filter FPGA uses lookup tables for stage 1 and therefore the sample encoding is buried in those LUTs. The narrow band data from the Filter FPGAs, samples and phase error, are coded as 2's complement but the most negative state (0x8 for 4-bit samples and 0x80 for 8-bit samples) is not allowed and is used as the data invalid marker. The default invalid encoding for 7-bit samples that are going to the BlB has an MSB of 1 for a valid sample and MSB of 0 for an invalid sample to conform to the BlB's bit-dependent protocol.

Another general feature of the StB is that control, model and monitor information is controlled by a 10 millisecond tick. The tick is derived from the system time and aligned

with the data samples by the Input FPGA and this alignment is carried on throughout the board by having a tick accompany every data bus as it travels between FPGAs. In this way, the absolute time of the tick is delayed as it proceeds through the FPGAs but is always aligned with the correct data sample. The hardware tick also generates an interrupt to the CMIB to allow it write or read synchronously with the hardware. Registers can be written at any time but in the cases that matter the information placed in those registers will not take effect until the next hardware tick. Similarly, the reading of registers that will contain the information saved at the last hardware tick for those that matter. This includes measurements and status indicators. The interrupt can be delayed relative to the hardware tick by a programmable number of clocks to make sure that all FPGAs have used the tick before the CMIB writes new values or reads old values. Other signals that may accompany a data bus as it travels inside and between FPGAs is valid indicator, noise diode waveform, uncorrected fractional delay or phase with its frame indicator and clock or sample indicator.

Another general feature of the StB is high speed data interconnection checking using CRCs integrated over the 10 millisecond period. For a given copper interconnect ("wire"), the transmitting FPGA and the receiving FPGA both calculate the 4-bit CRC between ticks. The two CRCs are read and compared by the CMIB during an interrupt. If they are the same then the transmission was likely OK, if not then we have a problem. Because the CRC is only 4-bits, the transmission is not guaranteed to be OK but the probability becomes very high if the comparison is OK for a large enough number of 10 millisecond periods. Normally, there is only one CRC generator or checker for a given bus and the CMIB has to select which wire to check by writing to a register in the FPGA at each end of the wire. No data is lost using this scheme so checking can take place all the time. This feature can also be used for testing a board being fed with a test pattern that repeats every 10 milliseconds (which is true for all the TPGs) because the **value** of the CRC should be constant and the same as a known working board.

Finding parts on the StB can be a problem because of its size and complexity. There are three files that are useful for this task. Two are searchable PDF assembly drawings (top and bottom) and the other is the PCB design file (sb.pcb). The PCB design file requires the **free** PCB Browser from Mentor Graphics. In addition, there is a set of schematic diagrams (sb_V1.2_schem.pdf) which are searchable.

1.

Figure 4-3 Simplified Layout of the Station Board

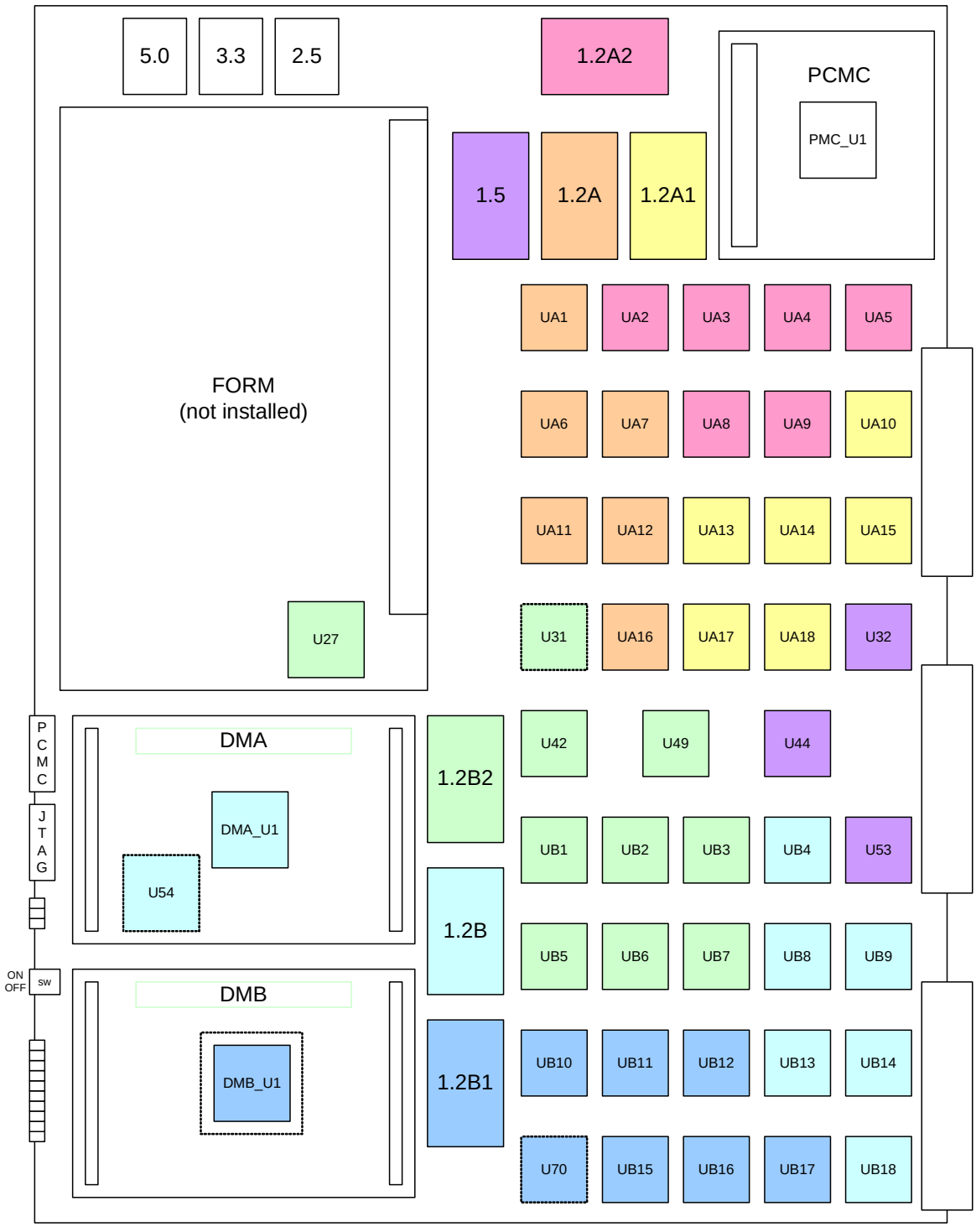


Figure 4-4 Power Map of the Station Board

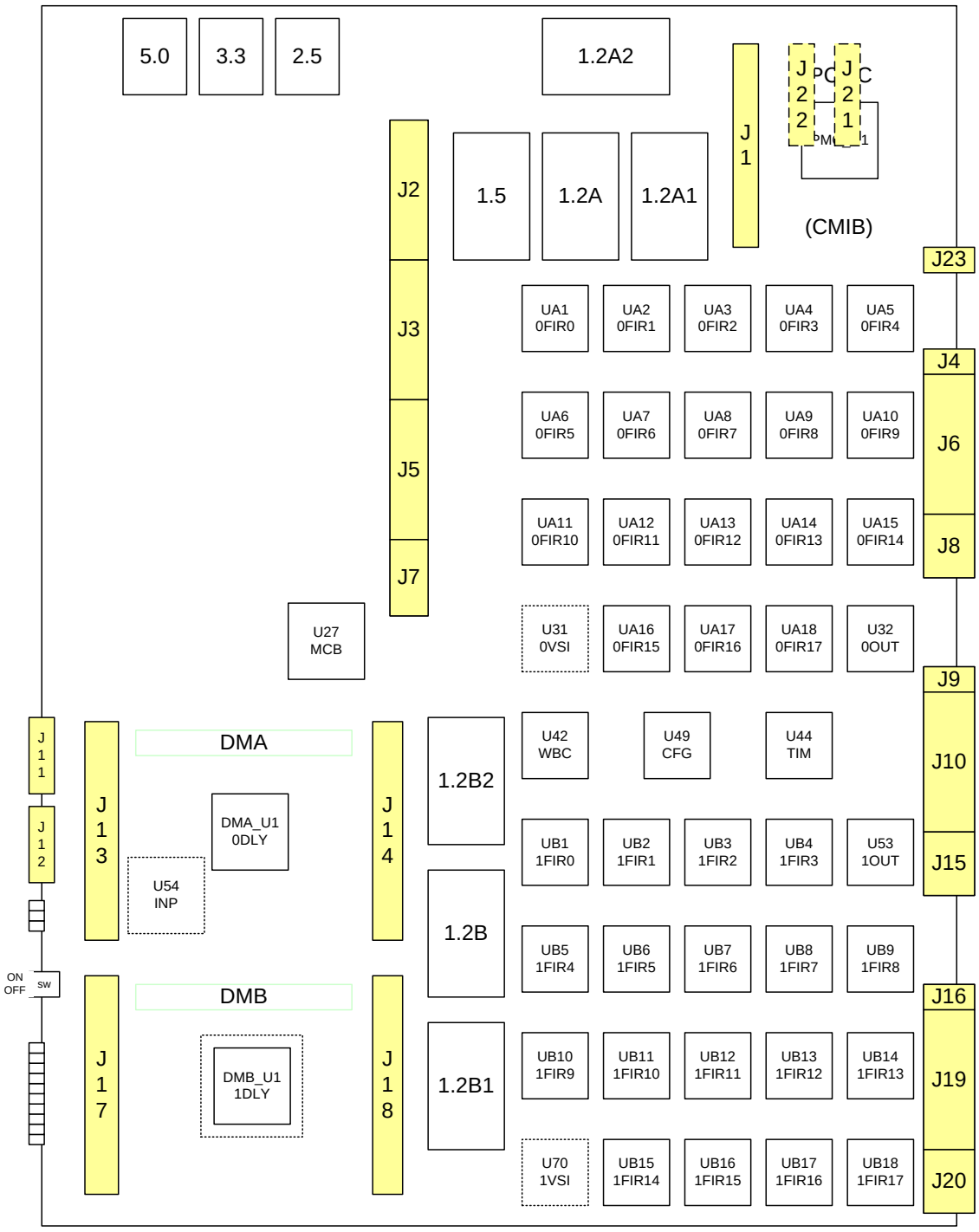


Figure 4-5 Connector Map of the Station Board

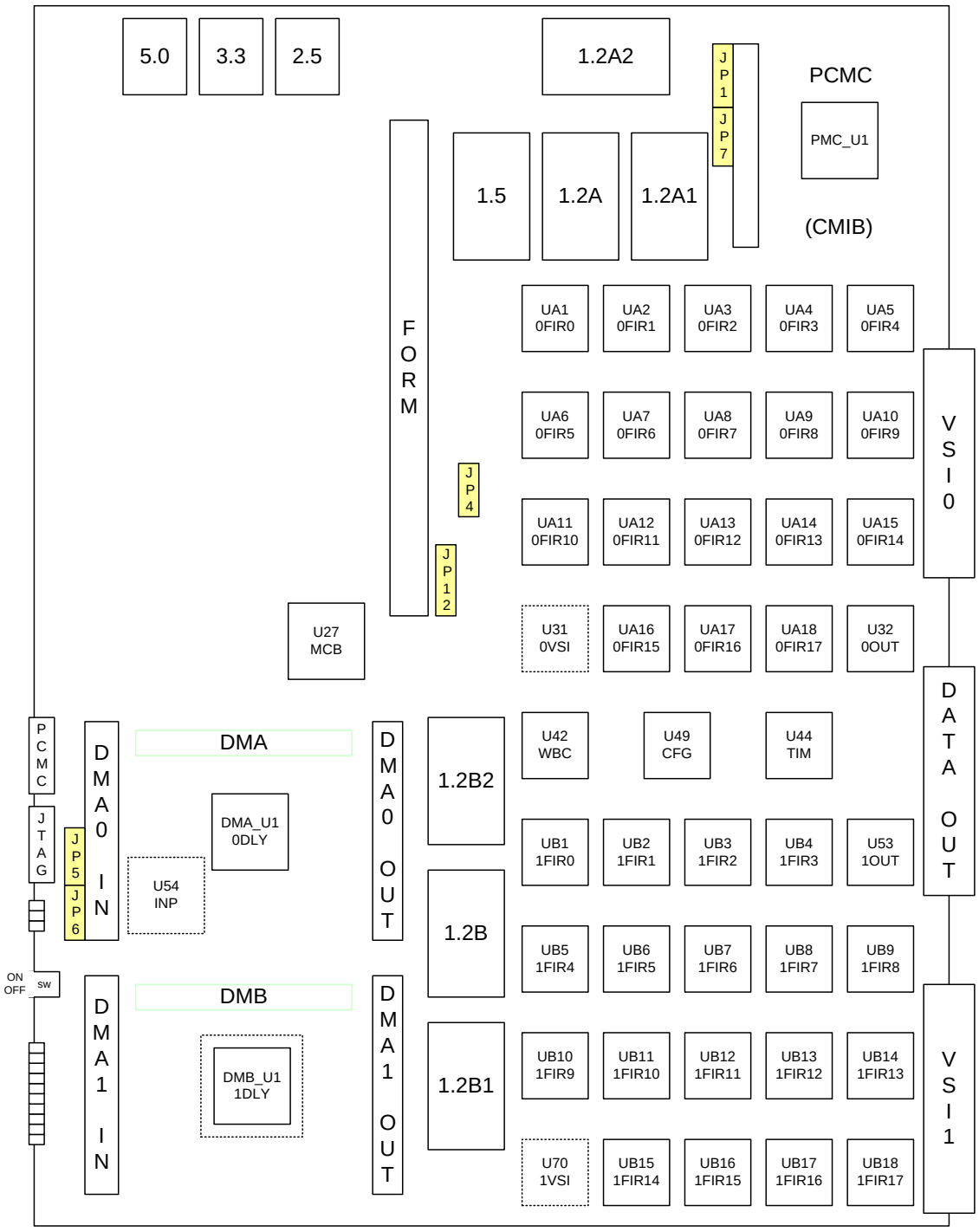


Figure 4-6 Jumper Map of the Station Board

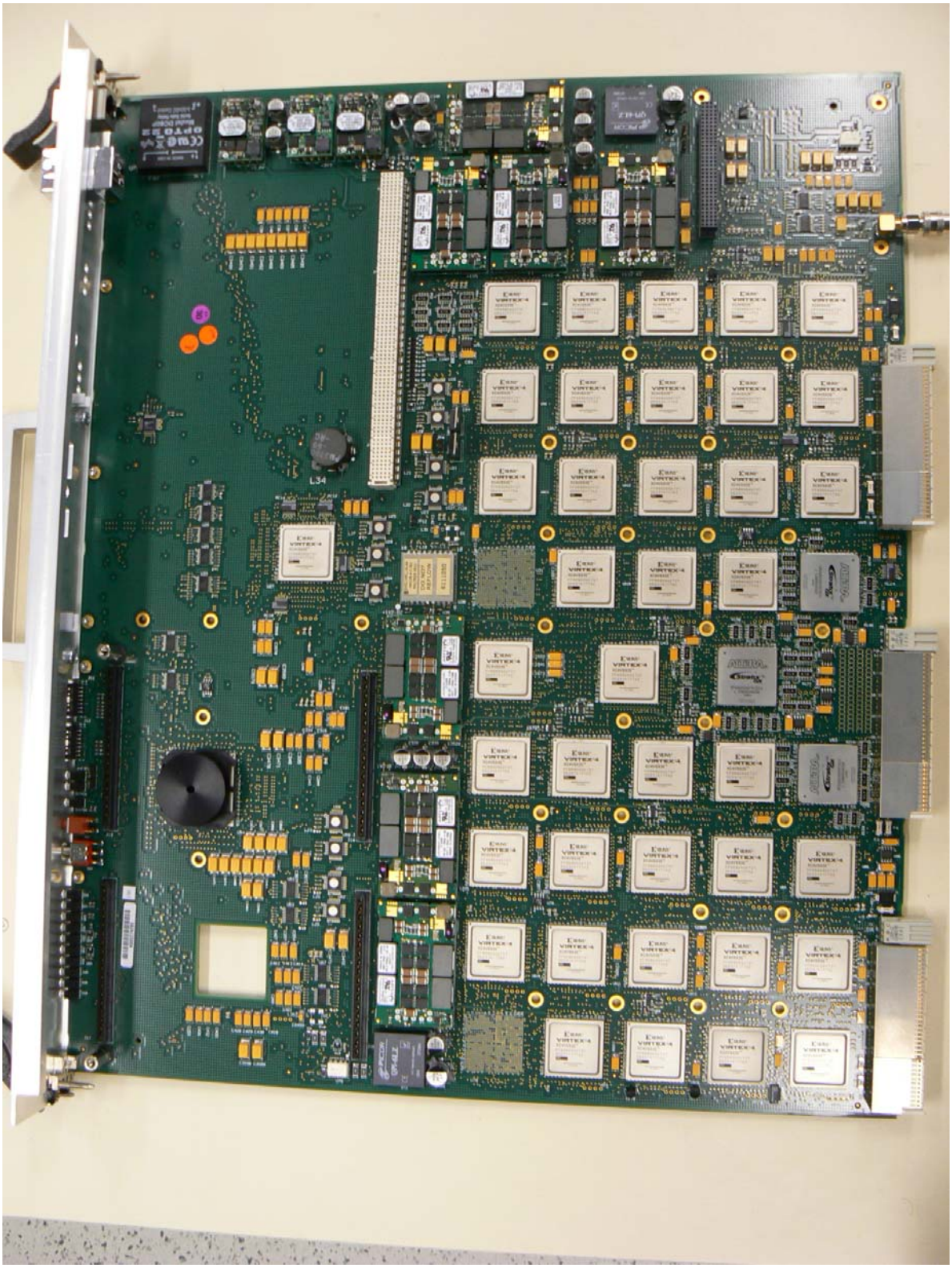


Figure 4-7 Basic Station Board

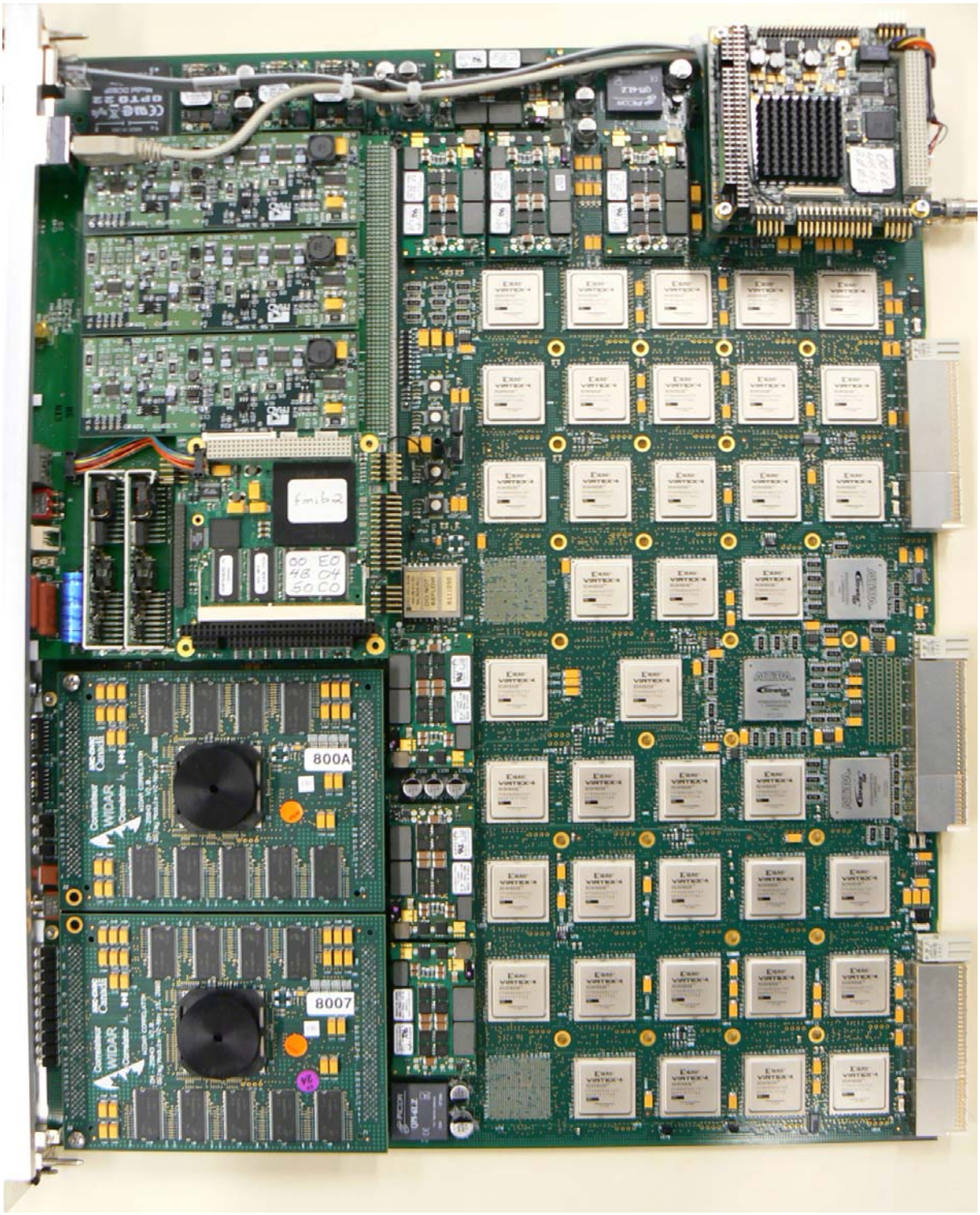


Figure 4-8 Station Board with Mezzanine Cards

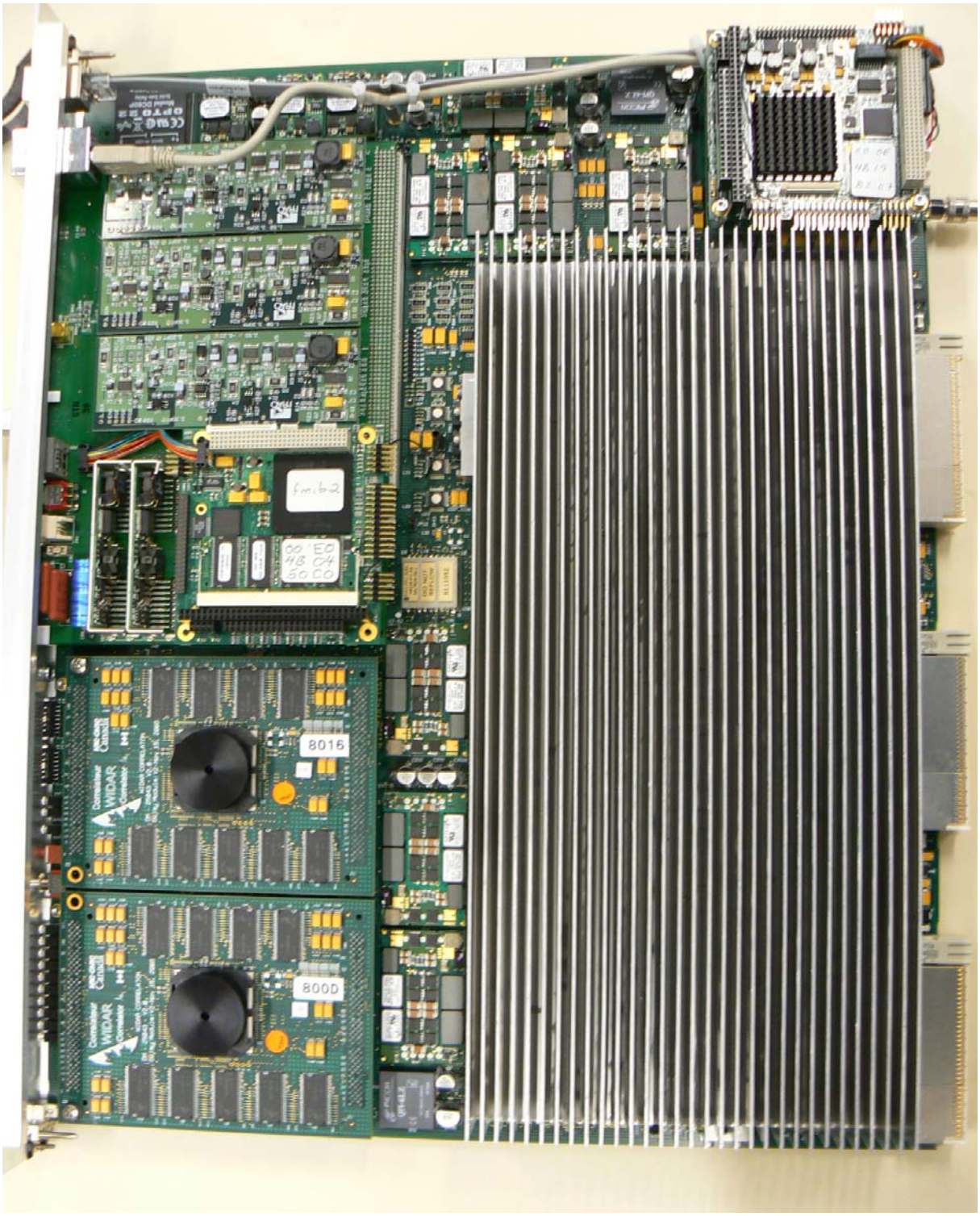


Figure 4-9 Station Board with Heat Sink

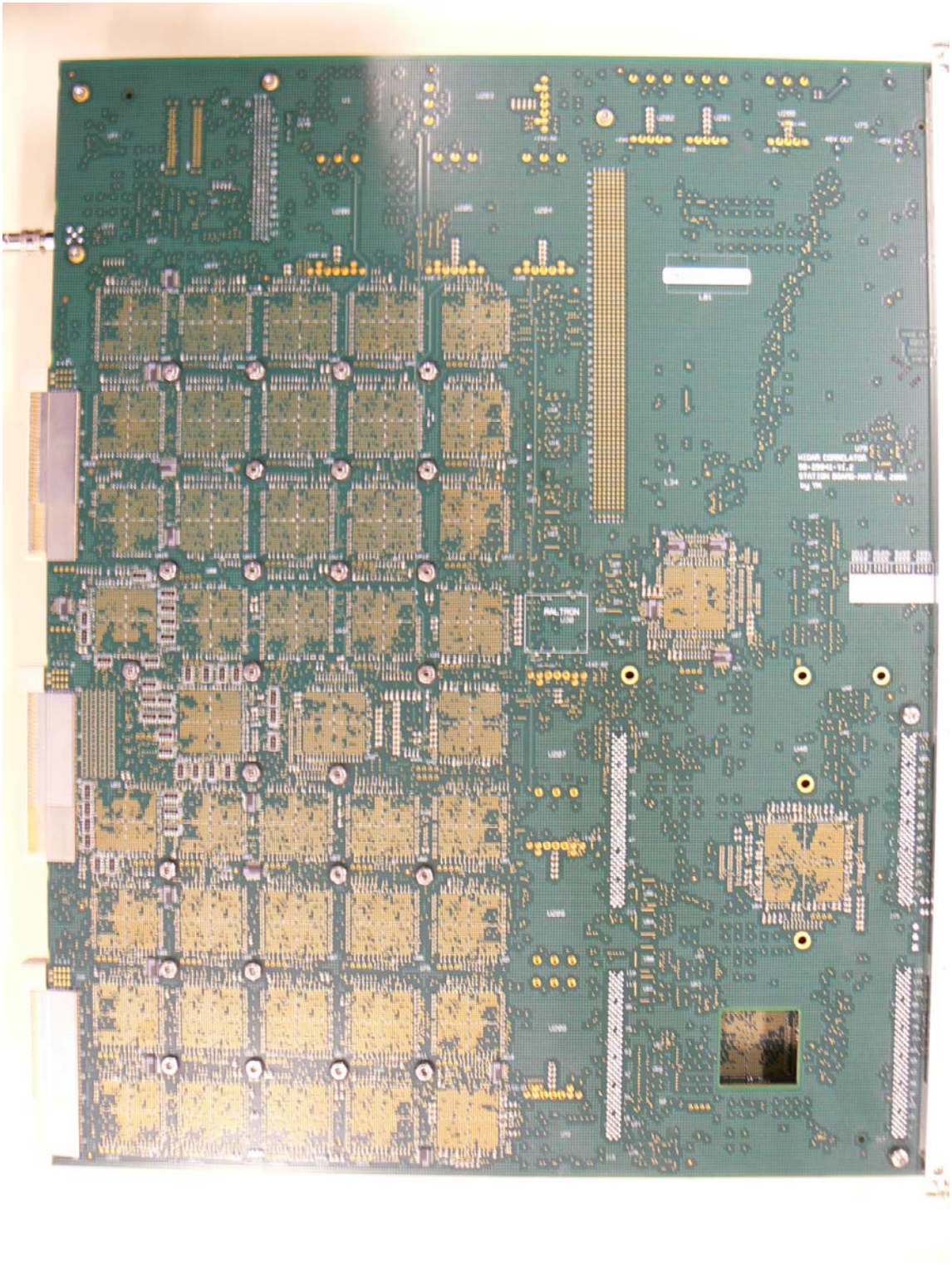


Figure 4-10 Station Board from back

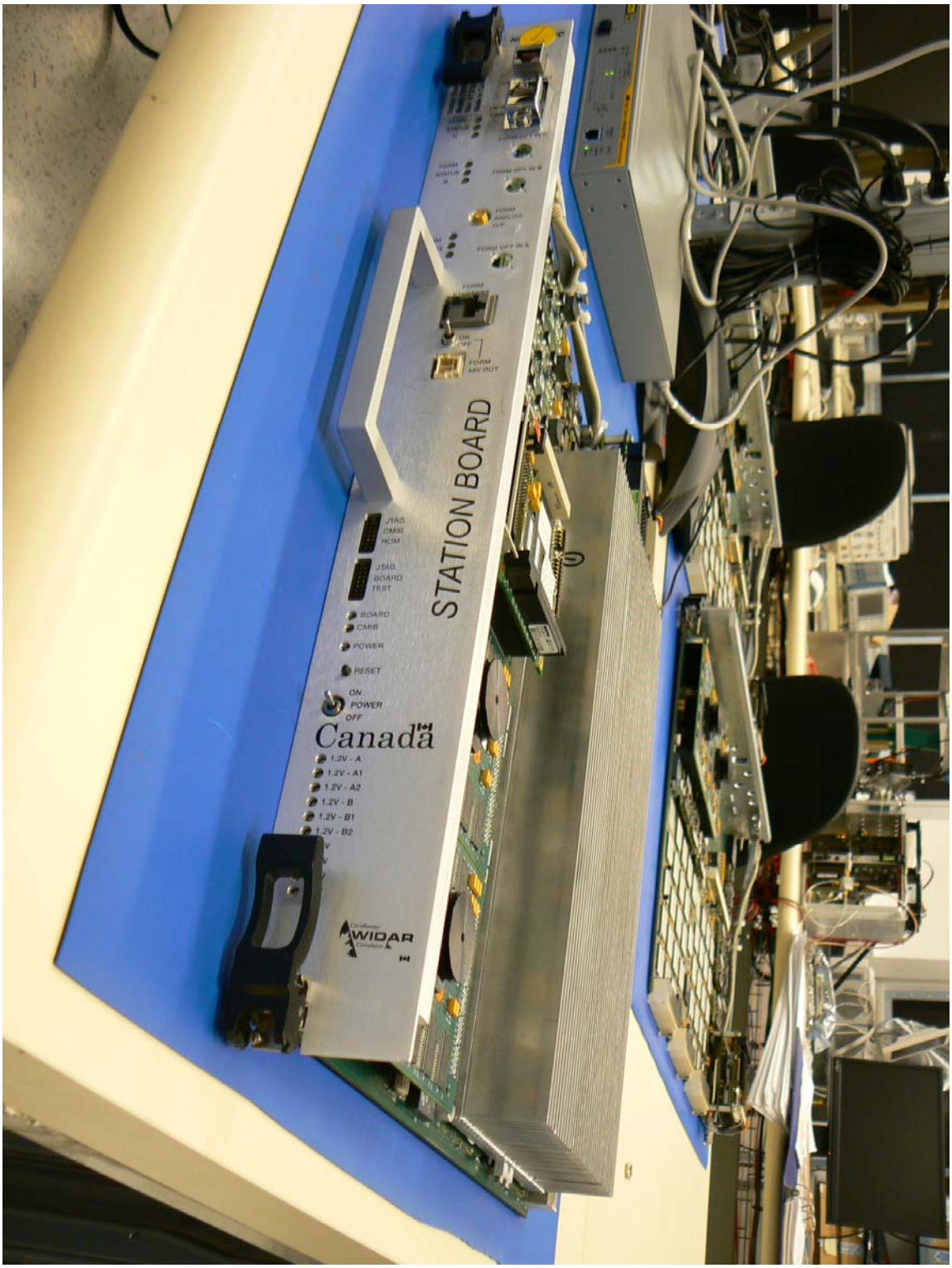


Figure 4-11 Station Board from front

5 Functional Description

5.1 Top-Level Board GUI Description

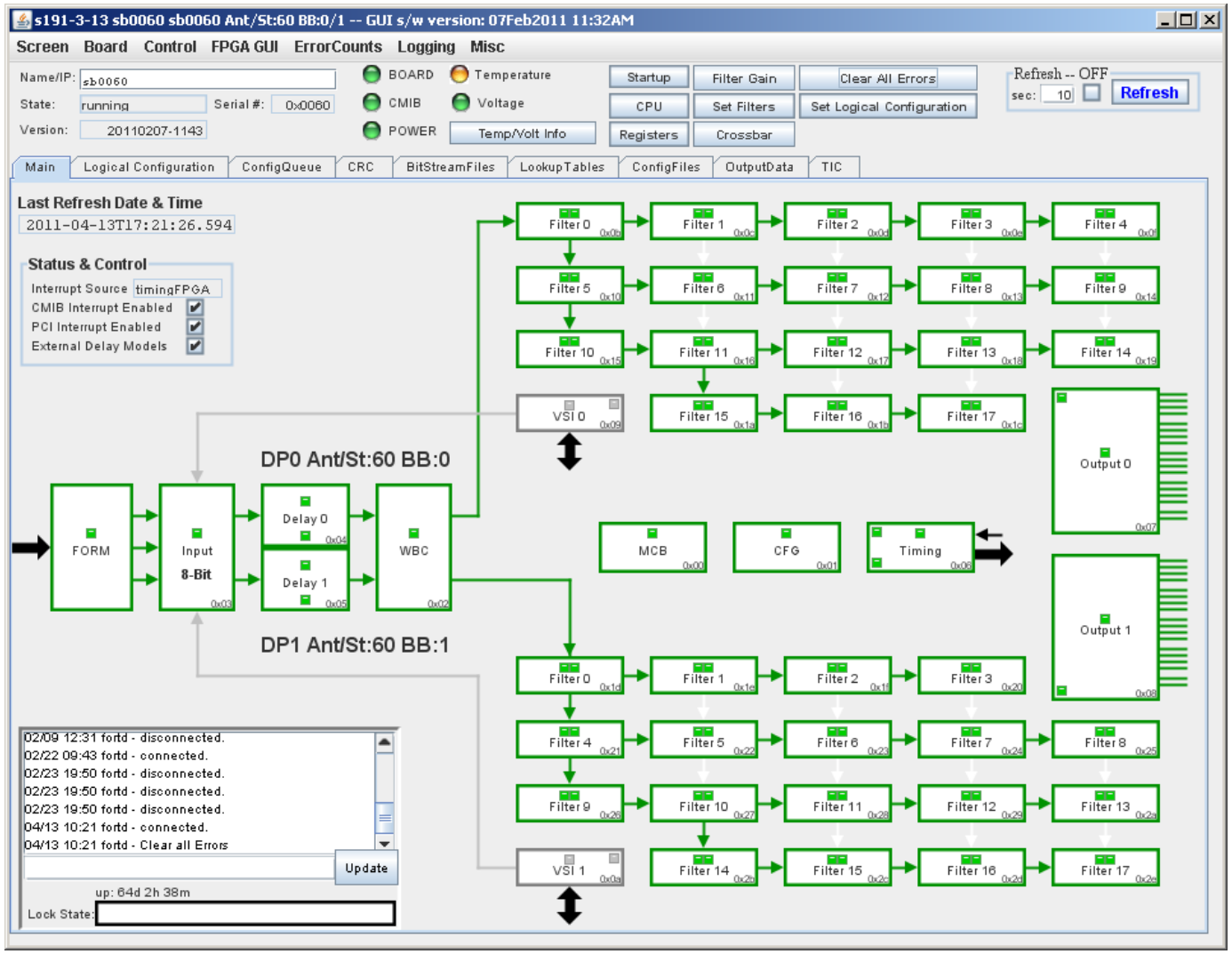


Figure 5-1 Station Board GUI

5.2 FORM Functions

The main function of the FORM is to decode the signals on the three fibres that originate in the antenna, align them in time and output them for use by the Input FPGA and the rest of the StB. Normally this is done by firmware and software described elsewhere but there exists a bit file for the three FPGAs on the FORM which produces signals using TPGs. Configuration of the FPGAs can be done using *form.exe* which is under version control and is described in document A25285N0000 "Miscellaneous Station Board Software" User Manual. One TPG produces random noise while the other uses a user loadable RAM that can be made to output square waves, sine waves, pulse trains etc. This capability was used in the production testing to check the FORM interface with the StB and could be used to test StBs outside of the operational correlator. It requires a FORM but the optical parts are irrelevant.

5.3 Input FPGA Functions

The main functions of the Input FPGA are:

1. Sample encoding conversion
2. FORM interface
3. VSI interface
4. TPG can produce noise or delta function 4-bit or 8-bit samples
5. Switch to select FORM, VSI or TPG data input
6. Produces noise diode switching waveform to accompany downstream data
7. State counters for monitoring purposes (measures 16 states per bus per interrupt)

5.3.1 INP GUI Description

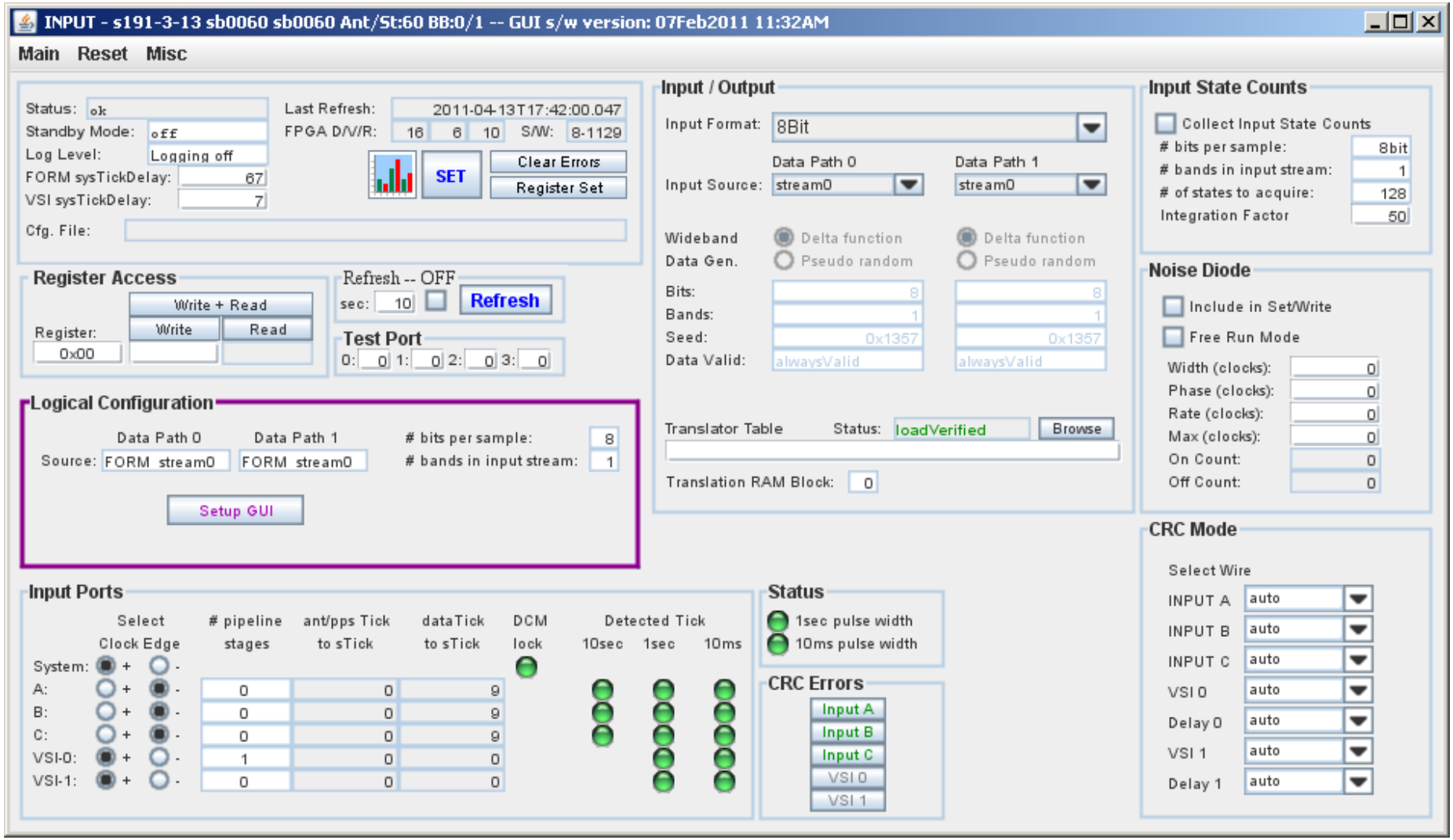


Figure 5-2 Input FPGA GUI

5.4 Delay Module Functions

5.4.1 DLY GUI Description

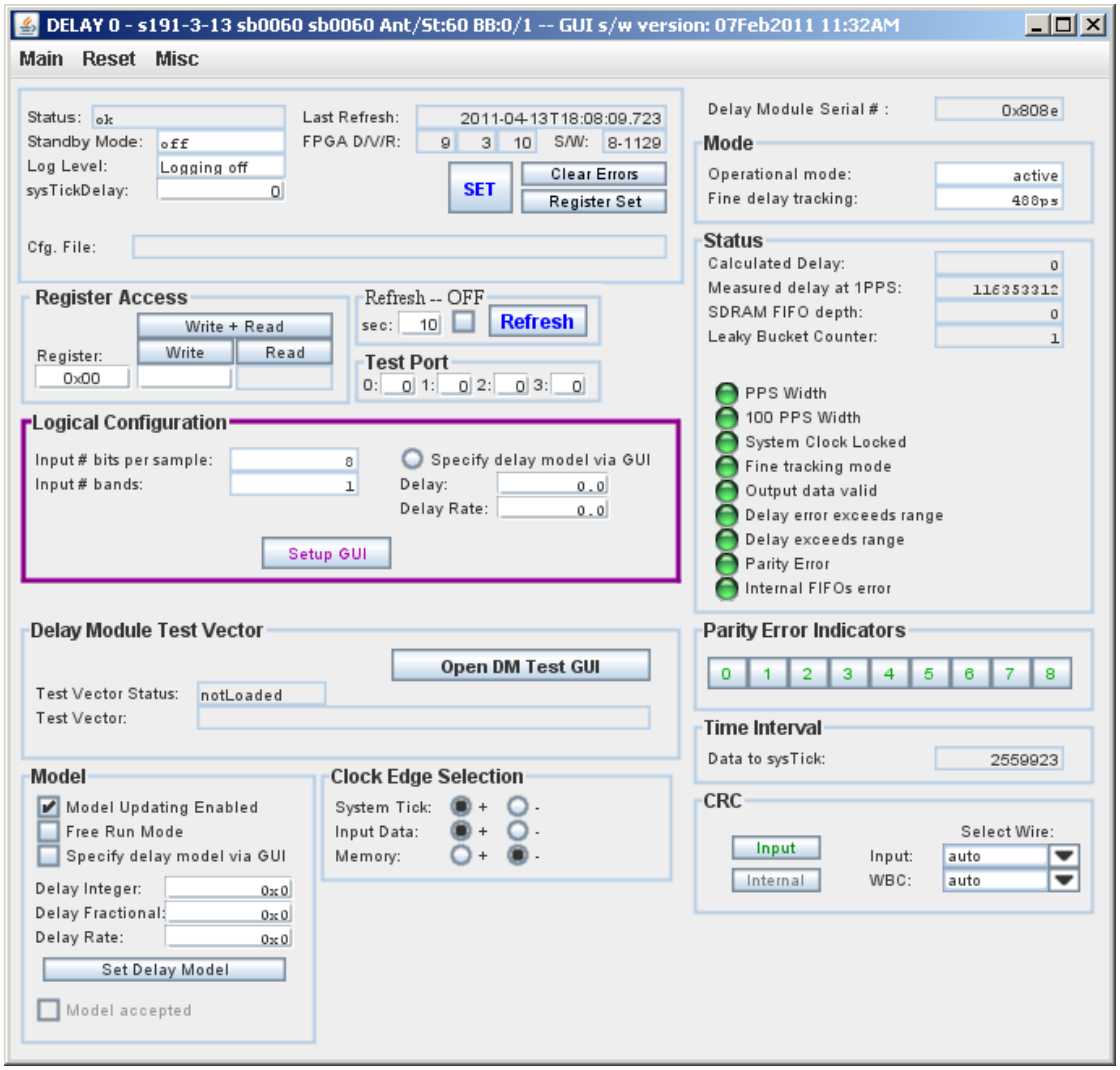


Figure 5-3 Delay Module GUI

5.5 Wide Band Correlator FPGA Functions

5.5.1 WBC GUI Description

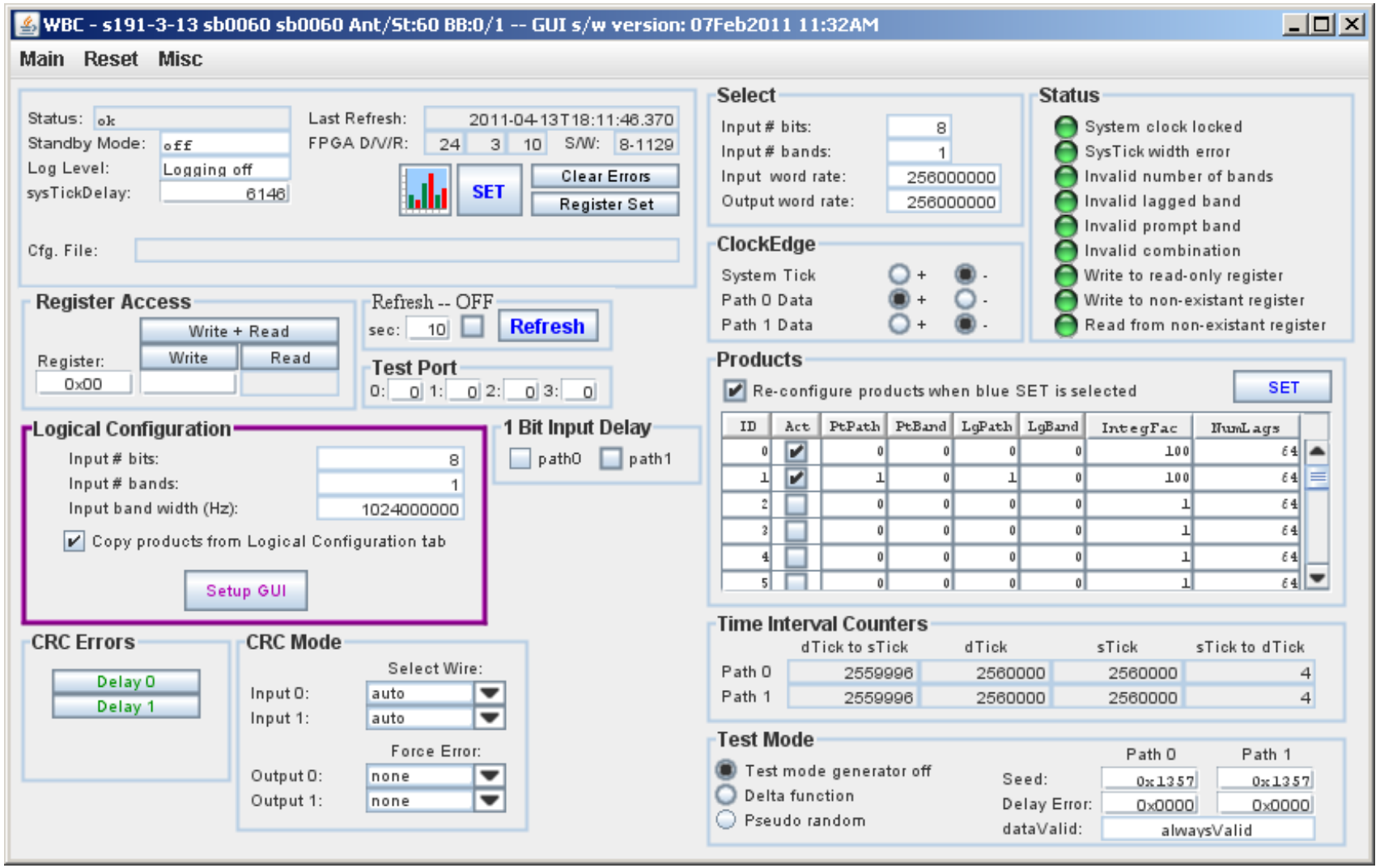


Figure 5-4 Wide Band Correlator FPGA GUI

5.6 Filter FPGA Functions

5.6.1 FIR GUI Description

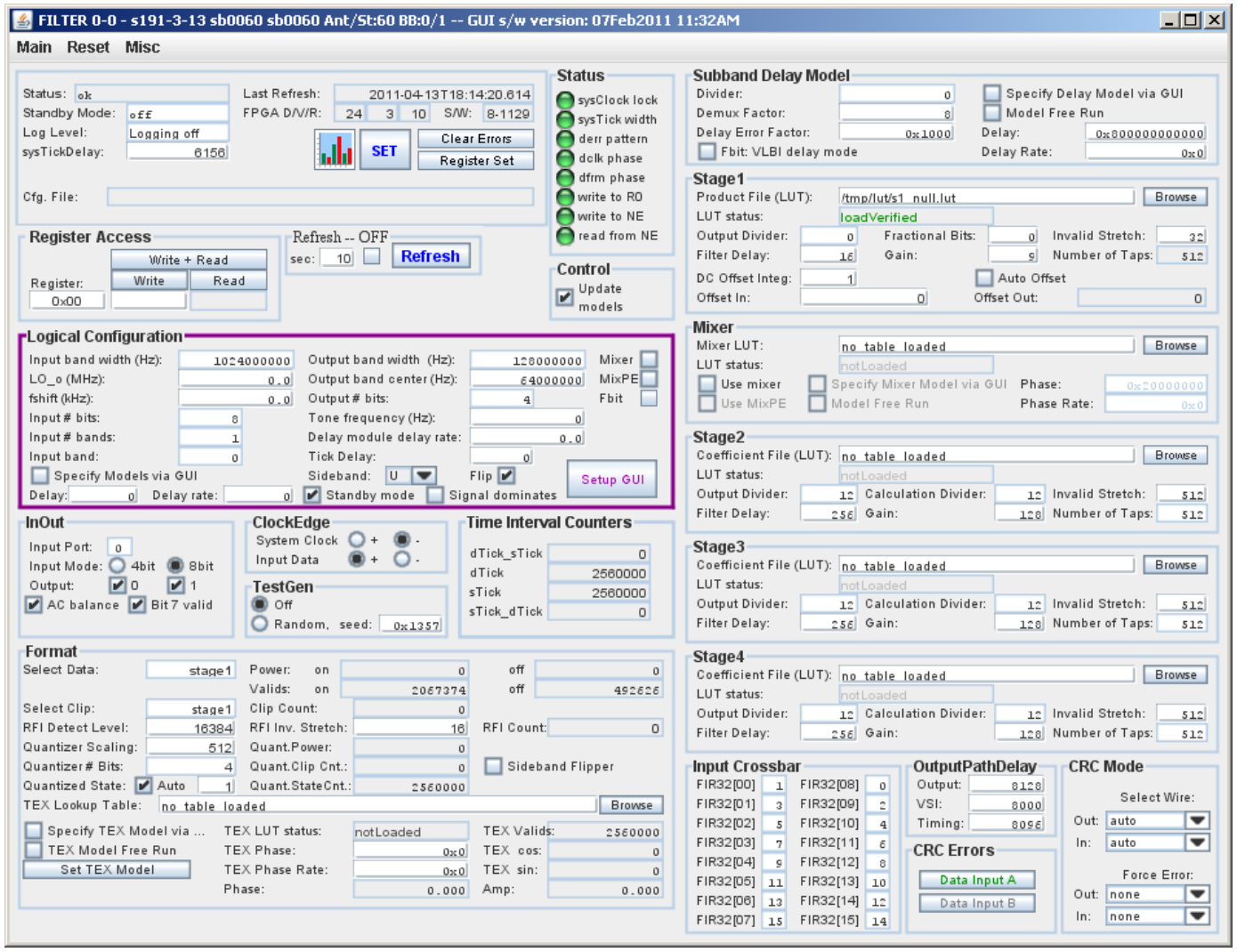
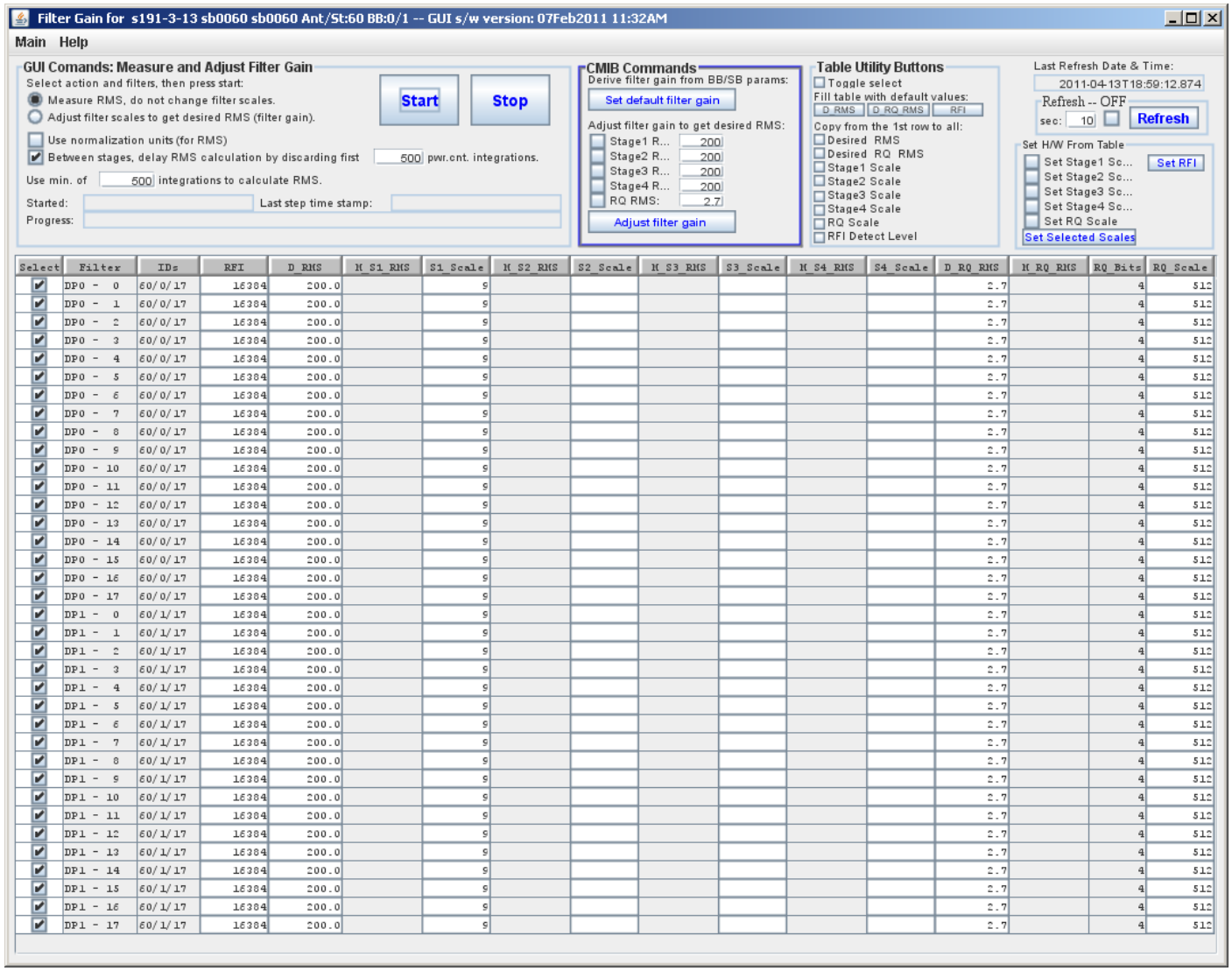


Figure 5-5 Filter FPGA GUI



Select	Filter	IDs	RFI	D_RMS	M_S1_RMS	S1_Scale	M_S2_RMS	S2_Scale	M_S3_RMS	S3_Scale	M_S4_RMS	S4_Scale	D_RQ_RMS	M_RQ_RMS	RQ_Bits	RQ_Scale
☑	DP0 - 0	60/0/17	16384	200.0		9							2.7		4	512
☑	DP0 - 1	60/0/17	16384	200.0		9							2.7		4	512
☑	DP0 - 2	60/0/17	16384	200.0		9							2.7		4	512
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☑	DP1 - 7	60/1/17	16384	200.0		9							2.7		4	512
☑	DP1 - 8	60/1/17	16384	200.0		9							2.7		4	512
☑	DP1 - 9	60/1/17	16384	200.0		9							2.7		4	512
☑	DP1 - 10	60/1/17	16384	200.0		9							2.7		4	512
☑	DP1 - 11	60/1/17	16384	200.0		9							2.7		4	512
☑	DP1 - 12	60/1/17	16384	200.0		9							2.7		4	512
☑	DP1 - 13	60/1/17	16384	200.0		9							2.7		4	512
☑	DP1 - 14	60/1/17	16384	200.0		9							2.7		4	512
☑	DP1 - 15	60/1/17	16384	200.0		9							2.7		4	512
☑	DP1 - 16	60/1/17	16384	200.0		9							2.7		4	512
☑	DP1 - 17	60/1/17	16384	200.0		9							2.7		4	512

Figure 5-5A Filter Gain GUI

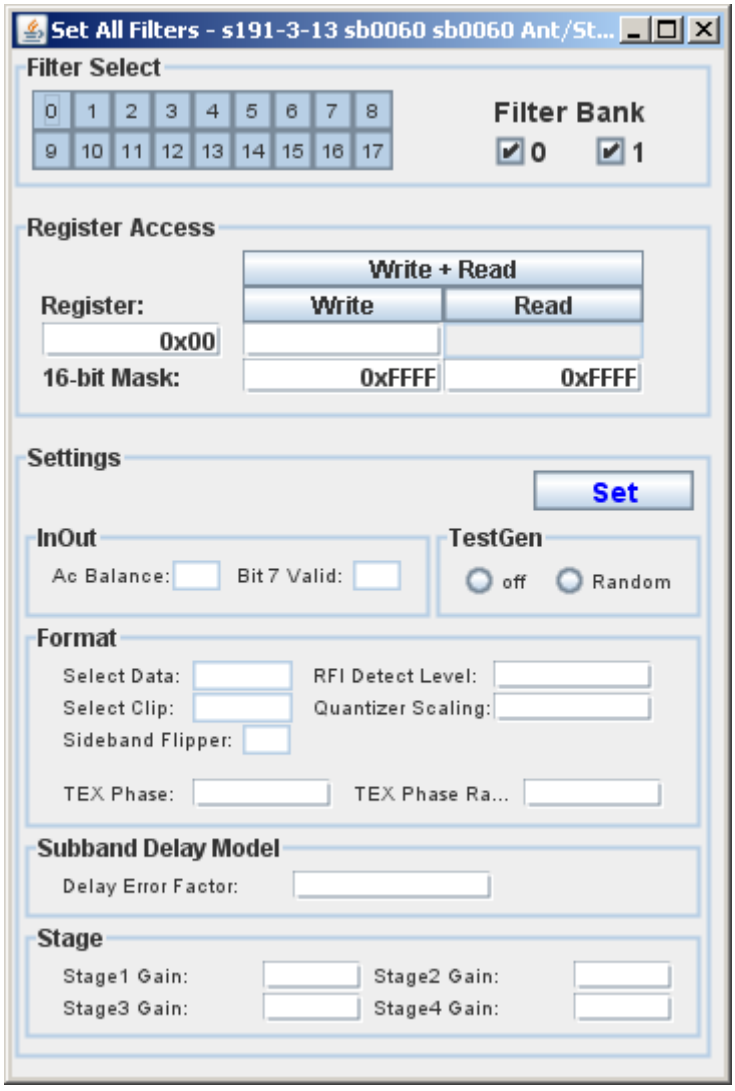

Figure 5-5B Filter Setup GUI

5.7 Output FPGA Functions

5.7.1 OUT GUI Description

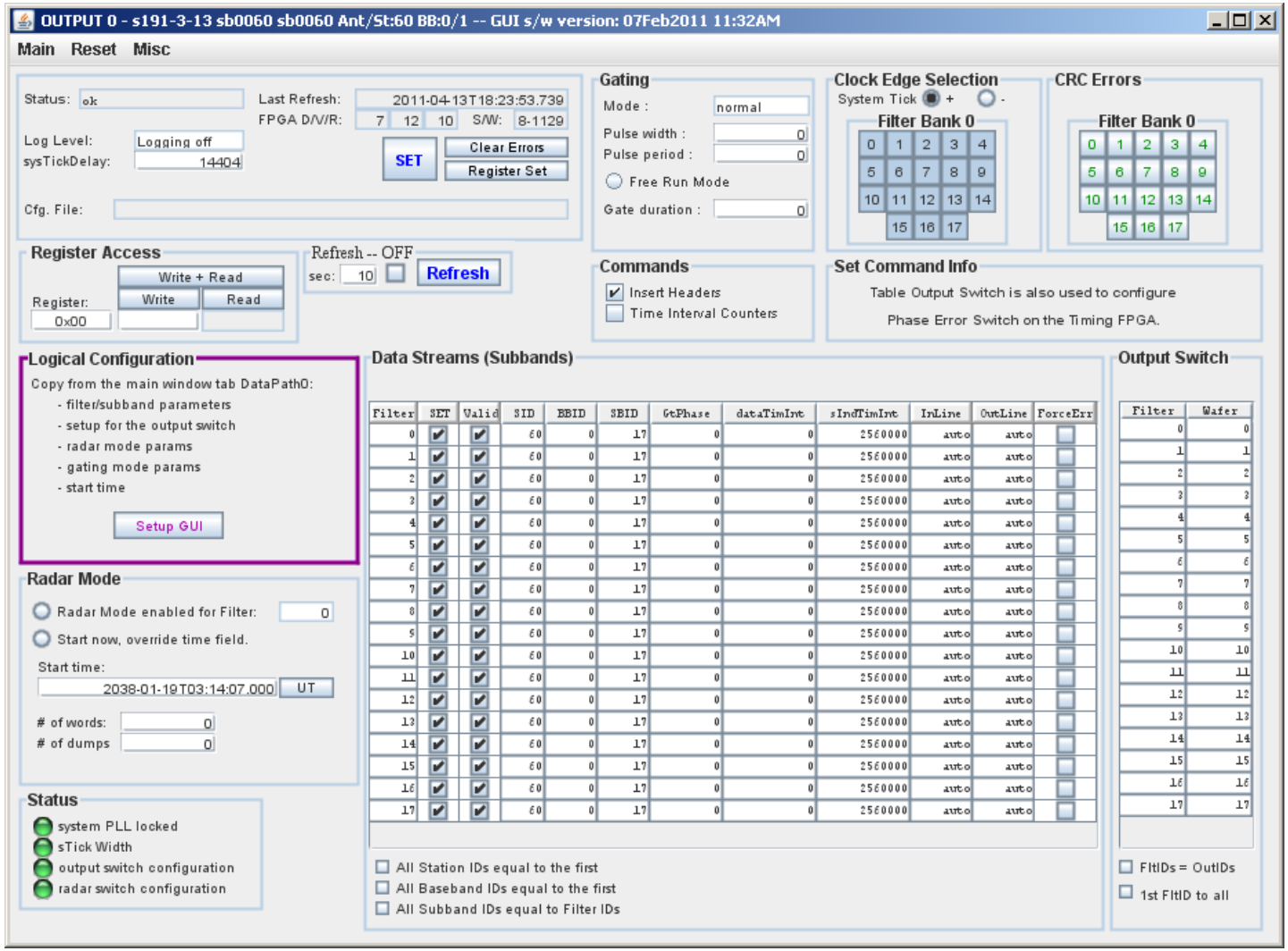

Figure 5-6 Output FPGA GUI

5.8 Timing FPGA Functions

5.8.1 TIM GUI Description

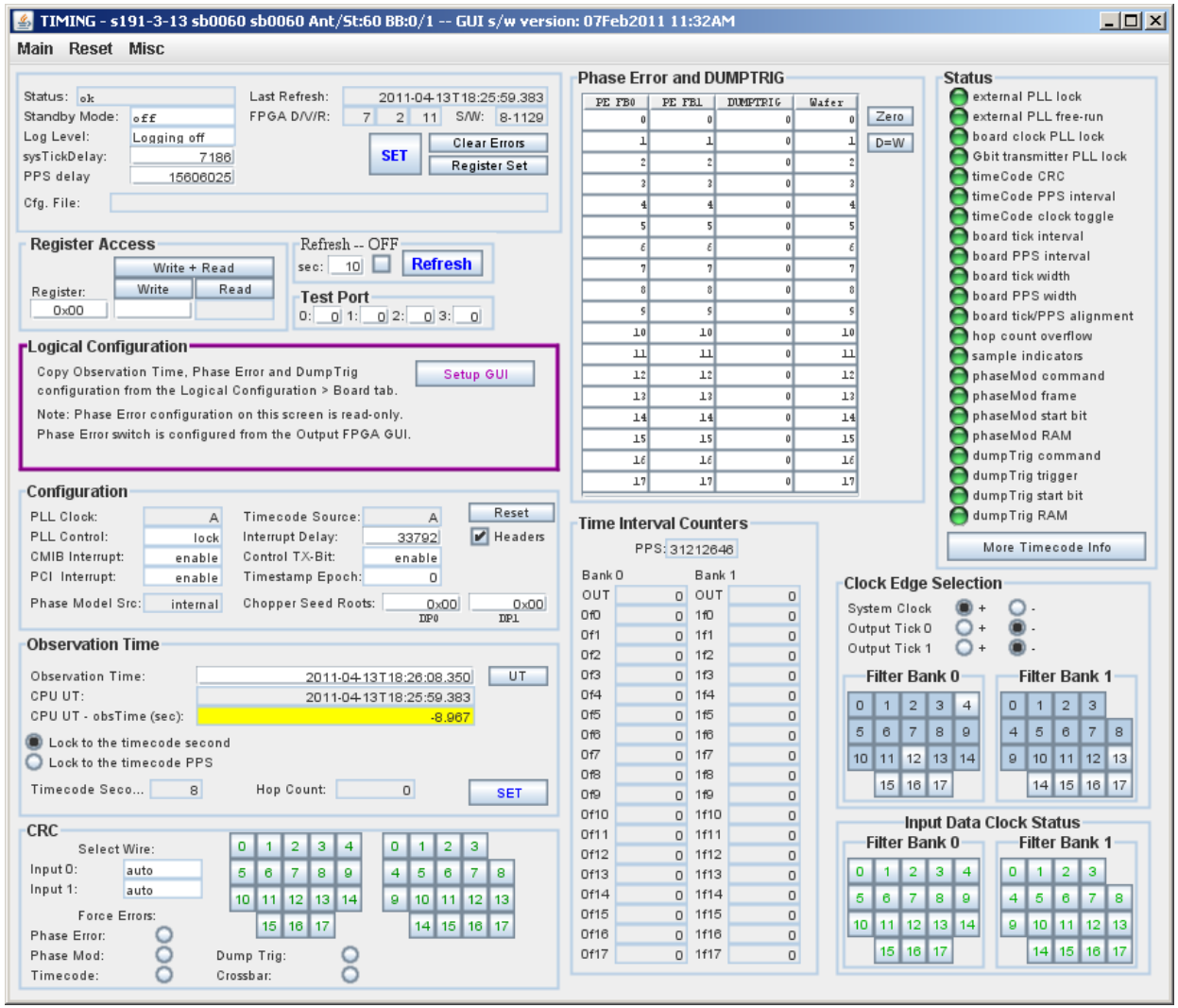

Figure 5-7 Timing FPGA GUI

5.9 Configuration FPGA Functions

5.9.1 CFG GUI Description

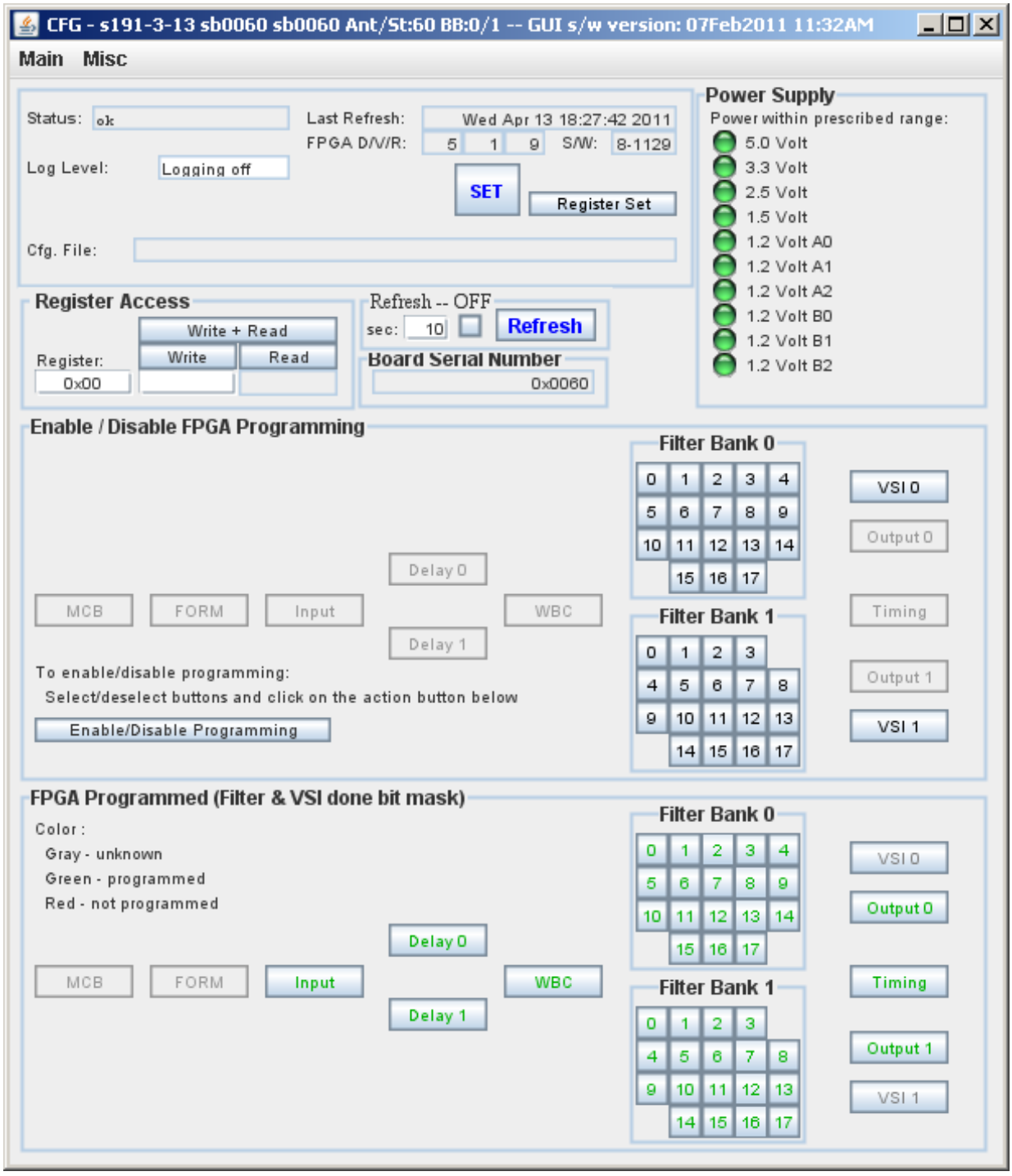

Figure 5-8 Configuration FPGA GUI

5.10 MCB FPGA Functions

5.10.1 MCB GUI Description

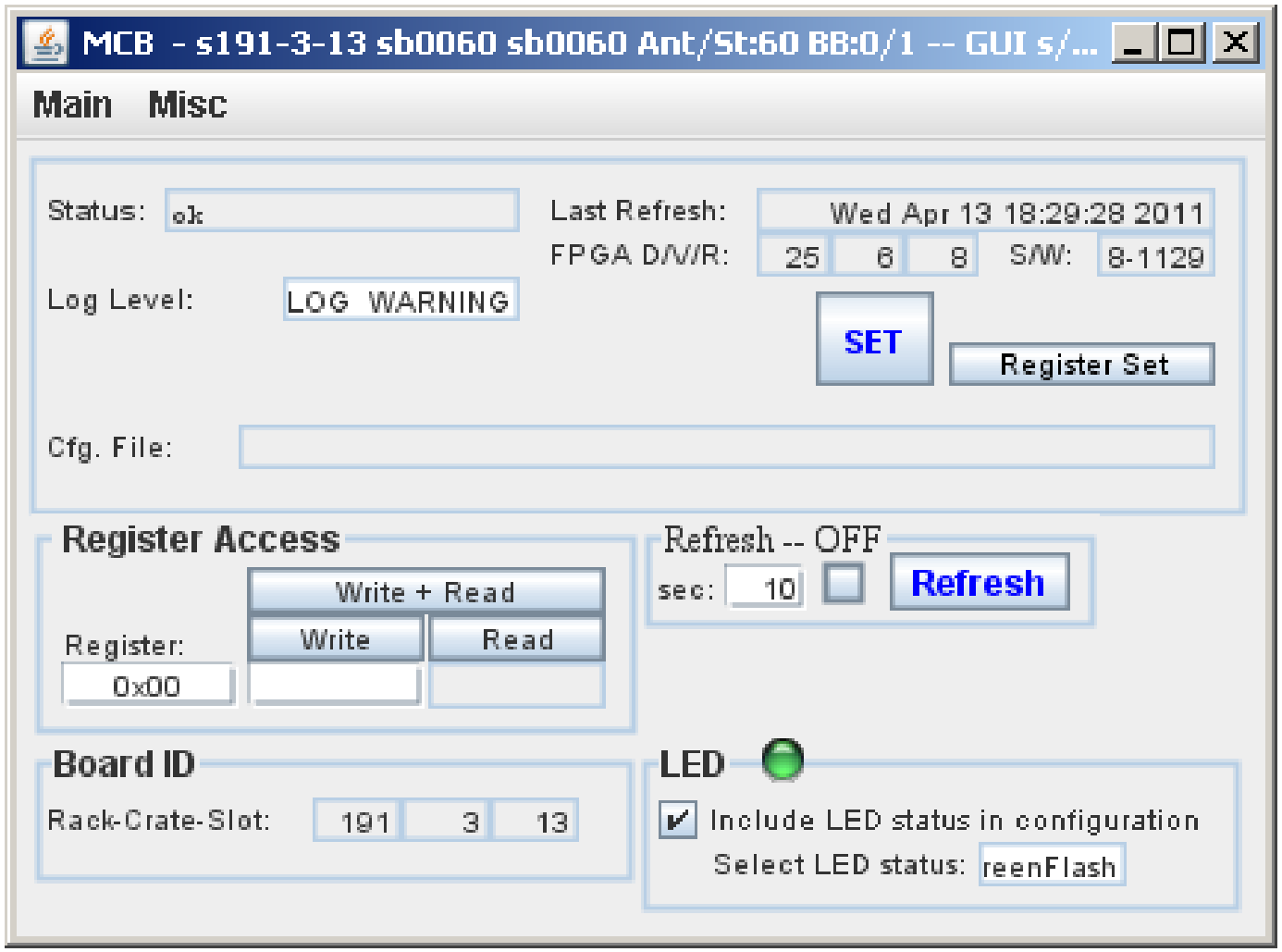

Figure 5-9 MCB FPGA GUI

5.11 Voltage and Temperature Monitoring Functions

5.11.1 Voltage and Temperature GUI Description

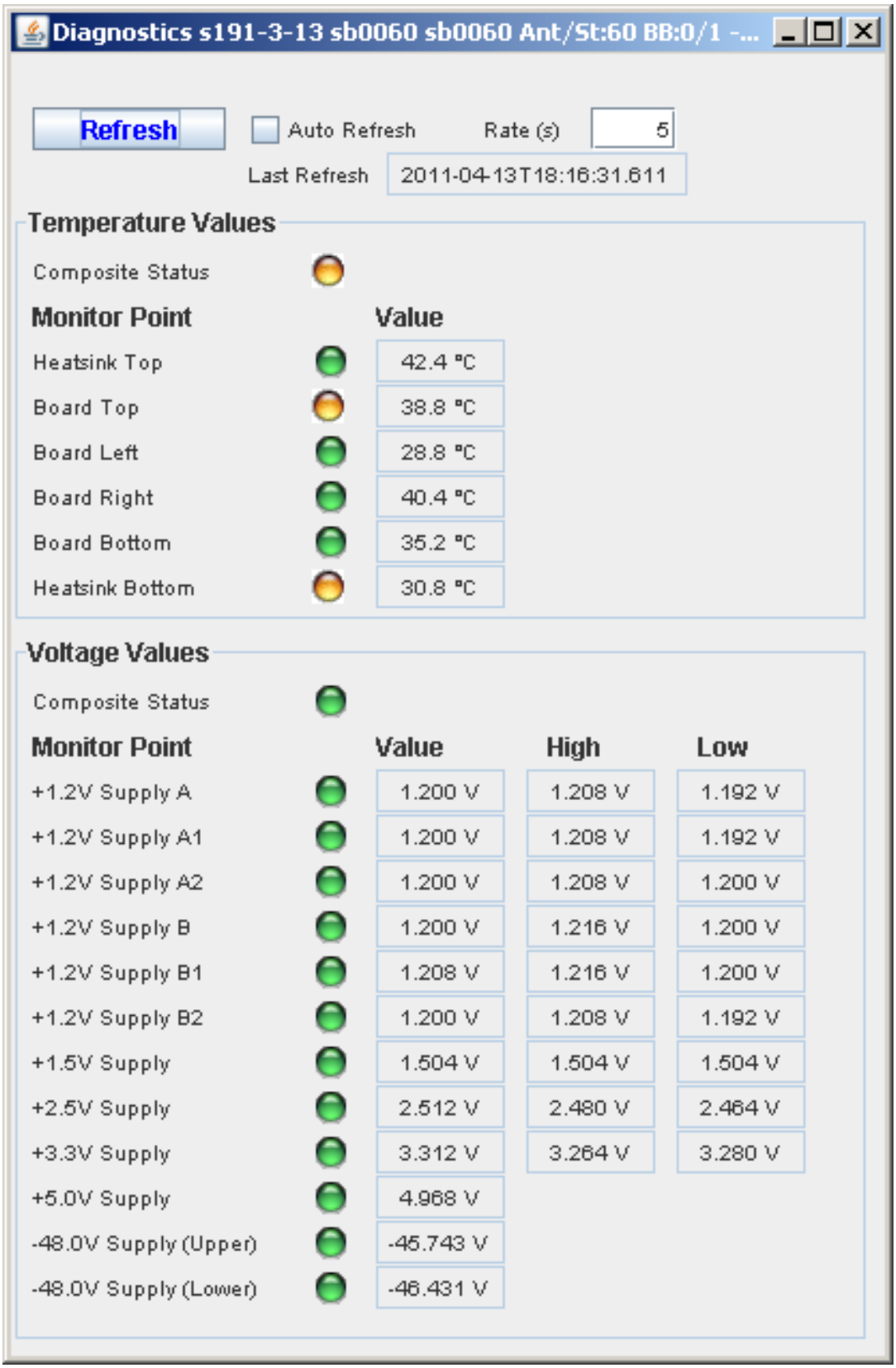

Figure 5-10 Voltage and Temperature GUI

5.12 Dead-Man Thermal Overload Protection

There are two in-series, normally-closed, thermostat/switches on the board, fastened to the heat sink with a hard-set trip temperature of 65 C. These TO-220 packages are located in the upper-left corner of the heat sink. If either one of them, or any wiring in-series with the trip signal path, goes open-circuit, it inhibits the power supplies on the board, preventing thermal run-away and possible destruction of the board.

5.13 -48 VDC Power, M&C, Transient Protection and EMI Filtering

-48 VDC is the mains power supply for the board, and it must be within the range of -36 VDC to -58 VDC. The maximum total current requirement is ~11 A (at -48 V). DC enters the board via the two power ("PWR") connectors (**Error! Reference source not found.**). Each PWR connector contains 3 contacts, 48VDC Return ("**48VR**") (i.e. power supply ground, isolated from signal ground), -48 VDC Hot ("**48V**"), and an opto-coupler-isolated TTL monitor (M) or control (C) line, referenced to signal and chassis ground with assignment to the connectors as shown in **Error! Reference source not found.**.

Each PWR connector 48V and 48VR line is independent, meaning they are not connected to each other on the PCB. Each 48V line has -60 WVDC, 1500 W surface-mount transorbs, with 10 A crow-bar solder-in fuse protection, to provide transient voltage suppression. Additionally, all of the ¼-brick Artesyn/Emmerson "LQS" power supplies are capable of withstanding 100 V transients, and so the power supplies on the board are well protected.

The 48VR and 48V lines are completely isolated from signal/chassis ground on the board. A typical application will tie 48VR to earth ground at the central power supply distribution panel.

Each 48V supply input has integral EMI filtering using PICOR common-mode filters, and this filtering achieves very close to FCC Part 15 Class B conducted EMI levels, except for the switching power supply fundamental frequency of ~480 kHz, which is slightly above the level. This filtering is provided to minimize the effect of conducted common-mode power supply noise coupling into board-to-board non-isolated communications lines, rather than strictly having to meet an agency specification (i.e. HM Gbps LVDS pairs).

Each DC power supply on the board has its own 47 µF, 80 V electrolytic capacitor for line-side decoupling. The chips on the board require no special power-supply sequencing.

There is a fault in the design, in that there is no in-rush current protection for the DC supply; the many 47 µF decoupling capacitors are instantaneously charged when DC is applied. Thus, it is recommended that the board be plugged into mating power connectors without DC present to avoid inrush currents and arcing on the power connector contacts. Even if the board is occasionally plugged into hot DC, no serious damage to the connector results.

5.14 Front-Panel Power Supply LEDs

The front-panel power supply indicator LEDs are driven by active window comparators, powered by the single +3.3 V supply. Thus, if a particular power supply LED is dark, it indicates the voltage is out of range, either too high, or too low, and not necessarily that the power supply is dead (although this is normally the case). The front-panel "POWER" LED is the combination of all of these window comparators and will be dark if any power supply LED is dark.

5.15 Front Panel USB Port

The CMIB CPU (PC/104+) USB port is broken out via a cable to a front-panel USB connector. This function is for future considerations, and is not normally used. The cable shield is only grounded at the front-panel side, but not the CPU side, and there is some evidence that this generates noise on the USB lines causing unnecessary CPU interrupts to occur. It would seem that this problem can be mitigated by plugging a USB memory stick into the connector. The USB connector on the CPU side is very small and fragile, and so there may be problems with using this interface in practise. Refer to the PC/104+ CPU manufacturer's board User Manual for more information on this and other ports which may be available. Normally, the only CPU port that is used in practise is the 100Base-T port.

6 Interfaces

This section describes details of all physical interfaces to the Station Board.

J1	PCMC	J13	DMA Input
J2	FORM	J14	DMA Output
J3	FORM	J15	Data
J4	Upper Power	J16	Lower Power
J5	FORM	J17	DMB Input
J6	Upper VSI	J18	DMB Output
J7	FORM	J19	Lower VSI
J8	Upper VSI	J20	Lower VSI
J9	Data	J21	Soft Touch Header
J10	Data	J22	Soft Touch Header
J11	JTAG PROM	J23	128 MHz Coaxial
J12	JTAG TEST		

Table 6-1 Connector Summary

6.1 Power

There are two power connectors (“PWR (M)” and “PWR(C)”, **Error! Reference source not found.**). Both are used to deliver the -48 VDC mains power supply to the board (separately, their -48 V hot and return lines are not connected on the board, but power must be supplied to both connectors for the board to function).

The PWR (M) connector uses 1 pin as the signal/chassis-referenced GND TTL *monitor* line. If the line is high, it indicates that all power supplies on the board are operating and within range.

The PWR (C) connector uses 1 pin as the signal/chassis-referenced GND TTL *control* line. If this line is pulled high, it enables all the power supplies on the board, if pulled low, all power supplies are disabled.

Both the (M) and (C) lines are completely electrically isolated from the -48 V hot and return lines.

A picture looking into the connector, with signal assignments is shown below.

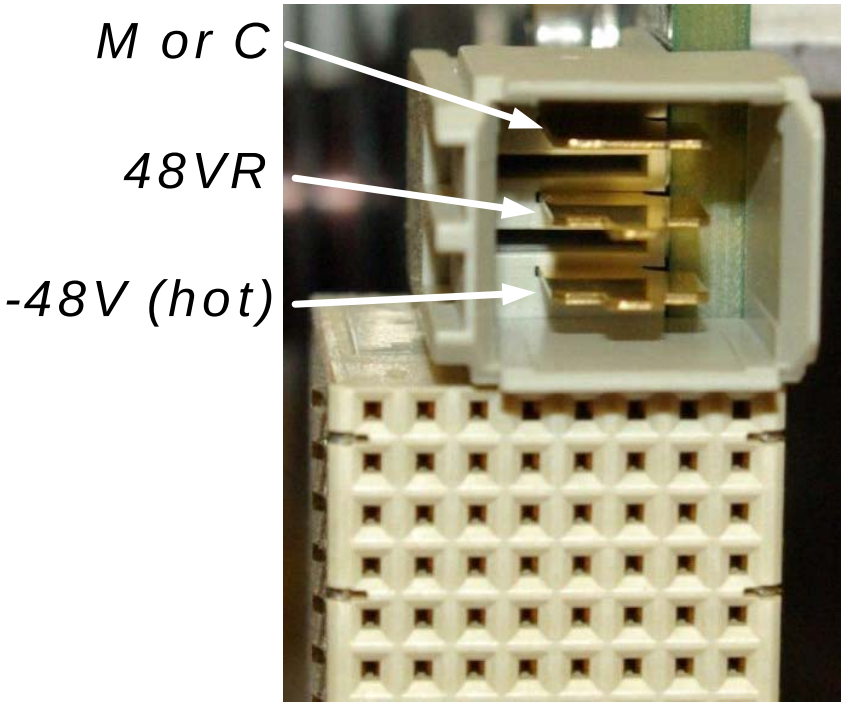

Figure 6-1 Power Connector

6.1.1 Upper Power Connector – J4

Pin	A	B	C
1	-48V_UP	-48V_RET_UP	pw_ctr
2	-48V_UP	-48V_RET_UP	pw_ctr
3	-48V_UP	-48V_RET_UP	pw_ctr
4	-48V_UP	-48V_RET_UP	pw_ctr

Signal –48V_UP is –48V.

Signal –48V_RET_UP is 0V.

Signal pw_ctr is LVTTL input.

Table 6-2 Upper Power Connector J4

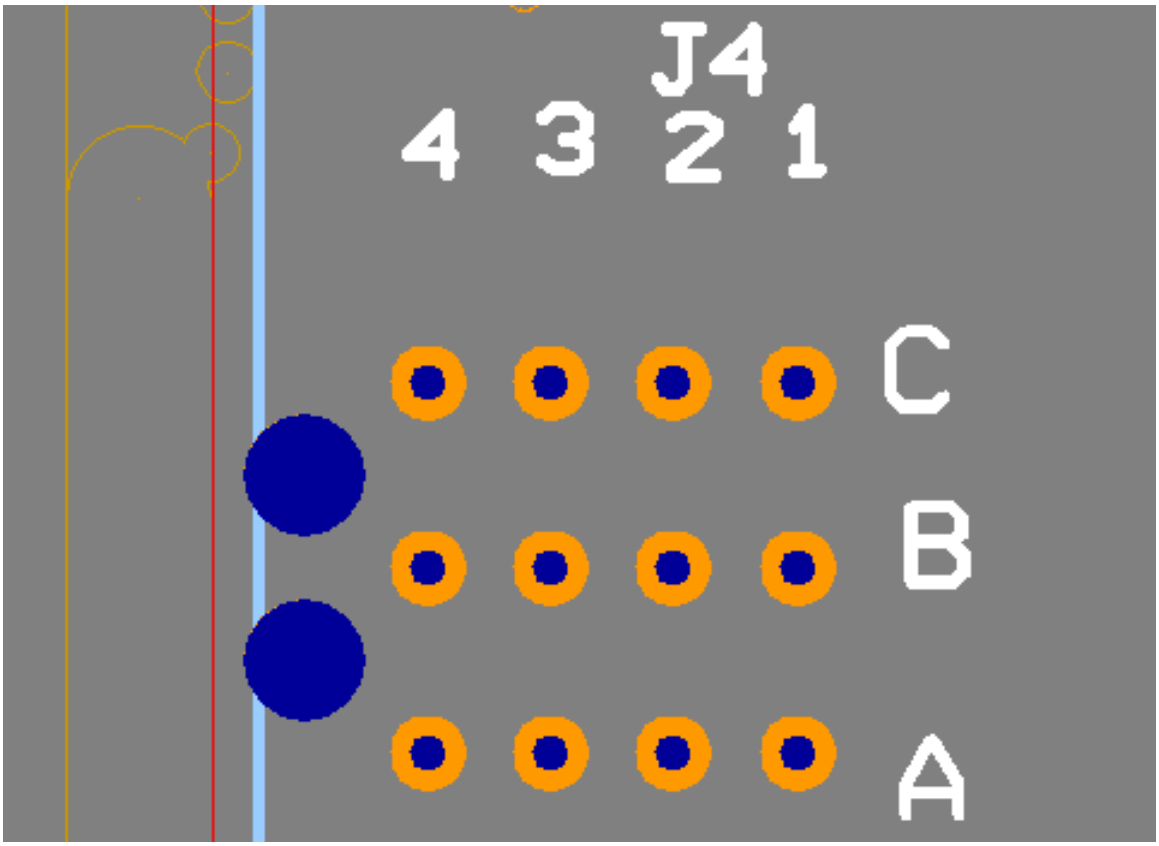

Figure 6-2 Upper Power Connector J4

6.1.2 Lower Power Connector – J16

Pin	A	B	C
1	-48V_LOW	-48V_RET_LOW	power_monitor
2	-48V_LOW	-48V_RET_LOW	power_monitor
3	-48V_LOW	-48V_RET_LOW	power_monitor
4	-48V_LOW	-48V_RET_LOW	power_monitor

Signal –48V_LOW is –48V.

Signal –48V_RET_LOW is 0V.

Signal power_monitor is LVTTL input.

Table 6-3 Lower Power Connector J16

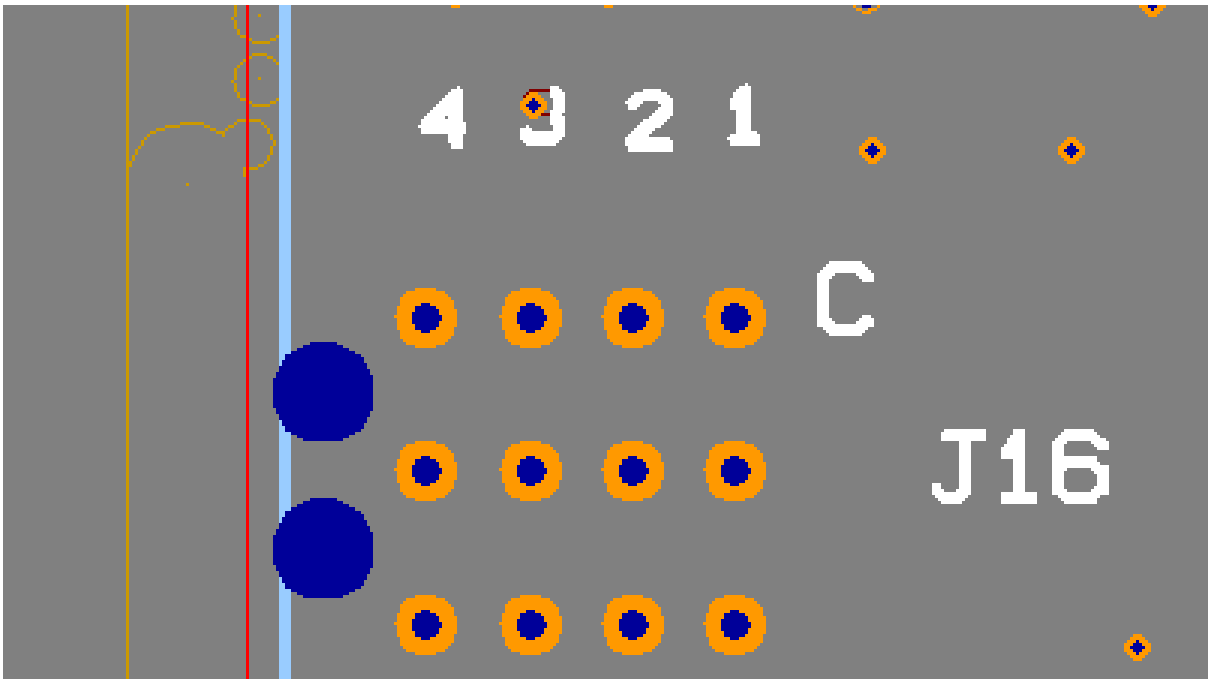

Figure 6-3 Lower Power Connector J16

6.2 Front Panel "JTAG CMIB ROM", J11

This 14-pin 2 mm male connector is the gateway used to program the PCMC FPGA EEPROM. Normally programming of the EEPROM must only be done once, as it can thereafter be programmed by the PC/104+ CPU module via the PCMC FPGA, unless it gets corrupted. The connector is a JTAG programming interface, and the EEPROM must be programmed using the Xilinx ISE software using JTAG, and a cable pod such as the Xilinx "Platform Cable USB II".

Pin #	Pin name	Description
1, 3, 5, 7, 9, 11, 13	GND	Signal Ground
2	+3.3 V	Connected to the +3.3 V power supply rail.
4	TMS	Test Mode Select input to the board.
6	TCK	Test Clock input to the board
8	TDO	Test Data output from the board
10	TDI	Test Data Input to the board
12, 14	N/C	No connection

Table 6-4 Front panel "JTAG CMIB ROM" J5 connector pinouts.

6.3 Front Panel "JTAG BOARD TEST" J12

This connector is used for pre-final assembly JTAG manufacturing test of the board. Connector pinouts are identical to Table 6-3, except pin 2 is connected to the +2.5V power supply rail.

6.4 Rear External Clock SMA Connector J23

This is a right-angle female SMA connector located pointing towards the rear of the board. It is for connection to an external 128 MHz input (-3 to +9 dBm), AC-coupled, and 50-ohm terminated on the board. It routes through a buffer to the TIMING FPGA and may be selected as the StB reference for testing or actual operation if coherent with the TIMECODE A and B signals.

6.5 JTAG Chain

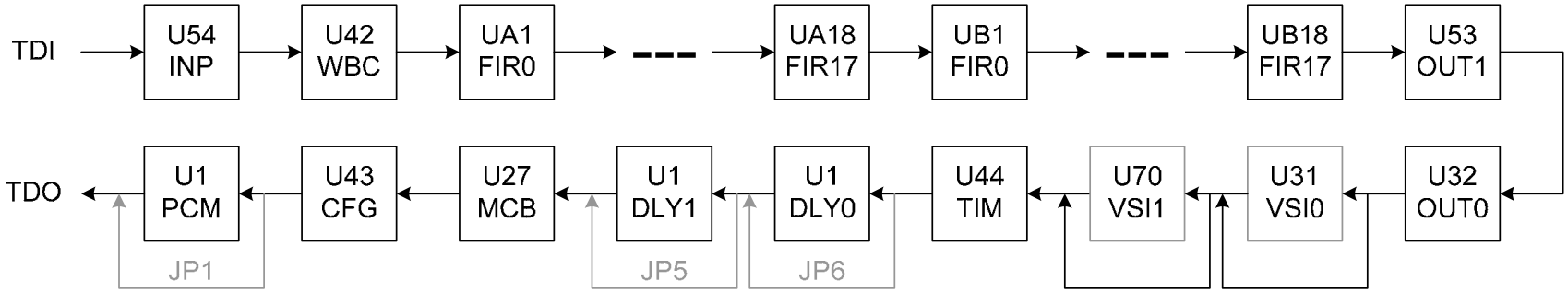

Figure 6-4 JTAG Chain

The JTAG test that is available includes PCM, DLY0 and DLY1 but does not include VSI0 or VSI1.

6.6 PCMC, J1

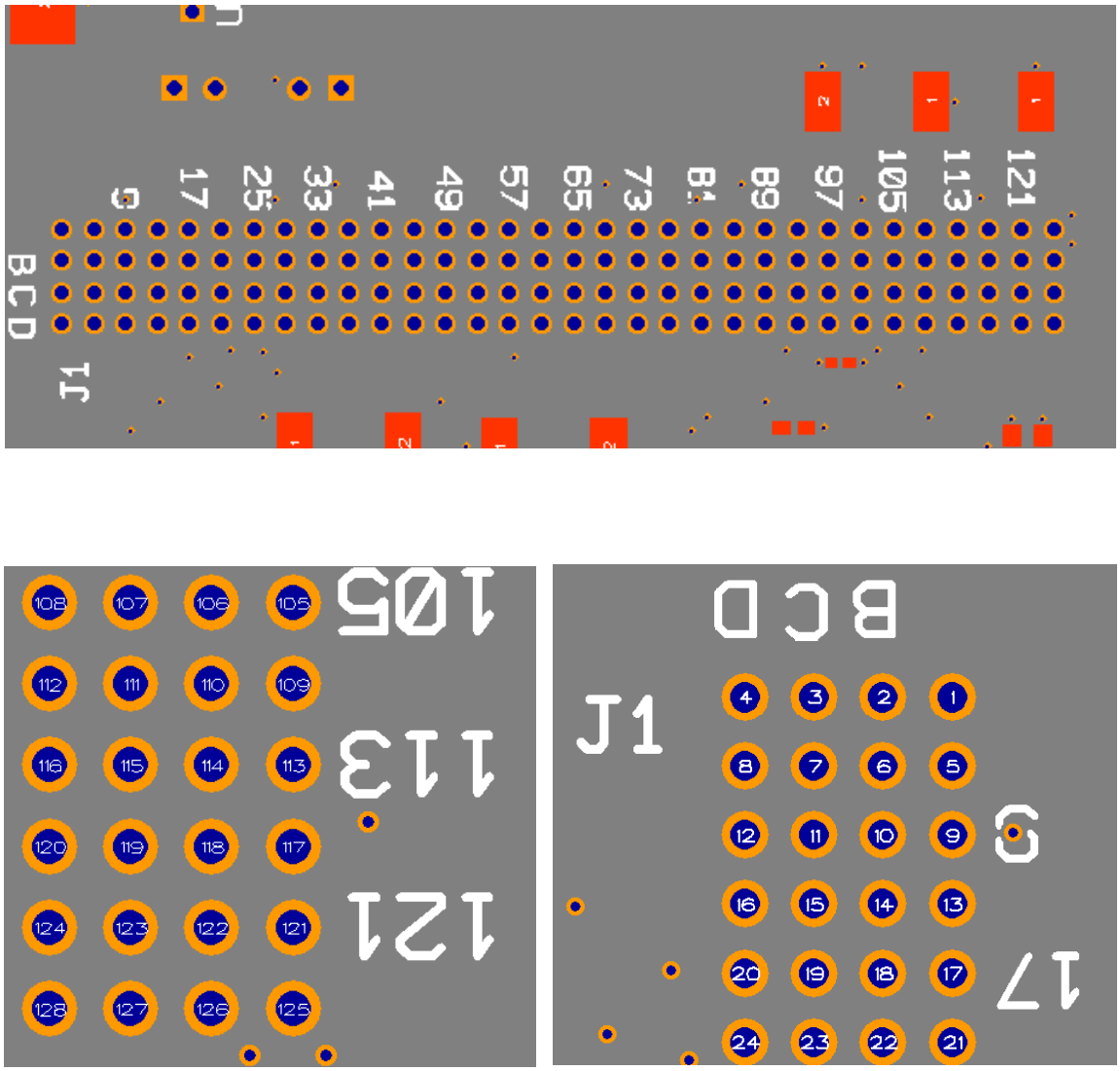

Figure 6-5 PCMC Connector J1

Pin	Name	Direction	Standard
1	GND		Ground
2	GND		Ground
3	GND		Ground
4	GND		Ground
5	GND		Ground
6	5.0V		Power
7	3.3V		Power
8	GND		Ground
9	V/T[0]	In	Analog
10	AMUX_OUT	In	Analog
11	V/T[2]	In	Analog
12	V/T[3]	In	Analog
13	PCM_1V2A	In	Analog
14	PCM_1V2B	In	Analog
15	PCM_1V5	In	Analog
16	PCM_3V3	In	Analog
17	PCM_1V2A1	In	Analog
18	PCM_1V2B1	In	Analog
19	PCM_2V5	In	Analog
20	PCM_5V0	In	Analog
21	GND		Ground
22	1.5V		Power
23	5.0V		Power
24	GND		Ground
25	TCK_PROM	In	LVTTL
26	TMS_PROM	In	LVTTL
27	TDI_PROM	In	LVTTL
28	TDO_PROM	Out	LVTTL
29	TCK_Test	In	LVTTL
30	TMS_Test	In	LVTTL
31	TDO_CFGP	Out	LVTTL
32	TDO_Test	Out	LVTTL

33	PCMC_Status[0]	Out	LVTTL
34	PCMC_Status[1]	Out	LVTTL
35	RESET_PCM	Out	LVTTL
36	GND		Ground
37	nPCMC_PROG	In	Analog
38	CBUS_EN	Out	LVTTL
39	GND		Ground
40	CCLK	Out	LVTTL
41	CDATA[0]	Out	LVTTL
42	CDATA[1]	Out	LVTTL
43	CDATA[2]	Out	LVTTL
44	CDATA[3]	Out	LVTTL
45	CDATA[4]	Out	LVTTL
46	CDATA[5]	Out	LVTTL
47	CDATA[6]	Out	LVTTL
48	CDATA[7]	Out	LVTTL
49	GND		Ground
50	5.0V		Power
51	GND		Ground
52	GND		Ground
53	nPROG[0]	Out	LVTTL
54	DONE[0]	In	LVTTL
55	nPROG[1]	Out	LVTTL
56	DONE[1]	In	LVTTL
57	nPROG[2]	Out	LVTTL
58	DONE[2]	In	LVTTL
59	nPROG[3]	Out	LVTTL
60	DONE[3]	In	LVTTL
61	nPROG[4]	Out	LVTTL
62	DONE[4]	In	LVTTL
63	nPROG[5]	Out	LVTTL
64	DONE[5]	In	LVTTL
65	nPROG[6]	Out	LVTTL
66	DONE[6]	In	LVTTL
67	nPROG[7]	Out	LVTTL

68	DONE[7]	In	LVTTL
69	nPROG[8]	Out	LVTTL
70	DONE[8]	In	LVTTL
71	nPROG[9]	Out	LVTTL
72	DONE[9]	In	LVTTL
73	nPROG[10]	Out	LVTTL
74	DONE[10]	In	LVTTL
75	nPROG[11]	Out	LVTTL
76	DONE[11]	In	LVTTL
77	GND		Ground
78	3.3V		Power
79	1.5V		Power
80	GND		Ground
81	MCB_Addr[0]	Out	LVTTL
82	MCB_Addr[1]	Out	LVTTL
83	MCB_Addr[2]	Out	LVTTL
84	MCB_Addr[3]	Out	LVTTL
85	MCB_Addr[4]	Out	LVTTL
86	MCB_Addr[5]	Out	LVTTL
87	MCB_Addr[6]	Out	LVTTL
88	MCB_Addr[7]	Out	LVTTL
89	MCB_Addr[8]	Out	LVTTL
90	MCB_Addr[9]	Out	LVTTL
91	MCB_Addr[10]	Out	LVTTL
92	MCB_Addr[11]	Out	LVTTL
93	MCB_Addr[12]	Out	LVTTL
94	MCB_Addr[13]	Out	LVTTL
95	MCB_Addr[14]	Out	LVTTL
96	MCB_Addr[15]	Out	LVTTL
97	nMCB_BS	Out	LVTTL
98	MCB_RD/nWR	Out	LVTTL
99	MCB_CLK	Out	LVTTL
100	MCB_INT	In	LVTTL
101	GND		Ground
102	5.0V		Power

103	GND		Ground
104	GND		Ground
105	MCB_Data[0]	In/Out	LVTTL
106	MCB_Data[1]	In/Out	LVTTL
107	MCB_Data[2]	In/Out	LVTTL
108	MCB_Data[3]	In/Out	LVTTL
109	MCB_Data[4]	In/Out	LVTTL
110	MCB_Data[5]	In/Out	LVTTL
111	MCB_Data[6]	In/Out	LVTTL
112	MCB_Data[7]	In/Out	LVTTL
113	MCB_Data[8]	In/Out	LVTTL
114	MCB_Data[9]	In/Out	LVTTL
115	MCB_Data[10]	In/Out	LVTTL
116	MCB_Data[11]	In/Out	LVTTL
117	MCB_Data[12]	In/Out	LVTTL
118	MCB_Data[13]	In/Out	LVTTL
119	MCB_Data[14]	In/Out	LVTTL
120	MCB_Data[15]	In/Out	LVTTL
121	GND		Ground
122	3.3V		Power
123	1.5V		Power
124	GND		Ground
125	3.3V		Power
126	GND		Ground
127	GND		Ground
128	GND		Ground

Table 6-5 PCMC Connector J1

6.7 FORM J2, J3, J5, J7

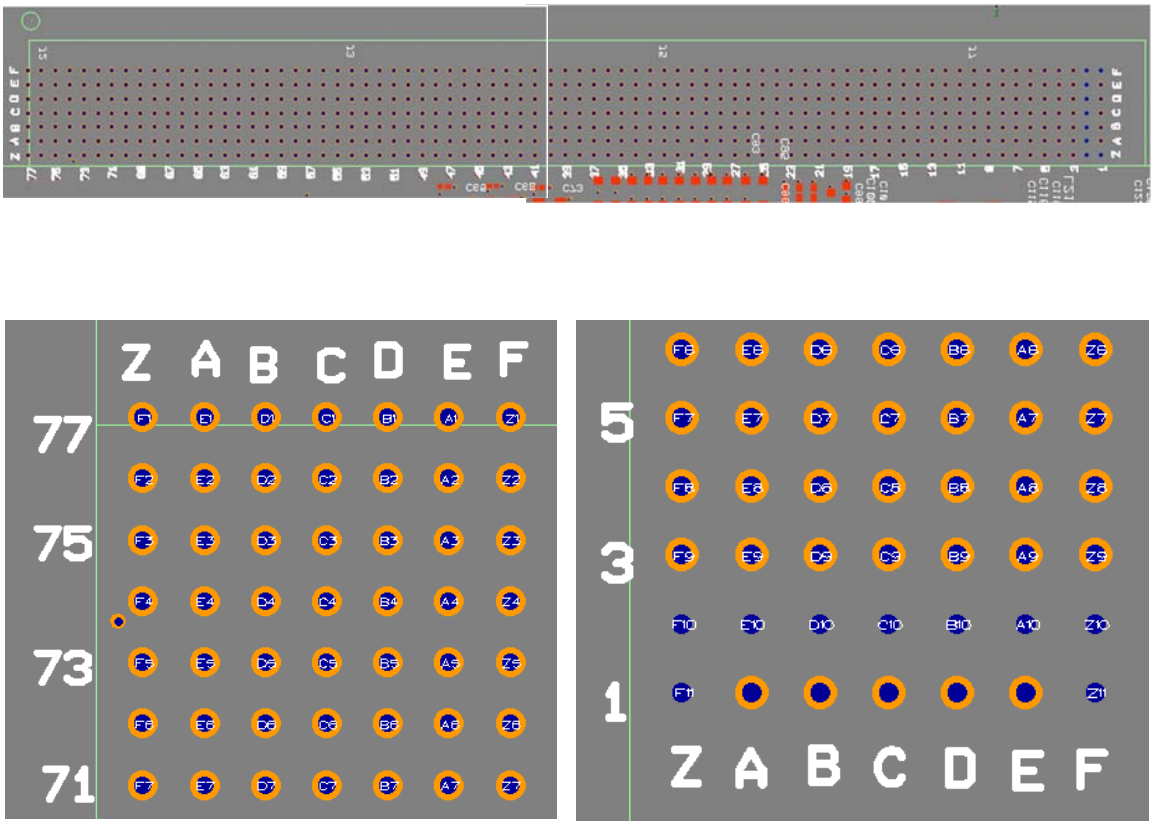

Figure 6-6 FORM Connector J2, J3, J5 and J7.

	A	B	C	D	E
J7					
1	+48V_FCM	+48V_FCM	NC	-48V_FCM	-48V_FCM
2	NC	NC	NC	NC	NC
3	NC	GND	GND	GND	GND
4	GND	coreio[15]	GND	coreio[16]	GND
5	fe_lvcmos25[2]	GND	coreio[13]	GND	coreio[14]
6	GND	coreio[11]	GND	coreio[12]	GND
7	fe_lvcmos25[1]	GND	coreio[9]	GND	coreio[10]
8	GND	coreio[7]	GND	coreio[8]	GND
9	fe_lvcmos25[0]	GND	coreio[5]	GND	coreio[6]
10	GND	coreio[3]	GND	coreio[4]	GND
11	coreio[0]	GND	coreio[1]	GND	coreio[2]
J5					
12	GND	fe_hstl[2]	GND	fe_hstl[6]	GND
13	fe_hstl[0]	GND	fe_hstl[4]	GND	fe_hstl[8]
14	GND	fe_hstl[3]	GND	fe_hstl[7]	GND
15	fe_hstl[1]	GND	fe_hstl[5]	GND	DSPAREA0
16	GND	DATA_A[0]	GND	DATA_A[1]	GND
17	DATA_A[2]	GND	DATA_A[3]	GND	DATA_A[4]
18	GND	DATA_A[5]	GND	DATA_A[6]	GND
19	DATA_A[7]	GND	DATA_A[8]	GND	DATA_A[9]
20	GND	DATA_A[10]	GND	DATA_A[11]	GND
21	DATA_A[12]	GND	DATA_A[13]	GND	RCLOCKA
22	GND	DATA_A[14]	GND	spare_in_a	GND
23	DATA_A[15]	GND	ATIMEA	GND	RTIMEA
24	GND	DATA_A[16]	GND	DTIMEA	GND
25	DATA_A[17]	GND	DATA_A[18]	GND	res_pll_a
26	GND	DATA_A[19	GND	DATA_A[20]	GND
27	DATA_A[21]	GND	DATA_A[22]	GND	DATA_A[23]
28	GND	DATA_A[24]	GND	DATA_A[25]	GND
29	DATA_A[26]	GND	DATA_A[27]	GND	DATA_A[28]
30	GND	DATA_A[29]	GND	DATA_A[30]	GND
31	NC	GND	DVALIDA	GND	DATA_A[31]
32	GND	fe_hstl[10]	GND	fe_hstl[12]	GND

33	fe_hstl[9]	GND	fe_hstl[11]	GND	fe_hstl[13]
J3					
34	GND	fe_hstl[16]	GND	fe_hstl[20]	GND
35	fe_hstl[14]	GND	fe_hstl[18]	GND	fe_hstl[22]
36	GND	fe_hstl[17]	GND	fe_hstl[21]	GND
37	fe_hstl[15]	GND	fe_hstl[19]	GND	DSPAREB0
38	GND	DATA_B[0]	GND	DATA_B[1]	GND
39	DATA_B[2]	GND	DATA_B[3]	GND	DATA_B[4]
40	GND	DATA_B[5]	GND	DATA_B[6]	GND
41	DATA_B[7]	GND	DATA_B[8]	GND	DATA_B[9]
42	GND	DATA_B[10]	GND	DATA_B[11]	GND
43	DATA_B[12]	GND	DATA_B[13]	GND	RCLOCKB
44	GND	DATA_B[14]	GND	spare_in_b	GND
45	DATA_B[15]	GND	ATIMEB	GND	RTIMEB
46	GND	DATA_B[16]	GND	DTIMEB	GND
47	DATA_B[17]	GND	DATA_B[18]	GND	res_pll_b
48	GND	DATA_B[19]	GND	DATA_B[20]	GND
49	DATA_B[21]	GND	DATA_B[22]	GND	DATA_B[23]
50	GND	DATA_B[24]	GND	DATA_B[25]	GND
51	DATA_B[26]	GND	DATA_B[27]	GND	DATA_B[28]
52	GND	DATA_B[29]	GND	DATA_B[30]	GND
53	fe_hstl[23]	GND	DVALIDB	GND	DATA_B[31]
54	GND	fe_hstl[25]	GND	fe_hstl[27]	GND
55	fe_hstl[24]	GND	fe_hstl[26]	GND	fe_hstl[28]
J2					
56	GND	fe_hstl[31]	GND	fe_hstl[35]	GND
57	fe_hstl[29]	GND	fe_hstl[33]	GND	fe_hstl[37]
58	GND	fe_hstl[32]	GND	fe_hstl[36]	GND
59	fe_hstl[30]	GND	fe_hstl[34]	GND	DSPAREC0
60	GND	DATA_C[0]	GND	DATA_C[1]	GND
61	DATA_C[2]	GND	DATA_C[3]	GND	DATA_C[4]
62	GND	DATA_C[5]	GND	DATA_C[6]	GND
63	DATA_C[7]	GND	DATA_C[8]	GND	DATA_C[9]
64	GND	DATA_C[10]	GND	DATA_C[11]	GND
65	DATA_C[12]	GND	DATA_C[13]	GND	RCLOCKC

66	GND	DATA_C[14]	GND	spare_in_c	GND
67	DATA_C[15]	GND	ATIMEC	GND	RTIMEC
68	GND	DATA_C[16]	GND	DTIMEC	GND
69	DATA_C[17]	GND	DATA_C[18]	GND	res_pll_c
70	GND	DATA_C[19]	GND	DATA_C[20]	GND
71	DATA_C[21]	GND	DATA_C[22]	GND	DATA_C[23]
72	GND	DATA_C[24]	GND	DATA_C[25]	GND
73	DATA_C[26]	GND	DATA_C[27]	GND	DATA_C[28]
74	GND	DATA_C[29]	GND	DATA_C[30]	GND
75	fe_hstl[38]	GND	DVALIDC	GND	DATA_C[31]
76	GND	fe_hstl[40]	GND	fe_hstl[42]	GND
77	fe_hstl[39]	GND	fe_hstl[41]	GND	fe_hstl[43]

Table 6-6 FORM Connector J2, J3, J5 and J7.

Signal Group	Direction	Signal Standard
DATA_A[xy],spare_in_a, DTIMEA, DSPAREA, ATIMEA, DVALIDA, DATA_B[xy],spare_in_b, DTIMEB, DSPAREB, ATIMEB, DVALIDB, DATA_C[xy],spare_in_c, DTIMEC, DSPAREC, ATIMEC, DVALIDC.	Input	HSTL-I-DCI
fe_hstl[xy]	Input/Output	HSTL-I-DCI
fe_lvcmos25[xy]	Input/Output	LVCMOS1V5
coreio[XY]	Input/Output	LVTTL
res_pll_a, RCLOCKA, RTIMEA, res_pll_b, RCLOCKB, RTIMEB, res_pll_c, RCLOCKC, RTIMEC.	Output	HSTL-I-DCI

Table 6-7 FORM Signals.

6.8 Delay Modules

6.8.1 DMA Input – J13;

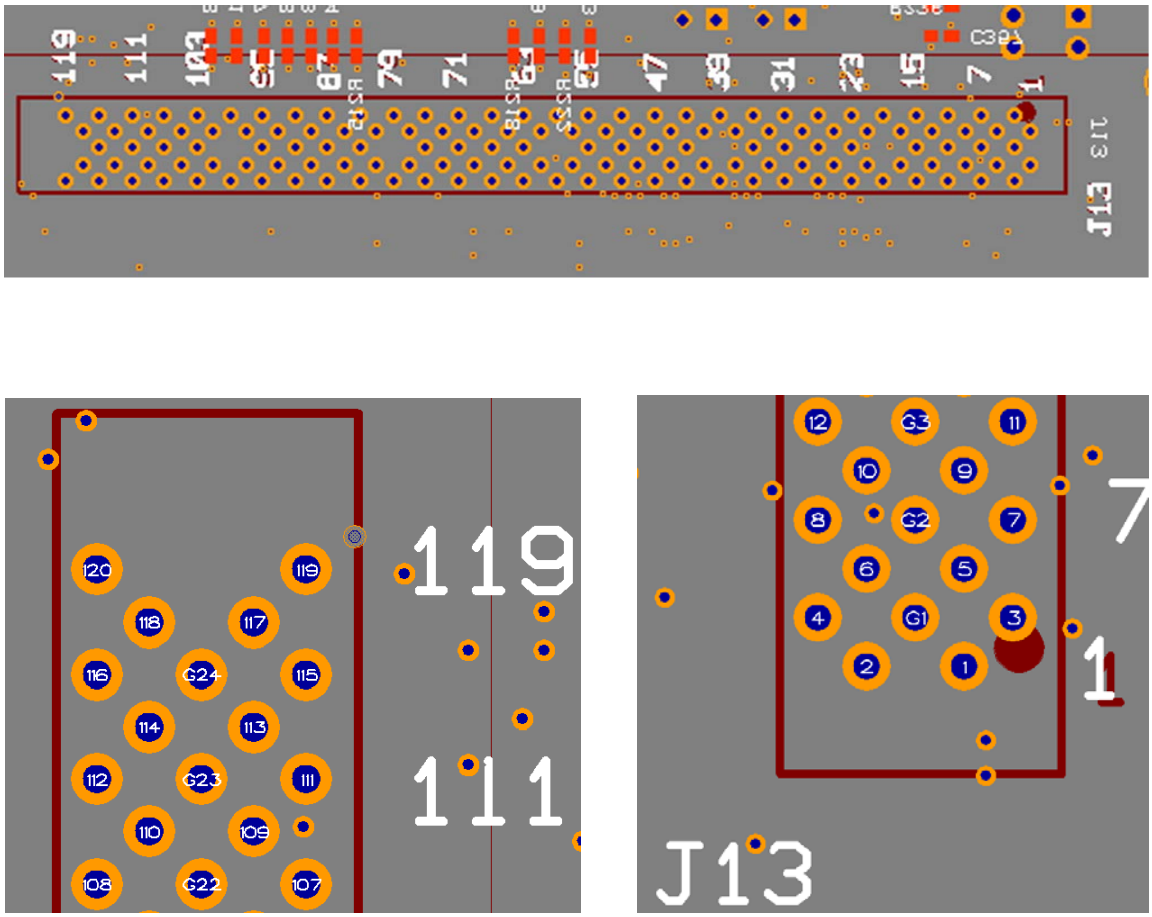

Figure 6-7 DMA Input Connector J13.

Pin	Name	Direction	Description
P1	MCB_33_Data[0]	In/Out	LVTTL
P2	MCB_33_Data[1]	In/Out	LVTTL
P3	MCB_33_Data[2]	In/Out	LVTTL
P4	MCB_33_Data[3]	In/Out	LVTTL
P5	MCB_33_Data[4]	In/Out	LVTTL
P6	MCB_33_Data[5]	In/Out	LVTTL
P7	MCB_33_Data[6]	In/Out	LVTTL
P8	MCB_33_Data[7]	In/Out	LVTTL
P9	MCB_33_Data[8]	In/Out	LVTTL
P10	MCB_33_Data[9]	In/Out	LVTTL
P11	MCB_33_Data[10]	In/Out	LVTTL
P12	MCB_33_Data[11]	In/Out	LVTTL
P13	MCB_33_Data[12]	In/Out	LVTTL
P14	MCB_33_Data[13]	In/Out	LVTTL
P15	MCB_33_Data[14]	In/Out	LVTTL
P16	MCB_33_Data[15]	In/Out	LVTTL
P17	MCB_33_Addr[0]	In	LVTTL
P18	MCB_33_Addr[1]	In	LVTTL
P19	MCB_33_Addr[2]	In	LVTTL
P20	MCB_33_Addr[3]	In	LVTTL
P21	MCB_33_Addr[4]	In	LVTTL
P22	MCB_CLK_DMA	In	MCB clock, LVTTL
P23	MCB_RW_33	In	MCB read/write, LVTTL
P24	CS_DMA	In	MCB chip select, active low, LVTTL
P25	RESET_PCM	In	System reset, act. low,LVTTL
P26	GND		
P27	GND		
P28	MCB_33_Addr[7]	In	LVTTL
P29	MCB_33_Addr[6]	In	LVTTL
P30	MCB_33_Addr[5]	In	LVTTL
P31	GND		
P32	GND		

P33	GND		
P34	GND		
P35	GND		
P36	GND		
P37	GND		
P38	GND		
P39	GND		
P40	GND		
P41	DMA_data_in[0]	In	HSTL-III-DCI
P42	DMA_data_in[1]	In	HSTL-III-DCI
P43	DMA_data_in[2]	In	HSTL-III-DCI
P44	DMA_data_in[3]	In	HSTL-III-DCI
P45	DMA_data_in[4]	In	HSTL-III-DCI
P46	DMA_data_in[5]	In	HSTL-III-DCI
P47	DMA_data_in[6]	In	HSTL-III-DCI
P48	DMA_data_in[7]	In	HSTL-III-DCI
P49	DMA_data_in[8]	In	HSTL-III-DCI
P50	DMA_data_in[9]	In	HSTL-III-DCI
P51	DMA_data_in[10]	In	HSTL-III-DCI
P52	DMA_data_in[11]	In	HSTL-III-DCI
P53	DMA_data_in[12]	In	HSTL-III-DCI
P54	DMA_data_in[13]	In	HSTL-III-DCI
P55	DMA_data_in[14]	In	HSTL-III-DCI
P56	DMA_data_in[15]	In	HSTL-III-DCI
P57	DMA_data_in[16]	In	HSTL-III-DCI
P58	DMA_data_in[17]	In	HSTL-III-DCI
P59	DMA_data_in[18]	In	HSTL-III-DCI
P60	DMA_data_in[19]	In	HSTL-III-DCI
P61	DMA_data_in[20]	In	HSTL-III-DCI
P62	DMA_data_in[21]	In	HSTL-III-DCI
P63	DMA_data_in[22]	In	HSTL-III-DCI
P64	DMA_data_in[23]	In	HSTL-III-DCI
P65	DMA_data_in[24]	In	HSTL-III-DCI
P66	DMA_data_in[25]	In	HSTL-III-DCI
P67	DMA_data_in[26]	In	HSTL-III-DCI

P68	DMA_data_in[27]	In	HSTL-III-DCI
P69	DMA_data_in[28]	In	HSTL-III-DCI
P70	DMA_data_in[29]	In	HSTL-III-DCI
P71	DMA_data_in[30]	In	HSTL-III-DCI
P72	DMA_data_in[31]	In	HSTL-III-DCI
P73	DMA_data_in[32]	In	HSTL-III-DCI
P74	DMA_data_in[33]	In	HSTL-III-DCI
P75	DMA_data_in[34]	In	HSTL-III-DCI
P76	DMA_data_in[35]	In	HSTL-III-DCI
P77	DMA_data_in[36]	In	HSTL-III-DCI
P78	DMA_data_in[37]	In	HSTL-III-DCI
P79	DMA_data_in[38]	In	HSTL-III-DCI
P80	DMA_data_in[39]	In	HSTL-III-DCI
P81	DMA_data_in[40]	In	HSTL-III-DCI
P82	DMA_data_in[41]	In	HSTL-III-DCI
P83	DMA_data_in[42]	In	HSTL-III-DCI
P84	DMA_data_in[43]	In	HSTL-III-DCI
P85	DMA_data_in[44]	In	HSTL-III-DCI
P86	DMA_data_in[45]	In	HSTL-III-DCI
P87	DMA_data_in[46]	In	HSTL-III-DCI
P88	DMA_data_in[47]	In	HSTL-III-DCI
P89	DMA_data_in[48]	In	HSTL-III-DCI
P90	DMA_data_in[49]	In	HSTL-III-DCI
P91	DMA_data_in[50]	In	HSTL-III-DCI
P92	DMA_data_in[51]	In	HSTL-III-DCI
P93	DMA_data_in[52]	In	HSTL-III-DCI
P94	DMA_data_in[53]	In	HSTL-III-DCI
P95	DMA_data_in[54]	In	HSTL-III-DCI
P96	DMA_data_in[55]	In	HSTL-III-DCI
P97	DMA_data_in[56]	In	HSTL-III-DCI
P98	DMA_data_in[57]	In	HSTL-III-DCI
P99	DMA_data_in[58]	In	HSTL-III-DCI
P100	DMA_data_in[59]	In	HSTL-III-DCI
P101	DMA_data_in[60]	In	HSTL-III-DCI
P102	DMA_data_in[61]	In	HSTL-III-DCI

P103	DMA_data_in[62]	In	HSTL-III-DCI
P104	DMA_data_in[63]	In	HSTL-III-DCI
P105	GND		
P106	GND		
P107	GND		
P108	GND		
P109	TDO_DMA	Out	JTAG, Test data out, LVTTL
P110	DV_IN_DMA	In	Data valid input, HSTL-III-DCI
P111	ANT_PPS_DMA	In	Antenna PPS input, HSTL-III-DCI
P112	spare_out_a	In/Out	HSTL-III-DCI
P113	TDO_TC	In	JTAG, Test data in, LVTTL
P114	DATA_100PPS_IN_DMA	In	Data tick, 10ms pulse, HSTL-III-DCI
P115	NC		
P116	ND_IN_DMA	In	Noise diode input, HSTL-III-DCI
P117	TCK_DMA	In	JTAG, Test clock, LVTTL
P118	GND		
P119	TMS_DMA	In	JTAG, Test mode select,LVTTL
P120	GND		

Pin	Signal
G1	3.3V
G2	3.3V
G3	3.3V
G4	3.3V
G5	3.3V
G6	3.3V
G7	3.3V
G8	3.3V
G9	2.5V
G10	2.5V
G11	2.5V
G12	2.5V
G13	GND
G14	GND
G15	GND
G16	GND
G17	GND
G18	GND
G19	GND
G20	GND
G21	GND
G22	GND
G23	GND
G24	GND

Table 6-8 DMA Input Connector J13.

6.8.2 DMA Output – J14

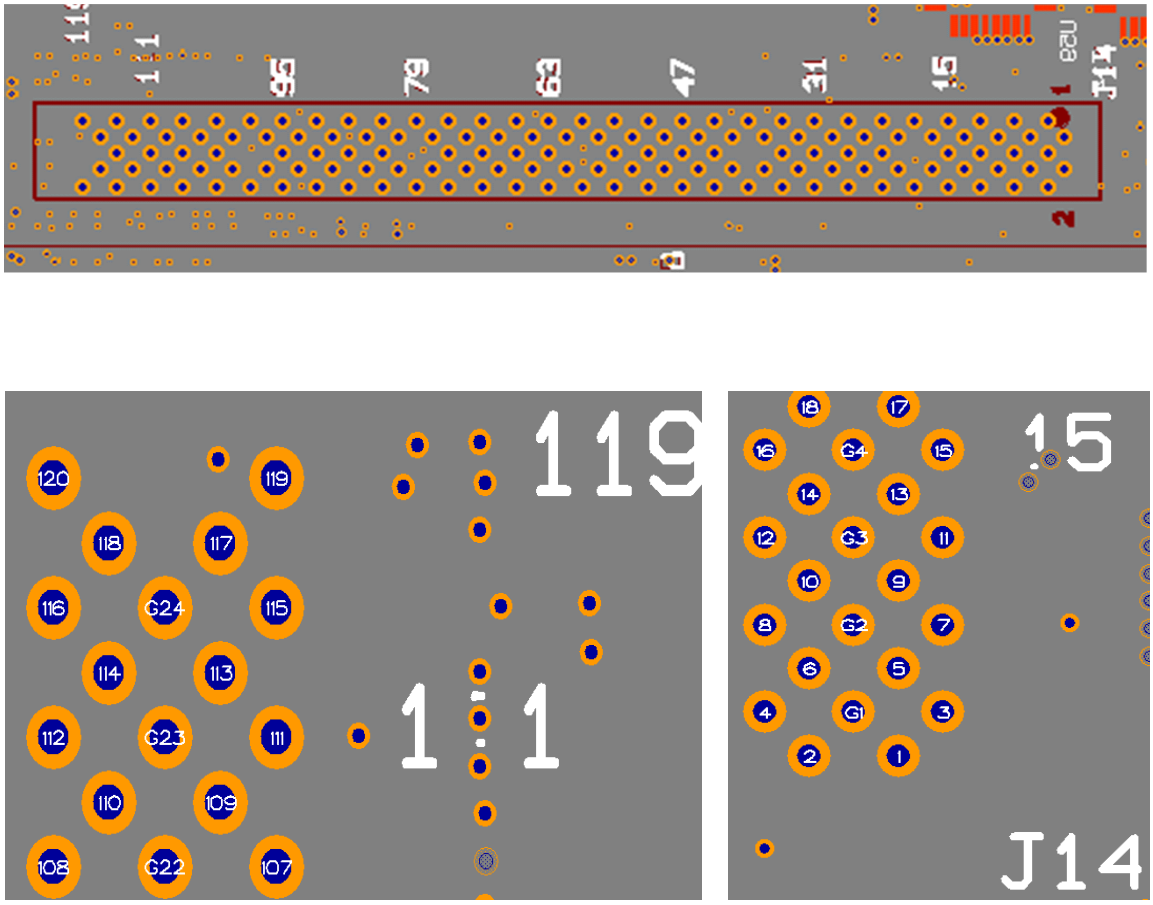

Figure 6-8 DMA Output Connector J14.

Pin	Name	Dir	Standard
P1	CDATA_33[0]	In	Configuration bus, LVTTL
P2	CDATA_33[1]	In	Configuration bus, LVTTL
P3	CDATA_33[2]	In	Configuration bus, LVTTL
P4	CDATA_33[3]	In	Configuration bus, LVTTL
P5	CDATA_33[4]	In	Configuration bus, LVTTL
P6	CDATA_33[5]	In	Configuration bus, LVTTL
P7	CDATA_33[6]	In	Configuration bus, LVTTL
P8	CDATA_33[7]	In	Configuration bus, LVTTL
P9	GND		
P10	GND		
P11	GND		
P12	GND		
P13	GND		
P14	GND		
P15	GND		
P16	GND		
P17	GND		
P18	GND		
P19	GND		
P20	GND		
P21	DONE_DMA	Out	Programming done, LVTTL
P22	PROG_DMA	In	Programming enable, LVTTL
P23	CCLK_DMA	In	Configuration clock, LVTTL
P24	GND		
P25	GND		
P26	GND		
P27	SL03_clk_neg_DMA	In	System clock neg. 128MHz, LVDS (2.5V)
P28	GND		
P29	SL03_clk_pos_DMA	In	System clock pos. 128MHz, LVDS (2.5V)
P30	GND		
P31	SL03_100PPS_neg_DMA	In	System tick 10ms, neg., LVDS (2.5V)
P32	GND		

P33	SL03_100PPS_pos_DMA	In	System tick 10ms, pos., LVDS (2.5V)
P34	GND		
P35	SL03_PPS_neg_DMA	In	System PPS, neg., LVDS (2.5V)
P36	GND		
P37	SL03_PPS_pos_DMA	In	System PPS, pos., LVDS (2.5V)
P38	GND		
P39	GND		
P40	GND		
P41	GND		
P42	GND		
P43	GND		
P44	GND		
P45	DMA_data_o[0]	Out	HSTL-III-DCI
P46	DMA_data_o[1]	Out	HSTL-III-DCI
P47	DMA_data_o[2]	Out	HSTL-III-DCI
P48	DMA_data_o[3]	Out	HSTL-III-DCI
P49	DMA_data_o[4]	Out	HSTL-III-DCI
P50	DMA_data_o[5]	Out	HSTL-III-DCI
P51	DMA_data_o[6]	Out	HSTL-III-DCI
P52	DMA_data_o[7]	Out	HSTL-III-DCI
P53	DMA_data_o[8]	Out	HSTL-III-DCI
P54	DMA_data_o[9]	Out	HSTL-III-DCI
P55	DMA_data_o[10]	Out	HSTL-III-DCI
P56	DMA_data_o[11]	Out	HSTL-III-DCI
P57	DMA_data_o[12]	Out	HSTL-III-DCI
P58	DMA_data_o[13]	Out	HSTL-III-DCI
P59	DMA_data_o[14]	Out	HSTL-III-DCI
P60	DMA_data_o[15]	Out	HSTL-III-DCI
P61	DMA_data_o[16]	Out	HSTL-III-DCI
P62	DMA_data_o[17]	Out	HSTL-III-DCI
P63	DMA_data_o[18]	Out	HSTL-III-DCI
P64	DMA_data_o[19]	Out	HSTL-III-DCI
P65	DMA_data_o[20]	Out	HSTL-III-DCI
P66	DMA_data_o[21]	Out	HSTL-III-DCI
P67	DMA_data_o[22]	Out	HSTL-III-DCI

P68	DMA_data_o[23]	Out	HSTL-III-DCI
P69	DMA_data_o[24]	Out	HSTL-III-DCI
P70	DMA_data_o[25]	Out	HSTL-III-DCI
P71	DMA_data_o[26]	Out	HSTL-III-DCI
P72	DMA_data_o[27]	Out	HSTL-III-DCI
P73	DMA_data_o[28]	Out	HSTL-III-DCI
P74	DMA_data_o[29]	Out	HSTL-III-DCI
P75	DMA_data_o[30]	Out	HSTL-III-DCI
P76	DMA_data_o[31]	Out	HSTL-III-DCI
P77	DMA_data_o[32]	Out	HSTL-III-DCI
P78	DMA_data_o[33]	Out	HSTL-III-DCI
P79	DMA_data_o[34]	Out	HSTL-III-DCI
P80	DMA_data_o[35]	Out	HSTL-III-DCI
P81	DMA_data_o[36]	Out	HSTL-III-DCI
P82	DMA_data_o[37]	Out	HSTL-III-DCI
P83	DMA_data_o[38]	Out	HSTL-III-DCI
P84	DMA_data_o[39]	Out	HSTL-III-DCI
P85	DMA_data_o[40]	Out	HSTL-III-DCI
P86	DMA_data_o[41]	Out	HSTL-III-DCI
P87	DMA_data_o[42]	Out	HSTL-III-DCI
P88	DMA_data_o[43]	Out	HSTL-III-DCI
P89	DMA_data_o[44]	Out	HSTL-III-DCI
P90	DMA_data_o[45]	Out	HSTL-III-DCI
P91	DMA_data_o[46]	Out	HSTL-III-DCI
P92	DMA_data_o[47]	Out	HSTL-III-DCI
P93	DMA_data_o[48]	Out	HSTL-III-DCI
P94	DMA_data_o[49]	Out	HSTL-III-DCI
P95	DMA_data_o[50]	Out	HSTL-III-DCI
P96	DMA_data_o[51]	Out	HSTL-III-DCI
P97	DMA_data_o[52]	Out	HSTL-III-DCI
P98	DMA_data_o[53]	Out	HSTL-III-DCI
P99	DMA_data_o[54]	Out	HSTL-III-DCI
P100	DMA_data_o[55]	Out	HSTL-III-DCI
P101	DMA_data_o[56]	Out	HSTL-III-DCI
P102	DMA_data_o[57]	Out	HSTL-III-DCI

P103	DMA_data_o[58]	Out	HSTL-III-DCI
P104	DMA_data_o[59]	Out	HSTL-III-DCI
P105	DMA_data_o[60]	Out	HSTL-III-DCI
P106	DMA_data_o[61]	Out	HSTL-III-DCI
P107	DMA_data_o[62]	Out	HSTL-III-DCI
P108	DMA_data_o[63]	Out	HSTL-III-DCI
P109	DMA_error_frame	Out	Frame error, HSTL-III-DCI
P110	GND		
P111	GND		
P112	DMA_clk_data_out	Out	Output data clock, HSTL-III-DCI
P113	DMA_data_val_out	Out	Data valid output, HSTL-III-DCI
P114	DMA_data_100pps_out	Out	Data tick output, 10ms, HSTL-III-DCI
P115	DMA_nd_out	Out	Noise diode output, HSTL-III-DCI
P116	GND		
P117	DMA_ser_error	Out	Serial error, HSTL-III-DCI
P118	GND		
P119	GND		
P120	GND		

Pin	Signal
G1	1V2-B
G2	1V2-B
G3	1V2-B
G4	1V2-B
G5	1V2-B
G6	1V2-B
G7	1V2-B
G8	1V2-B
G9	GND
G10	GND
G11	GND
G12	GND
G13	GND
G14	GND
G15	GND
G16	GND
G17	1.5V
G18	1.5V
G19	1.5V
G20	1.5V
G21	1.5V
G22	1.5V
G23	1.5V
G24	1.5V

Table 6-9 DMA Output Connector J14.

6.8.3 DMB Input – J17

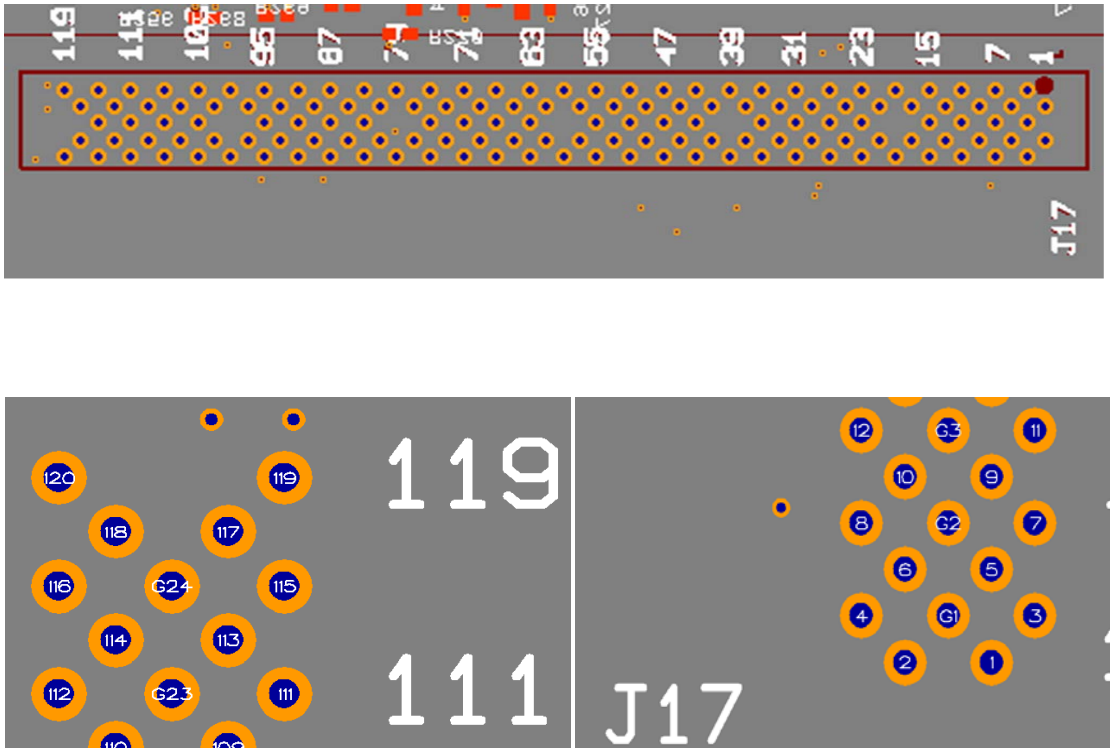

Figure 6-9 DMB Input Connector J17.

Pin	Name	Dir	Description
P1	MCB_33_Data[0]	In/Out	LVTTL
P2	MCB_33_Data[1]	In/Out	LVTTL
P3	MCB_33_Data[2]	In/Out	LVTTL
P4	MCB_33_Data[3]	In/Out	LVTTL
P5	MCB_33_Data[4]	In/Out	LVTTL
P6	MCB_33_Data[5]	In/Out	LVTTL
P7	MCB_33_Data[6]	In/Out	LVTTL
P8	MCB_33_Data[7]	In/Out	LVTTL
P9	MCB_33_Data[8]	In/Out	LVTTL
P10	MCB_33_Data[9]	In/Out	LVTTL
P11	MCB_33_Data[10]	In/Out	LVTTL
P12	MCB_33_Data[11]	In/Out	LVTTL
P13	MCB_33_Data[12]	In/Out	LVTTL
P14	MCB_33_Data[13]	In/Out	LVTTL
P15	MCB_33_Data[14]	In/Out	LVTTL
P16	MCB_33_Data[15]	In/Out	LVTTL
P17	MCB_33_Addr[0]	In	LVTTL
P18	MCB_33_Addr[1]	In	LVTTL
P19	MCB_33_Addr[2]	In	LVTTL
P20	MCB_33_Addr[3]	In	LVTTL
P21	MCB_33_Addr[4]	In	LVTTL
P22	MCB_CLK_DMA	In	MCB clock, LVTTL
P23	MCB_RW_33	In	MCB read/write, LVTTL
P24	CS_DMB	In	MCB chip select, active low, LVTTL
P25	RESET_PCM	In	System reset, act. low,LVTTL
P26	GND		
P27	GND		
P28	MCB_33_Addr[7]	In	LVTTL
P29	MCB_33_Addr[6]	In	LVTTL
P30	MCB_33_Addr[5]	In	LVTTL
P31	GND		
P32	GND		

P33	GND		
P34	GND		
P35	GND		
P36	GND		
P37	GND		
P38	GND		
P39	GND		
P40	GND		
P41	DMB_data_in[0]	In	HSTL-III-DCI
P42	DMB_data_in[1]	In	HSTL-III-DCI
P43	DMB_data_in[2]	In	HSTL-III-DCI
P44	DMB_data_in[3]	In	HSTL-III-DCI
P45	DMB_data_in[4]	In	HSTL-III-DCI
P46	DMB_data_in[5]	In	HSTL-III-DCI
P47	DMB_data_in[6]	In	HSTL-III-DCI
P48	DMB_data_in[7]	In	HSTL-III-DCI
P49	DMB_data_in[8]	In	HSTL-III-DCI
P50	DMB_data_in[9]	In	HSTL-III-DCI
P51	DMB_data_in[10]	In	HSTL-III-DCI
P52	DMB_data_in[11]	In	HSTL-III-DCI
P53	DMB_data_in[12]	In	HSTL-III-DCI
P54	DMB_data_in[13]	In	HSTL-III-DCI
P55	DMB_data_in[14]	In	HSTL-III-DCI
P56	DMB_data_in[15]	In	HSTL-III-DCI
P57	DMB_data_in[16]	In	HSTL-III-DCI
P58	DMB_data_in[17]	In	HSTL-III-DCI
P59	DMB_data_in[18]	In	HSTL-III-DCI
P60	DMB_data_in[19]	In	HSTL-III-DCI
P61	DMB_data_in[20]	In	HSTL-III-DCI
P62	DMB_data_in[21]	In	HSTL-III-DCI
P63	DMB_data_in[22]	In	HSTL-III-DCI
P64	DMB_data_in[23]	In	HSTL-III-DCI
P65	DMB_data_in[24]	In	HSTL-III-DCI
P66	DMB_data_in[25]	In	HSTL-III-DCI
P67	DMB_data_in[26]	In	HSTL-III-DCI

P68	DMB_data_in[27]	In	HSTL-III-DCI
P69	DMB_data_in[28]	In	HSTL-III-DCI
P70	DMB_data_in[29]	In	HSTL-III-DCI
P71	DMB_data_in[30]	In	HSTL-III-DCI
P72	DMB_data_in[31]	In	HSTL-III-DCI
P73	DMB_data_in[32]	In	HSTL-III-DCI
P74	DMB_data_in[33]	In	HSTL-III-DCI
P75	DMB_data_in[34]	In	HSTL-III-DCI
P76	DMB_data_in[35]	In	HSTL-III-DCI
P77	DMB_data_in[36]	In	HSTL-III-DCI
P78	DMB_data_in[37]	In	HSTL-III-DCI
P79	DMB_data_in[38]	In	HSTL-III-DCI
P80	DMB_data_in[39]	In	HSTL-III-DCI
P81	DMB_data_in[40]	In	HSTL-III-DCI
P82	DMB_data_in[41]	In	HSTL-III-DCI
P83	DMB_data_in[42]	In	HSTL-III-DCI
P84	DMB_data_in[43]	In	HSTL-III-DCI
P85	DMB_data_in[44]	In	HSTL-III-DCI
P86	DMB_data_in[45]	In	HSTL-III-DCI
P87	DMB_data_in[46]	In	HSTL-III-DCI
P88	DMB_data_in[47]	In	HSTL-III-DCI
P89	DMB_data_in[48]	In	HSTL-III-DCI
P90	DMB_data_in[49]	In	HSTL-III-DCI
P91	DMB_data_in[50]	In	HSTL-III-DCI
P92	DMB_data_in[51]	In	HSTL-III-DCI
P93	DMB_data_in[52]	In	HSTL-III-DCI
P94	DMB_data_in[53]	In	HSTL-III-DCI
P95	DMB_data_in[54]	In	HSTL-III-DCI
P96	DMB_data_in[55]	In	HSTL-III-DCI
P97	DMB_data_in[56]	In	HSTL-III-DCI
P98	DMB_data_in[57]	In	HSTL-III-DCI
P99	DMB_data_in[58]	In	HSTL-III-DCI
P100	DMB_data_in[59]	In	HSTL-III-DCI
P101	DMB_data_in[60]	In	HSTL-III-DCI
P102	DMB_data_in[61]	In	HSTL-III-DCI

P103	DMB_data_in[62]	In	HSTL-III-DCI
P104	DMB_data_in[63]	In	HSTL-III-DCI
P105	GND		
P106	GND		
P107	GND		
P108	GND		
P109	TDO_DMB	Out	JTAG, Test data out, LVTTL
P110	DV_IN_DMB	In	Data valid input, HSTL-III-DCI
P111	ANT_PPS_DMB	In	Antenna PPS input, HSTL-III-DCI
P112	spare_out_b	In/Out	HSTL-III-DCI
P113	TDO_TC	In	JTAG, Test data in, LVTTL
P114	DATA_100PPS_IN_DMB	In	Data tick, 10ms pulse, HSTL-III-DCI
P115	NC		
P116	ND_IN_DMB	In	Noise diode input, HSTL-III-DCI
P117	TCK_DMB	In	JTAG, Test clock, LVTTL
P118	GND		
P119	TMS_DMB	In	JTAG, Test mode select, LVTTL
P120	GND		

Pin	Signal
G1	3.3V
G2	3.3V
G3	3.3V
G4	3.3V
G5	3.3V
G6	3.3V
G7	3.3V
G8	3.3V
G9	2.5V
G10	2.5V
G11	2.5V
G12	2.5V
G13	GND
G14	GND
G15	GND
G16	GND
G17	GND
G18	GND
G19	GND
G20	GND
G21	GND
G22	GND
G23	GND
G24	GND

Table 6-10 DMB Input Connector J17.

6.8.4 DMB Output – J18

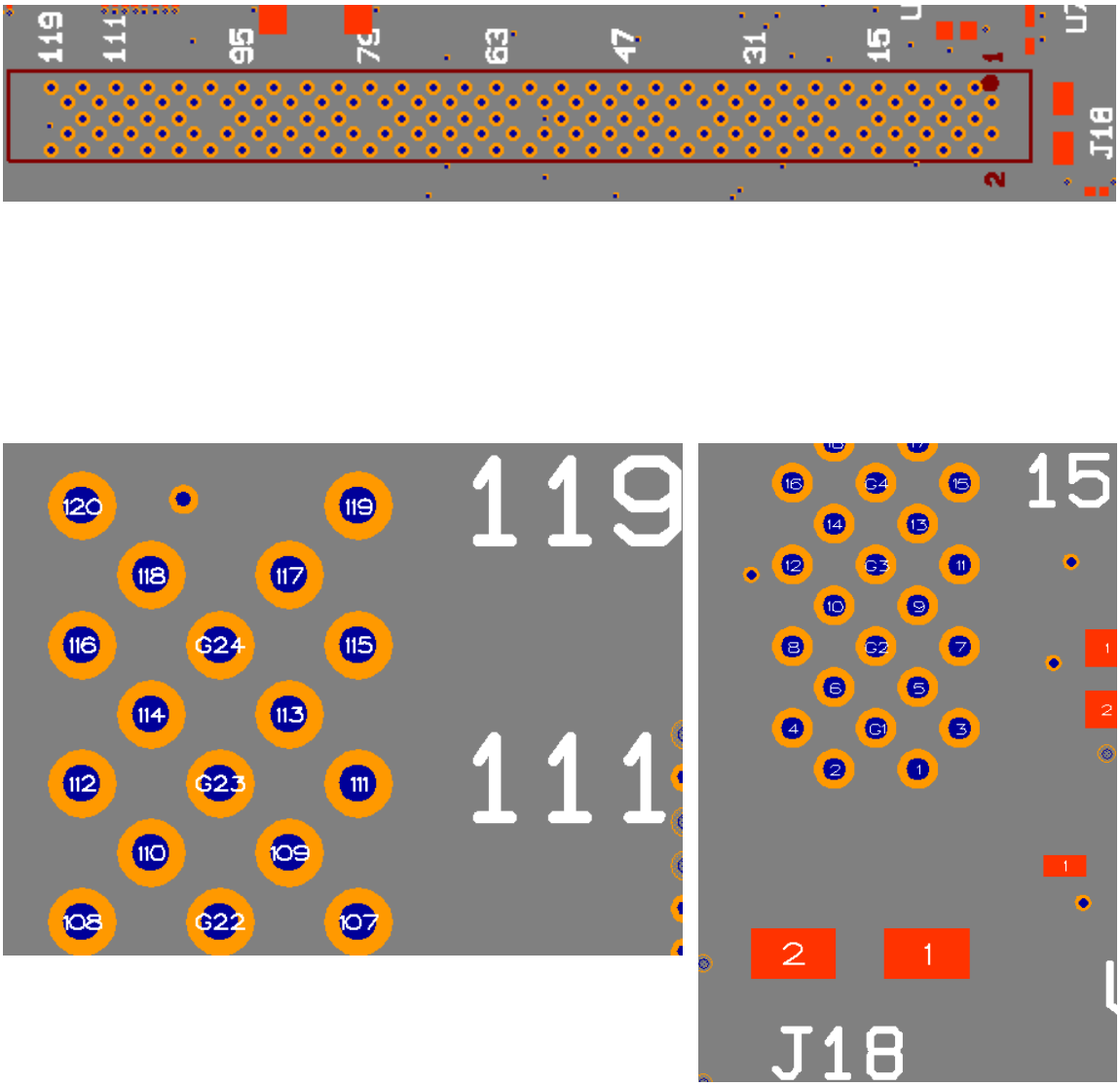

Figure 6-10 DMB Output Connector J18.

Pin	Name	Dir	Standard
P1	CDATA_33[0]	In	Configuration bus, LVTTL
P2	CDATA_33[1]	In	Configuration bus, LVTTL
P3	CDATA_33[2]	In	Configuration bus, LVTTL
P4	CDATA_33[3]	In	Configuration bus, LVTTL
P5	CDATA_33[4]	In	Configuration bus, LVTTL
P6	CDATA_33[5]	In	Configuration bus, LVTTL
P7	CDATA_33[6]	In	Configuration bus, LVTTL
P8	CDATA_33[7]	In	Configuration bus, LVTTL
P9	GND		
P10	GND		
P11	GND		
P12	GND		
P13	GND		
P14	GND		
P15	GND		
P16	GND		
P17	GND		
P18	GND		
P19	GND		
P20	GND		
P21	DONE_DMB	Out	Programming done, LVTTL
P22	PROG_DMB	In	Programming enable, LVTTL
P23	CCLK_DMB	In	Configuration clock, LVTTL
P24	GND		
P25	GND		
P26	GND		
P27	SL03_clk_neg_DMB	In	System clock neg. 128MHz, LVDS (2.5V)
P28	GND		
P29	SL03_clk_pos_DMB	In	System clock pos. 128MHz, LVDS (2.5V)
P30	GND		
P31	SL03_100PPS_neg_DMB	In	System tick 10ms, neg., LVDS (2.5V)
P32	GND		

P33	SL03_100PPS_pos_DMB	In	System tick 10ms, pos., LVDS (2.5V)
P34	GND		
P35	SL03_PPS_neg_DMB	In	System PPS, neg., LVDS (2.5V)
P36	GND		
P37	SL03_PPS_pos_DMB	In	System PPS, pos., LVDS (2.5V)
P38	GND		
P39	GND		
P40	GND		
P41	GND		
P42	GND		
P43	GND		
P44	GND		
P45	DMB_data_o[0]	Out	HSTL-III-DCI
P46	DMB_data_o[1]	Out	HSTL-III-DCI
P47	DMB_data_o[2]	Out	HSTL-III-DCI
P48	DMB_data_o[3]	Out	HSTL-III-DCI
P49	DMB_data_o[4]	Out	HSTL-III-DCI
P50	DMB_data_o[5]	Out	HSTL-III-DCI
P51	DMB_data_o[6]	Out	HSTL-III-DCI
P52	DMB_data_o[7]	Out	HSTL-III-DCI
P53	DMB_data_o[8]	Out	HSTL-III-DCI
P54	DMB_data_o[9]	Out	HSTL-III-DCI
P55	DMB_data_o[10]	Out	HSTL-III-DCI
P56	DMB_data_o[11]	Out	HSTL-III-DCI
P57	DMB_data_o[12]	Out	HSTL-III-DCI
P58	DMB_data_o[13]	Out	HSTL-III-DCI
P59	DMB_data_o[14]	Out	HSTL-III-DCI
P60	DMB_data_o[15]	Out	HSTL-III-DCI
P61	DMB_data_o[16]	Out	HSTL-III-DCI
P62	DMB_data_o[17]	Out	HSTL-III-DCI
P63	DMB_data_o[18]	Out	HSTL-III-DCI
P64	DMB_data_o[19]	Out	HSTL-III-DCI
P65	DMB_data_o[20]	Out	HSTL-III-DCI
P66	DMB_data_o[21]	Out	HSTL-III-DCI
P67	DMB_data_o[22]	Out	HSTL-III-DCI

P68	DMB_data_o[23]	Out	HSTL-III-DCI
P69	DMB_data_o[24]	Out	HSTL-III-DCI
P70	DMB_data_o[25]	Out	HSTL-III-DCI
P71	DMB_data_o[26]	Out	HSTL-III-DCI
P72	DMB_data_o[27]	Out	HSTL-III-DCI
P73	DMB_data_o[28]	Out	HSTL-III-DCI
P74	DMB_data_o[29]	Out	HSTL-III-DCI
P75	DMB_data_o[30]	Out	HSTL-III-DCI
P76	DMB_data_o[31]	Out	HSTL-III-DCI
P77	DMB_data_o[32]	Out	HSTL-III-DCI
P78	DMB_data_o[33]	Out	HSTL-III-DCI
P79	DMB_data_o[34]	Out	HSTL-III-DCI
P80	DMB_data_o[35]	Out	HSTL-III-DCI
P81	DMB_data_o[36]	Out	HSTL-III-DCI
P82	DMB_data_o[37]	Out	HSTL-III-DCI
P83	DMB_data_o[38]	Out	HSTL-III-DCI
P84	DMB_data_o[39]	Out	HSTL-III-DCI
P85	DMB_data_o[40]	Out	HSTL-III-DCI
P86	DMB_data_o[41]	Out	HSTL-III-DCI
P87	DMB_data_o[42]	Out	HSTL-III-DCI
P88	DMB_data_o[43]	Out	HSTL-III-DCI
P89	DMB_data_o[44]	Out	HSTL-III-DCI
P90	DMB_data_o[45]	Out	HSTL-III-DCI
P91	DMB_data_o[46]	Out	HSTL-III-DCI
P92	DMB_data_o[47]	Out	HSTL-III-DCI
P93	DMB_data_o[48]	Out	HSTL-III-DCI
P94	DMB_data_o[49]	Out	HSTL-III-DCI
P95	DMB_data_o[50]	Out	HSTL-III-DCI
P96	DMB_data_o[51]	Out	HSTL-III-DCI
P97	DMB_data_o[52]	Out	HSTL-III-DCI
P98	DMB_data_o[53]	Out	HSTL-III-DCI
P99	DMB_data_o[54]	Out	HSTL-III-DCI
P100	DMB_data_o[55]	Out	HSTL-III-DCI
P101	DMB_data_o[56]	Out	HSTL-III-DCI
P102	DMB_data_o[57]	Out	HSTL-III-DCI

P103	DMB_data_o[58]	Out	HSTL-III-DCI
P104	DMB_data_o[59]	Out	HSTL-III-DCI
P105	DMB_data_o[60]	Out	HSTL-III-DCI
P106	DMB_data_o[61]	Out	HSTL-III-DCI
P107	DMB_data_o[62]	Out	HSTL-III-DCI
P108	DMB_data_o[63]	Out	HSTL-III-DCI
P109	DMA_error_frame	Out	Frame error, HSTL-III-DCI
P110	GND		
P111	GND		
P112	DMB_clk_data_out	Out	Output data clock, HSTL-III-DCI
P113	DMB_data_val_out	Out	Data valid output, HSTL-III-DCI
P114	DMB_data_100pps_out	Out	Data tick output, 10ms, HSTL-III-DCI
P115	DMB_nd_out	Out	Noise diode output, HSTL-III-DCI
P116	GND		
P117	DMB_ser_error	Out	Serial error, HSTL-III-DCI
P118	GND		
P119	GND		
P120	GND		

Pin	Signal
G1	1V2-B1
G2	1V2-B1
G3	1V2-B1
G4	1V2-B1
G5	1V2-B1
G6	1V2-B1
G7	1V2-B1
G8	1V2-B1
G9	GND
G10	GND
G11	GND
G12	GND
G13	GND
G14	GND
G15	GND
G16	GND
G17	1.5V
G18	1.5V
G19	1.5V
G20	1.5V
G21	1.5V
G22	1.5V
G23	1.5V
G24	1.5V

Table 6-11 DMB Output Connector J18.

6.9 Data Connector

6.9.1 Gb/s Data – J10

Pin	A	B	C	D	E	F	G	H
1	NC	NC	NC	NC	hsp_rx_0_p	hsp_rx_0_N	hsp_tx_0_p	hsp_tx_0_n
2	NC	NC	NC	NC	hsp_tim_rx_p	hsp_tim_rx_n	hsp_tim_tx_p	hsp_tim_tx_n
3	clk_out1_P[0]	clk_out1_N[0]	cntr_P[0]	cntr_N[0]	data_out_OUT1_P[0]	data_out_OUT1_N[0]	data_out_OUT2_P[0]	data_out_OUT2_N[0]
4	clk_out1_P[1]	clk_out1_N[1]	cntr_P[1]	cntr_N[1]	data_out_OUT1_P[1]	data_out_OUT1_N[1]	data_out_OUT2_P[1]	data_out_OUT2_N[1]
5	clk_out1_P[2]	clk_out1_N[2]	cntr_P[2]	cntr_N[2]	data_out_OUT1_P[2]	data_out_OUT1_N[2]	data_out_OUT2_P[2]	data_out_OUT2_N[2]
6	clk_out1_P[3]	clk_out1_N[3]	cntr_P[3]	cntr_N[3]	data_out_OUT1_P[3]	data_out_OUT1_N[3]	data_out_OUT2_P[3]	data_out_OUT2_N[3]
7	clk_out1_P[4]	clk_out1_N[4]	cntr_P[4]	cntr_N[4]	data_out_OUT1_P[4]	data_out_OUT1_N[4]	data_out_OUT2_P[4]	data_out_OUT2_N[4]
8	clk_out1_P[5]	clk_out1_N[5]	cntr_P[5]	cntr_N[5]	data_out_OUT1_P[5]	data_out_OUT1_N[5]	data_out_OUT2_P[5]	data_out_OUT2_N[5]
9	clk_out1_P[6]	clk_out1_N[6]	cntr_P[6]	cntr_N[6]	data_out_OUT1_P[6]	data_out_OUT1_N[6]	data_out_OUT2_P[6]	data_out_OUT2_N[6]
10	clk_out1_P[7]	clk_out1_N[7]	cntr_P[7]	cntr_N[7]	data_out_OUT1_P[7]	data_out_OUT1_N[7]	data_out_OUT2_P[7]	data_out_OUT2_N[7]
11	clk_out1_P[8]	clk_out1_N[8]	cntr_P[8]	cntr_N[8]	data_out_OUT1_P[8]	data_out_OUT1_N[8]	data_out_OUT2_P[8]	data_out_OUT2_N[8]
12	clk_out2_P[0]	clk_out2_N[0]	cntr_P[9]	cntr_N[9]	data_out_OUT1_P[9]	data_out_OUT1_N[9]	data_out_OUT2_P[9]	data_out_OUT2_N[9]
13	clk_out2_P[1]	clk_out2_N[1]	cntr_P[10]	cntr_N[10]	data_out_OUT1_P[10]	data_out_OUT1_N[10]	data_out_OUT2_P[10]	data_out_OUT2_N[10]
14	clk_out2_P[2]	clk_out2_N[2]	cntr_P[11]	cntr_N[11]	data_out_OUT1_P[11]	data_out_OUT1_N[11]	data_out_OUT2_P[11]	data_out_OUT2_N[11]
15	clk_out2_P[3]	clk_out2_N[3]	cntr_P[12]	cntr_N[12]	data_out_OUT1_P[12]	data_out_OUT1_N[12]	data_out_OUT2_P[12]	data_out_OUT2_N[12]
16	clk_out2_P[4]	clk_out2_N[4]	cntr_P[13]	cntr_N[13]	data_out_OUT1_P[13]	data_out_OUT1_N[13]	data_out_OUT2_P[13]	data_out_OUT2_N[13]
17	clk_out2_P[5]	clk_out2_N[5]	cntr_P[14]	cntr_N[14]	data_out_OUT1_P[14]	data_out_OUT1_N[14]	data_out_OUT2_P[14]	data_out_OUT2_N[14]
18	clk_out2_P[6]	clk_out2_N[6]	cntr_P[15]	cntr_N[15]	data_out_OUT1_P[15]	data_out_OUT1_N[15]	data_out_OUT2_P[15]	data_out_OUT2_N[15]
19	clk_out2_P[7]	clk_out2_N[7]	cntr_P[16]	cntr_N[16]	data_out_OUT1_P[16]	data_out_OUT1_N[16]	data_out_OUT2_P[16]	data_out_OUT2_N[16]
20	clk_out2_P[8]	clk_out2_N[8]	cntr_P[17]	cntr_N[17]	data_out_OUT1_P[17]	data_out_OUT1_N[17]	data_out_OUT2_P[17]	data_out_OUT2_N[17]
21	NC	NC	NC	NC	NC	NC	NC	NC

22	CLK64A_P	CLK64A_N	TCA0_P	TCA0_N	NC	NC	NC	NC
23	clk_a_o_P	clk_a_o_N	tc_a_o_P	tc_a_o_N	NC	NC	NC	NC
24	CLK64B_P	CLK64B_N	TCB0_P	TCB0_N	NC	NC	NC	NC
25	clk_b_o_P	clk_b_o_N	tc_b_o_P	tc_b_o_N	NC	NC	NC	NC

All signals are outputs, except for: CLK64A_P/N, TCA0_P/N, CLK64B_P/N and TCB0_P/N which are inputs.

All signals are LVDS.

Table 6-12 Data Connector J10.

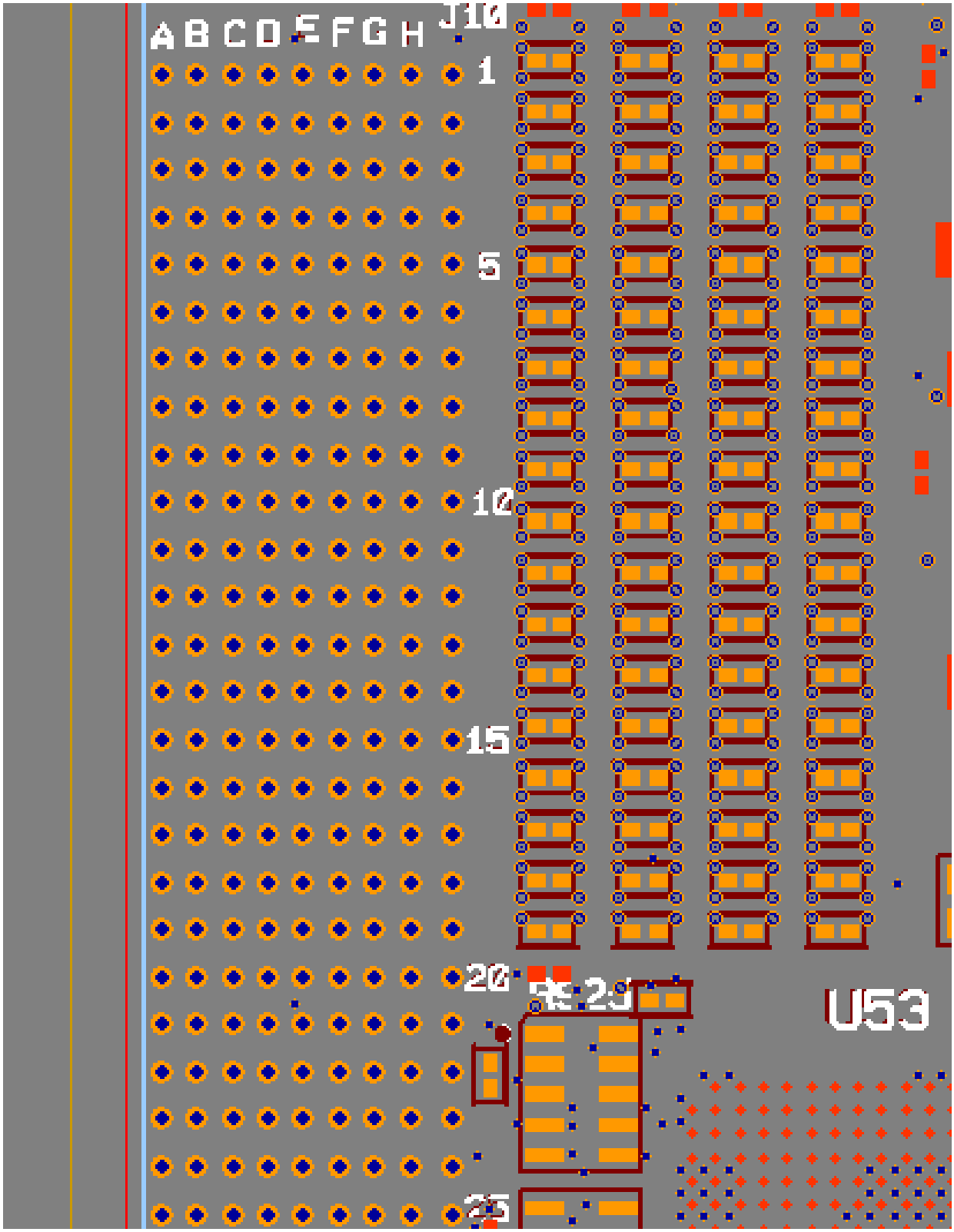

Figure 6-11 Data Connector J10.

6.9.2 J15 Connector (below J10)

Pin	A	B	C	D	E	F	G	H
1	GND	GND	GND	GND	GND	GND	GND	GND
2	NC	NC	NC	NC	NC	NC	NC	NC
3	3V3_tocon2	3V3_tocon2	3V3_tocon2	3V3_tocon2	3V3_tocon2	3V3_tocon2	3V3_tocon2	3V3_tocon2
4	NC	NC	NC	NC	NC	NC	NC	NC
5	2V2_tocon2	2V2_tocon2	2V2_tocon2	2V2_tocon2	2V2_tocon2	2V2_tocon2	2V2_tocon2	2V2_tocon2
6	NC	NC	NC	NC	NC	NC	NC	NC
7	NC	NC	NC	NC	NC	NC	NC	NC
8	NC	NC	NC	NC	NC	NC	NC	NC
9	NC	NC	NC	NC	NC	NC	NC	NC
10	GND	GND	GND	GND	GND	GND	GND	GND
11	NC	NC	NC	NC	hsp_rx_1_p	hsp_rx_1_n	hsp_tx_1_p	hsp_tx_1_n

Signals hsp_rx_1_p/n and hsp_tx_1_p/n are outputs LVDS. Signal 3V3_tocon2 is 3.3V. Signal 2V2_tocon2 is 2.5V.

Table 6-13 Data Connector J15.

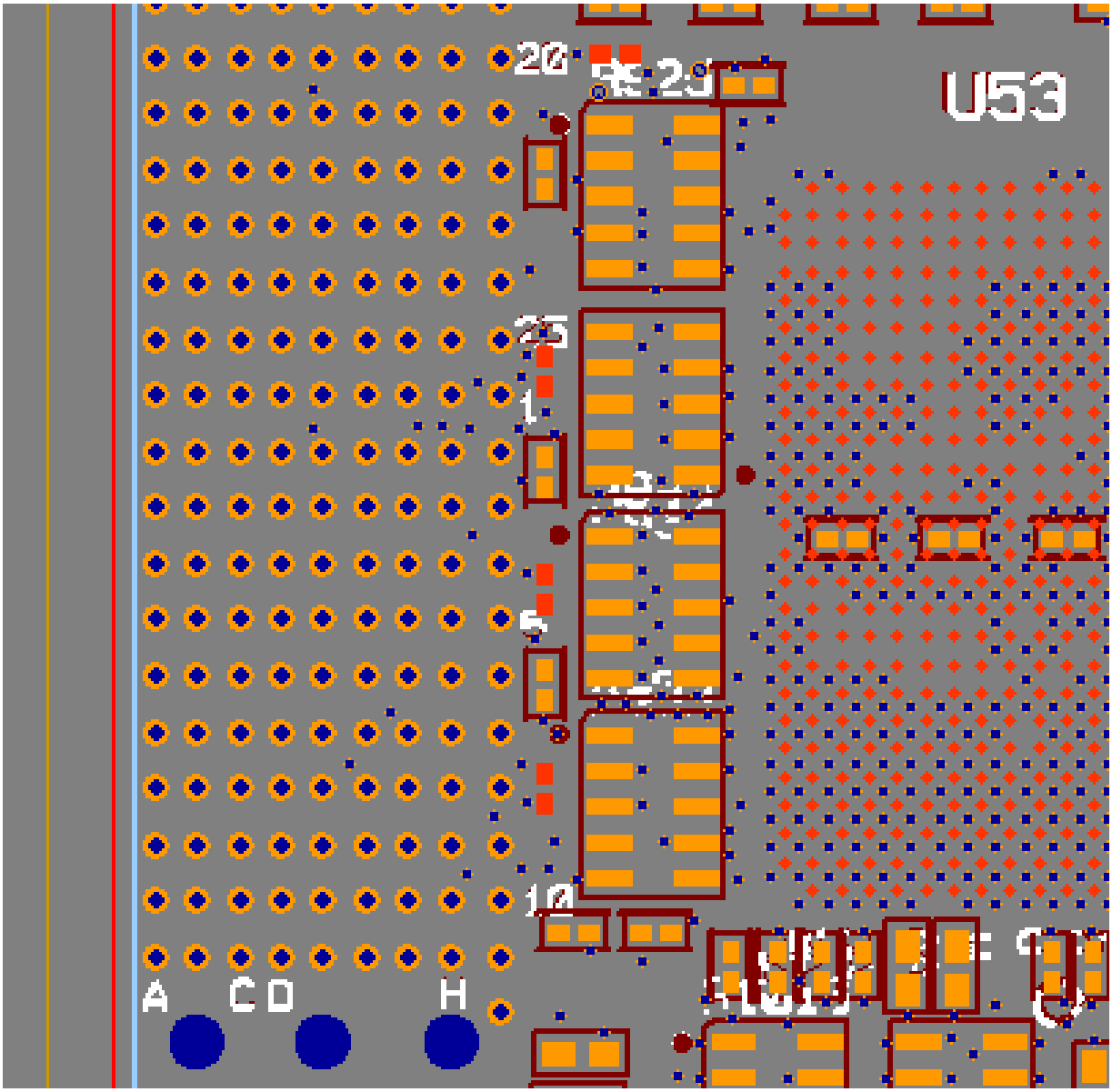

Figure 6-12 Data Connector J15.

6.9.3 J9 (above J10)

Pin	A	B	C
1	NC	NC	NC
2	NC	NC	NC
3	NC	NC	NC
4	NC	NC	NC

Table 6-14 Data Connector J9.

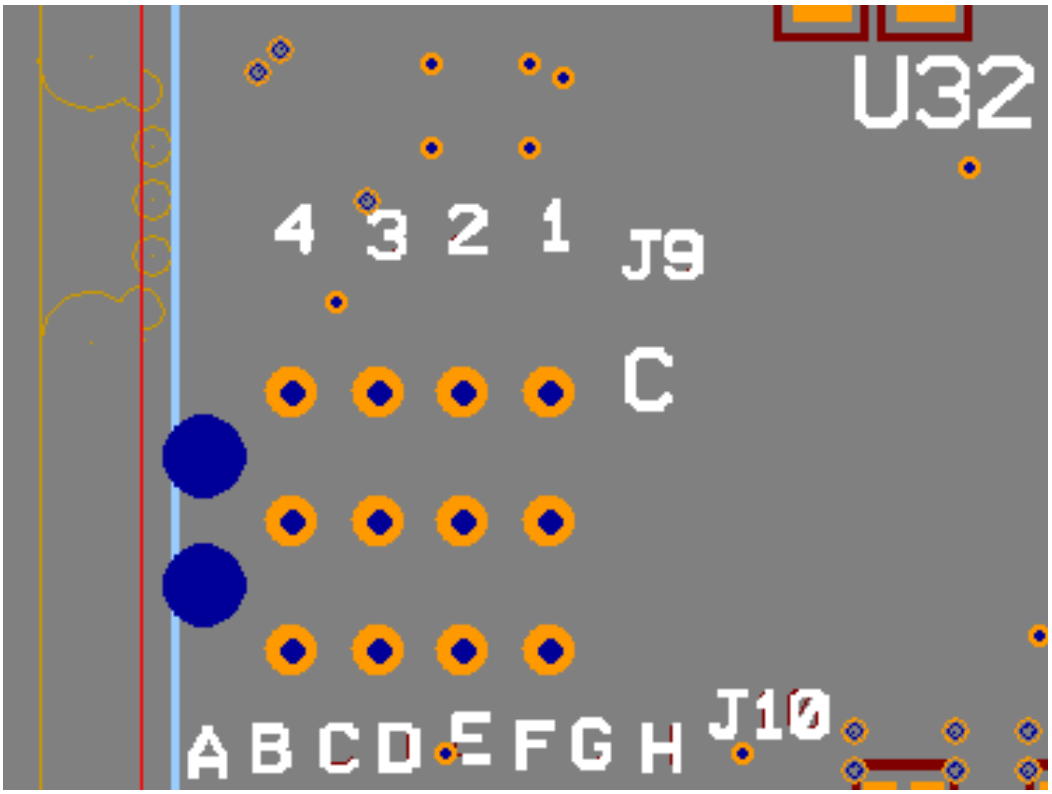

Figure 6-13 Data Connector J9.

6.10 VSI Connectors

6.10.1 Upper VSI Connector – J6

Pin	A	B	C	D	E	F	G	H
1	VSI0_out_P[0]	VSI0_out_N[0]	VSI0_out_P[1]	VSI0_out_N[1]	VSI0_out_P[2]	VSI0_out_N[2]	VSI0_out_P[3]	VSI0_out_N[3]
2	VSI0_out_P[4]	VSI0_out_N[4]	VSI0_out_P[5]	VSI0_out_N[5]	VSI0_out_P[6]	VSI0_out_N[6]	VSI0_out_P[7]	VSI0_out_N[7]
3	VSI0_out_P[8]	VSI0_out_N[8]	VSI0_out_P[9]	VSI0_out_N[9]	VSI0_out_P[10]	VSI0_out_N[10]	VSI0_out_P[11]	VSI0_out_N[11]
4	VSI0_out_P[12]	VSI0_out_N[12]	VSI0_out_P[13]	VSI0_out_N[13]	VSI0_out_P[14]	VSI0_out_N[14]	VSI0_out_P[15]	VSI0_out_N[15]
5	VSI0_out_P[16]	VSI0_out_N[16]	VSI0_out_P[17]	VSI0_out_N[17]	VSI0_out_P[18]	VSI0_out_N[18]	VSI0_out_P[19]	VSI0_out_N[19]
6	VSI0_out_P[20]	VSI0_out_N[20]	VSI0_out_P[21]	VSI0_out_N[21]	VSI0_out_P[22]	VSI0_out_N[22]	VSI0_out_P[23]	VSI0_out_N[23]
7	VSI0_out_P[24]	VSI0_out_N[24]	VSI0_out_P[25]	VSI0_out_N[25]	VSI0_out_P[26]	VSI0_out_N[26]	VSI0_out_P[27]	VSI0_out_N[27]
8	VSI0_out_P[28]	VSI0_out_N[28]	VSI0_out_P[29]	VSI0_out_N[29]	VSI0_out_P[30]	VSI0_out_N[30]	VSI0_out_P[31]	VSI0_out_N[31]
9	VSI0_out_P[32]	VSI0_out_N[32]	VSI0_out_P[33]	VSI0_out_N[33]	VSI0_out_P[34]	VSI0_out_N[34]	VSI0_out_P[35]	VSI0_out_N[35]
10	VSI0_out_P[36]	VSI0_out_N[36]	VSI0_out_P[37]	VSI0_out_N[37]	VSI0_out_P[38]	VSI0_out_N[38]	VSI0_out_P[39]	VSI0_out_N[39]
11	NC	NC	NC	NC	NC	NC	NC	NC
12	TC_P[0]	TC_N[0]	TC_P[1]	TC_N[1]	NC	NC	NC	NC
13	NC	NC	NC	NC	NC	NC	NC	NC
14	NC	NC	NC	NC	NC	NC	NC	NC
15	NC	NC	NC	NC	NC	NC	NC	NC
16	VSI0_in_P[0]	VSI0_in_N[0]	VSI0_in_P[1]	VSI0_in_N[1]	VSI0_in_P[2]	VSI0_in_N[2]	VSI0_in_P[3]	VSI0_in_N[3]
17	VSI0_in_P[4]	VSI0_in_N[4]	VSI0_in_P[5]	VSI0_in_N[5]	VSI0_in_P[6]	VSI0_in_N[6]	VSI0_in_P[7]	VSI0_in_N[7]
18	VSI0_in_P[8]	VSI0_in_N[8]	VSI0_in_P[9]	VSI0_in_N[9]	VSI0_in_P[10]	VSI0_in_N[10]	VSI0_in_P[11]	VSI0_in_N[11]

19	VSI0_in_P[12]	VSI0_in_N[12]	VSI0_in_P[13]	VSI0_in_N[13]	VSI0_in_P[14]	VSI0_in_N[14]	VSI0_in_P[15]	VSI0_in_N[15]
20	VSI0_in_P[16]	VSI0_in_N[16]	VSI0_in_P[17]	VSI0_in_N[17]	VSI0_in_P[18]	VSI0_in_N[18]	VSI0_in_P[19]	VSI0_in_N[19]
21	VSI0_in_P[20]	VSI0_in_N[20]	VSI0_in_P[21]	VSI0_in_N[21]	VSI0_in_P[22]	VSI0_in_N[22]	VSI0_in_P[23]	VSI0_in_N[23]
22	VSI0_in_P[24]	VSI0_in_N[24]	VSI0_in_P[25]	VSI0_in_N[25]	VSI0_in_P[26]	VSI0_in_N[26]	VSI0_in_P[27]	VSI0_in_N[27]
23	VSI0_in_P[28]	VSI0_in_N[28]	VSI0_in_P[29]	VSI0_in_N[29]	VSI0_in_P[30]	VSI0_in_N[30]	VSI0_in_P[31]	VSI0_in_N[31]
24	VSI0_in_P[32]	VSI0_in_N[32]	VSI0_in_P[33]	VSI0_in_N[33]	VSI0_in_P[34]	VSI0_in_N[34]	VSI0_in_P[35]	VSI0_in_N[35]
25	VSI0_in_P[36]	VSI0_in_N[36]	VSI0_in_P[37]	VSI0_in_N[37]	VSI0_in_P[38]	VSI0_in_N[38]	VSI0_in_P[39]	VSI0_in_N[39]

All signals are LVDS. Signals VSI0_out_[n] are outputs, all other signals are inputs.

Table 6-15 Upper VSI Connector J6.

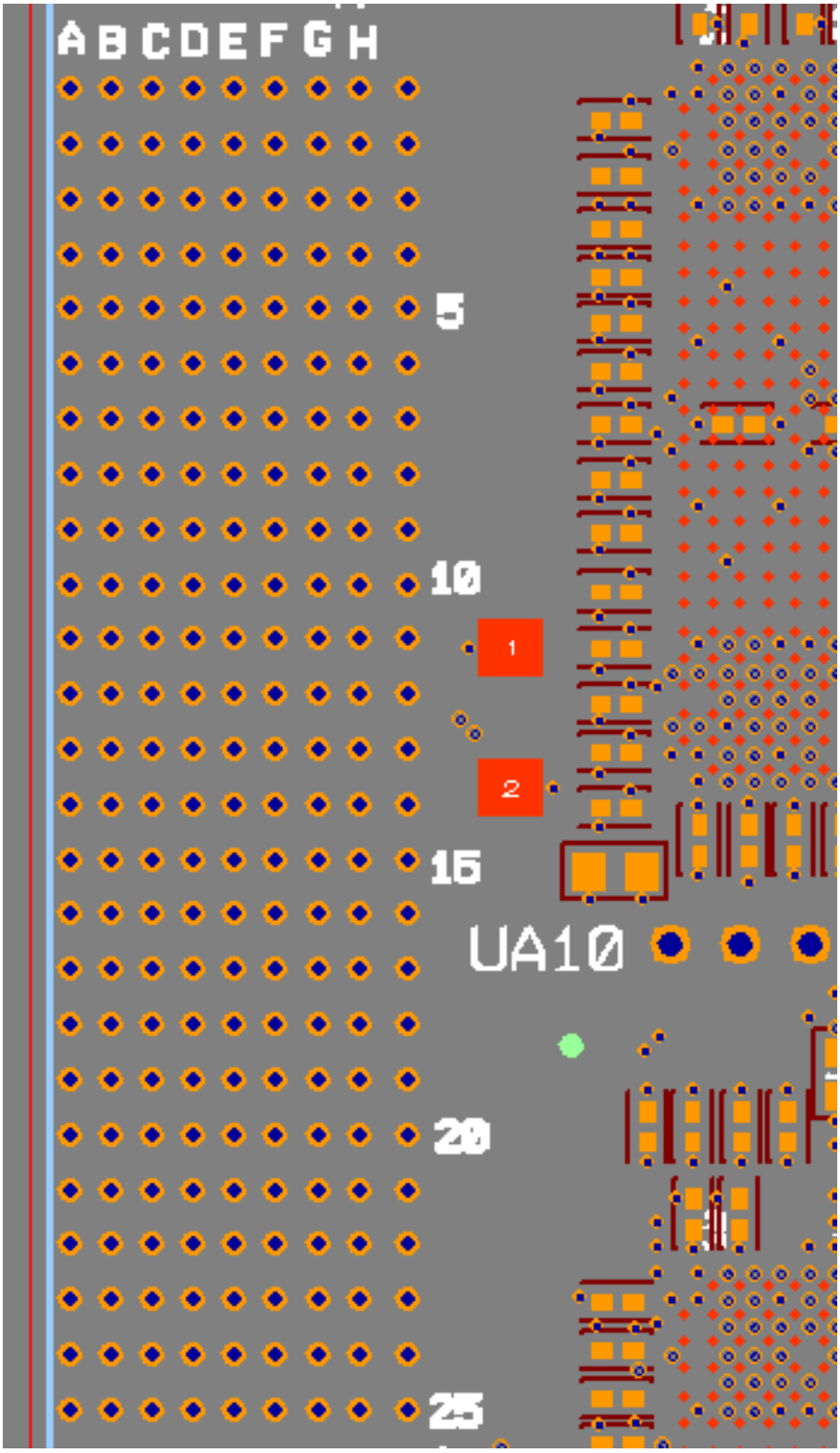

Figure 6-14 Upper VSI Connector J6.

6.10.2 Upper VSI Connector – J8

Pin	A	B	C	D	E	F	G	H
1	NC	NC	NC	NC	NC	NC	NC	NC
2	NC	NC	NC	NC	NC	NC	NC	NC
3	3V3_tocon1	3V3_tocon1	3V3_tocon1	3V3_tocon1	3V3_tocon1	3V3_tocon1	3V3_tocon1	3V3_tocon1
4	NC	NC	NC	NC	NC	NC	NC	NC
5	2V2_tocon1	2V2_tocon1	2V2_tocon1	2V2_tocon1	2V2_tocon1	2V2_tocon1	2V2_tocon1	2V2_tocon1
6	NC	NC	NC	NC	NC	NC	NC	NC
7	NC	NC	NC	NC	NC	NC	NC	NC
8	NC	NC	NC	NC	NC	NC	NC	NC
9	NC	NC	NC	NC	NC	NC	NC	NC
10	GND	GND	GND	GND	GND	GND	GND	GND
11	slot_id[8]	slot_id[9]	slot_id[10]	slot_id[11]	slot_id[12]	slot_id[13]	slot_id[14]	slot_id[15]

Signals slot_id[n] are LVTTL inputs. Signal 3V3_tocon1 is 3.3V. Signal 2V2_tocon1 is 2.5V.

Table 6-16 Upper VSI Connector J8.

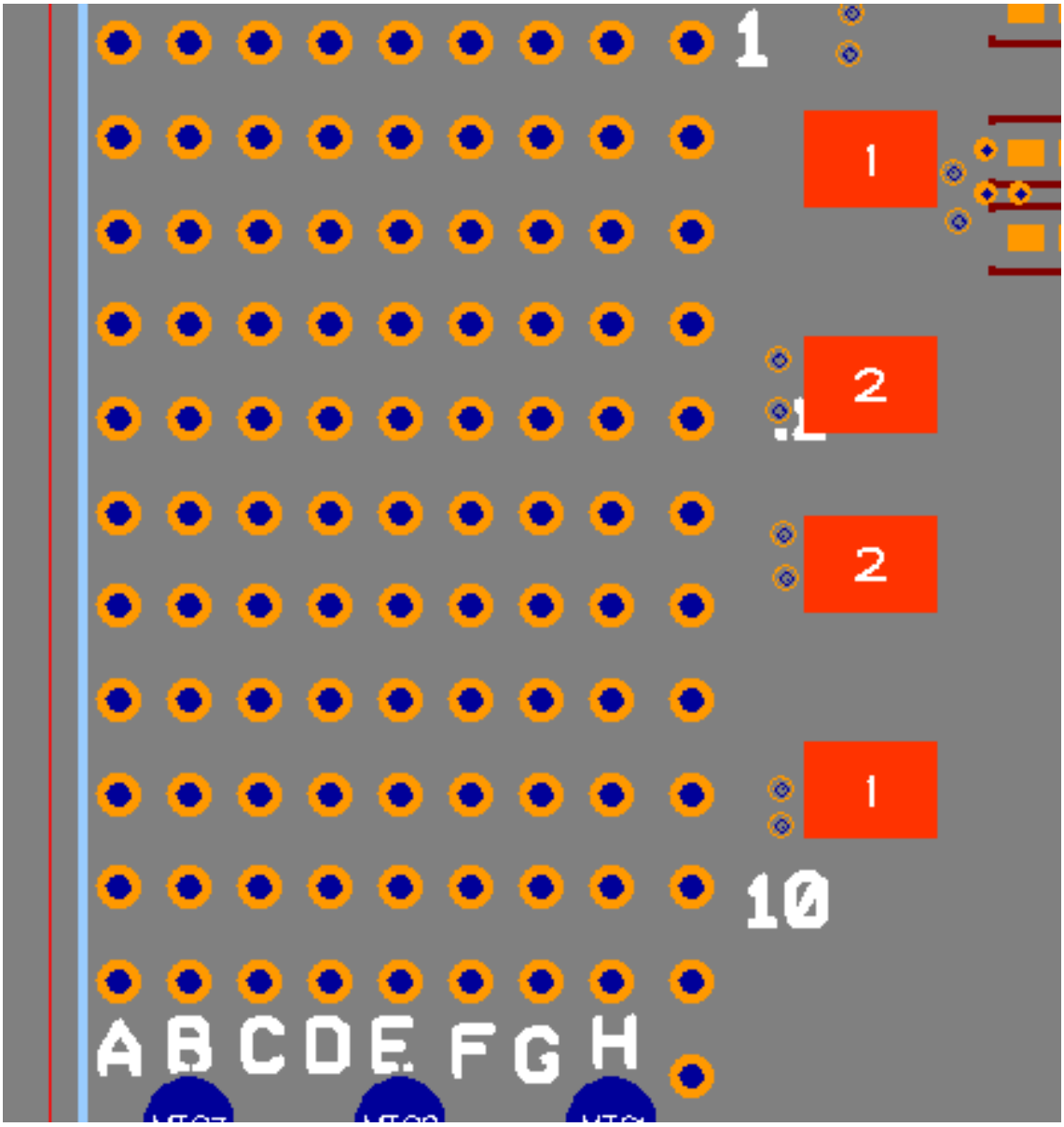

Figure 6-15 Upper VSI Connector J8.

6.10.3 Lower VSI Connector – J19

Pin	A	B	C	D	E	F	G	H
1	VSI1_out_P[0]	VSI1_out_N[0]	VSI1_out_P[1]	VSI1_out_N[1]	VSI1_out_P[2]	VSI1_out_N[2]	VSI1_out_P[3]	VSI1_out_N[3]
2	VSI1_out_P[4]	VSI1_out_N[4]	VSI1_out_P[5]	VSI1_out_N[5]	VSI1_out_P[6]	VSI1_out_N[6]	VSI1_out_P[7]	VSI1_out_N[7]
3	VSI1_out_P[8]	VSI1_out_N[8]	VSI1_out_P[9]	VSI1_out_N[9]	VSI1_out_P[10]	VSI1_out_N[10]	VSI1_out_P[11]	VSI1_out_N[11]
4	VSI1_out_P[12]	VSI1_out_N[12]	VSI1_out_P[13]	VSI1_out_N[13]	VSI1_out_P[14]	VSI1_out_N[14]	VSI1_out_P[15]	VSI1_out_N[15]
5	VSI1_out_P[16]	VSI1_out_N[16]	VSI1_out_P[17]	VSI1_out_N[17]	VSI1_out_P[18]	VSI1_out_N[18]	VSI1_out_P[19]	VSI1_out_N[19]
6	VSI1_out_P[20]	VSI1_out_N[20]	VSI1_out_P[21]	VSI1_out_N[21]	VSI1_out_P[22]	VSI1_out_N[22]	VSI1_out_P[23]	VSI1_out_N[23]
7	VSI1_out_P[24]	VSI1_out_N[24]	VSI1_out_P[25]	VSI1_out_N[25]	VSI1_out_P[26]	VSI1_out_N[26]	VSI1_out_P[27]	VSI1_out_N[27]
8	VSI1_out_P[28]	VSI1_out_N[28]	VSI1_out_P[29]	VSI1_out_N[29]	VSI1_out_P[30]	VSI1_out_N[30]	VSI1_out_P[31]	VSI1_out_N[31]
9	VSI1_out_P[32]	VSI1_out_N[32]	VSI1_out_P[33]	VSI1_out_N[33]	VSI1_out_P[34]	VSI1_out_N[34]	VSI1_out_P[35]	VSI1_out_N[35]
10	VSI1_out_P[36]	VSI1_out_N[36]	VSI1_out_P[37]	VSI1_out_N[37]	VSI1_out_P[38]	VSI1_out_N[38]	VSI1_out_P[39]	VSI1_out_N[39]
11	NC	NC	NC	NC	NC	NC	NC	NC
12	TC1_P[0]	TC1_N[0]	TC1_P[1]	TC1_N[1]	NC	NC	NC	NC
13	NC	NC	NC	NC	NC	NC	NC	NC
14	NC	NC	NC	NC	NC	NC	NC	NC
15	NC	NC	NC	NC	NC	NC	NC	NC
16	VSI1_in_P[0]	VSI1_in_N[0]	VSI1_in_P[1]	VSI1_in_N[1]	VSI1_in_P[2]	VSI1_in_N[2]	VSI1_in_P[3]	VSI1_in_N[3]
17	VSI1_in_P[4]	VSI1_in_N[4]	VSI1_in_P[5]	VSI1_in_N[5]	VSI1_in_P[6]	VSI1_in_N[6]	VSI1_in_P[7]	VSI1_in_N[7]
18	VSI1_in_P[8]	VSI1_in_N[8]	VSI1_in_P[9]	VSI1_in_N[9]	VSI1_in_P[10]	VSI1_in_N[10]	VSI1_in_P[11]	VSI1_in_N[11]
19	VSI1_in_P[12]	VSI1_in_N[12]	VSI1_in_P[13]	VSI1_in_N[13]	VSI1_in_P[14]	VSI1_in_N[14]	VSI1_in_P[15]	VSI1_in_N[15]
20	VSI1_in_P[16]	VSI1_in_N[16]	VSI1_in_P[17]	VSI1_in_N[17]	VSI1_in_P[18]	VSI1_in_N[18]	VSI1_in_P[19]	VSI1_in_N[19]

21	VSI1_in_P[20]	VSI1_in_N[20]	VSI1_in_P[21]	VSI1_in_N[21]	VSI1_in_P[22]	VSI1_in_N[22]	VSI1_in_P[23]	VSI1_in_N[23]
22	VSI1_in_P[24]	VSI1_in_N[24]	VSI1_in_P[25]	VSI1_in_N[25]	VSI1_in_P[26]	VSI1_in_N[26]	VSI1_in_P[27]	VSI1_in_N[27]
23	VSI1_in_P[28]	VSI1_in_N[28]	VSI1_in_P[29]	VSI1_in_N[29]	VSI1_in_P[30]	VSI1_in_N[30]	VSI1_in_P[31]	VSI1_in_N[31]
24	VSI1_in_P[32]	VSI1_in_N[32]	VSI1_in_P[33]	VSI1_in_N[33]	VSI1_in_P[34]	VSI1_in_N[34]	VSI1_in_P[35]	VSI1_in_N[35]
25	VSI1_in_P[36]	VSI1_in_N[36]	VSI1_in_P[37]	VSI1_in_N[37]	VSI1_in_P[38]	VSI1_in_N[38]	VSI1_in_P[39]	VSI1_in_N[39]

All signals are LVDS. Signals VSI1_out_[n] are outputs, all other signals are inputs.

Table 6-17 Lower VSI Connector J19.

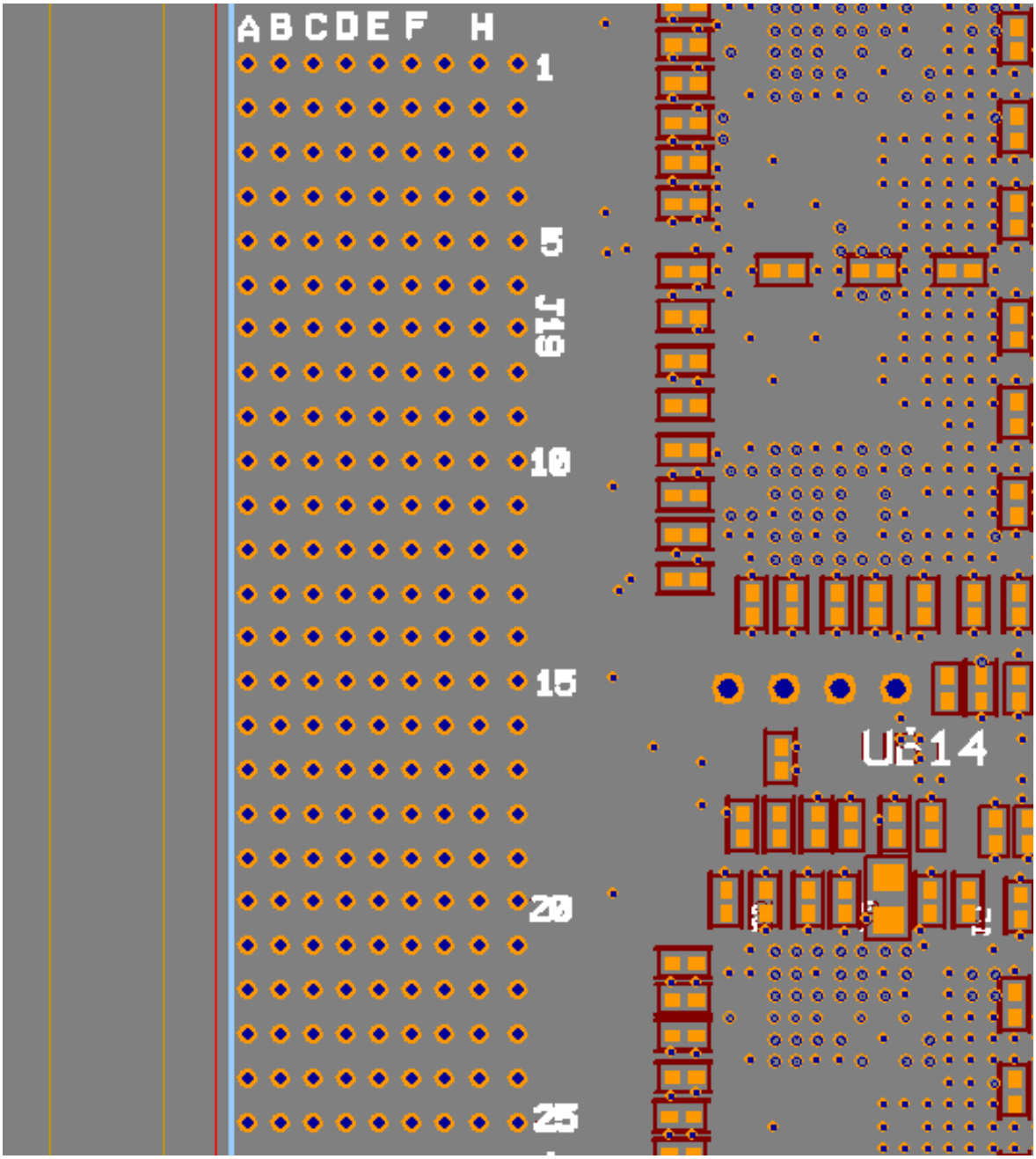

Figure 6-16 Lower VSI Connector J19

6.10.4 Lower VSI Connector – J20

Pin	A	B	C	D	E	F	G	H
1	NC	NC	NC	NC	NC	NC	NC	NC
2	NC	NC	NC	NC	NC	NC	NC	NC
3	3V3_tocon3	3V3_tocon3	3V3_tocon3	3V3_tocon3	3V3_tocon3	3V3_tocon3	3V3_tocon3	3V3_tocon3
4	NC	NC	NC	NC	NC	NC	NC	NC
5	2V2_tocon3	2V2_tocon3	2V2_tocon3	2V2_tocon3	2V2_tocon3	2V2_tocon3	2V2_tocon3	2V2_tocon3
6	NC	NC	NC	NC	NC	NC	NC	NC
7	NC	NC	NC	NC	NC	NC	NC	NC
8	NC	NC	NC	NC	NC	NC	NC	NC
9	NC	NC	NC	NC	NC	NC	NC	NC
10	GND	GND	GND	GND	GND	GND	GND	GND
11	slot_id[0]	slot_id[1]	slot_id[2]	slot_id[3]	slot_id[4]	slot_id[5]	slot_id[6]	slot_id[7]

Signals slot_id[n] are LVTTL inputs. Signal 3V3_tocon3 is 3.3V. Signal 2V2_tocon3 is 2.5V.

Table 6-18 Lower VSI Connector J20.

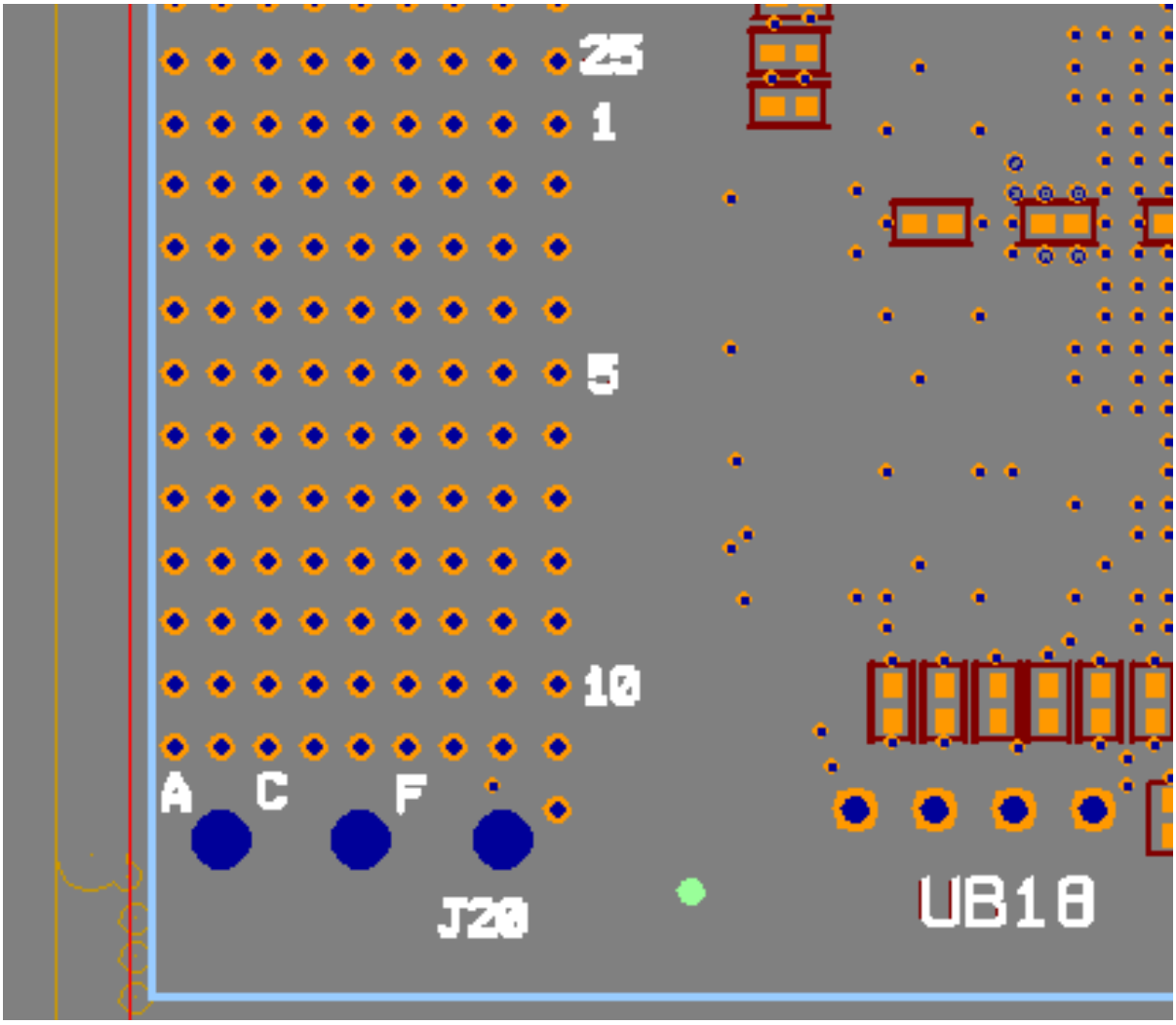

Figure 6-17 Lower VSI Connector J20

6.11 Agilent Soft-Touch Probe Header – J21 and J22

There are two un-populated test header locations on the board near the MCB FPGAwhich allows a logic analyzer to be attached to the MCB for testing purposes. Each test header, referred to as J21 and J22, is built to allow for the installation of an Agilent soft-touch probe header. The solder-in header is Agilent part E5405-68702 and is shown below:

Figure 6-18 Agilent solder-in probe header, E5405-68702.

The soft-touch probe head is Agilent E5406A and is shown below:

Figure 6-19 Agilent soft-touch probe, E5406A.

The entire soft-touch probe pod assembly is shown below:

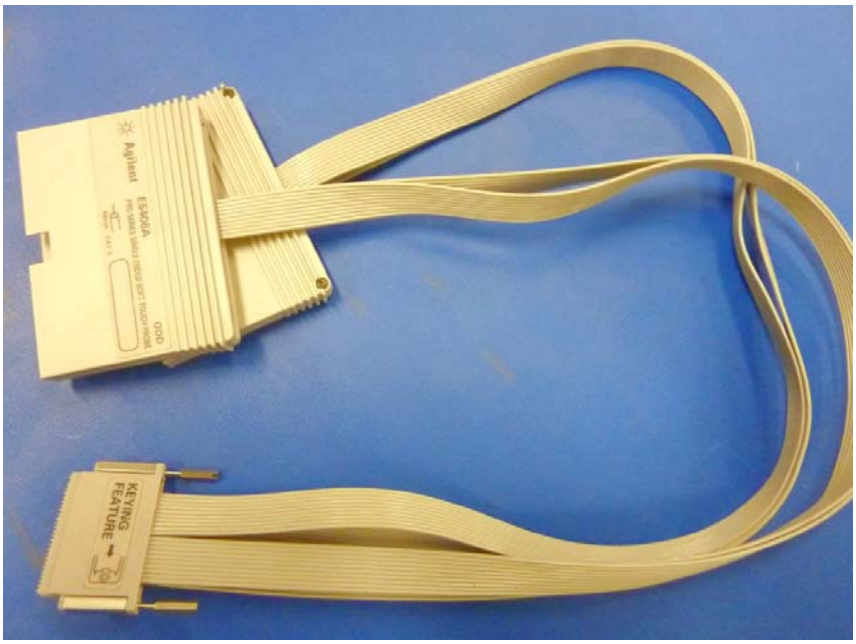

Figure 6-20 Agilent soft-touch E5406A pod assembly.

Pin	Signal		Pin	Signal
A1	CDATA[7]		B1	GND
A2	CDATA[6]		B2	nMCB_BS
A3	GND		B3	MCB_INT
A4	CDATA[5]		B4	GND
A5	CDATA[4]		B5	CBUS_EN
A6	GND		B6	NC
A7	CCLK		B7	GND
A8	GND		B8	NC
A9	GND		B9	NC
A10	CDATA[3]		B10	GND
A11	CDATA[2]		B11	NC
A12	GND		B12	NC
A13	CDATA[1]		B13	GND
A14	CDATA[0]		B14	NC
A15	GND		B15	NC
A16	NC		B16	GND
A17	NC		B17	NC
A18	GND		B18	NC
A19	NC		B19	GND
A20	NC		B20	NC
A21	GND		B21	NC
A22	NC		B22	GND
A23	NC		B23	NC
A24	GND		B24	NC
A25	NC		B25	GND
A26	NC		B26	NC
A27	GND		B27	NC

Table 6-22 Agilent test header J21 pinout

Pin	Signal		Pin	Signal
A1	MCB_DATA[15]		B1	GND
A2	MCB_DATA[14]		B2	MCB_Addr[15]
A3	GND		B3	MCB_Addr[14]
A4	MCB_DATA[13]		B4	GND
A5	MCB_DATA[12]		B5	MCB_Addr[13]
A6	GND		B6	MCB_Addr[12]
A7	MCB_CLK		B7	GND
A8	GND		B8	MCB_Addr[11]
A9	GND		B9	MCB_Addr[10]
A10	MCB_DATA[11]		B10	GND
A11	MCB_DATA[10]		B11	MCB_Addr[9]
A12	GND		B12	MCB_Addr[8]
A13	MCB_DATA[9]		B13	GND
A14	MCB_DATA[8]		B14	MCB_Addr[7]
A15	GND		B15	MCB_Addr[6]
A16	MCB_DATA[7]		B16	GND
A17	MCB_DATA[6]		B17	MCB_Addr[5]
A18	GND		B18	MCB_Addr[4]
A19	MCB_DATA[5]		B19	GND
A20	MCB_DATA[4]		B20	GND
A21	GND		B21	MCB_Addr[3]
A22	MCB_DATA[3]		B22	GND
A23	MCB_DATA[2]		B23	MCB_Addr[2]
A24	GND		B24	MCB_Addr[1]
A25	MCB_DATA[1]		B25	GND
A26	MCB_DATA[0]		B26	MCB_Addr[0]
A27	GND		B27	MCB_RD/nWR

Table 6-23 Agilent test header J22 pinout

6.12 Resets JP12 and JP7

JP12 and JP7 are two-pin 0.100" headers which route to the front-panel reset switch. When the front panel reset switch is pressed, both pins of JP12 and JP7 are grounded. Normally, a short wire routes from this header to the reset pin of the PC/104+ CPU module. JP7 is for the PC/104+ CPU one the PCMC and JP12 is for the PC/104+ CPU on the FORM.

6.13 USB Port

This is a USB standard port, routed by cable directly to the CMIB PC/104+ CPU module header. Refer to industry-standard pinout and the User Manual for more information.

6.14 Front Panel LEDs

All front-panel LEDs are labeled and their association and function is self-evident.

6.15 CMIB PC/104+ CPU Module

The PC/104+ CPU module meets industry-standard requirement for board-stack pluggable connectors, outside dimensions, and hole mounting locations. However, any non-standard connectors can be anywhere and any orientation. This makes it possible, but not without difficulty, in using other manufacturers' PC/014+ CPU modules as replacements, and so replacement manufacturer's modules must be carefully chosen.

This section contains information on the location and pinouts of non-PC/104+ standard connectors on the Kontron MOPSlcdLX module, which are used by the board, or which are used for low-level CPU setup and debug functions.

A cartoon graphic of the Kontron CPU module is shown below with connector names, locations, and pin-1 designations.

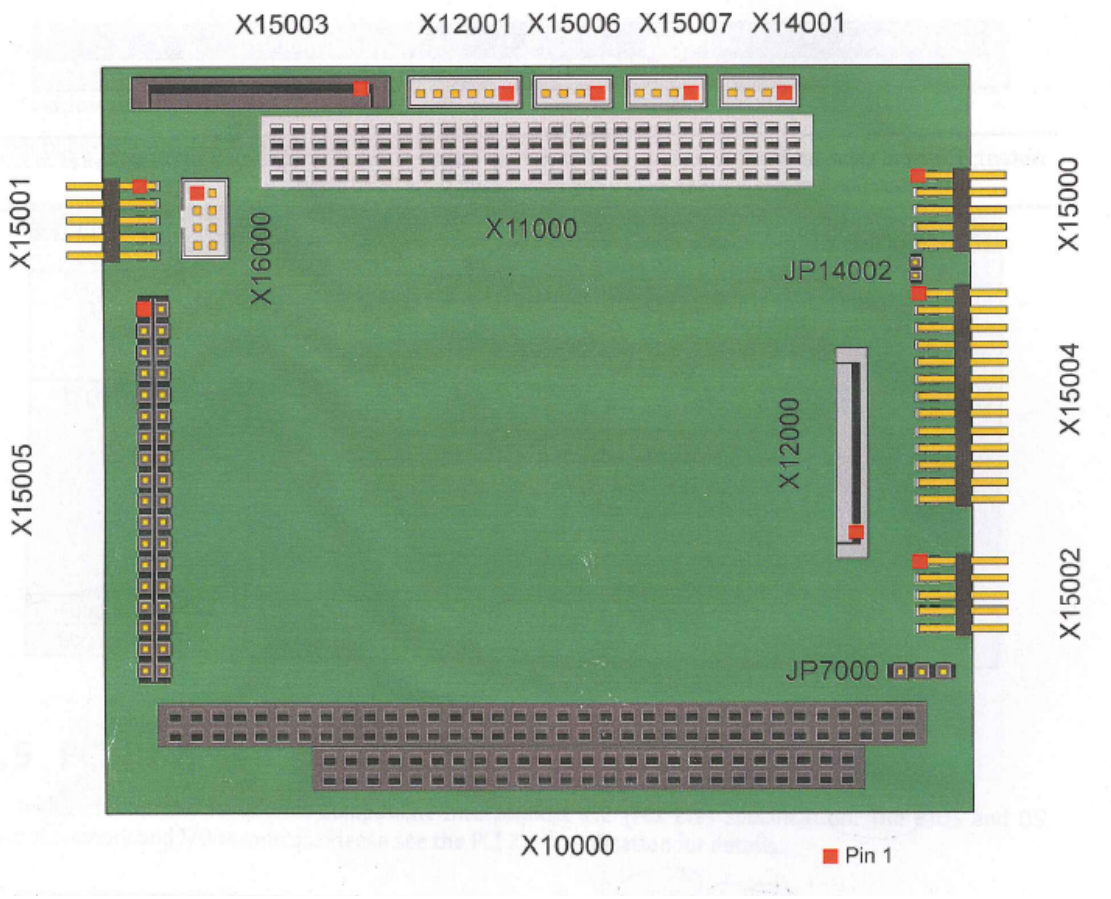

Figure 6-21 Kontron MOPSlcdLX layout showing connector locations and names

Connector **X16000** is the 100Base-T Ethernet connector (2 mm, 8 pos, Berg 89361-144 or compatible), which routes via a conversion cable to the front-panel RJ-45 connector.

Connector **X12001** is the CRT monitor connector (1.25 mm, 6 position, Molex 51021-0600 or compatible) and is useful for looking at low-level CPU boot states.

Connector **X15002** is the keyboard connector (0.100”, 10 position, AMP 1-215882-0 or compatible) for an AT keyboard, or a PS/2 keyboard.

Connector **X15006** is the USB connector (1.25 mm, 4 position, Molex 51021-0400 or compatible) used for the front-panel USB port.

Pin/Con	X16000 (Eth)	X12001 (CRT)	X15002 (kbrd)	X15006 (USB)
1	TXD+	RED	SPEAKER	VCC
2	TXD-	GRN	GND	USB00
3	RXD+	BLU	/RESIN	USB01
4	SHLDGND	GND	/KBLOCK	GND
5	SHLDGND	VSYNC	KBDAT	
6	RXD-	HSYNC	KBCLK	
7	SHLDGND		GND	
8	SHLDGND		VCC	
9			BATT	
10			PWRGOOD	

Table 6-24 Kontron PC/104+ CPU peripheral connector pinouts.

Refer to the Kontron MOPSlcdLX User's Guide for more detailed information on the board and other connector pinouts.

Additionally, note that the wizards at Kontron decided not to route the X11000 (PC/104+) connector's standard +5V pins to the +5V power supply rail on the board. The +5V pins on this connector are the mechanism the PCMC card uses to deliver +5V to the CPU module. As such, a workaround was developed to route X11000 +5V from the PCMC to the Kontron power connector (not shown in Figure 6-). Refer to ECO-A25300N0016-25140 for more information. The X11000 connector has press-fit connectivity issues if it is the black connector (refer to ECO-A25300N0047-CPU50_1_SOLDER) and must be soldered. Finally, the X11000 pins can shed gold hairs; the connector should be inspected and cleaned of these hairs every mating cycle.

6.16 XML Protocol

The full XML schema for communicating with the Baseline Board can be found in:

http://www.aoc.nrao.edu/asg/widar/schemata/cmib/stationBoard/stationBoard.html

7 Monitor and Control

This section defines how the module is controlled. For a circuit board, it would define addressing, memory maps, and register bits and their functions.

7.1 Station Board Memory Map

The 16-bit address is divided into 2 groups of 8 bits. The most significant 8 bits is the address of the FPGA as shown in the table below. The least significant 8 bits are used to access the individual registers in each FPGA as shown further below.

MS ADDR	FPGA on Station Board	Program
0x00	MCB - MCB FPGA	1
0x01	CFG - Configuration FPGA	0
0x02	WBC - Wide Band Correlator FPGA	5
0x03	INP - Input FPGA	4
0x04	DLYA - Delay Module FPGA A	2
0x05	DLYB - Delay Module FPGA B	3
0x06	TIM - Timing FPGA	6
0x07	OUTA - Output FPGA A	7
0x08	OUTB - Output FPGA B	8
0x09	VSIA - VLBI Standard Interface FPGA A	9
0x0A	VSIB - VLBI Standard Interface FPGA B	9
0x0B	FIRA0 - Filter Bank A FPGA 0	10
0x0C	FIRA1 - Filter Bank A FPGA 1	10
0x0D	FIRA2 - Filter Bank A FPGA 2	10
0x0E	FIRA3 - Filter Bank A FPGA 3	10
0x0F	FIRA4 - Filter Bank A FPGA 4	10
0x10	FIRA5 - Filter Bank A FPGA 5	10
0x11	FIRA6 - Filter Bank A FPGA 6	10
0x12	FIRA7 - Filter Bank A FPGA 7	10
0x13	FIRA8 - Filter Bank A FPGA 8	10
0x14	FIRA9 - Filter Bank A FPGA 9	10

MS ADDR	FPGA on Station Board	Program
0x15	FIRA10 - Filter Bank A FPGA 10	10
0x16	FIRA11 - Filter Bank A FPGA 11	10
0x17	FIRA12 - Filter Bank A FPGA 12	10
0x18	FIRA13 - Filter Bank A FPGA 13	10
0x19	FIRA14 - Filter Bank A FPGA 14	10
0x1A	FIRA15 - Filter Bank A FPGA 15	10
0x1B	FIRA16 - Filter Bank A FPGA 16	10
0x1C	FIRA17 - Filter Bank A FPGA 17	10
0x1D	FIRB0 - Filter Bank B FPGA 0	11
0x1E	FIRB1 - Filter Bank B FPGA 1	11
0x1F	FIRB2 - Filter Bank B FPGA 2	11
0x20	FIRB3 - Filter Bank B FPGA 3	11
0x21	FIRB4 - Filter Bank B FPGA 4	11
0x22	FIRB5 - Filter Bank B FPGA 5	11
0x23	FIRB6 - Filter Bank B FPGA 6	11
0x24	FIRB7 - Filter Bank B FPGA 7	11
0x25	FIRB8 - Filter Bank B FPGA 8	11
0x26	FIRB9 - Filter Bank B FPGA 9	11
0x27	FIRB10 - Filter Bank B FPGA 10	11
0x28	FIRB11 - Filter Bank B FPGA 11	11
0x29	FIRB12 - Filter Bank B FPGA 12	11
0x2A	FIRB13 - Filter Bank B FPGA 13	11
0x2B	FIRB14 - Filter Bank B FPGA 14	11
0x2C	FIRB15 - Filter Bank B FPGA 15	11
0x2D	FIRB16 - Filter Bank B FPGA 16	11
0x2E	FIRB17 - Filter Bank B FPGA 17	11

Table 7-1 Station Board Memory Map

7.1.1 MCB FPGA Memory Map (MS address bits 00h)

ADDR	MCB Register	Description	Access	Reset
00h	SBID	Station Board ID (rack, crate, slot)	R	
01h	FVR	MCB Fanout FPGA Version/Revision	R	
02h	RBT	MCB Read Back Test	R/W	0000h
03h	CC	MCB Configurations and Control	R/W	0000h
04h	AM	Analog MUX register	R/W	007Ch

Table 7-2 MCB Fanout FPGA memory map

7.1.2 CFG FPGA memory map (MS address bits 01h)

ADDR	CFG Register	Description	Access	Reset
0x00	FVR	CFG Fan-out FPGA Version/Revision	R	
0x01	RBT	CFG Read Back Test	R/W	0x0000
0x02	CC	CFG Configurations and Control	R/W	0x0000
0x03	CD1	CFG Configuration Disable 1	R/W	0x0000
0x04	CD2	CFG Configuration Disable 2	R/W	0x0000
0x05	DONEA1	CFG DONE signals for Group A 1	R	0x0000
0x06	DONEA2	CFG DONE signals for Group A 2	R	0x0000
0x07	DONEB1	CFG DONE signals for Group B 1	R	0x0000
0x08	DONEB2	CFG DONE signals for Group B 2	R	0x0000
0x09	DONE	CFG individual DONE signals	R	0x0000
0x0a	SBSER	CFG Station Board Serial number	R	
0x0b	PWS	CFG Power Status	R	0x0000

Table 7-3 CFG FPGA Memory Map

7.1.3 WBC FPGA Memory Map (MS address bits 02h)

Address	Name	Dir	Bits	Description
0x00	CM_STS	R/W	15:0	Status Register
0x01	CM_CFG	R/W	15:0	Configuration Register
0x02	CM_CTL	R/W	15:0	Control Register
0x03	CM_ERR	R/W	2:0	Error Register
0x04	CM_DEF	R	15:0	Default Register
0x05	CM_DID	R	15:0	Design Identifier
0x06	CM_TST0	R/W	7:0	Address of signal to connect to test port 0
0x07	CM_TST1	R/W	7:0	Address of signal to connect to test port 1
0x08	CM_TST2	R/W	7:0	Address of signal to connect to test port 2
0x09	CM_TST3	R/W	7:0	Address of signal to connect to test port 3
0x10	IO_ESEL_A	R/W	6:0	Error select for wide band A CRC.
0x11	IO_ESEL_B	R/W	6:0	Error select for wide band B CRC.
0x12	IO_DSEL_A	R/W	5:0	Wide band A bit for CRC calculation
0x13	IO_ICRC_A	R/W	3:0	4-bit CRC for selected A input bit
0x14	IO_DSEL_B	R/W	5:0	Wide band B bit for CRC calculation
0x15	IO_ICRC_B	R/W	3:0	4-bit CRC for selected B input bit
0x16	IO_TINT1_A	R/W	15:0	MS time interval data tick to system tick
0x17	IO_TINT0_A	R/W	15:0	LS time interval
0x18	IO_TINT1_B	R/W	15:0	MS time interval data tick to system tick

Address	Name	Dir	Bits	Description
0x19	IO_TINT0_B	R/W	15:0	LS time interval
0x1A	IO_SEED_A	R/W	15:0	Seed for pseudo random bit stream generator A
0x1B	IO_SEED_B	R/W	15:0	Seed for pseudo random bit stream generator B
0x1C	IO_SDLY	R/W	15:0	System tick delay to offset IO_TINT_A/B.
0x1D	IO_OCRC_A	R/W	3:0	4-bit CRC for selected A output bit
0x1E	IO_OCRC_B	R/W	3:0	4-bit CRC for selected B output bit
0x1F	IO_DERR_A	R/W	15:0	Delay error for wideband test pattern generator
0x20	IO_DERR_B	R/W	15:0	Delay error for wideband test pattern generator
0x30	SL_IDEC	R/W	3:0	Input data rate divider
0x31	SL_NBND	R/W	3:0	Number of bands in word – 1
0x32	SL_DBND	R/W	3:0	Lagged band to process – 1
0x33	SL_PBND	R/W	3:0	Prompt band to process – 1
0x34	SL_ODEC	R/W	3:0	Output data rate divider
0x40	DL_LDLY	R/W	14:0	Lag delay
0x41	DL_PLDLY	R	14:0	Previous Lag delay
0x60	XC_NBIT	R/W	2:0	Number of bits in samples– 1
0x61	XC_VCNT1	R	5:0	Valid count [21:16]
0x62	XC_VCNT0	R	15:0	Valid count [15:0]
0x63	XC_PACC2	R	6:0	Product accumulation [38:32]
0x64	XC_PACC1	R	15:0	Product accumulation [32:16]

Address	Name	Dir	Bits	Description
0x65	XC_PACC0	R	15:0	Product accumulation [15:0]

Table 7-4 WBC FPGA Memory Map

7.1.4 INP FPGA Memory Map (MS address bits 03h)

ADDR	INP Register	Description	Access	Reset
0x00	FVR	DM FPGA Version/Revision	R	
0x01	RBT	Read Back Test	R/W	0x0000
0x02	MEMA	MEMory Address	R/W	0x00ff
0x03	CRCFS	CRC FORM Selection	R/W	0x0000
0x04	CRCIS	CRC Input Selection	R/W	0x0000
0x05	CRCOS	CRC Output Selection	R/W	0x0000
0x06	CRCVS	CRC VSI Selection	R/W	0x0000
0x07	DP	Data Path	R/W	0x0000
0x08	IOS	Input/Output Setup	R/W	0x0000
0x09	DCML	DCM Lock	R	0x0000
0x0A	CRCFV	CRC FORM Value	R	0x0000
0x0B	CRCIV	CRC Input Value	R	0x0000
0x0C	CRCVOV	CRC VSI & Output Value	R	0x0000
0x0D	SCC	State Counters Control signals	R/W	0x0000
0x0E	NDWH	Noise Diode Width High	R/W	0x0000
0x0F	NDWL	Noise Diode Width Low	R/W	0x0000
0x10	NDPH	Noise Diode Phase High	R/W	0x0000
0x11	NDPL	Noise Diode Phase Low	R/W	0x0000
0x12	NDRH	Noise Diode Rate High	R/W	0x0000
0x13	NDRL	Noise Diode Rate Low	R/W	0x0000
0x14	NDPCH	Noise Diode Max Count High	R/W	0x0000
0x15	NDPCL	Noise Diode Max Count Low	R/W	0x0000
0x16	ITS	Input Ticks Status	R	0x0000
0x17	PATCH	Port A Tick Counter High	R	0x0000
0x18	PATCL	Port A Tick Counter Low	R	0x0000
0x19	PBTCH	Port B Tick Counter High	R	0x0000
0x1A	PBTCL	Port B Tick Counter Low	R	0x0000
0x1B	PCTCH	Port C Tick Counter High	R	0x0000
0x1C	PCTCL	Port C Tick Counter Low	R	0x0000
0x1D	V0TCH	VSI0 Tick Counter High	R	0x0000

0x1E	V0TCL	VSI0 Tick Counter Low	R	0x0000
0x1F	STDV	System Tick Delay VSI	R/W	0x0000
0x20	V1TCH	VSI1 Tick Counter High	R	0x0000
0x21	V1TCL	VSI1 Tick Counter Low	R	0x0000
0x22	STDF	System Tick Delay FORM	R/W	0x0000
0x23	IPD	Input Ports Delay	R/W	0x0000
0x24	BSL1	Band Selection register 1	R/W	0x0000
0x25	BSL2	Band Selection register 2	R/W	0x0000
0x26	BSL3	Band Selection register 3	R/W	0x0000
0x27	BSL4	Band Selection register 4	R/W	0x0000
0x28	SSL1	State Selection register 1	R/W	0x0000
0x29	SSL2	State Selection register 2	R/W	0x0000
0x2A	SSL3	State Selection register 3	R/W	0x0000
0x2B	SSL4	State Selection register 4	R/W	0x0000
0x2C	8SSL1	8-bits mode State Selection register 1	R/W	0x0000
0x2D	8SSL2	8-bits mode State Selection register 2	R/W	0x0000
0x2E	8SSL3	8-bits mode State Selection register 3	R/W	0x0000
0x2F	8SSL4	8-bits mode State Selection register 4	R/W	0x0000
0x30	SCLB0_6	State Counter Lower Block0 top 6 bits	R	0x0000
0x31	SCLB0_16	State Counter Lower Block0 lower 16 bits	R	0x0000
0x32	SCHB0_6	State Counter Higher Block0 top 6 bits	R	0x0000
0x33	SCHB0_16	State Counter Higher Block0 lower 16 bits	R	0x0000
0x34	SCLB1_6	State Counter Lower Block1 top 6 bits	R	0x0000
0x35	SCLB1_16	State Counter Lower Block1 lower 16 bits	R	0x0000
0x36	SCHB1_6	State Counter Higher Block1 top 6 bits	R	0x0000
0x37	SCHB1_16	State Counter Higher Block1 lower 16 bits	R	0x0000
0x38	SCLB2_6	State Counter Lower Block2 top 6 bits	R	0x0000
0x39	SCLB2_16	State Counter Lower Block2 lower 16 bits	R	0x0000
0x3A	SCHB2_6	State Counter Higher Block2 top 6 bits	R	0x0000
0x3B	SCHB2_16	State Counter Higher Block2 lower 16 bits	R	0x0000
0x3C	SCLB3_6	State Counter Lower Block3 top 6 bits	R	0x0000
0x3D	SCLB3_16	State Counter Lower Block3 lower 16 bits	R	0x0000
0x3E	SCHB3_6	State Counter Higher Block3 top 6 bits	R	0x0000

0x3F	SCHB3_16	State Counter Higher Block3 lower 16 bits	R	0x0000
0x40	SCLB4_6	State Counter Lower Block4 top 6 bits	R	0x0000
0x41	SCLB4_16	State Counter Lower Block4 lower 16 bits	R	0x0000
0x42	SCHB4_6	State Counter Higher Block4 top 6 bits	R	0x0000
0x43	SCHB4_16	State Counter Higher Block4 lower 16 bits	R	0x0000
0x44	SCLB5_6	State Counter Lower Block5 top 6 bits	R	0x0000
0x45	SCLB5_16	State Counter Lower Block5 lower 16 bits	R	0x0000
0x46	SCHB5_6	State Counter Higher Block5 top 6 bits	R	0x0000
0x47	SCHB5_16	State Counter Higher Block5 lower 16 bits	R	0x0000
0x48	SCLB6_6	State Counter Lower Block6 top 6 bits	R	0x0000
0x49	SCLB6_16	State Counter Lower Block6 lower 16 bits	R	0x0000
0x4A	SCHB6_6	State Counter Higher Block6 top 6 bits	R	0x0000
0x4B	SCHB6_16	State Counter Higher Block6 lower 16 bits	R	0x0000
0x4C	SCLB7_6	State Counter Lower Block7 top 6 bits	R	0x0000
0x4D	SCLB7_16	State Counter Lower Block7 lower 16 bits	R	0x0000
0x4E	SCHB7_6	State Counter Higher Block7 top 6 bits	R	0x0000
0x4F	SCHB7_16	State Counter Higher Block7 lower 16 bits	R	0x0000
0x50	TEST_0	Test Port 0 signal select	R/W	0x0000
0x51	TEST_1	Test Port 1 signal select	R/W	0x0000
0x52	TEST_2	Test Port 2 signal select	R/W	0x0000
0x53	TEST_3	Test Port 3 signal select	R/W	0x0000
0x54	NDONH	Noise Diode ON count [21:16]	R	0x0000
0x55	NDONL	Noise Diode ON count [15:0]	R	0x0000
0x56	NDOFH	Noise Diode OFF count [21:16]	R	0x0000
0x57	NDOFL	Noise Diode OFF count [15:0]	R	0x0000
0x58	TCNTRLA	Wideband Test Signal Generator Control	R/W	0x0000
0x59	TCNTRLB	Wideband Test Signal Generator Control	R/W	0x0000
0x5A	TSEEDA	Wideband Test Signal Generator Seed	R/W	0x1357
0x5B	TSEEDB	Wideband Test Signal Generator Seed	R/W	0x1357
0x5C	CPSCTL0	Clock Phase Shift Control (data)	R/W	0x0000
0x5D	CPSCTL1	Clock Phase Shift Control (FORM/system)	R/W	0x0000

Table 7-5 INP FPGA Memory Map

7.1.5 DLY FPGA Memory Map (MS address bits 04h and 05h)

ADDR	DLY Register	Description	Access	Reset
00h	FVR	DM FPGA Version/Revision	R	0001h
01h	RBT	Read Back Test	R/W	0000h
02h	CC	Configurations and Control	R/W	0000h
03h	STAT	Status	R	0000h
04h	PEB0	Parity Error Bank 0	R	0000h
05h	PEB1	Parity Error Bank 1	R	0000h
06h	MDL	Measured Delay, Low part	R	0000h
07h	MDH	Measured Delay, High part	R	0000h
08h	PDL	Pointers Delay, Low part	R	0000h
09h	PDH	Pointers Delay, High part	R	0000h
0Ah	SFD	SDRAM FIFO Depth	R	0000h
0Bh	LFS	Load FIFO Status	R	0000h
0Ch	TD	Test Data	R/W	0000h
0Dh	STD	System Tick Delay	R/W	0000h
0Eh	CRCC	CRC Control	R/W	0000h
0Fh	CRCO	CRC Outputs	R	0000h
10h	BID	Board ID	R	????h
11h	TPC12	Test Port Control 1 and 2	R/W	0000h
12h	TPC34	Test Port Control 3 and 4	R/W	0000h
13h	DD1	Delay Data register 1	R/W	0000h
14h	DD2	Delay Data register 2	R/W	0000h
15h	DD3	Delay Data register 3	R/W	0000h
16h	DD4	Delay Data register 4	R/W	0000h
17h	DD5	Delay Data register 5	R/W	0000h
18h	DD6	Delay Data register 6	R/W	0000h
19h	SWROA	SDRAM Write Roll Over Address	R/W	7FFFh
1Ah	SRROA	SDRAM Read Roll Over Address	R/W	7FFFh
1Bh	SWA	SDRAM Write Address	R	0000h
1Ch	SRA	SDRAM Read Address	R	0000h
1Dh	ITL	Input Ticks Low	R	0000h

ADDR	DLY Register	Description	Access	Reset
1Eh	ITH	Input Ticks High register	R	0000h

Table 7-6 DLY FPGA Memory Map

7.1.6 TIM FPGA Memory Map (MS address bits 06h)

TIM Register	Access	Address	Description
DESIGNID	R	00h	Design ID
TESTPIN0	R/W	01h	Test Pin Register 0 and 1
TESTPIN1	R/W	02h	Test Pin Register 2 and 3
PECRCSEL	R/W	03h	PERR Input CRC Select (A and B)
PECRCA0	R	04h	PERR A Inputs 0-3 CRCs
PECRCA1	R	05h	PERR A Inputs 4-7 CRCs
PECRCA2	R	06h	PERR A Inputs 8-11 CRCs
PECRCA3	R	07h	PERR A Inputs 12-15 CRCs
PECRCA4	R	08h	PERR A Inputs 16-17 CRCs
PECRCB0	R	09h	PERR B Inputs 0-3 CRCs
PECRCB1	R	0Ah	PERR B Inputs 4-7 CRCs
PECRCB2	R	0Bh	PERR B Inputs 8-11 CRCs
PECRCB3	R	0Ch	PERR B Inputs 12-15 CRCs
PECRCB4	R	0Dh	PERR B Inputs 16-17 CRCs
PTICKSEL	R/W	0Eh	PTICK Select (A and B)
PTICKCNTA0	R	0Fh	PTICK Count A [15:0]
PTICKCNTA1	R	10h	PTICK Count A [20:16]
PTICKCNTB0	R	11h	PTICK Count B [15:0]
PTICKCNTB1	R	12h	PTICK Count B [20:16]
PPSDLY0	R/W	13h	PPS Delay [15:0]
PPSDLY1	R/W	14h	PPS Delay [26:16]
SYSDLY	R/W	15h	System Delay [15:0]
INTDLY	R/W	16h	Interrupt Delay [15:0]
TCSTAMP0	R/W	17h	Seconds since EPOCH [15:0]
TCSTAMP1	R/W	18h	Seconds since EPOCH [31:16]
TCSTAMP2	R/W	19h	T, C, EPOCH, TCOUNT[9:0]
PPSCODE	R	1Ah	Received PPS and hop counts
STATUS0	R/W	1Bh	Status 0
STATUS1	R/W	1Ch	Status 1
STATUS2	R/W	1Dh	Status 2

TIM Register	Access	Address	Description
STATUS3	R/W	1Eh	Status 3
STATUS4	R/W	1Fh	Status 4
CONTROL	R/W	20h	Control
DTWADDR	R	21h	DUMPTRIG Buffer Write Address
DTRADDR	R	22h	DUMPTRIG Buffer Read Address
DTTRIGCNT0	R	23h	DUMPTRIG TRIG Count [15:0]
DTTRIGCNT1	R	24h	DUMPTRIG TRIG Count [20:16]
PESWCFG0	R/W	25h	Phase Error Switch 0 Configuration
PESWCFG1	R/W	26h	Phase Error Switch 1 Configuration
PESWCFG2	R/W	27h	Phase Error Switch 2 Configuration
PESWCFG3	R/W	28h	Phase Error Switch 3 Configuration
PESWCFG4	R/W	29h	Phase Error Switch 4 Configuration
PESWCFG5	R/W	2Ah	Phase Error Switch 5 Configuration
PESWCFG6	R/W	2Bh	Phase Error Switch 6 Configuration
PESWCFG7	R/W	2Ch	Phase Error Switch 7 Configuration
PESWCFG8	R/W	2Dh	Phase Error Switch 8 Configuration
PESWCFG9	R/W	2Eh	Phase Error Switch 9 Configuration
PESWCFG10	R/W	2Fh	Phase Error Switch 10 Configuration
PESWCFG11	R/W	30h	Phase Error Switch 11 Configuration
PESWCFG12	R/W	31h	Phase Error Switch 12 Configuration
PESWCFG13	R/W	32h	Phase Error Switch 13 Configuration
PESWCFG14	R/W	33h	Phase Error Switch 14 Configuration
PESWCFG15	R/W	34h	Phase Error Switch 15 Configuration
PESWCFG16	R/W	35h	Phase Error Switch 16 Configuration
PESWCFG17	R/W	36h	Phase Error Switch 17 Configuration
PMPORT	R/W	37h	PHASEMOD Memory Port
DTPORT	R/W	38h	DUMPTRIG Memory Port
CLKSELA	R/W	39h	Select DDR clock for PERR A 0-15
CLKSELB	R/W	3Ah	Select DDR clock for PERR B 0-15
CLKSELABT	R/W	3Bh	Select DDR clock for TO, PERR 16-17
PLEN0	R/W	3Ch	PPS length in 128 MHz clocks [15:0]
PLEN1	R/W	3Dh	PPS length in 128 MHz clocks [26:16]

TIM Register	Access	Address	Description
TLEN0	R/W	3Eh	TICK length in 128 MHz clocks [15:0]
TLEN1	R/W	3Fh	TICK length in 128 MHz clocks [20:16]
MCBTEST	R/W	40h	16 bit register for testing MCB interface.
INTRIND	R/W	41h	Poor man's interrupt indicator.
TIMER0	R/W	42h	TIMER count in microsecond [15:0]
TIMER1	R/W	43h	TIMER count in microsecond [31:16]
PMWADDR	R	44h	PHASEMOD Buffer Write Address
PMRADDR	R	45h	PHASEMOD Buffer Read Address
TCOUNT	R	46h	Tick Counter
TPESEL	R/W	47h	Tick Phase Error Select
TPEOUT	R	48h	Tick Phase Error Output
TIMOUTA0	R	49h	OUTA/TIM timing difference [15:0]
TIMOUTA1	R	4Ah	OUTA/TIM timing difference [21:16]
TIMOUTB0	R	4Bh	OUTB/TIM timing difference [15:0]
TIMOUTB1	R	4Ch	OUTB/TIM timing difference [21:16]
DTSELECT	R/W	4Dh	DUMPTRIG Generator select.
DTSWITCH0	R/W	4Eh	DUMPTRIG Generator switch 0 to3.
DTSWITCH1	R/W	4Fh	DUMPTRIG Generator switch 4 to 7.
DTSWITCH2	R/W	50h	DUMPTRIG Generator switch 8 to 11.
DTSWITCH3	R/W	51h	DUMPTRIG Generator switch 12 to 15.
DTSWITCH4	R/W	52h	DUMPTRIG Generator switch 16 to 17.
PCSTATE	R/W	53h	PPSCODE status bits and selections.
CSRR	R/W	54h	Chopper Seed Root Register.
PPSCNT0	R/W	55h	PPS Time Interval[15:0].
PPSCNT1	R/W	56h	PPS Time Interval[26:16].
XBADDR	R/W	57h	Address for Crossbar Board command.
XBDATA	R/W	58h	Data for Crossbar Board command.

TIM Register	Access	Address	Description
PPSCODE_A	R	59h	Received second and hop count from A
PPSCODE_B	R	5Ah	Received second and hop count from B
TOGCOUNT_A	R	5Bh	A clock toggle count (test)
TOGCOUNT_B	R	5Ch	B clock toggle count (test)
TOGCOUNT_S	R	5Dh	S clock toggle count (test)
TOGCOUNT_X	R	5Eh	X clock toggle count (test)
PCCTLSTS	R	5Fh	PPSCODE control/status (test)
SYSDLY_MS	R	60h	System Delay [16]

Table 7-7 TIM FPGA Memory Map

7.1.7 OUT FPGA Memory Map (MS address bits 07h and 08h)

ADDR	OUT Register	Description	Access	Reset
00h	FVR	DM FPGA Version/Revision	R	0001h
01h	RBT	Read Back Test register	R/W	0000h
02h	MC	Main Control register	R/W	0000h
03h	STAT	Status register	R	0000h
04h	PWL	Pulse Width Low register	R/W	0000h
05h	PWH	Pulse Width High register	R/W	0000h
06h	PMPL	Pulse Mode Period Low register	R/W	0000h
07h	PMPH	Pulse Mode Period High register	R/W	0000h
08h	MCBG	MCB Gate register	R/W	0000h
09h	RM	Radar Mode register	R/W	0000h
0Ah	RAD	Radar Data register	R	0000h
0Bh	RDRP	Radar Data Read Pointer	R	0000h
0Ch	IPL	Input Ports Low register	R/W	0000h
0Dh	IPH	Input Ports High register	R/W	0000h
0Eh	ITCL	Input Tick Counter Low register	R	0000h
0Fh	ITCH	Input Tick Counter High register	R	0000h
10h	CRCIS1	CRC Input Selection 1 register	R/W	0000h
11h	CRCIS2	CRC Input Selection 2 register	R/W	0000h
12h	CRCIS3	CRC Input Selection 3 register	R/W	0000h
13h	CRCOS1	CRC Output Selection 1 register	R/W	0000h
14h	CRCOS2	CRC Output Selection 2 register	R/W	0000h
15h	CRCOS3	CRC Output Selection 3 register	R/W	0000h
16h	ERFO1	Error Force 1 register	R/W	0000h
17h	ERFO2	Error Force 2 register	R/W	0000h
18h	OSWS1	Output Switch Select 1 register	R/W	0000h
19h	OSWS2	Output Switch Select 2 register	R/W	0000h
1Ah	OSWS3	Output Switch Select 3 register	R/W	0000h
1Bh	OSWS4	Output Switch Select 4 register	R/W	0000h
1Ch	OSWS5	Output Switch Select 5 register	R/W	0000h
1Dh	OSWS6	Output Switch Select 6 register	R/W	0000h

ADDR	OUT Register	Description	Access	Reset
1Eh	CRCIV1	CRC Input Value 1. Register	R	0000h
1Fh	CRCIV2	CRC Input Value 2. Register	R	0000h
20h	CRCIV3	CRC Input Value 3. Register	R	0000h
21h	CRCIV4	CRC Input Value 4. Register	R	0000h
22h	CRCIV5	CRC Input Value 5. Register	R	0000h
23h	CRCOV1	CRC Output Value 1. Register	R	0000h
24h	CRCOV2	CRC Output Value 2. Register	R	0000h
25h	CRCOV3	CRC Output Value 3. Register	R	0000h
26h	CRCOV4	CRC Output Value 4. Register	R	0000h
27h	CRCOV5	CRC Output Value 5. Register	R	0000h
28h	DI0	Data Info 0. Register	R/W	0000h
29h	DI1	Data Info 1. Register	R/W	0000h
2ah	DI2	Data Info 2. Register	R/W	0000h
2bh	DI3	Data Info 3. Register	R/W	0000h
2ch	DI4	Data Info 4. Register	R/W	0000h
2dh	DI5	Data Info 5. Register	R/W	0000h
2eh	DI6	Data Info 6. Register	R/W	0000h
2fh	DI7	Data Info 7. Register	R/W	0000h
30h	DI8	Data Info 8. Register	R/W	0000h
31h	DI9	Data Info 9. Register	R/W	0000h
32h	DI10	Data Info 10. Register	R/W	0000h
33h	DI11	Data Info 11. Register	R/W	0000h
34h	DI12	Data Info 12. Register	R/W	0000h
35h	DI13	Data Info 13. Register	R/W	0000h
36h	DI14	Data Info 14. Register	R/W	0000h
37h	DI15	Data Info 15. Register	R/W	0000h
38h	DI16	Data Info 16. Register	R/W	0000h
39h	DI17	Data Info 17. Register	R/W	0000h
3Ah	PL0	Phase Low 0. Register	R/W	0000h
3Bh	PH0	Phase High 0. Register	R/W	0000h
3Ch	PL1	Phase Low 1. Register	R/W	0000h
3Dh	PH1	Phase High 1. Register	R/W	0000h

ADDR	OUT Register	Description	Access	Reset
3Eh	PL2	Phase Low 2. Register	R/W	0000h
3Fh	PH2	Phase High 2. Register	R/W	0000h
40h	PL3	Phase Low 3. Register	R/W	0000h
41h	PH3	Phase High 3. Register	R/W	0000h
42h	PL4	Phase Low 4. Register	R/W	0000h
43h	PH4	Phase High 4. Register	R/W	0000h
44h	PL5	Phase Low 5. Register	R/W	0000h
45h	PH5	Phase High 5. Register	R/W	0000h
46h	PL6	Phase Low 6. Register	R/W	0000h
47h	PH6	Phase High 6. Register	R/W	0000h
48h	PL7	Phase Low 7. Register	R/W	0000h
49h	PH7	Phase High 7. Register	R/W	0000h
4Ah	PL8	Phase Low 8. Register	R/W	0000h
4Bh	PH8	Phase High 8. Register	R/W	0000h
4Ch	PL9	Phase Low 9. Register	R/W	0000h
4Dh	PH9	Phase High 9. Register	R/W	0000h
4Eh	PL10	Phase Low 10. Register	R/W	0000h
4Fh	PH110	Phase High 10. Register	R/W	0000h
50h	PL11	Phase Low 11. Register	R/W	0000h
51h	PH11	Phase High 11. Register	R/W	0000h
52h	PL12	Phase Low 12. Register	R/W	0000h
53h	PH12	Phase High 12. Register	R/W	0000h
54h	PL13	Phase Low 13. Register	R/W	0000h
55h	PH13	Phase High 13. Register	R/W	0000h
56h	PL14	Phase Low 14. Register	R/W	0000h
57h	PH14	Phase High 14. Register	R/W	0000h
58h	PL15	Phase Low 15. Register	R/W	0000h
59h	PH15	Phase High 15. Register	R/W	0000h
5Ah	PL16	Phase Low 16. Register	R/W	0000h
5Bh	PH16	Phase High 16. Register	R/W	0000h
5Ch	PL17	Phase Low 17. Register	R/W	0000h
5Dh	PH17	Phase High 17. Register	R/W	0000h

ADDR	OUT Register	Description	Access	Reset
5Eh	STDR	System Tick Delay Register	R/W	0000h
5Fh	CSRR	Chopper Seed Root Register	R/W	0000h
60h	STDR_MS	System Tick Delay Register – MS bits	R/W	0000h

Table 7-8 OUT FPGA Memory Map

7.1.8 VSI FPGA Memory Map (MS address bits 09h and 0Ah)

Address	Name	Dir	Bits	Description
0x00	CM_STS	R/W	15:0	Status Register
0x01	CM_CFG	R/W	15:0	Configuration Register
0x02	CM_CTL	R/W	15:0	Control Register
0x03	CM_ERR	R/W	15:0	Error Register
0x04	CM_DEF	R/W	15:0	Default Register
0x05	CM_DID	R	15:0	Design ID
0x06	CM_TST0	R/W	7:0	Address of signal to connect to test port 0
0x07	CM_TST1	R/W	7:0	Address of signal to connect to test port 1
0x08	CM_TST2	R/W	7:0	Address of signal to connect to test port 2
0x09	CM_TST3	R/W	7:0	Address of signal to connect to test port 3
0x10	IO_NSEL0	R/W	15:0	Select DDR clock edge for NB inputs [15:0]
0x11	IO_NSEL1	R/W	1:0	Select DDR clock edge for NB inputs [17:16]
0x12	IO_VINT1	R	5:0	MS VSI time interval count
0x13	IO_VINT0	R	15:0	LS VSI time interval count
0x14	IO_STDLY	R/W	15:0	System Tick Delay for IO_TINT
0x15-1B				Not used
0x1C	IO_ICER0	R	15:0	Input data clock error for inputs [15:0]
0x1D	IO_ICER1	R	1:0	Input data clock error for inputs [17:16]
0x1E	IO_TSEL	R/W	4:0	Input to select for time interval counter
0x1F	IO_TINT1	R	5:0	MS time interval count
0x20	IO_TINT0	R	15:0	LS time interval count
0x21	VS_VSEL	R/W	5:0	Select bit stream for CRC checking and read CRCs
0x22	NB_DSEL	R/W	1:0	Select bit stream for CRC calculation
0x23	NB_CRC0	R/W	15:0	4-bit CRC for inputs 0 to 3
0x24	NB_CRC1	R/W	15:0	4-bit CRC for inputs 4 to 7
0x25	NB_CRC2	R/W	15:0	4-bit CRC for inputs 8 to 11
0x26	NB_CRC3	R/W	15:0	4-bit CRC for inputs 12 to 15
0x27	NB_CRC4	R/W	7:0	4-bit CRC for inputs 16 and 17
0x28	TC_TLEN1	R/W	4:0	MS number of 128 MHz clocks per tick minus one
0x29	TC_TLEN0	R/W	15:0	LS number of 128 MHz clocks per tick minus one
0x2A	TC_PLEN	R/W	6:0	Number of ticks per pps minus one

Address	Name	Dir	Bits	Description
0x2B	VD_DSEL	R/W	5:0	Select bit stream for CRC calculation
0x2C	VD_CRC	R/W	3:0	4-bit CRC
0x30	VD_ESEL	R/W	5:0	Error select for VLBI output CRC.
0x31	VS_ESEL	R/W	6:0	Error select for VSI output CRC.
0x32	CM_SEED	R/W	15:0	Seed for all pseudo random bit stream generators.
0x33	TC_HOPC	R/W	7:0	Hop count for test PPSCODE generator.
0x34	TC_SECS	R/W	5:0	Set seconds in test PPSCODE generator.

Table 7-9 VSI FPGA Memory Map

7.1.9 FIR Memory Map (MS address bits 0Bh to 2Eh)

ADDR	FIR Name	Dir	Bits	Description
0x00	CM_STS	R/W	15:0	Status Register
0x01	CM_CFG	R/W	15:0	Configuration Register
0x02	CM_CTL	R/W	15:0	Control Register
0x03	CM_ERR	R/W	15:0	Error Register
0x04	CM_DEF	R/W	15:0	Default Register
0x05	CM_DID	R	15:0	Design identifier
0x06	CM_TST0	R/W	7:0	Address of signal to connect to test port 0
0x07	CM_TST1	R/W	7:0	Address of signal to connect to test port 1
0x08	CM_TST2	R/W	7:0	Address of signal to connect to test port 2
0x09	CM_TST3	R/W	7:0	Address of signal to connect to test port 3
0x10	IO_ESEL	R/W	15:0	Select input data bit for CRC error
0x11	IO_DSEL	R/W	5:0	Select input data bit for CRC calculation
0x12	IO_CRC	R	3:0	4-bit CRC for selected input bit
0x13	IO_SDLY	R/W	15:0	System tick delay to time interval counter.
0x14	IO_TINT1	R/W	5:0	MS time interval count
0x15	IO_TINT0	R/W	15:0	LS time interval count
0x16	IO_SID	R/W	15:0	SID from MCB FPGA
0x20	D1_DDEC	R/W	3:0	Data input rate
0x21	D1_DMUX	R/W	3:0	Demux Factor–1
0x22	D1_DLY2	R/W	15:0	Delay [47:32]
0x23	D1_DLY1	R/W	15:0	Delay [31:16]
0x24	D1_DLY0	R/W	15:0	Delay [15:0]
0x25	D1_DLYR1	R/W	15:0	Delay rate [31:16]
0x26	D1_DLYR0	R/W	15:0	Delay rate [15:0]
0x27	D1_DEPE	R/W	15:0	Delay error to phase error factor
0x28	D1_TDLY	R/W	12:0	Tick delay
0x29	D1_DERR	R	15:0	Delay error before model saved at tick
0x2A	D1_PERR	R	15:0	Phase error after model saved at tick
0x2B	D1_ODLY2	R	15:0	Output Delay [47:32]
0x2C	D1_ODLY1	R	15:0	Output Delay [31:16]
0x2D	D1_ODLY0	R	15:0	Output Delay [15:0]
0x40	S1_DDEC	R/W	3:0	Data output rate

0x41	S1_XBAR3	R/W	15:0	Crossbar addresses for FIR32 3-0
0x42	S1_XBAR2	R/W	15:0	Crossbar addresses for FIR32 7-4
0x43	S1_XBAR1	R/W	15:0	Crossbar addresses for FIR32 11-8
0x44	S1_XBAR0	R/W	15:0	Crossbar addresses for FIR32 15-12
0x45	S1_CADD	R/W	3:0	Product address
0x46	S1_CVAL	R/W	11:0	Product value
0x47	S1_VLEN	R/W	9:0	Invalid stretch length
0x48	S1_FDLY	R/W	9:0	Filter delay
0x49	S1_SCALE	R/W	15:0	Scale factor
0x4A	S1_FBIT	R/W	3:0	Fractional bit select
0x4B	S1_IDC1	R/W	15:0	DC offset to stage 1 [31:16]
0x4C	S1_IDC0	R/W	15:0	DC offset to stage 1 [15:0]
0x4D	S1_ODC2	R/W	15:0	DC offset from stage 1 [48:32]
0x4E	S1_ODC1	R/W	15:0	DC offset from stage 1 [31:16]
0x4F	S1_ODC0	R/W	15:0	DC offset from stage 1 [15:0]
0x50	S1_VDC1	R/W	6:0	DC valid count from stage 1 [21:16]
0x51	S1_VDC0	R/W	15:0	DC valid count from stage 1 [15:0]
0x60	S2_DDEC	R/W	3:0	Output data rate
0x61	S2_CADD	R/W	3:0	Coefficient address
0x62	S2_CVAL	R/W	15:0	Coefficient value
0x63	S2_VLEN	R/W	9:0	Invalid stretch length
0x64	S2_FDLY	R/W	9:0	Filter delay
0x65	S2_SCALE	R/W	15:0	Scale factor
0x66	S2_MADD	R/W	9:0	Mixer LUT address
0x67	S2_MCOS	R/W	15:0	Mixer COS LUT value
0x68	S2_MSIN	R/W	15:0	Mixer SIN LUT value
0x69	S2_MFAZ1	R/W	15:0	Mixer phase [31:16]
0x6A	S2_MFAZ0	R/W	15:0	Mixer phase [15:0]
0x6B	S2_MFAZR1	R/W	15:0	Mixer phase rate [31:16]
0x6C	S2_MFAZR0	R/W	15:0	Mixer phase rate [15:0]
0x6D	S2_CDEC	R/W	3:0	Filter calculation rate
0x6E	S2_NTAP	R/W	8:0	Number of taps-1
0x6F	S2_WADD	R	9:0	Data RAM write address last tick
0x80	S3_DDEC	R/W	3:0	Data output rate
0x81	S3_CADD	R/W	6:0	Coefficient address

0x82	S3_CVAL	R/W	15:0	Coefficient value
0x83	S3_VLEN	R/W	9:0	Invalid stretch length
0x84	S3_FDLY	R/W	9:0	Filter delay
0x85	S3_SCALE	R/W	15:0	Scale factor
0x86	S3_CDEC	R/W	3:0	Filter calculation rate
0x87	S3_NTAP	R/W	8:0	Number of taps-1
0x88	S3_WADD	R	9:0	Data RAM write address last tick
0xA0	S4_DDEC	R/W	3:0	Data output rate
0xA1	S4_CADD	R/W	8:0	Coefficient address
0xA2	S4_CVAL	R/W	15:0	Coefficient value
0xA3	S4_VLEN	R/W	9:0	Invalid stretch length
0xA4	S4_FDLY	R/W	9:0	Filter delay
0xA5	S4_SCALE	R/W	15:0	Scale factor
0xA6	S4_CDEC	R/W	3:0	Filter calculation rate
0xA7	S4_NTAP	R/W	8:0	Number of taps-1
0xA8	S4_WADD	R	9:0	Data RAM write address last tick
0xC0	FM_DSEL	R/W	3:0	Select signals.
0xC1	FM_VCF1	R	5:0	Valid count [21:16] for noise diode off
0xC2	FM_VCF0	R	15:0	Valid count [15:0] for noise diode off
0xC3	FM_VCN1	R	5:0	Valid count [21:16] for noise diode on
0xC4	FM_VCN0	R	15:0	Valid count [15:0] for noise diode on
0xC5	FM_PWF3	R	3:0	Power [51:48 for noise diode off
0xC6	FM_PWF2	R	15:0	Power [47:32] for noise diode off
0xC7	FM_PWF1	R	15:0	Power [31:16] for noise diode off
0xC8	FM_PWF0	R	15:0	Power [15:0] for noise diode off
0xC9	FM_PWN3	R	3:0	Power [51:48] for noise diode on
0xCA	FM_PWN2	R	15:0	Power [47:32] for noise diode on
0xCB	FM_PWN1	R	15:0	Power [31:16] for noise diode on
0xCC	FM_PWN0	R	15:0	Power [15:0] for noise diode on
0xCD	FM_TADD	R/W	7:0	Tone LUT address
0xCE	FM_TVAL	R/W	15:0	Tone COS [15:8] & SIN [7:0] values
0xCF	FM_TFAZ1	R/W	15:0	Tone model phase [31:16]
0xD0	FM_TFAZ0	R/W	15:0	Tone model phase [15:0]
0xD1	FM_TFAZR1	R/W	15:0	Tone model phase rate [31:16]
0xD2	FM_TFAZR0	R/W	15:0	Tone model phase rate [15:0]

0xD3	FM_TVC1	R	5:0	Tone valid count [21:16]
0xD4	FM_TVC0	R	15:0	Tone valid count [15:0]
0xD5	FM_TCOS2	R	3:0	Tone extractor COS result [35:32]
0xD6	FM_TCOS1	R	15:0	Tone extractor COS result [31:16]
0xD7	FM_TCOS0	R	15:0	Tone extractor COS result [15:0]
0xD8	FM_TSIN2	R	3:0	Tone extractor SIN result [35:32]
0xD9	FM_TSIN1	R	15:0	Tone extractor SIN result [31:16]
0xDA	FM_TSIN0	R	15:0	Tone extractor SIN result [15:0]
0xDB	FM_QSCL	R/W	15:0	Quantizer scaling
0xDC	FM_QCC1	R	5:0	Quantizer clip count [21:16]
0xDD	FM_QCC0	R	15:0	Quantizer clip count [15:0]
0xDE	FM_QBIT	R/W	2:0	Quantized number of bits – 1
0xDF	FM_QST	R/W	7:0	Quantizer output state to count
0xE0	FM_QSTC1	R	5:0	Quantizer state count [21:16]
0xE1	FM_QSTC0	R	15:0	Quantizer state count [15:0]
0xE2	FM_QPW2	R	3:0	Quantized power [35:32]
0xE3	FM_QPW1	R	15:0	Quantized power [31:16]
0xE4	FM_QPW0	R	15:0	Quantized power [15:0]
0xE5	FM_CCNT1	R	5:0	Clip count [21:16]
0xE6	FM_CCNT0	R	15:0	Clip count [15:0]
0xE7	FM_BLEV	R/W	15:0	RFI detection level
0xE8	FM_BLEN	R/W	15:0	RFI invalidation length
0xE9	FM_BCNT1	R	5:0	RFI detection count [21:16]
0xEA	FM_BCNT0	R	15:0	RFI detection count [15:0]
0xEB	FM_IDATA	R	15:0	Primary input data at tick for testing
0xF0	D2_DSEL	R	2:0	Select wire for the three CRCs
0xF1	D2_CRC	R/W	11:0	4-bit CRCs for selected wire
0xF2	D2_ESEL	R/W	15:0	Select wire and enable for CRC error
0xF3	D2_ADLY	R/W	12:0	Output data delay for the A Outputs
0xF4	D2_BDLY	R/W	12:0	Output data delay for the B Outputs
0xF5	D2_CDLY	R/W	12:0	Output perr delay for the C Outputs
0xF6	D2_SEED	R/W	15:0	Seed for pseudo random bit generator.

Table 7-10 FIR FPGA Memory Map

8 Jumper Settings and Board Configurations

8.1 CMIB JTAG BYPASS JP1

The two pins of JP1 should be connected together if the PCMC is not installed and it is desired to do a JTAG test. No such test exists at the moment.

8.2 Thermal Shutdown Bypass JP4

The two pins of JP4 should be connected together if it is desired to bypass the automatic thermal shutdown. This jumper must never be installed for normal operation because it overrides the thermal overload protection and could lead to board self-destruction.

8.3 VSI JTAG BYPASS

These are copper traces on the board and should be cut if the VSI FPGAs are installed (?). No JTAG test exists for boards with the VSI FPGAs installed. Boards with the VSI FPGA installed were JTAG tested before the VSI FPGAs were installed.

8.4 DM JTAG BYPASS JP5 and JP6

The two pins of JP5 should be connected together if it is desired to do a JTAG test without DMA installed. The two pins of JP6 should be connected together if it is desired to do a JTAG test without DMB installed. There are no existing JTAG tests for either of the above cases.

8.5 Board Serial Number Setting

There are 16 pairs of pads located on the non-component side of the board near the middle front designated as R532 to R547. If a resistor is installed the value is ‘1’ and if not installed, the value is ‘0’. The 16 bits are read via the MCG FPGA. R547 (nearest the front of the board) is the LSB.

9 DC and Switching Characteristics

This section contains board-level DC and switching characteristics.

9.1 Power Supply, Control, and Thermal Shutdown

Parameter	Min	Typical	Max
-48 VDC supply voltage	-36 V	-48 V	-58 V
-48 VDC supply current	2 A	11 A	14.7 A
-48 VDC peak voltage transient, at peak surge current of 15.5 A for 1 msec. The power supply can withstand 100 V, 100 msec surges.			-97 V
Total board power dissipation	120 W	480 W	530 W
Input conducted ripple and noise tolerance		(EN61000-4-6 10 V)	
Output conducted EMI (standard LISN)		FCC Class B; peak of 62 dBµV @ SMPS fund. of 486 kHz	
CONTROL voltage V_{IH}	3.5	4.0	5.0
CONTROL voltage V_{IL}		0.8	
CONTROL current		8 mA @ 4V	
CONTROL filter time constant		3.7 msec	
MONITOR voltage V_{OH} (1 k-ohm source impedance)		3.3 V	
MONITOR voltage V_{OL} @ -50 mA		0.55 V	
Thermal shutdown heatsink trip temp	60 C	65 C	70 C
Thermal shutdown heatsink reset temp	45 C	60 C	
PWR connector, current rating per contact. (ERNI 114403 data sheet).		4.7 A	12.6 A (7.3)

Additional notes:

1. The CONTROL pin is in the TOP power connector (**Error! Reference source not found.**), and the MONITOR pin is in the BOTTOM power connector.
2. Reverse voltage protection is provided by the transorbs and 10 A fuses on each power connector; the fuse will blow with reverse voltage applied.

9.2 SMA External Clock In

Parameter	Min	Typical	Max
128 MHz input levels (sine)	-6 dBm	0 dBm	+9 dBm
128 MHz input levels (square) (pk-pk)	200 mV	600 mV	2400 mV
128 MHz input cycle-cycle jitter tolerance (pk-pk)			1 ns
128 MHz input frequency	100 MHz	128 MHz	132 MHz
Termination impedance		50 ohm	

Note: this input is AC-coupled.

9.3 VSI Connectors

All differential inputs are DC coupled. All differential outputs are DC coupled

9.4 Data Connector

All differential outputs are DC? coupled.

9.5 M&C 100Base-T Ethernet Port

The RJ-45 front-panel connector routes directly to the CMIB PC/104+ CPU board. Refer to the CPU board manufacturer's data sheet for information on this port.

9.6 USB Port

The USB front-panel connector routes directly to the CMIB PC/104+ CPU board. Refer to the CPU board manufacturer's data sheet for information on this port.

10 Physical, Environmental and Reliability Specifications

10.1 Station Board Physical Parameters

PCB outside dimensions: 15.748” W x 19.687” H (400 mm x 12U).

Slot width, with front panel and heatsink: 2.40”

Front panel outside dimensions: 2.40” W x 20.83” H

PCB thickness: 0.125”

Weight of heatsink: 7.06 lbs (3.20 kgs).

Refer to the Station Board exploded assembly drawing and related mechanical drawings for more detailed physical information.

Note that there is a 0.100” copper “keep-out boundary” on all PCB layers along the top and bottom edges of the board, to prevent any possibility of PCB copper from shorting out to metal guide rails.

10.2 Environmental Specifications

Minimum operating ambient temperature: 0 ^{o}C, non-condensing.

Maximum operating ambient temperature: +40 ^{o}C. This limit is imposed by chips on the CMIB Kontron PC/104+ CPU module. The board itself, with heatsink attached, can withstand an ambient operating temperature of 50 ^{o}C, with adequate airflow, holding the heatsink temperature at ~60-62 ^{o}C, just below thermal shutdown. Although normally, for reliable operation, the maximum ambient temperature should not exceed 40 ^{o}C, and the measured heatsink temperature should be kept below 50 ^{o}C.

Minimum storage temperature: -10 ^{o}C.

Maximum storage temperature: +85 ^{o}C.

Nominal airflow requirement bottom to top of the board, across all surfaces: 10-15 LFM. The board (via the heatsink-mounted thermostats) and on-board power supplies are thermally protected, and so if inadequate airflow is provided, the board and/or power supplies will shutdown.

Maximum operating altitude: 10,000 ft.

Operating orientation: any.

Humidity: minimum 30%, maximum 60% R.H. For ESD risk minimization.

ESD handling protection: The board must never be handled or placed on any surfaces that are not static-dissipative, with an absolute maximum impedance of 10^{10} ohms (preferably 10^{9} ohms) to earth ground.

Dust and contamination: Should be kept to minimum to avoid possible shorting of fine pitch leads/pins. ISO 14644-1 class 8 is the required air quality specification, which is the correlator room specification requirement (RFS document A25012N0000).

10.3 Reliability Estimates

The most un-reliable components on the boards are likely the ¼-brick DC-DC power supplies. The manufacturer (Artesyn) specs these LQS-series power supplies as having an MTBF of 3.9 Mhrs, according to Telcordia Tech SR-332 standard. A survey of FPGA manufacturers' data indicates that the nominal failure rate is ~50 FITs, or an MTBF of 20 Mhrs. The Correlator Chip ASIC original specification and reliability study indicated a similar failure rate of ~50 FITs. The Telcordia prediction for the Kontron CPU is an MTBF of ~390,000 hours. Total approximate MTBF, including only the power supplies and FPGAs is ~75,000 hours, or 8.5 years, not including any other devices on the board.

The following describes the Baseline Board - the Station Board is considerably simpler.

The correlator system reliability report #1 (A25010N0003, Report #1), based on a mixture of MIL-217B, Telcordia SR-332, and manufacturers' data, indicates an MTBF for the BlB of 56,000 hours or 6.4 years, or rather there is a 60-90% chance that the MTBF is greater than 6.4 years. In the EVLA system with 128 operating boards, therefore, it would not be unexpected to have some sort of Baseline Board failure every ~18 days, if these reliability predictions are approximately correct.

An independent study of the BlB bare PCB (manufactured by Merix) was performed by the contract manufacturer, BreconRidge (now Sanmina-SCI), to test for compliance to IPC6012. The conclusion of the report states:

- *The IPC testing performed by Merix and data demonstrates their PWB manufacturing compliance to IPC 6012.*
- *The Merix boards had acceptable as-received bow and only slightly exceed the twist limit for one out of three PWB's (IPC 2221). This did not cause any issues during SMT assembly.*
- *After SMT assembly, the bow did increase. Whether this will have negative impact will have to be determined at the next level assembly. If this does prove to be an issue, further evaluation of the board design and SMT assembly process will be required.*
- *IST testing (Interconnect Stress Test) was performed on four types of IST coupons which included PTH, via and blind via structures. These coupons use the same drill sizes and PWB stack-up that was used for the Baseline board manufacture. No failures, significant resistance changes or interconnect cracking were found during or after testing. These results demonstrate the robustness of the PWB technology used to manufacture the Baseline boards.*

11 FPGA Pinouts, Programming and Packaging Information

Pinouts, programming and packaging information for all FPGAs on the Station Board can be found in the relevant RFS documents.

12 Trouble Shooting Guide

Document A25204N0002 provides some guidance for trouble shooting the StB that may be built into the software to make sense of multiple errors and determine the real cause.

As one would expect, one error can lead to a number of other errors; therefore, in the following sections, the errors should be dealt with in the order presented. It is assumed that the preceding conditions have been corrected when determining the action to take. Where an error causes bad data (the normal case), the data should be forced invalid using the Output FPGA which allows whole data path invalidation or individual sub-band invalidation. This action is implicit in the sections below but is not always possible so the MCCC must inform post-processing when data is bad.

All errors probably could be integrated by the CMIB over a period of the order of one minute to determine the severity and to prevent flooding of the MCCC. A measure of severity could be the ratio of the number of interrupts with the error divided by the number of interrupts where the error was looked for.

It is important for hardware debugging that some record of the number of specific errors can be extracted from the error database for a given board or module.

Under some circumstances, not all of the Filter FPGAs on the Station Board are needed; therefore, it is possible to substitute a working FPGA for a non-working one. This possibility is not reflected in the following sections.

Abbreviations used:

FPG = PCM, FRM, INP, DLY, WBC, FIR, TIM, OUT, MCB or CFG.
DPx = Data Path 0 or 1
SBy = Sub Band 0 to 17
Wz = Wire 0 to 63, other
DTGx = Dump Trig Generator 0 to 15
TIC = Time Interval Count (or Counter)

12.1 CMIB cannot talk to board.

Condition: The file /proc/bus/pci/devices contains no reference to the PCMC Xilinx PCI Devices (10EE0000, 10EE0001 or 10EE0002). The PCMC FPGA is not programmed.

Action: Replace board or reboot or try to load PCMC PROM and then reboot?

Notifications:

1. Condition detected “PCM not programmed”.
2. Corrective action being taken “PCM programming”.
3. Result of corrective action “Goodbye, Cruel World”.

12.2 FPGA not programmed.

Condition: Cannot write/read to test register after programming attempt.

Action: Reprogram affected FPGAs up to twice(?) more.

Notifications:

1. Condition detected “FPG [DPx [SBy]] not programmed”.
2. Corrective action being taken “FPG [DPx [SBy]] programming”.
3. Result of corrective action “FPG [DPx [SBy]] OK” or “StB replace”.

12.3 Timing FPGA external clocks not toggling.

Condition: None of the input clocks (A, B or X) is toggling. The EVLA has not connected the external 128 MHz clock (X).

Action: No action is possible because the problem is likely outside the Station Board.

Notifications:

1. Condition detected “TIM no external clocks”.

12.4 Timing FPGA time code CRC errors.

Condition: The incoming external time code contains CRC errors.

Action: The automatic mode should have already tried to switch to a good edge and/or time code but go into manual mode and try the various possibilities. The software should be able to fly wheel over occasional occurrences but the internal time will likely be wrong if CRC errors occur too often. The hardware will not try to synchronize to the external PPS whose accompanying data contains CRC errors. If it becomes necessary to remove a Station Board that is supplying downstream boards with time code, it may be better to select the other time code ahead of time manually.

Notifications:

1. Condition detected “TIM TC CRC error”.
2. Corrective action being taken “TIM TC CRC correcting”.
3. Result of corrective action is “TIM TC CRC OK” or “TIM TC CRC error”.

12.5 Timing FPGA software second and tick counts not sequential.

Condition: The second count or the tick count does not progress in order. The second should progress from 0 to 59 and the interrupt count should progress from 0 to 99. A software version of the second count and the tick count incremented by counting 10 millisecond interrupts should always agree with the value of the second in the PPSCODE register and the tick count in the TCOUNT register (once they have been set equal once).

Action: Resynchronize using hardware values.

Notifications:

1. Condition detected “TIM second/tick not in sync”.
2. Corrective action being taken “TIM second/tick synchronizing”.
3. Result of corrective action is “TIM second/tick OK”.

12.6 Timing FPGA time code Hop Count change.

Condition: The hop count accompanying the external time code changes. This condition could result from the shutdown of the Station Board currently supplying the external time code. If the hop count changes legitimately to a new value, the Baseline Board will not be able to cope with the time difference between this board and other boards until PPSDLY is adjusted.

Action: This is a case where integrating the error will result in the loss of more data; therefore, the automatic mode should cope but the post processing still needs to know that the change took place. If the hop count changes then inspect the source of the external time code. If the source has changed while in automatic mode, then this should mean that the original source has gone bad possibly due to the upstream Station Board going bad. The CMIB software has to adjust PPSDLY to account for the new hop count. If the hop count is not stable then we have a bigger problem.

Notifications:

1. Condition detected “TIM hop count change”.
2. Corrective action being taken “TIM hop count adjust”.
3. Result of corrective action is “TIM hop count OK”.

12.7 Timing FPGA external time interval count not constant.

Condition: The time interval counter in the PPSCNT registers is not constant. The Timing FPGA manufactures and sends the board PPS to a number of FPGAs including itself. The PPSCNT register pair measures the time interval between the external time code PPS and the received board PPS. The value includes the delay set in PPSDLY.

Action: No corrective action can be taken because the cause of this condition is likely external to the Station Board.

Notifications:

1. Condition detected “TIM TIC error”.

12.8 Input FPGA external time interval count not constant.

Condition: The time interval counter in the P(A|B|C)TC registers measure the time interval between the board tick/pps and the antenna tick coming from the Deformatter Board or from the VSI FPGAs. The values should be constant.

Action: No action is possible because the problem is probably on the Deformatter Board.

Notifications:

1. Condition detected “INP FRM/VSI TIC error”.

12.9 Input FPGA external time interval counts not equal.

Condition: The time interval counter in the P(A|B|C)TC registers measure the time interval between the board tick/pps and the antenna tick coming from the deformatter. The values should be the same for A, B and C channels. If not corrected, the output will be rubbish because the samples are torn apart.

Action: If the error is persistent, change the number of pipeline stages in the IPD register. The pipeline delays should be the same for all Station Boards; if not, notify the Station Board engineer.

Notifications:

1. Condition detected “INP FRM TIC error.
2. Corrective action being taken “INP FRM TIC adjust”.
3. Result of corrective action is “INP FRM TIC OK”.

12.10 FPGA board clock not locked.

Condition: Individual FPGAs are not locked to the board 128 MHz clock. The output of any FPGA that is not locked to the board clock and the output of any downstream FPGA that uses the output will be bad.

Action: Software reset FPGA and reconfigure or replace Station Board.

Notifications:

1. Condition detected “FPG board clock error”.
2. Corrective action being taken “FPG board clock reset”.
3. Result of corrective action is “FPG board clock OK” or “StB replace”.

12.11 FPGA board pps or tick width error.

Condition: An FPGA reports a board pps and/or tick width error. If width errors are occurring, the data will be affected – possibly causing two lag patterns offset by one lag.

Action: If the condition is persistent, change the system clock edge. It should be the same for all Station Boards; if not, notify the Station Board engineer.

Notifications:

1. Condition detected “FPG board pps/tick width error”.
2. Corrective action being taken “FPG board pps/tick width adjust”.
3. Result of corrective action is “FPG board pps/tick width OK”.

12.12 Output FPGA sample indicator error.

Condition: Output FPGA indicates a "sind" error on one or more of the inputs from the Filter FPGAs. A sample indicator error occurs when the delayed system tick does not coincide with a real sample. Such an error can only occur for sub-band bandwidths less than 128 MHz for 4-bit samples or 64 MHz for 8-bit samples. If this error is present, it is possible for the baselines using the output of the affected FPGA to received no valid data at all – this is particularly true for the narrow bandwidths. For a bandwidth of 31.25 kHz, the sample is present for only one of 4096 256 MHz clocks – the rest of the "samples" are invalid.

Action: This is normally a configuration error and is caused by setting certain delays incorrectly (see next section).

Notifications:

1. Condition detected "OUT DPx SBy sample indicator error".

12.13 Timing and Output FPGAs time interval counts not correct.

Condition: The time interval between the ticks from each of the Output FPGAs and the delayed system tick in the Timing FPGA should be zero (TIMOUTA and TIMOUTB). The values of these intervals is controlled by adjusting the sysTickDelay in each FPGA. In addition, the time interval between the incoming data tick and the delayed system tick should also be zero (with exception – see later). This state is achieved by adjusting the output delays (one for each of Output and Timing FPGAs) in each of the Filter FPGAs and the system tick delay in the Timing and Output FPGAs. The exception is necessary if both wide and narrow sub-bands are desired. In this case the wide bands may not be able to be delayed enough to match the timing of the narrow bands because of the limited delay range in the Filter FPGA output delays and the narrow bands will have a non-zero time interval which must be a multiple of its sample interval. If the data tick to the delayed system tick interval must be set to a multiple of the sample width instead of zero then the time stamp of the downstream lag frames should be altered to reflect this.

Action: An algorithm could be developed to correct the configuration.

Notifications:

1. Condition detected “DPx TIC error”.
2. Corrective action being taken “DPx TIC adjust”.
3. Result of corrective action is “DPx TIC OK”.

12.14 All FPGAs time interval counts not correct.

Condition: Time interval counters do not have the expected value. One time interval counter in the Delay Module measures the delay through the delay line (normally changing) should be equal to the requested delay but all other intervals should be constant. Changes in time interval counter measurements will in all likelihood be reflected in the Baseline Board output with matching changes in lag structure.

Action: Appropriate clock edges can be changed. Clock edges should be the same for all Station Boards; if not, notify the Station Board engineer.

Notifications:

1. Condition detected “FPGA DPx [SBy] TIC error”.
2. Corrective action being taken “FPGA DPx [SBy] TIC adjust”
3. Result of corrective action “FPGA DPx [SBy] TIC OK” or “StB replace”.

12.15 Filter FPGA Fractional Sample error.

Condition: “derr pattern” and or “dfrm phase” status errors occur on some or all of the Filter FPGAs. These errors will cause the fractional sample correction in the Baseline board to be wrong and the high frequencies in the sub-band spectra will have lower signal-to-noise ratios.

Action: If only one Filter FPGA has the problem then another could be substituted. If all the Filter FPGAs in bank x have the error then there is a problem with DMx so if the problem is persistent, reset and reconfigure DMx. The problem could be in the Wide Band Correlator FPGA but this is much less likely, especially if the WBC is showing no errors. The WBC could be changed to check for these errors.

Notifications:

1. Condition detected “FIR DPx SBy FS error” or “DPx FS error”.
2. Corrective action being taken “FIR DPx SBy FS substitute” or “DMx reset”.
3. Result of corrective action is “FIR DPx SBy FS OK” or “FIR DPx SBy FS live with it” or “DMx OK” or “DMx replace”.

12.16 Delay Module FPGA parity errors.

Condition: The Delay FPGA is producing parity error status bits.

Action: Live with it or reset and reconfigure the Delay FPGA depending on the severity. If resetting and reconfiguring does not work, replace the Delay Module. Occasional errors can be tolerated. Parity errors indicate that the data output from the Delay Module is not correct.

Notifications:

1. Condition detected “DMx parity error”.
2. Corrective action being taken “DMx parity repair”.
3. Result of corrective action is “DMx parity OK” or “DMx parity live with it” or “DMx replace”.

12.17 Delay Module FPGA output data valid error.

Condition: The Delay FPGA is producing output data valid status errors. All output data from DPx will be marked invalid under this condition.

Action: If this condition persists, the Delay FPGA must be reset and reconfigured or replaced.

Notifications:

1. Condition detected “DMx Delay valid error”.
2. Corrective action being taken “DMx reset and reconfigure”.
3. Result of corrective action is “DMx OK” or “DMx replace”.

12.18 Delay Module FPGA FIFO error.

Condition: The Delay FPGA reports FIFO error.

Action: The Delay FPGA must be reset and reconfigured. If this action does not cure the condition, then replace the Delay Module. If this condition occurs often then some further FPGA design effort will be required.

Notifications: The output data will be marked invalid under this condition.

1. Condition detected “DMx FIFO error”.
2. Corrective action being taken “DMx reset and reconfigure”.
3. Result of corrective action is “DMx FIFO OK” or “DMx replace”.

12.19 FPGA pairs CRC errors.

Condition: CRC errors on any wire between any two FPGAs. CRC errors all the time will produce bad data. Occasional errors can be tolerated but there should be no errors.

Action: Try changing the corresponding edge. If that works, try the same edge on other boards. If that seems OK include the new edge in the default configuration file. If the initial edge change works but does not work on other boards, notify the Station Board engineer. If the edge change does not work, there is probably a real problem on the board. If the Delay Module is involved, check the connector for bent pins or, on sb0001 to sb0010, check the connector soldering.

Notifications:

1. Condition detected “FPG DPx SBy Wz CRC errors”.
2. Corrective action being taken “FPG DPx SBy Wz CRC adjust”.
3. Result of corrective action is “live with it” or “DMx replace” or “StB replace”.

12.20 Timing FPGA PHASEMOD errors.

Condition: PHASEMOD status errors. This is normally a software error in assembling the Hardware Executable Scripts for the PHASEMOD generators. This condition will result in unpredictable phase models.

Action: Restart writing phase models.

Notifications:

1. Condition detected “TIM PHASEMOD errors”.
2. Corrective action being taken “TIM PHASEMOD restart”.
3. Result of corrective action is “TIM PHASEMOD OK”.

12.21 Timing FPGA DUMPTRIG errors.

Condition: DUMPTRIG status errors on one of the DUMPTRIG generators being used. This condition is normally a software error in assembling the Hardware Executable Scripts for the DUMPTRIG generators. This condition will result in unpredictable correlator dump intervals.

Action: Restart writing dump triggers.

Notifications:

1. Condition detected “TIM DUMPTRIG DTGx errors”.
2. Corrective action being taken “TIM DUMPTRIG DTGx restart”.
3. Result of corrective action is “TIM DUMPTRIG DTGx OK”.

12.22 Filter FPGA stage 2, 3 and 4 write address error.

Condition: The registers Sx_WADD (x = 2, 3,4) are not as expected. This condition will result in unpredictable filtering producing bad data. Stages 2, 3 and 4 (if in use) must have their write addresses (WADD) reset at a tick at least once. After that WADD is predictable and should be checked. The changing WADD is the result of having a buffer length of 1024 which is not integral to the 10 millisecond interval. For further information, see the Programmer's Guide and for an example of calculating the expected address see the "firt" command of the "illegal" software cmib.c).

Action: Reset write address.

Notifications:

1. Condition detected "FIR DPx SBy Sz WADD error".
2. Corrective action being taken "FIR DPx SBy Sz WADD reset".
3. Result of corrective action is "FIR DPx SBy Sz WADD OK".

12.23 Timing FPGA interrupt delay error.

Condition: The interrupt to the CMIB is not delayed enough so that new models are written before the current models are used. This condition is most likely to occur for narrow sub-band bandwidths and for models applied late in the data chain such as the tone extractor model. This condition will result in the wrong model being applied although it will only be wrong by 10 milliseconds.

Action: This is a configuration issue. The value written to the INTDLY register is too small. INTDLY must be greater than largest time interval between the delayed system tick and the data tick from any sub-band. Note that the TIC will normally be zero or a large number of 256 MHz clocks which means that the data tick came after the delayed system tick. To get the correct value subtract the TIC from 2560000 and divide by 4 (256 MHz to 64 MHz). INTDLY must be larger than this value.

Notifications:

1. Condition detected "TIM INTDLY error".
2. Corrective action being taken "TIM INTDLY increase".

3. Result of corrective action is “TIM INTDLY OK”.

12.24 Timing FPGA external clock not toggling.

Condition: One of the input clocks (A or B [or X]) is not toggling. The EVLA is not using the external 128 MHz clock (X).

Action: No action is possible because the problem is likely on outside the Station Board. No action is needed because one of the other clocks is toggling but the MCCC should know about this condition anyway.

Notifications:

1. Condition detected “TIM clock A or B [or X] no toggle”.

13 Testing Procedures and Notes

13.1 Testing Without Heatsink Attached

If a board is to be tested without the heatsink attached, adequate airflow must be provided to prevent overheating. Overheating is the condition where any part of the board PCB exceeds 50 ^{o}C. In addition, it is important that the FIR FPGAs be operated without actually filtering (coefficients set to zero), as they will quickly get hot and possibly be damaged (although so far they have always deprogrammed before any damage has been done). The Delay Module FPGAs and the Input FPGA should have heat sinks installed but can be operated for a few minutes without them.

13.2 Production Tests

The MITR database contains details of testing procedures for Station Boards used during production. These procedures appear in every instance of a Station Board in the database. All the production tests use the Miscellaneous Station Board (aka “illegal”) Software (see A25285N0000). This software contains a number of built-in tests which can be run from a command line or from simple ASCII scripts.

13.3 CRM Test

Not yet available (Dave DelRizzo). Since it is preferred that “golden” files not be used, the tests will be limited to inspection of status bits and comparisons of integrated values (eg power) with the same values from other Filter FPGAs and between paths 0 and 1. In addition, the source of the signal, likely the TPG at the front of the Input FPGA, repeats every interrupt; therefore, the integrated values should repeat from one interrupt to the next. It is also desired that the each Station Board be tested independent of the others which means that comparisons between boards is discouraged.

13.4 DM Test Vector Tests

Quite sophisticated data processing tests can be run using DM Test Vectors (see A25285N0000). Normally, these tests would involve creating a test vector set for one or more paths on one or more Station Boards, configuring the Station and Baseline Boards involved (including loading the DMs with the test vectors), running a test and inspecting the results using ”lagfan” (see A25080N0001) or the CBE. These tests are most useful for checking filter shapes, rejection of out-of-band tones, application of PHASERR, and other checks of the hardware data processing chain on both Station Boards and Baseline Boards. A test vector file can be set up to include

receiver noise, multiple source noise (polarization), multiple source tones (spectral lines), multiple calibration tones (phase calibration), multiple bands (VLBA and eMERLIN) and pulsars.

14 Known Bugs, Workarounds and Anomalies

14.1 No -48 VDC In-Rush Current Protection

There is no in-rush current protection on the -48 VDC supply lines. Due to the input decoupling capacitors, if the board is plugged into a -48 VDC powered socket, arcing on the power connector contacts will occur. This is not particularly damaging unless it is done many times; therefore, it is good practice to plug the board into the socket and then apply power to the socket.

15 References

Brent Carlson, “Refined EVLA WIDAR Correlator Architecture”, NRC-EVLA Memo# 014, October 2, 2001.

Brent Carlson, “Detailed Technical Points”, EVLA Correlator Conceptual Design Review, November 2, 2001.

Brent Carlson, “A Closer Look at 2-stage Digital Filtering in the Proposed WIDAR Correlator for the EVLA” NRC-EVLA Memo# 003, June 29, 2000.

Brent Carlson, “Requirements for 8-bit Processing in the Proposed WIDAR Correlator for the EVLA”, NRC-EVLA Memo# 010, January 29, 2001.

Brent Carlson, “HM Gbps Cable Signaling Specification”, NRC-EVLA Document A25022N0041.

Brent Carlson, “EVLA Correlator Baseline Board”, NRC-EVLA Document A25080N0001.

Brent Carlson, “ Programmer’s Guide to EVLA Correlator System Timing, Synchronization, Data Products and Operation”, NRC-EVLA Document A25290N0000.

Brent Carlson and Dave Fort, “EVLA Correlator CMIB Monitor and Control Task Software Requirements”, NRC-EVLA Document A25204N0002.

Dave Fort, “Miscellaneous Station Board Software”, NRC-EVLA Document A25285N0000.

16 Appendix

16.1 EVLA Station Rack Decal

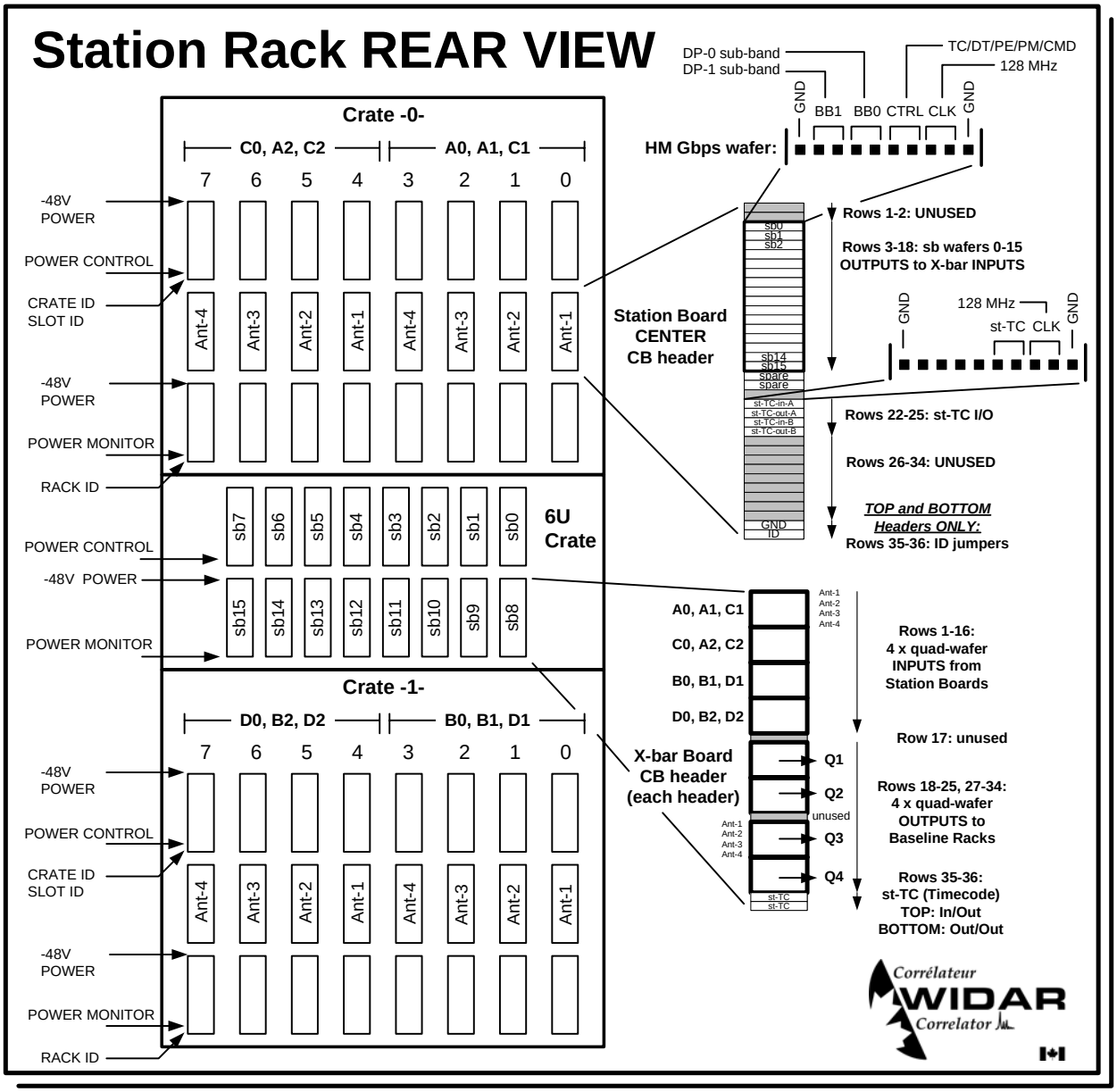

Figure 16-1 Station rack back-door decal.

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