Additional Tests of Correlator Chip Functionality as Required by the Correlator Chip Critical Design Review

NRC-EVLA Memo# 023

Brent Carlson, March 14, 2005

ABSTRACT

The Review Committed Report of the correlator chip CDR held from January 24-26, 2005 in Penticton recommended that additional functional/validation tests be performed to ensure that the correlator chip operates properly in the full suite of intended modes. This memo addresses these recommendations.

Introduction

This memo provides test results for the following modes of operation:

1. 7-bit correlation.
2. Recirculation correlation.

Additionally, justification is given for VLBA modes of operation, and narrowband correlation.

7-bit Correlation

7-bit correlation tests were performed by using a test bench that includes the X and Y Recirculation Controller RTL code and the correlator chip RTL code for the February 23, 2005 release. Thus, this test is run with the correlator chip embedded in the same functional environment in which it would normally operate—except that an LTA emulator, rather than the LTA RTL code was used. The HDL Designer block diagram of the test bench showing the instances of the Recirculation Controller FPGAs and the correlator chip is shown in Figure 1.

The tests were run for an integration time of about 60 μsec and were compared with the results from the 'C' behavioural simulator. A bit-exact comparison was performed by controlling the data valid within the integration time so as to factor out pipeline delays and blanking time of the correlator chip, as compared to the behavioural simulator. Some upgrade of the test bench was necessary for a bit-exact comparison, but it was felt the bit-exact test was necessary for proper testing. The least-significant products are at a very low level, but are necessary for dynamic-range—the whole reason for 7-bit testing.

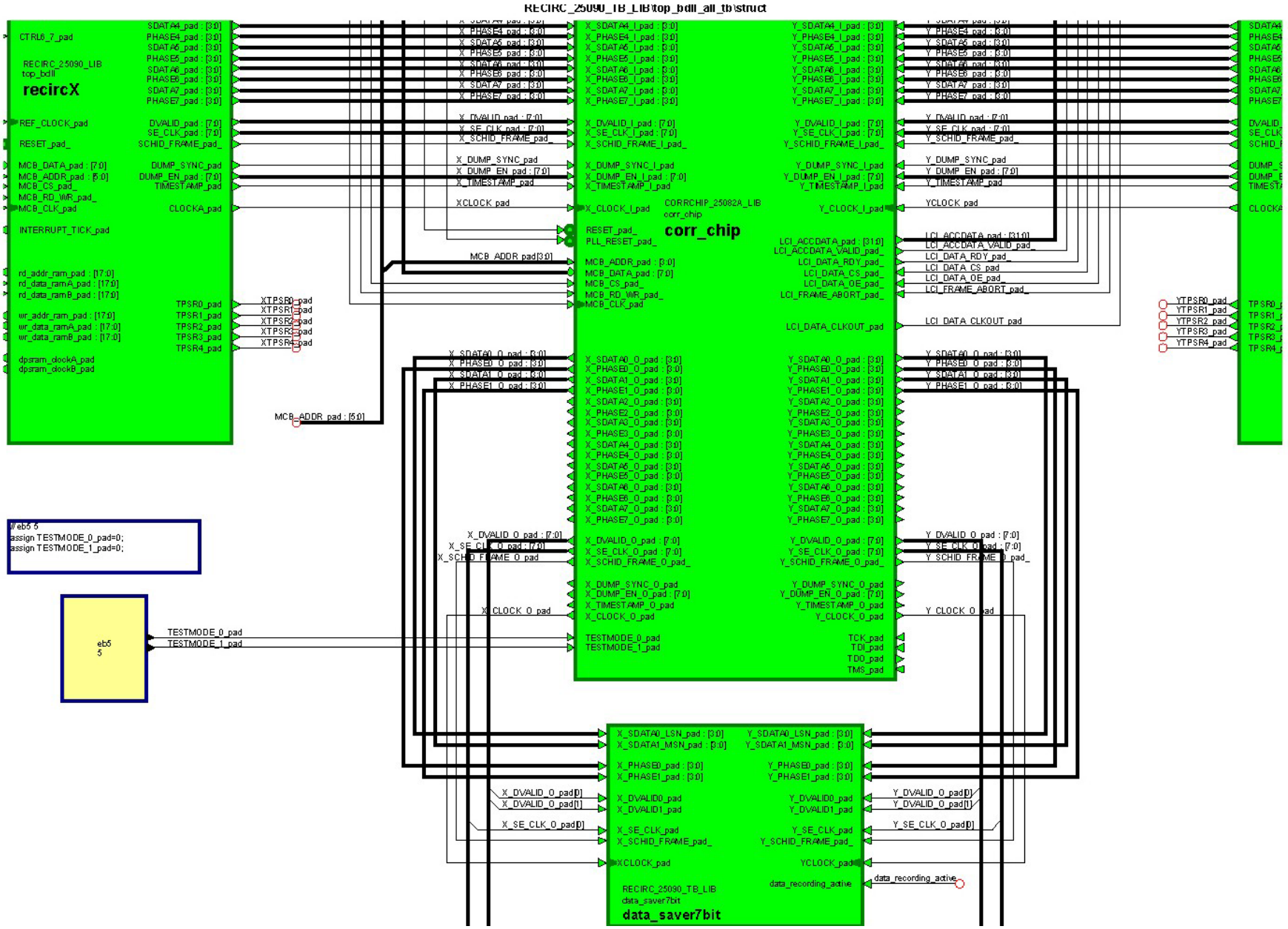

Figure 1 Correlator Chip test bench with Recirculation Controllers.

For the 7-bit test, the test bench was set for 512 lags for each 4-bit product. A 7-bit data capture module was connected to the daisy-chained output of the correlator chip. This module captures data and writes it to files to be used for correlation with the C behavioural simulator. Thus, the correlator chip RTL simulation and the C behavioural simulator correlated *exactly* the same data. The output of the RTL simulation was analyzed and written to files using the correlator chip utility test software [1] so that data valid counts used for converting integer numbers to floating-point numbers were identical in both cases. In the final comparison, floating-point numbers from the behavioural simulator and the RTL simulation were compared—thus some small, but insignificant differences can be expected.

The following figures show the RTL and behavioural simulation results and differences.

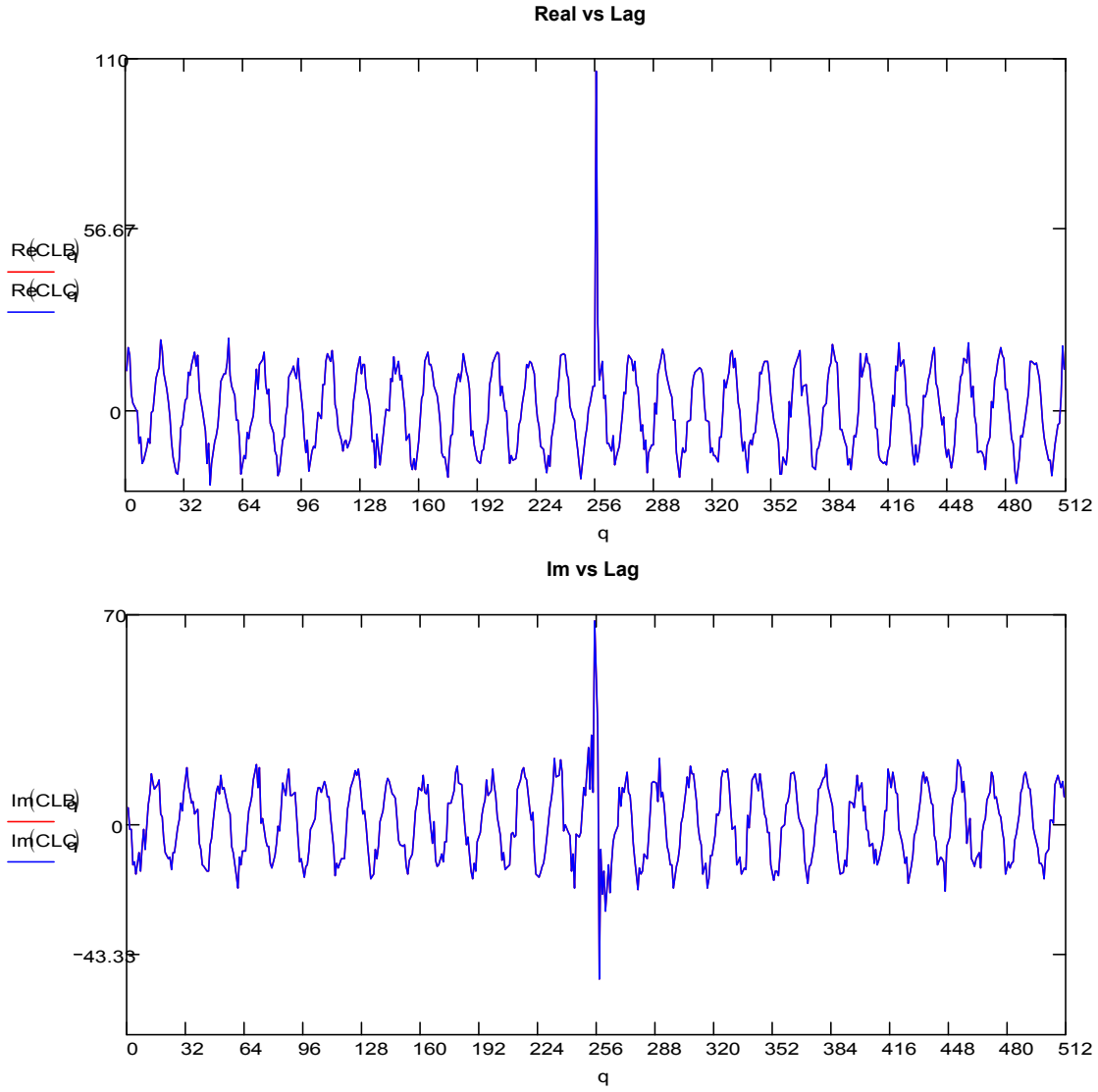

Figure 2 Plots of Real and Imaginary correlation results vs lag for the behavioural simulation (CLB) and the correlator chip RTL simulation (CLC). Only one plot (CLC) appears to be shown because it exactly overwrites the first plot.

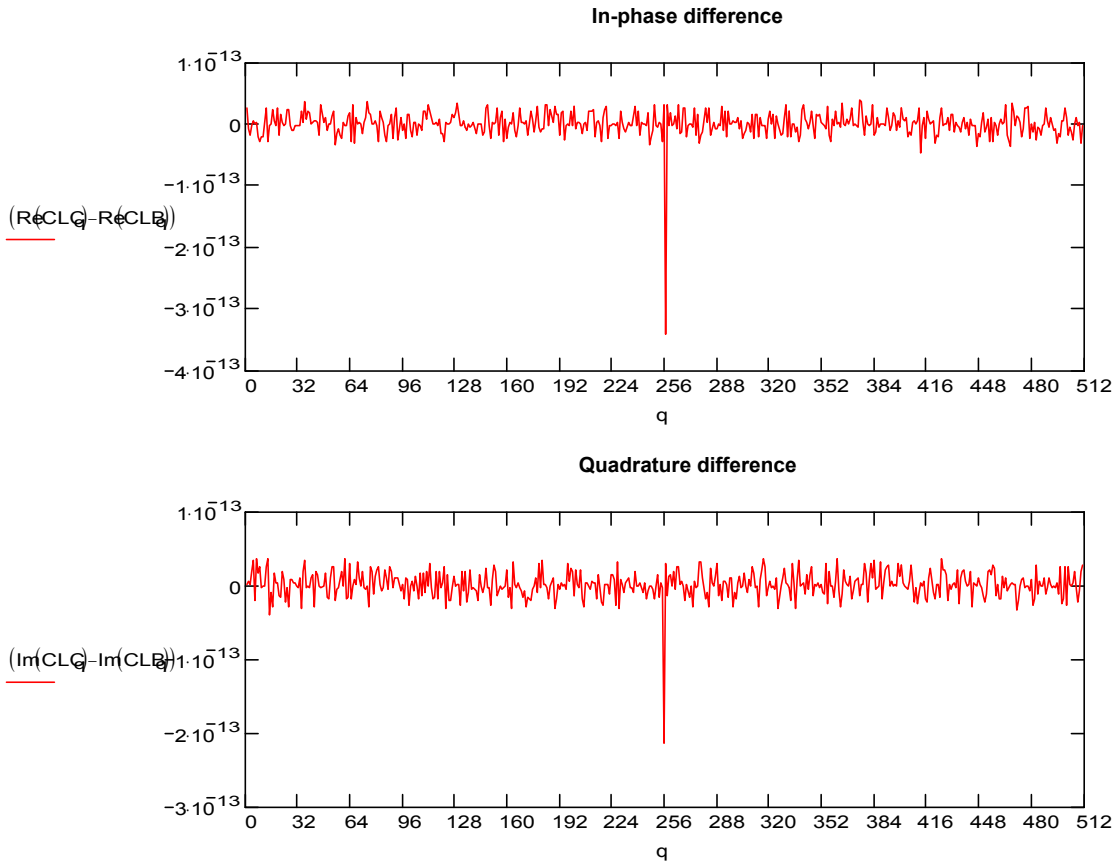

Figure 3 Plot of differences between the behavioural simulator and the RTL simulation. Errors of the order of 10^{-13} are attributed to floating-point numerical error.

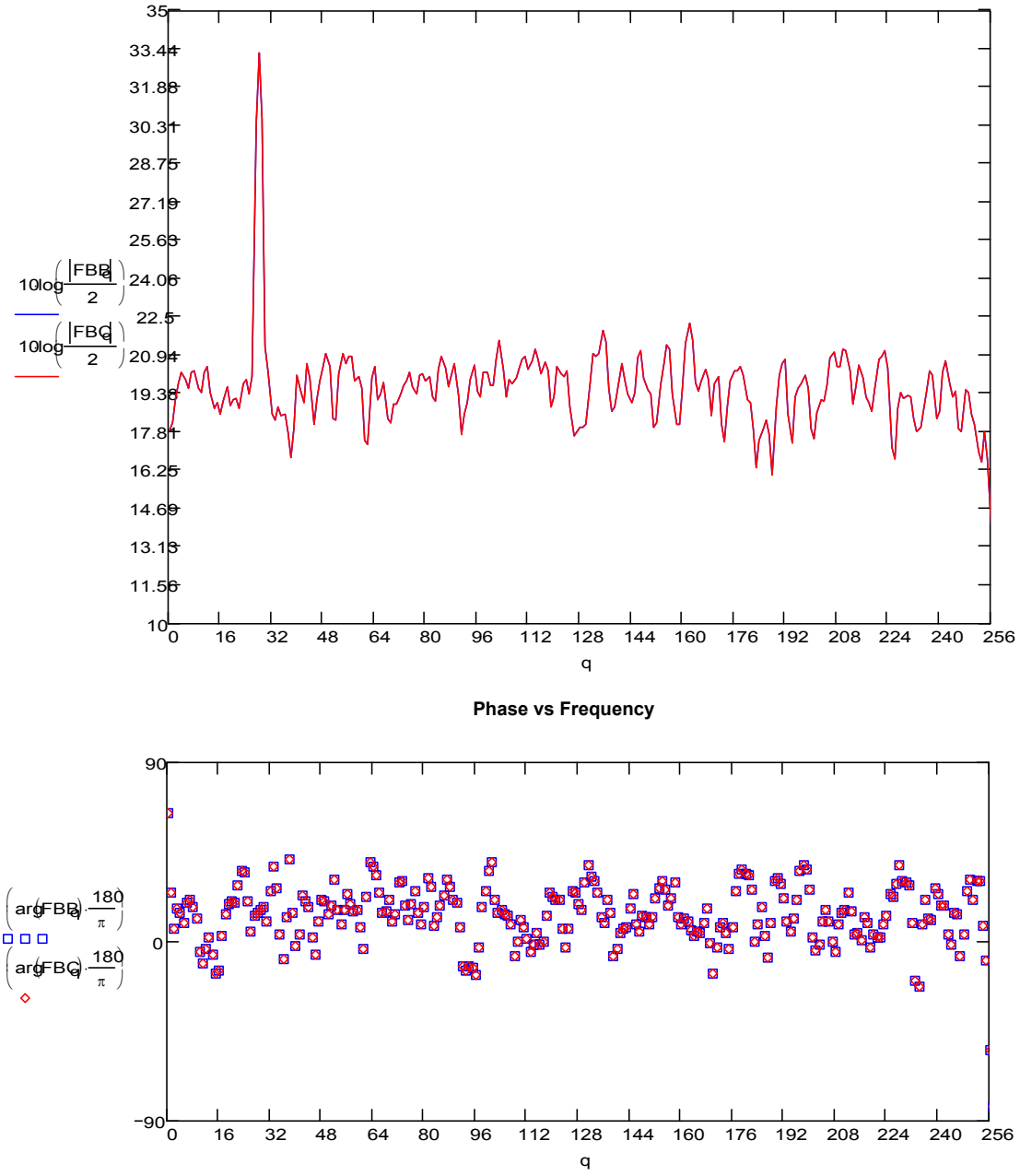

Figure 4 Plots of amplitude and phase vs frequency for the behavioural simulation (FBB) and the correlator chip RTL simulation (FBC).

Clearly, this bit-exact test demonstrates that the RTL simulation of the correlator chip matches the behavioural simulation, and thus the conclusion is that the correlator chip is properly operating in 7-bit mode. Note that in these tests, as in [2] the individual sub-products were scaled and added according to the following equation to produce the final correlation results.

$$\langle r_7 \rangle = \frac{64}{N}\sum_{i=0}^{N-1} B_{3456_{iX}} B_{3456_{iY}} e^{j\hat{\phi}_i} + \frac{8}{N}\sum_{i=0}^{N-1} B_{3456_{i_X}} B_{0120_{i_Y}} e^{j\hat{\phi}_i} + \frac{8}{N}\sum_{i=0}^{N-1} B_{0120_{i_X}} B_{3456_{i_Y}} e^{j\hat{\phi}_i} + \frac{1}{N}\sum_{i=0}^{N-1} B_{0120_{i_X}} B_{0120_{i_Y}} e^{j\hat{\phi}_i}$$

i.e. the MSNxMSN products are multiplied by 64, the MSNxLSN products are multiplied by 8, and the LSNxLSN products are multiplied by 1.

Recirculation Correlation

Due to complexity and time restrictions, a bit-exact comparison of recirculation correlations was not performed. Nevertheless, the results presented in this section should be sufficiently convincing to demonstrate that recirculation works as designed. It is also important to realize that the correlator chip does not do anything special when it comes to recirculation—most of the recirculation functions are provided by the Recirculation Controller FPGA. Thus, the results reported are mostly verification that recirculation, the driving FPGA, and the correlator chip's role in it function as intended. The correlator chip functions that support recirculation are as follows:

- The correlator chip passes on the X and Y recirculation block numbers present on the DUMP_EN lines, without modification, to the output frame.
- The correlator chip has a holdoff function to inhibit correlation so that data in the lag shift registers from the previous recirculation burst do not correlate. This holdoff function has been demonstrated to work, and the holdoff signal and duration is driven and controlled by the Recirculation Controller FPGA.

A critical requirement for recirculation is to ensure that a contiguous set of lags are produced. This requires some care in the test setup, in particular the design of the test signal used for correlation. For this test, a continuum component is used, as well as one spectral-line so that it is possible to detect if a "lag slip"—a non-contiguous set of lags—has occurred. A plot of the Real component of the correlation of this signal is shown in Figure 5 below.

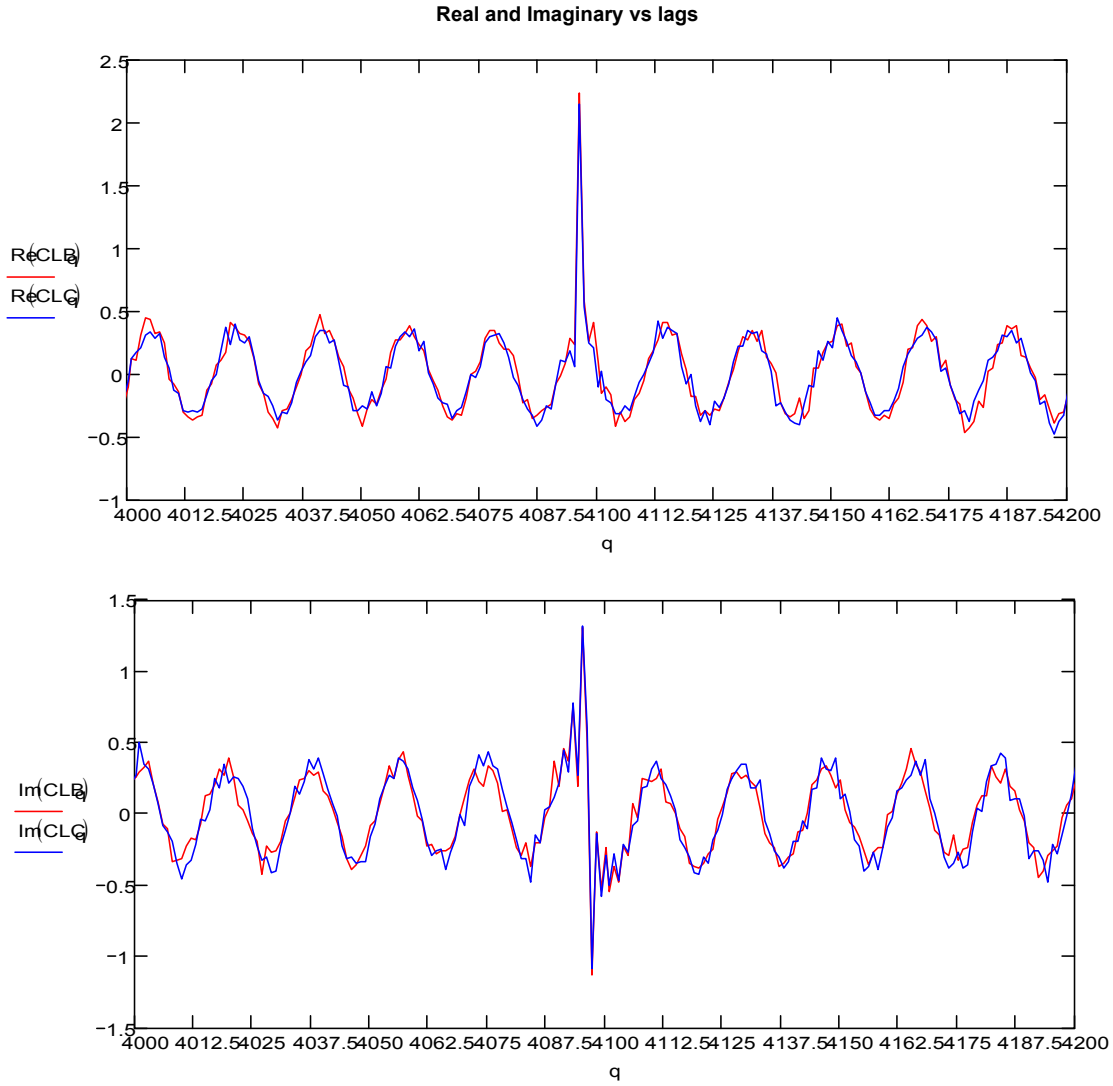

Figure 5 Plots of Real and Imaginary components vs lags of the behavioural (CLB) and RTL simulation (CLC) for the central lags. The continuum and spectral line components are clearly visible.

In normal observing, it is entirely possible that a lag slip could occur and remain undetected in any analysis since the effects on amplitude and phase can be very subtle. For this reason, a number of slip-detection mechanisms are built into the system as follows:

- Recirculation Controller FPGAs perform all recirculation functions relative to DUMPTRIG—the station-based dump-control signal originating on the Station Board.

- DUMPTRIG is synchronized to TIMECODE via hardware and software in the Station Board. Nevertheless, there is a "synchronization test frame" in the DUMPTRIG signal that ensures that locking circuitry in the Recirculation Controller properly locks the DUMPTRIG signal to TIMECODE, even when

dumping is synchronized to an external object such as a pulsar. Thus, if the DUMPTRIG stream is synchronized to the TIMECODE stream, provided the Station Boards generate their respective DUMPTRIGs all synchronized together properly, the data flowing to the correlator chip, and thus the "continuity of lags" should be maintained.

- In the event that some undetectable slip occurs, the correlator chip provides the final dump synchronization detection via the DESSR registers. If recirculation is active, and these registers show synchronization errors, there is a lag slip.

- The X and Y recirculation block numbers—generated in the Recirculation Controllers and passed on to the output frames via the correlator chip—are checked in the LTA Controller to ensure that they are consistent with the expected results. If not, the LTA Controller will discard the frame and flag the error.

The recirculation results from RTL testing, using the test bench as shown in Figure 1 is compared with the 'C' behavioural simulation results using the same input test vectors, but set to produce the entire set of lags at one time. For these tests, the RTL simulation was set for a recirculation factor of 4X, using a lag-block size of 2048 lags (all lags in the correlator chip), for a total of 8192 lags. A sensitive comparison is used to detect lag slips, and the comparison equations are as follows:

$$ReDiff_{lags} = Re(RTL_{lags}) - Re(Behave_{lags})$$

$$ImDiff_{lags} = Im(RTL_{lags}) - Im(Behave_{lags})$$

Thus, with a spectral-line component in the data, a lag slip in the above difference will produce a phase shift between the **RTL** simulation and **Behav**ioural simulation and produce a sinusoidal component in the difference. To demonstrate this, a lag slip in the test data was deliberately induced at around lag 5800 by editing the behavioural ASCII file manually, deleting a line, and adding a dummy line at the end of the file. The Real component difference plot is shown below in Figure 6.

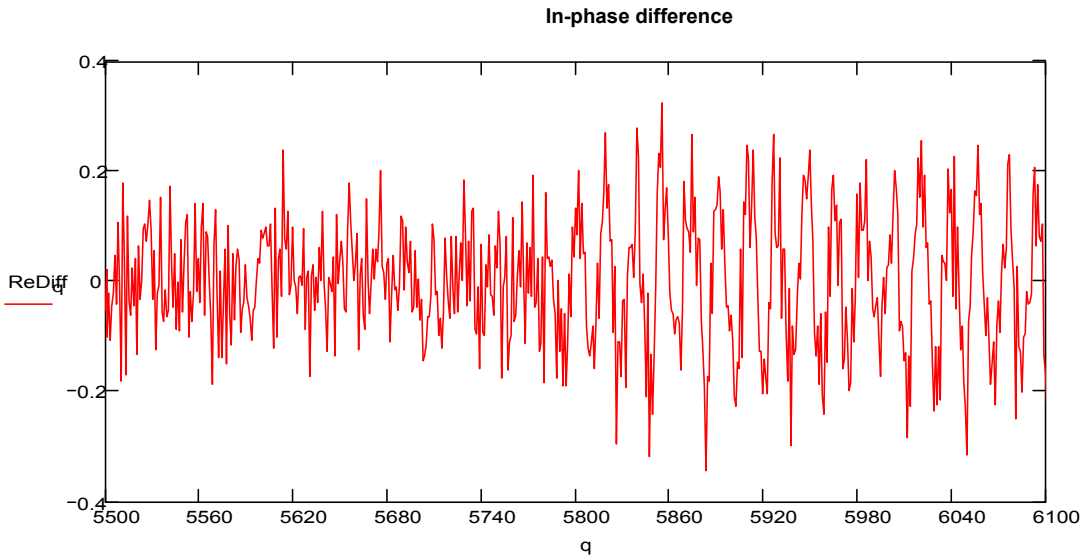

Figure 6 Real difference plot with lag-slip deliberately induced.

This difference is also evident if the entire set of lags are plotted:

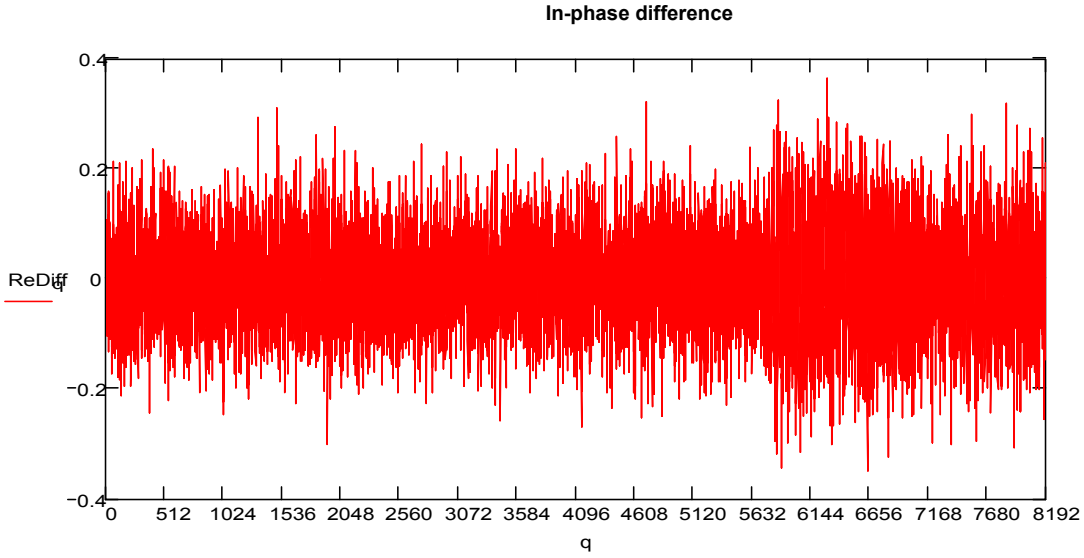

Figure 7 Real difference plot with lag slip deliberately induced, showing all lags.

Additionally, the FFT of the magnitude of the differences fft(|Re + jIm|), produced a clear spectral line where there should be none if there were no lag slip:

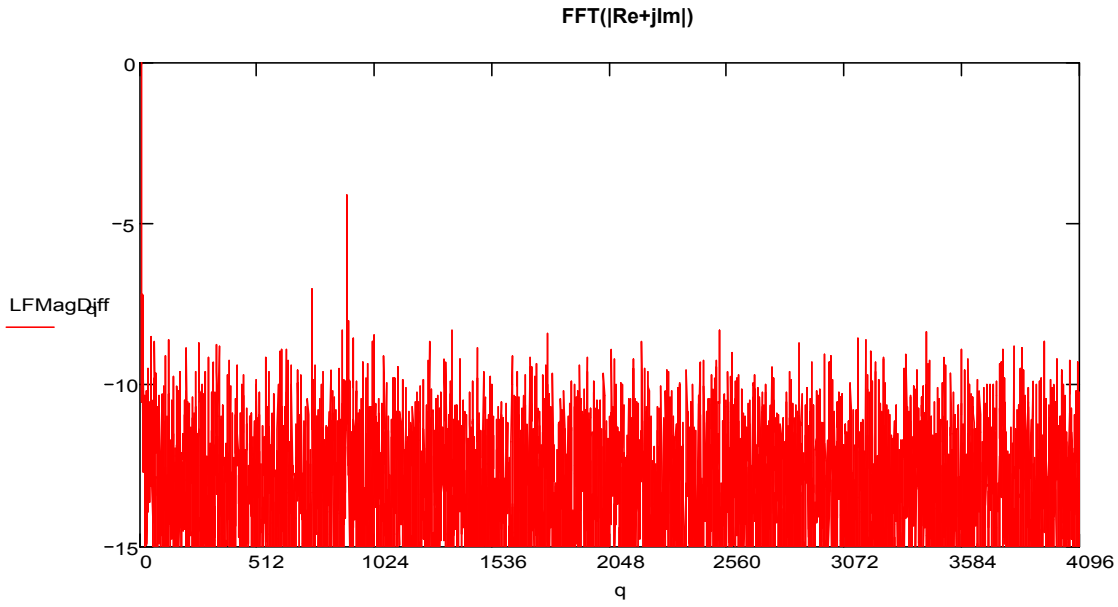

Figure 8 FFT of the magnitude of the real and imaginary differences with an induced lag slip.

The identical plots, showing the difference between the 'C' behavioural simulation and the RTL simulation with recirculation of 4X, **without** an induced lag slip are shown below:

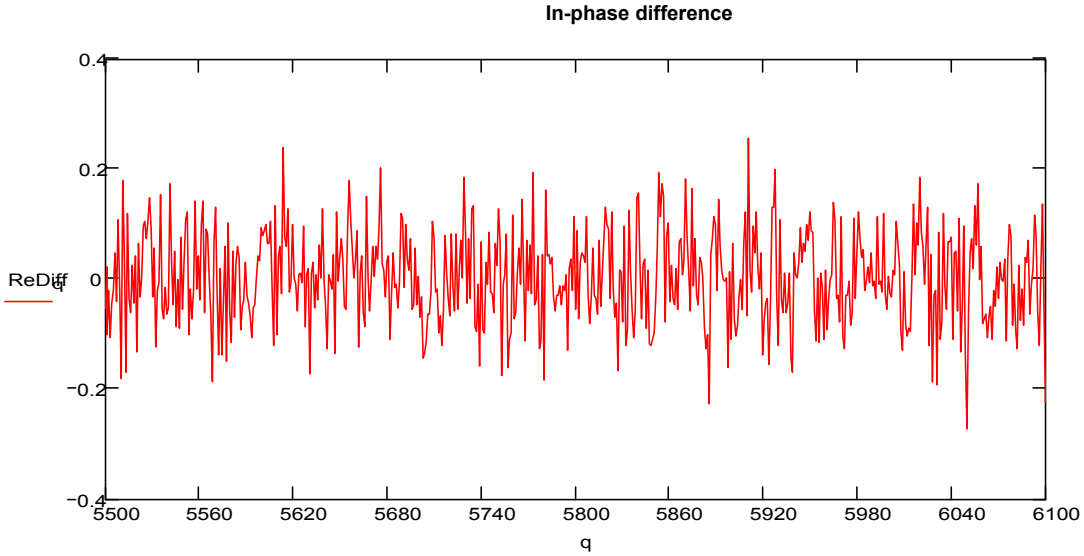

Figure 9 Real difference plot with no induced lag slip. Note the lack of a sinusoidal component.

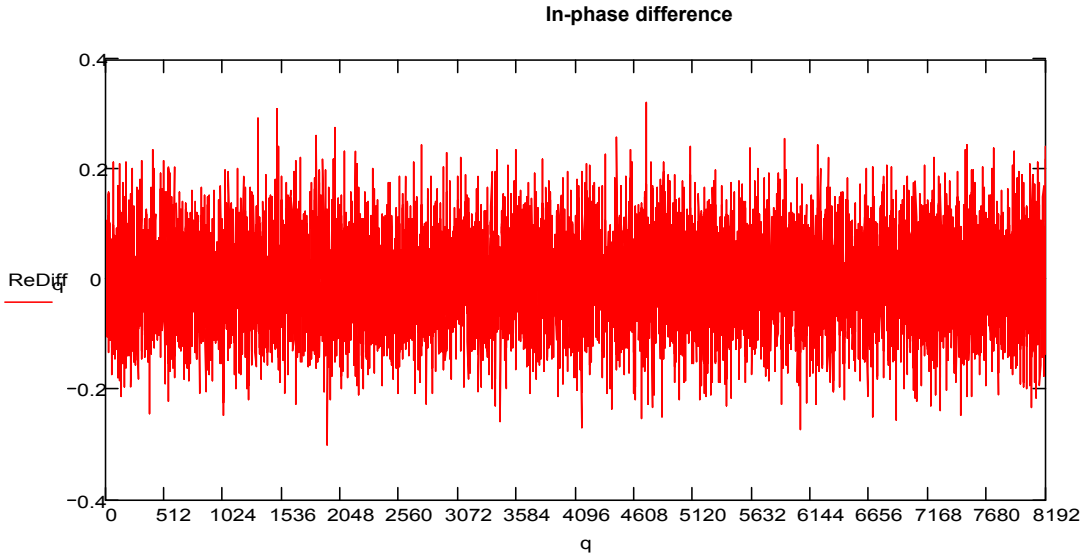

Figure 10 Real difference plot with no induced lag slip showing the entire set of lags.

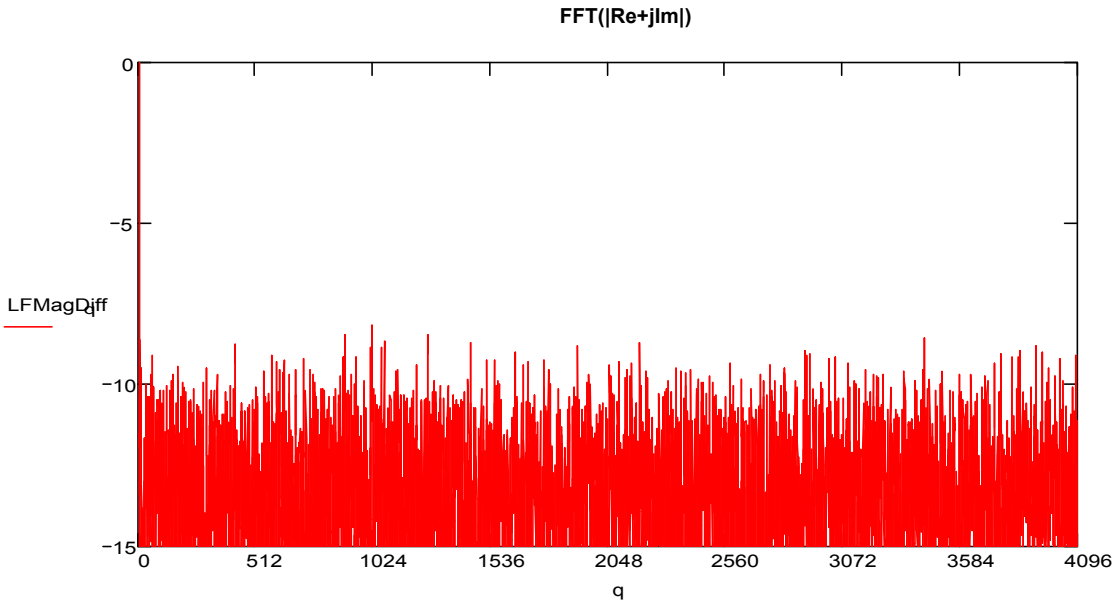

Figure 11 FFT of the magnitude of the real and imaginary differences with no induced lag slip. The spectral line of Figure 8 is clearly absent.

The conclusion is that the RTL simulation and behavioural simulation comparison shown in the preceding figures is sufficient to conclude that recirculation, and the correlator chip's small part in it, function as required.

VLBA Modes of Operation

There was some concern in the Review Committee Report for the correlator chip CDR that the VLBA modes of operation need to be tested. Specifically regarding the correlator chip, the following statements can be made that address this concern:

- NRC-EVLA Memo# 006 (B. Carlson, September 28, 2000) explores this issue in detail and indeed some of the correlator chip's architecture was influenced by this mode of operation. Refer to this memo for a detailed explanation of these modes.

- The correlator is designed to be VLBI ready, including the ability to perform high phase-rate fringe stopping, and narrowband sub-sample delay tracking with the Filter chip on the Station Board.

- The Station Board contains optional VSI-H I/O connectors and chip locations to allow connection to VSI (VLBI Standard Interface) record or playback units.

Narrowband Correlation

There was concern in the Review Committed Report that the correlator chip be able to correlate signals at very narrow bandwidths. These concerns should be addressed by the following statements.

- Narrow(er)-band correlations are performed in the correlator chip with the use of the shift-enable clock (SE_CLK), that allows data to shift along the lag shift registers only when it is asserted.

- This mode has been tested in RTL simulations for sample rates down to 32 MHz. The mechanism for narrower-band correlation is identical and there is no reason the chip should not function identically at much lower rates. Lower sample rate RTL simulations have not been performed because of excessive simulation times, and because lower-sample-rate correlations are believed to be unnecessary.

- The lowest rate that can be supported is 62.5 kHz. This means that there is one SE_CLK pulse every 4096th 256 MHz clock. SE_CLK is generated in the Recirculation Controller synchronized to the TIMECODE 'T' bit, and according to the correlator chip specification, it is asserted on every SCHID_FRAME_ pulse—a pulse derived from TIMECODE. Thus, it is necessary that there are an integer number of SE_CLK pulses between SCHID_FRAME_ pulses. At 62.5 kHz, there are 62,500/100 = 625 SE_CLK pulses every SCHID_FRAME_ pulse, thus meeting this requirement.

- The only possible side-effect that users should be aware of is that within an integration time used for a u-v point, there must be enough fringe phase-rotation cycles such that the coarse mixer functions properly as a mixer. This requirement should be met if there are at least 10 phase rotation cycles. For example, with a

10 msec integration time used for a u-v data point the minimum frequency offset between antennas should thus be 1 kHz.

Conclusions

This memo has successfully addressed concerns arising from the Review Committee Report from the Correlator Chip Critical Design Review held in Penticton from January 24-25, 2005. 7-bit correlation, recirculation, VLBA modes of operation, and narrowband correlation were concerns addressed in this memo.

References

[1] Frances Lau, EVLA Correlator Chip Test Analysis Software, RFS, A25082N0011 Rev. 1.1, June 19, 2003.

[2] Brent Carlson, Requirements for 8-bit Processing in the Proposed WIDAR Correlator for the EVLA, NRC-EVLA Memo# 010, January 29, 2001.