Thermal Analysis of Cooling Strategies for the EVLA Correlator Baseline Board

NRC-EVLA Memo# 017

Brent Carlson, September 3, 2004

ABSTRACT

The EVLA Baseline Board is expected to be the most complex circuit board in the system. Not only that, but the large array of high-speed custom correlator chips could generate significant heat—probably 3.5 to 6.5 W each—that may require more than standard air-cooling. Long-term reliability of the correlator chips is also a significant concern and it is desired to keep junction temperature of the chips as low as possible without resorting to extreme cooling measures. This memo describes the results of various thermal analysis simulations of the Baseline Board for a range of correlator chip power dissipations and cooling arrangements with the goal of keeping the junction temperature of the chip at or below 40 °C.

Introduction

The correlator's Baseline Board (BB) contains an 8x8 array of correlator chips (CCs), 16 FPGA Recirculation Controllers (RCs) to feed them, and an array of LTA Controllers (LTACs) to readout the data, store it, and send it to the final Gbit Ethernet FPGA for transmission to the backend.

The design and place-and-route (PAR) of the RCs and the LTACs has been completed and the FPGA design tools indicate a power dissipation of 2.7 W for each RC and 1.1 W for each LTAC. Each DDR SDRAM associated with the LTAC will dissipate about 0.5 W (this is an estimate from the data sheet depending on activity), and each of the two DPSRAMs associated with the RCs could dissipate up to 1 W each. Current estimates for the correlator chip indicate that, depending on supplier, it could dissipate anywhere from 3.5 W to 6.5 W each.

The total power dissipation of the BB, including power supplies with efficiency of ~85%, the PC104+ board, and the PCMC card could be in the range of 500 to 700 W (correlator chip dissipating 3.5 W and 6.5 W respectively). The CCs and the RCs, both mounted on the front-side of the PCB) themselves could generate 265 to 460 W.

There are 8 BBs (each board 15.7" wide x 19" high) mounted in a crate, and there are two crates in a rack. Thus, the total rack power dissipation could be in the range of 8 to 11.2 kW. This is roughly double the power dissipation normally deemed acceptable for a ~7 ft high rack. Clearly, a suitable strategy must be developed to remove this much heat from the boards and the rack.

It is generally known that for long-term reliability, the junction temperature of the chip should be kept below 50 °C, and if at all possible, 40 °C or less. Simply put, the lower

the junction temperature, the longer the chips will last. This assertion is backed up by extensive reliability data, in particular MIL_HDBK-217F indicates that roughly a factor of 2.5 increase in reliability will be realized for every 10°C drop in junction temperature.

This system must be engineered for a lifetime of 20 years, and thus it is a design requirement to engineer the cooling system to keep the junction temperature of the correlator chips (and other high quantity chips on the board) to ≤ 40 °C.

This memo will aim to develop cooling strategies that will keep the junction temperature of the CCs and RCs at or below 40 °C, initially taking into account only their power dissipations and finally including all circuit board heat sources in the analysis.

Study Method

The "BetaSoft" thermal analysis software purchased and bundled with the Mentor Graphics toolset was used to study various configurations. The software is quite powerful, and claims to produce results that are within 10% of actual implementations if properly used. However, the software does have some difficulties in modeling chip array heat sinks and thus some workarounds had to be developed based on input from the BetaSoft company to overcome these limitations. The results employing the workarounds correlate very well with initial results available from the physical model being developed by Mark Halman using a finned heat sink of the same size used in much of the analysis. Indeed, the results from the physical model and the BetaSoft analysis agree to within 1 °C.

The software is able to take post-PAR PCB designs, along with chip power dissipations and produce a thermal profile of the chips and the board. The software can also be used for "what-if" analysis, where a simple circuit board can be built, chips added, power dissipations assigned and airflows and temperatures assigned to produce credible results. Since a post-PAR BB does not yet exist, the latter approach was taken. With the software it is additionally possible to:

1. Set the atmospheric pressure and relative humidity. There is some effect here, given that the correlator will be operating at 7000 ft altitude, and low humidity. For the tests, the pressure is set to 586 mmHg, and the relative humidity set to 10%.
2. Set the airflow velocity and direction of airflow.
3. Set whether the front and back of the board have access to airflow.
4. Set the temperature or power dissipation of adjacent boards.
5. Define board spacing, thicknesses, material, and volume percent of circuit-board traces.
6. Define emissivity of the board, heatsinks, and adjacent boards.
7. Define boundary temperatures of board edges. Used in this analysis to simulate the effect of attached cold plates.

8. Add heatsinks and specify their thermal resistance.

Results With No Heatsinks

The circuit board parameters were set for the expected configuration of 15.7" x 19", ~0.2" thick, FR-4 material and some small volume fraction of copper. Adjacent boards were set to a power dissipation of 500 W each. Both the CCs and the RCs were set to 672-pin BGA devices with a thermal resistance (θ_{ja}) of 8 ^{o}C/W at 3ft/sec and about 6.5 ^{o}C/W at 6 ft/sec (including θ_{jc} in both cases set to 0.1 ^{o}C/W)—numbers taken from Altera application note [1].

Figure 1 shows the result of this analysis with an airflow of 3 ft/sec (180 LFM) with 15 ^{o}C input temperature, with CCpd = 3.5 W, and RCpd = 2.7 W. This configuration is the "standard" rack cooling configuration and is clearly unacceptable since the maximum case temperature of the CCs is 86 ^{o}C.

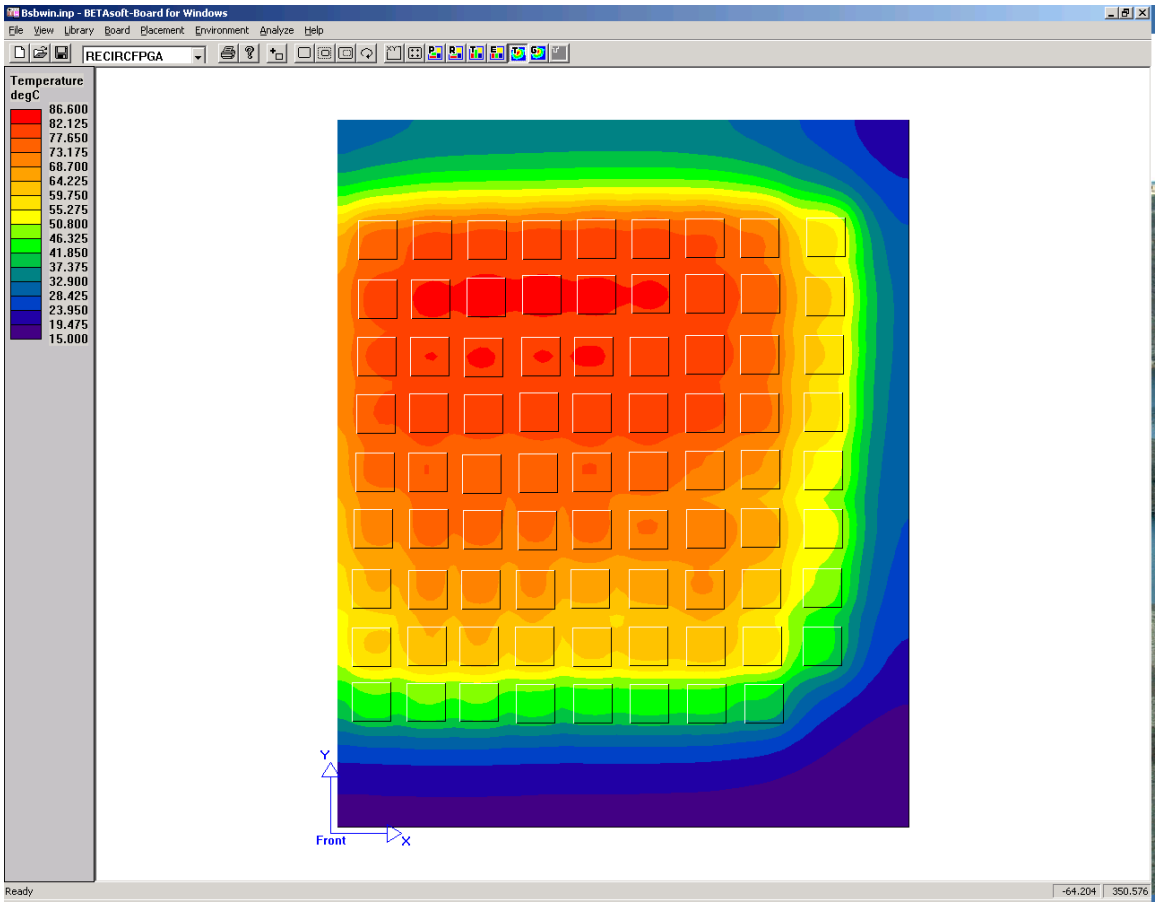

Figure 1 Baseline Board with CCs and RCs, no heatsink, and 3 ft/sec, 15 ^{o}C air entering from the bottom. Note that, as expected, chips increase in temperature higher up the board. The maximum case temperature is 86 ^{o}C—clearly an unacceptable result. Correlator chip power dissipation is 3.5 W.

Figure 2 shows the same configuration except that the airflow velocity has been increased to 6 ft/sec. The temperature profile is the same and there has been some drop in temperature to 72 °C—still unacceptable.

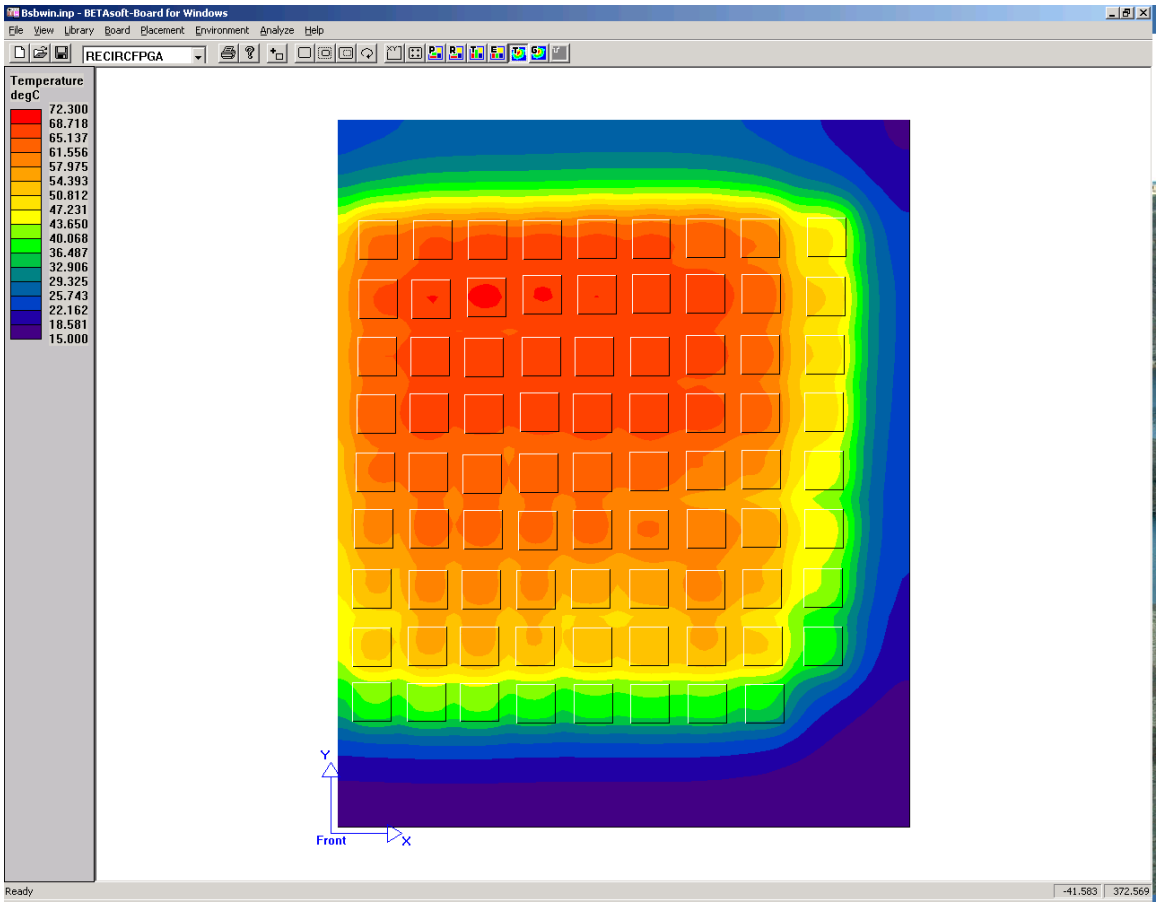

Figure 2 Thermal analysis with the same configuration as Figure 1 except that the airflow has been increased to 6 ft/sec. The maximum chip temperature in this case is 72 °C—still an unacceptable result. Correlator chip power dissipation is 3.5 W.

Results With a Finned Heat Sink

The next configuration that was studied was a configuration where a finned heat sink was bolted to the array of CCs and RCs. It is expected that this is possible in the actual system because there will be enough room between the circuit boards to do so, and because it is expected that the CC and the RC can use the same package (i.e. a 672-pin BGA). Indeed, even if this is not the case, the heat sink could be machined to compensate for the difference.

The BetaSoft thermal analysis software is not capable of attaching a heat sink to an array of chips mounted on the circuit board. Fortunately, a work-around is possible by putting the total power dissipation of the chips onto a dummy device the size of the heat sink, and then attaching the heat sink to the dummy device and setting its thermal resistance data

according to the manufacturer's data sheet. In this test, an aluminum-finned heat sink with the following parameters was used:

- Thermal resistance of ~0.13 at 3 ft/sec and 0.07 ^{o}C/W at 10 ft/sec, based on manufacturer's data with 1" fins, and ~30% fin-to-gap ratio.
- Heat sink total height of 33 mm.
- Heat sink dimensions 350 mm x 350 mm.
- Radiative Emissivity of 0.8.
- Adjacent board power dissipation 500 W with a 50 mm spacing on the front and back side of the board.

The heat sink improves the situation significantly and achieves a temperature of 46.5 ^{o}C[1] at 3 ft/sec airflow. Figure 3 shows the thermal profile for an incoming air temperature of 15 ^{o}C.

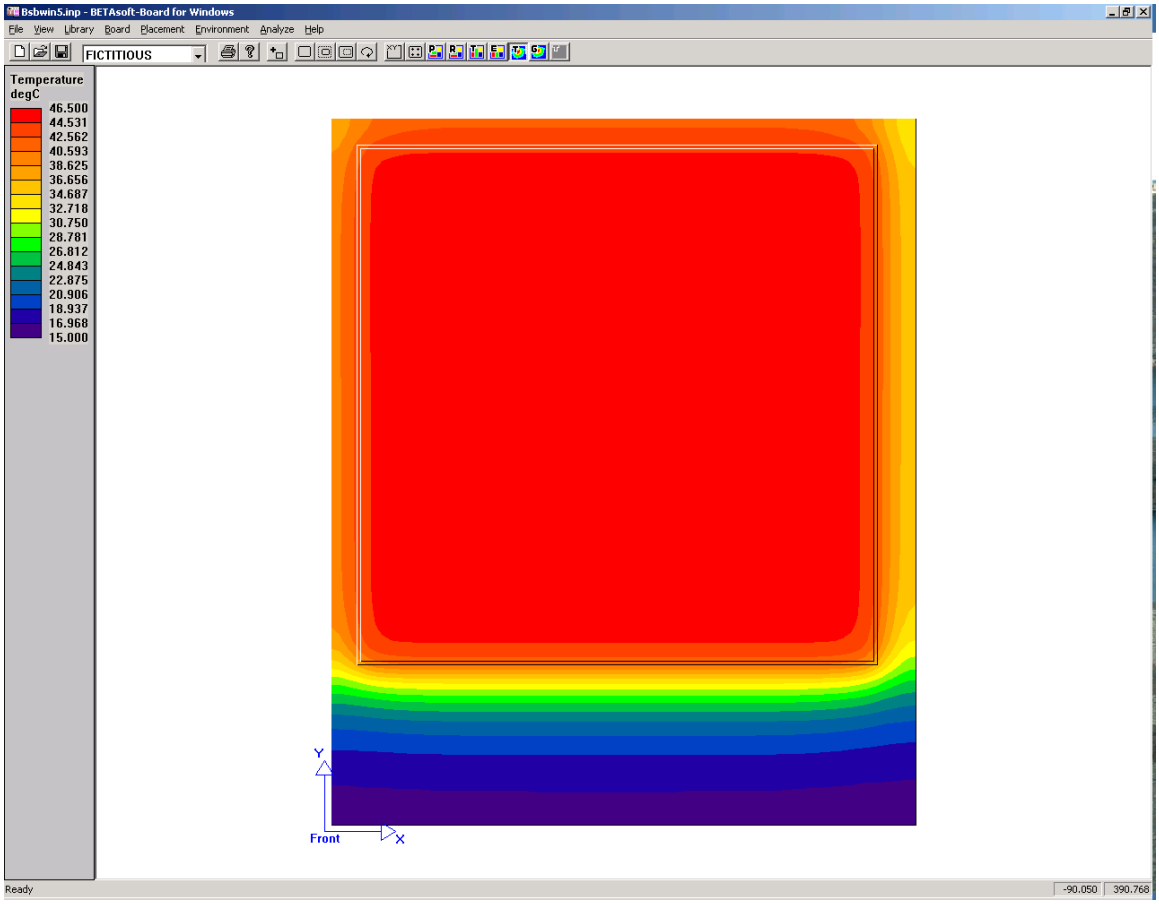

Figure 3 33 mm thick aluminum heat sink, with 15 ^{o}C air entering from the bottom at a velocity of 3 ft/sec and a correlator chip power dissipation of 3.5 W. This measure reduces the chip temperature to 46.5 ^{o}C.

[1] It is assumed that a package with a low θ_{jc} will be used, and so the difference between the junction temperature and case temperature in this configuration is negligible.

When the air velocity is increased to 6 ft/sec, the results improve to 36.8 °C. Increasing the air velocity to 10 ft/sec reduces the temperature to 31.6 °C.

These results, for this simple case and under these conditions, agree well with a simple calculation using manufacturer's data, and running tests where the thermal coupling of the components to the PCB is minimized. For example, at 3.5 W/chip, and with 16 RCs dissipating 2.7 W per chip each, the total power dissipated by the heat sink is 267 W. At a thermal resistance of 0.13 °C/W, the calculated temperature rise is 34.7 °C, and for an incoming air temperature of 15 °C, the heat sink temperature is 49.7 °C. The slightly lower heat sink temperature of 46.5 °C in Figure 3 is the software taking into account the coupling of the chips to the PCB, and resulting heat dissipation. At 10 ft/sec, the simple calculation yields a 19 °C rise for a resulting temperature of 34 °C. The analysis with coupling to the PCB yields a result of 31.6 °C, as reported above. These results seem self-consistent and establish some confidence in the results reported in this memo.

Additionally, the results for this simple case correlate well with initial results from the physical model as previously mentioned. In this case, the physical model was run with the finned heat sink (350 x 350 mm, 33 mm thick) at a power dissipation of 160 W, with T_{amb}=20 °C, and airflow at ~10 ft/sec. The physical model and the BetaSoft model agree to within 1 °C. The heat sink temperature in this case is about 30 °C.

These results indicate that it is almost possible, ignoring effects of other chips on the board to achieve the desired results with a correlator chip power dissipation of 3.5 W and ignoring the effects of other heat sources on the board.

Adding Other Board Components

To analyze the effect of all of the other sources of heat on the board the model was upgraded to include all other known sources of power generation on the board, with manufacturer's data for package size and thermal resistance, and power dissipation values as follows:

- LTAC: 1.1 W ea—obtained from analysis of place-and-routed design.
- DDR SDRAM: 0.5 W ea—estimate based on activity level.
- DPSRAM: 1 W ea—estimate based on activity level.
- Power supplies (Vicor "mini" supplies) 6 W each.
- PC104 + PCMC: 10 W.
- 2 W each for the Gbit Ethernet chip and MCB bus controller.

The result of the analysis with 10 ft/sec of airflow and an incoming air temperature of 15 °C is shown in Figure 4. The heat sink temperature is now about 37 °C, however, the maximum chip temperature on the board is 44.3 °C. Further investigation indicates that the LTAC chips on the back side of the board are running at this temperature. The thermal plot of the back side of the PCB is shown in Figure 5, with the chip temperatures highlighted.

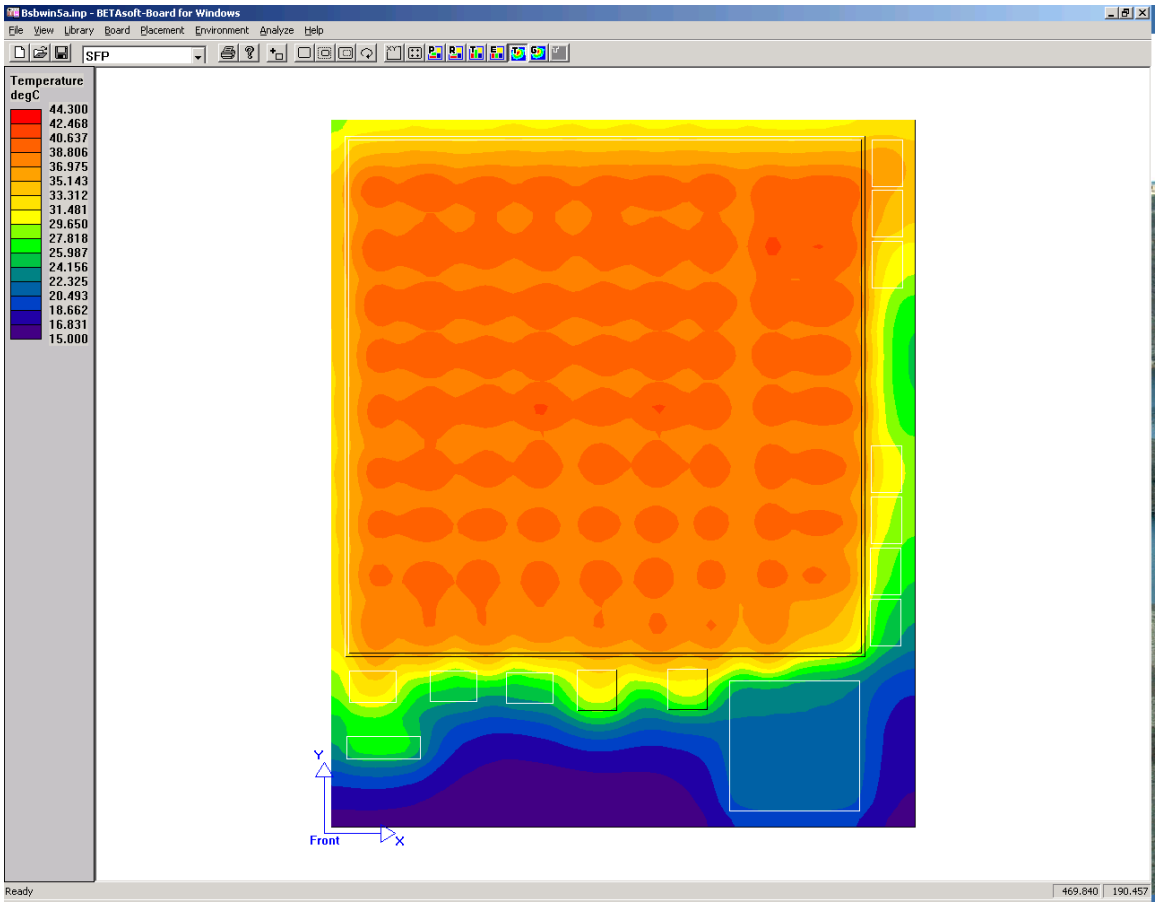

Figure 4 Thermal analysis of the Baseline Board with all components in place. This plot shows the PCB temperature. The correlator chip power dissipation is 3.5 W and the incoming air temperature is 15 ^{o}C with a velocity 10 ft/sec. The heat sink temperature is about 37 ^{o}C.

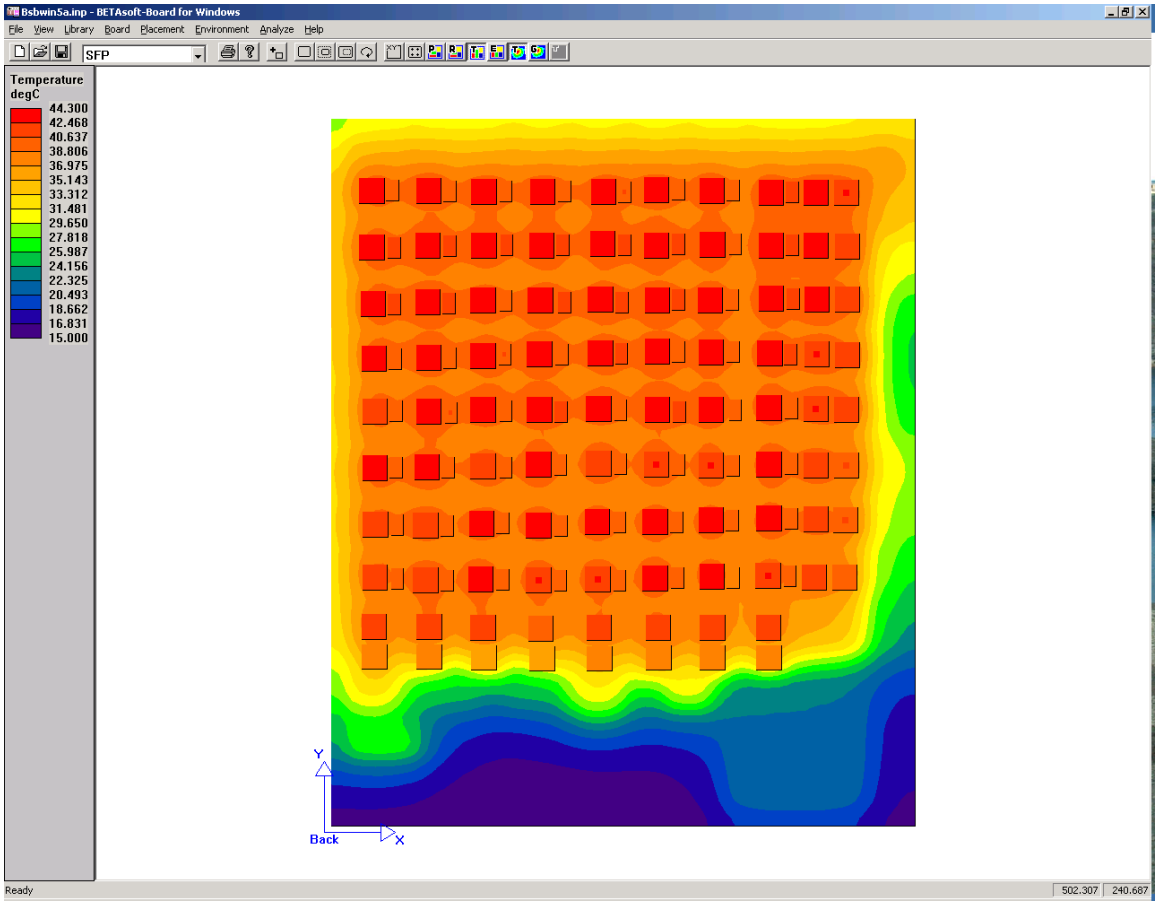

Figure 5 Plot of the rear of the Baseline Board under the same conditions as Figure 4. The LTAC chips are running at the highest temperature.

A number of tests were run with different correlator chip power dissipations and air velocities. These results are summarized in Table 1. The table notes the heat sink temperature and the maximum "other" chip temperature—the LTAC.

Corr chip power (W)	Total heat sink power (W)	3 ft/sec		6 ft/sec		10 ft/sec	
		$T_{heat\ sink}$	T_{max}	$T_{heat\ sink}$	T_{max}	$T_{heat\ sink}$	T_{max}
3.0	235	52	63	**41**	49	**35**	43
3.5	267	56	64	45	51	**37**	44
4.0	299	60	65	46	52	**38**	46
4.5	331	62	67	50	54	**41**	47
5.0	363	64	70	52	56	42	48
5.5	395	68	72	53	57	44	49
6.0	427	74	74	59	59	50	50
6.5	459	77	77	61	61	52	52

Table 1 Table of array heat sink temperature and maximum chip temperature on the board for a range of correlator chip power dissipations and airflows. Incoming air at 15 ^{o}C is used throughout.

The results in the above table clearly indicate that there are only a few cases where the design requirement of T_{jmax}=40 ^{o}C is met. At the lowest probable chip power dissipation of 3.5 W, air flow between 6 and 10 ft/sec will be required. At the highest power dissipation of 6.5 W, it is not possible to obtain the desired results even at 10 ft/sec of airflow.

It is not known what airflow is possible in the actual system. 3 ft/sec seems easily achievable, given the height of the heat sink, and the space between the boards. 6 ft/sec is also likely. 10 ft/sec may be an upper limit. A full rack physical model must be built to verify these results and determine actual airflow.

As indicated in the table, it is likely that any chip power dissipation over ~4 W will require more aggressive cooling methods than investigated thus far. Liquid cooling is likely required if the power dissipation of the chip exceeds 4 W, if the required T_{jmax} of 40 ^{o}C is to be obtained.

Liquid Cooling Strategies

This section presents two straw-man designs and some test results to study if it is possible to achieve T_{jmax} of 40 ^{o}C if the correlator chip power dissipation is > 4 W.

Non-Invasive Liquid Cooling

The first straw-man concept is designed to be as non-invasive as possible so that there is minimal chance that there could be a fluid leak in the system that falls onto a PCB, and so that there are no cooling lines that have to be disconnected/re-connected when replacing a board. This concept is shown in Figure 6.

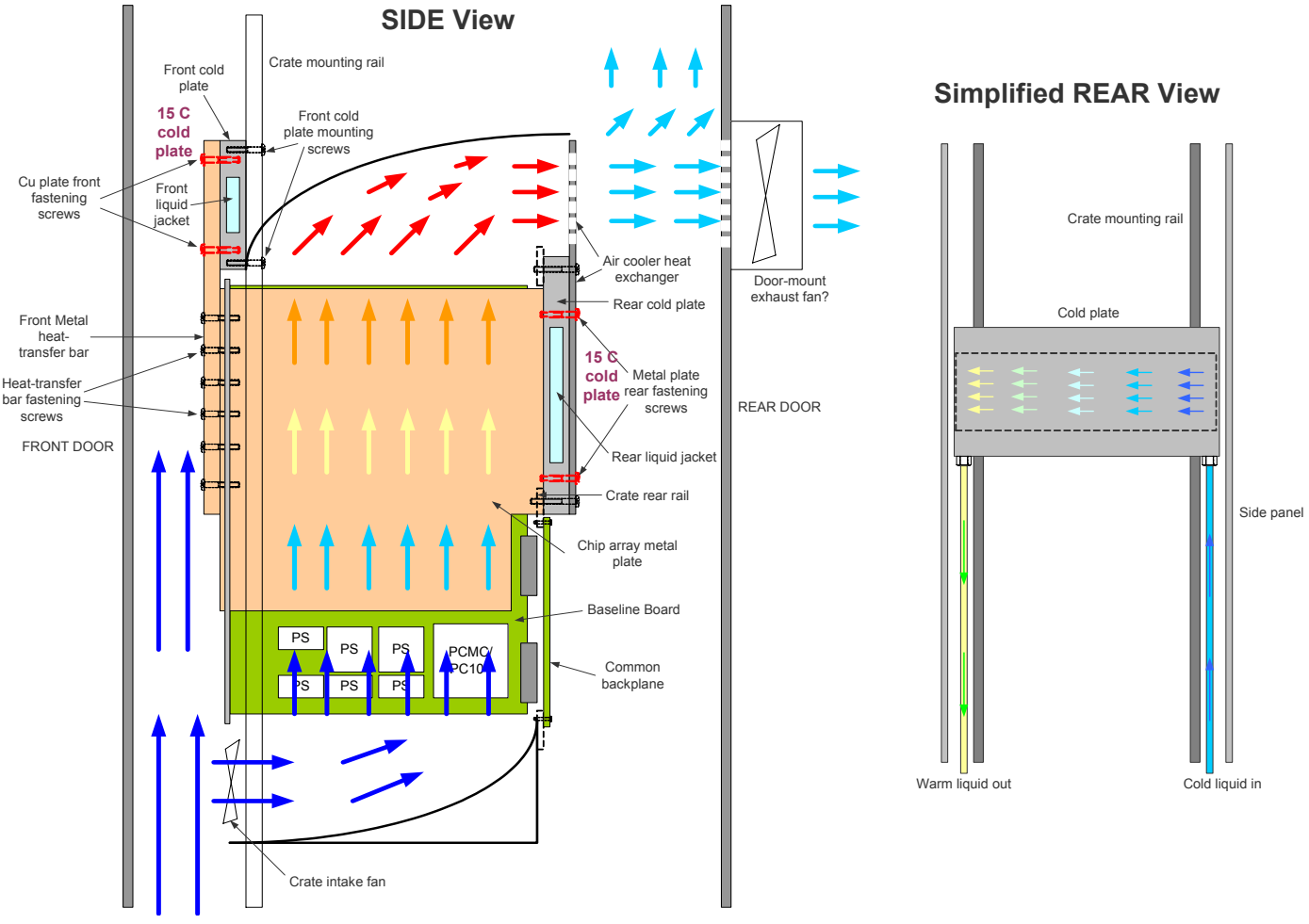

Figure 6 Straw-man concept for non-invasive liquid cooling design. In this design, heat from the array of chips is mostly conducted to front and back cold plates that have fluid running through them. Boards can be replaced by removing fastening screws. The coolant lines are always fixed in place.

An attempt was made to analyze this design using the BetaSoft software, however the software was not designed for this type of analysis. The software is capable of attaching a cold plate to the edge of a circuit board, but not to the edge of a heat sink. Thus, the workaround to this problem involves attaching the correlator chips and RC devices to a circuit board made of aluminum, then attaching the aluminum circuit board to the front and back cold plates as shown in Figure 6.

Establishing credibility for these test results required a number of steps—the associated test results are described in the following sub-sections.

Flat Aluminum Plate Thermal Resistance

The thermal resistance of a 350 x 350 mm x 5 mm thick plate of aluminum was determined by following a calibration scheme similar to that developed earlier in this document. This thermal resistance was found to be about 0.22 ^{o}C/W with 3 ft/sec airflow. The calibration test was performed with a 300 W load and the heat sink temperature rise above ambient was found to be 65 ^{o}C, yielding the 0.22 ^{o}C/W thermal resistance This value is consistent with manufacturer's data for a low-profile (7 mm) aluminum heat sink of the same size.

This same test was run with a 5 mm thick, 350 x 350 mm aluminum circuit board with the same power dissipation, and with airflow restricted to the "back side" of the PCB—equivalent to the front/exposed side of the heat sink in the previous test. The results of this test (15 ^{o}C air at 3 ft/sec) indicate a rise above ambient of only 37 ^{o}C—inconsistent with the above test. Thus, it was decided that for the cold-plate test, a closed-system would be modeled with no airflow, something that supposedly the software is good at modeling. In the actual system, air flowing across the flat plate can only serve to lower the temperature, and estimates will be made as to what that might be.

Closed System, No Airflow

The test was run with a flat-plate of aluminum, 5 mm thick and approximate dimensions that would allow it fit in the system as shown in Figure 6. No airflow was allowed in this closed system, and so all cooling was by way of conduction to the front and back cold plates.

The thermal resistance from the aluminum to the cold plate was set to 0 ^{o}C/W since it is assumed a torqued metal-to-metal thermal resistance value will be arbitrarily low. Small non-zero values were tested and the difference was not that significant. The thermal resistance of the aluminum plate over a long distance (216 W/m-K) appeared to be the dominant effect.

Test results with correlator chip power at 4 W each, and RC power at 2.7 W each is shown in Figure 7. The maximum chip temperature is 40 ^{o}C. Note that the heat load from any other chips on the board is not taken into account, and any cooling effect from real airflow across the flat plate of aluminum is not factored in. It is possible that these two effects will roughly cancel each other out.

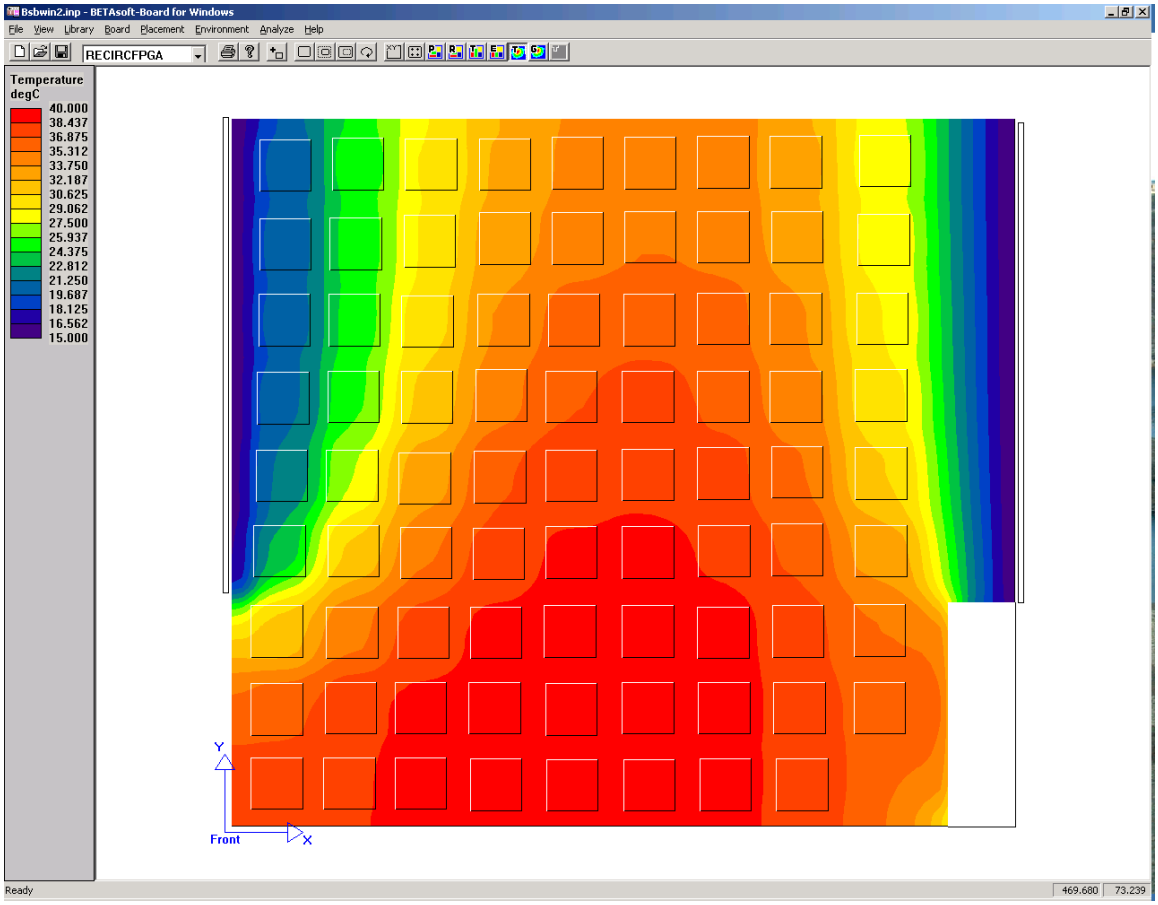

Figure 7 Thermal analysis with front and back cold plates at 15 °C according to Figure 6, with no airflow. All cooling is through conduction to the cold plates. The maximum chip temperature is 40 °C.

A number of tests were run for varying correlator chip power dissipations from 3 W to 6.5 W each, with both an aluminum and a copper plate. These results are summarized in Table 2.

Corr Chip Power (W)	T_{max} (5 mm aluminum plate)	T_{max} (5 mm copper plate)
3	35	23
3.5	38	24
4	40	26
4.5	42	28
5	45	30
5.5	47	32
6	50	34
6.5	52	36

Table 2 Maximum temperature for aluminum and copper plates for a range of power dissipations.

Note that the copper plate performs significantly better than the aluminum (12-16 ^{o}C lower T_{max}), and would likely be needed if the correlator chip power dissipation is greater than 4 W. Thus, if a cold plate is necessary, then the plate must be copper since the results for the aluminum plate are about the same as in the previous table with a finned aluminum heat sink with an airflow of 10 ft/sec.

If one factors in the effect of airflow across the plate, then the temperature may drop somewhat. For example, at 6.5 W with the aluminum plate and front and back cold plates, the maximum temperature rise is 52-15 = 37 ^{o}C. This is an effective thermal resistance of about 0.08 ^{o}C/W. If the thermal resistance with air cooling across the plate is 0.22 ^{o}C/W as established in the previous section, the combined thermal resistance is about 0.06 ^{o}C/W, and this could, for that power, drop the temperature another 10 ^{o}C. As mentioned, this could be proportionately offset by the heat from the other components on the board as demonstrated in previous sections of this memo.

If this liquid cooling scheme is to be seriously considered, then a physical model will have to be built to more accurately quantify its actual performance and perhaps verify or discount the results established in this analysis.

Engineering and Construction Costs

The non-invasive liquid cooling scheme, while simple in principle incurs a non-zero cost compared to a simple air-cooled system with a finned heat sink. While these costs are difficult to determine, the following factors must be taken into consideration when calculating costs:

- Copper plate material and machining costs.
- Front copper connect bar material and machining costs.
- Re-inforcing likely required in the sub-rack and the rack to bear the 20 lbs or so of copper plate weight per board.

- The front and rear water jackets have to be designed, tested, and manufactured.
- Cooling lines, a cooling pump, and heat exchanger must be designed and installed at the VLA site.
- Maintenance checks will likely have to be performed on a regular basis to ensure that there are no leaks (a negative-pressure system would ensure that leaks will not drip fluid into the racks).

A rough estimate is that the liquid cooling could add between $1000 and $2000 to the cost of each Baseline Board in the system, in addition to the engineering costs. Total costs for implementing this cooling scheme could be upwards of $600k.

Invasive Liquid Cooling

This scheme will yield the lowest thermal resistance and is capable of lowering the correlator chip temperatures, and most of the chips on the board to nearly the temperature of the liquid. This scheme consists of a metal plate with a circulating liquid jacket of coolant bolted to the array of correlator chips and RCs. Quick-connect/disconnect cooling lines will go to each jacket on each board, and these must be driven by an external pump.

Although commercial systems like this exist, potential failure modes could be damaging to the circuit board and racks. As one might imagine, maintenance costs, downtime, and reliability degradations in the system could be significant. Thus, this scheme should only be used if the liquid cooling scheme (or similar scheme) shown in the previous section does not perform as the analysis indicates, or is otherwise found to be infeasible.

Conclusions

This memo investigated the Baseline Board thermal properties for a range of correlator chip power dissipations and a range of thermal designs including air cooling and liquid cooling in various configurations. This analysis, based on the BetaSoft thermal analysis program—and if it is to be believed—indicates that with a finned heat sink and decent cold air flow, a correlator chip power dissipation of 3.5 or perhaps as much as 4 W can be tolerated and the junction temperature can be maintained at or below 40 ^{o}C. The results from the BetaSoft analysis program correlate well with initial results from a physical model being built to test an entire rack mechanical and thermal configuration.

Above a power dissipation of 4 W per correlator chip, it is evident that a liquid cooling strategy is required to maintain a junction temperature ≤40 ^{o}C. This low junction temperature is a design requirement for reliability and a 20 year system lifetime.

Due to some uncertainties in the actual airflows and temperatures that will exist in a fully populated rack, it is important that further investigations with a full rack physical model be built to verify the results reported in this memo.