Meeting Participants

Penticton	Amy, Brent, Dave F, Donna, Gary, Mark, Ralph, Sean, Sonja, Zhang, Zoran
Socorro	Bruce, Bryan, Hichem, Kevin, Mark, Martin, Michael
Jodrell Bank	Bryan, Christine

Software Focus

Sonja Vrcic

- Working on VCI tasks; making progress.
  - → Sonja encountered many problems with her personal workstation environment now that the move behind the firewall is complete. There seems to be an issue with running VMWare on top of Linux.
  - → **Action** – NRAO to test remote access to DRAO lab and contact Tony H directly if issues arise.
  - → The IT crew will work over the weekend to complete work required by new NRC policy.
  - → A power shutdown for the entire area is scheduled for Sunday, April 6 from 8:00 am until 3:00 pm (PDST).

Kevin Ryan

- The infrastructure software is working.
  - → It would be advantageous to have 2 boards installed in a rack at DRAO for remote CPCC testing.
  - → **Action** – Brent to consider possibilities for testing the CPCC and let Kevin know.
  - → Also, it would be good to hook up the CPCC to a rack at DRAO for remote testing of fan tachometers; Brent commented that for now 2 boards and some fans could be hooked up to the RPMIB. The RealLogic computer could be used to look at real fans.
  - → **Action** – Brent to ask Peter C re: Super Logics rack-mount computer. [done]

Bruce Rowen

- Dump trig is running on CMIB 8 and Baseline Board 2 with no CRC errors.
  - → Some testing has been completed, Bruce will add more features, e.g. phase bin bunching.
  - → Not yet implemented pulsar phase binning.
  - → New schema for the XML interface to be published later today.
- VCI obs prep tool is being designed for a factor of 128…but recirc is not yet configured for that.
  - → Will have to transition to driver software after the Baseline Board is released.

Martin Pokorny

- Summarized comments received re: BDF document.
  - → A meeting is scheduled for Monday to resolve BDF issues.
- Preparing binary lag sets to see how lag set assembly works in the backend software.
  - → Cannot yet create BDF files.

Hichem Ben Frej

- Testing delay models…look fine.
  - → Some confusion re: Barry's sample is in a different format from what Bruce published. Barry to produce the format required.
  - → Sonja commented that both formats (ISO 8601 and MJD) for the time could be included to avoid translations.
  - → **Action** – Sonja to initiate an email discussion to decide where messages will be intercepted and passed on.

→ Working on a rudimentary version of CPCC.
→ Bryan has set the end of May for an end-to-end test of getting delay models through the system.

Michael Rupen
- Working on BDF, discussions with Martin, and SDM.
  → Rich now has SDM from DECAF with real observing system in real time

Mark McKinnon
- Reviewing the schedule as forwarded by Amy.
  → Checking error dependencies between it and the overall schedule; will forward comments to Amy.
  → **Action** – Amy to release the schedule for posting to the WIDAR website once confirmed.

New Software Action Items

- NRAO to test remote access to DRAO lab and contact Tony H directly if issues arise.
- Brent to consider possibilities for testing the CPCC and let Kevin know.
- Sonja to initiate an email discussion to decide where messages will be intercepted and passed on.
- Amy to release the schedule to be posted to the WIDAR website once confirmed.

Continuing Software Action Items

- Sonja to set a review date for the VCI Protocol.
- Kevin to check re: if each board is identified with a serial number on the board.
- NRAO to clarify their schedule within the next few weeks re: 4-station prototype correlator and inform DRAO.
- Bryan to organize a meeting re: verify a process re: output to chips: participants to be Bryan, Barry, Bruce, Hichem and Ken S.
- Bruce to come up with a directory structure to support start up sequencer files.
- Martin to forward a copy of the CBE schema/config to Sonja once a stable copy is available.
- Brent to review the 4-bit and 7-bit correlation samples for the VCI as Sonja would like to ensure that the connections/syntax are agreed upon.
- Michael to clarify with Bryan re: Delay Model, on-the-fly observing, smoothing, buffering, and cuing and report back to Hichem and Bruce.
- Michael to define critical tests.

Hardware Update

Brent Carlson
- Received 1200 chips; Brent has tested 275 and encountered only one failure.
  → Sent 114 tested chips with the tester to MuAnalysis for further testing.
- Testing the 10G Ethernet on the Baseline Board; waiting for a part (new crystal) to test the connection.
  → Crystals have been ordered and shipped…should arrive DRAO within a week.
  → Curiously, initial testing showed 8 chips dead; mysteriously, all are working now. There is no explanation.
  → Running at full power. Will continue testing.
  → The COTS part is indicating that frames are working, but jitter is still being observed.

- → Focussing on signal integrity testing.
- → Currently have 37 minor items on the Baseline Board ECO. Zhang is keeping up on implementing changes listed on the ECO.
- → **Next**: Move on to thermal testing.
- → The new target date for go-ahead on the Baseline Board is the end of April.
- → Both the board and the decision to go ahead will be reviewed.

- The Station Board Work Order has been issued and the build is in process.
- On track for shipping the racks.
  - → It looks like there is a good solution for the rack shipping and board shipping containers.
  - → **Action** – Ralph to set rack ids. Next time, it might be more efficient to set the rack ids first.
- Brent is investigating contracting a Production Engineer via ORIC with a possible start date in beginning of April.
  - → If contracting through ORIC is not feasible, then Brent will pursue contracting Morley directly.
  - → **Action** – Brent to contact Mike Hare re: expediting a contract for a Production Engineer.

Dave Fort

- Testing the Station Board in the environmental chamber worked well.
  - → Thermal imaging photos resulted in the re-location of some power supplies.
  - → **Priority**: JTAG testing is not going as smoothly as hoped. Software required re-installation before it would work correctly. BMS needs results from the JTAG testing for Stage 3.
  - → The test claims that some things are connected together that shouldn't be connected together…something is not right. Could be the wrong version of the Delay Module is written in to the software.
  - → Emailed Gary Lee (BMS) explaining the issue but has not yet heard back.
- Working on the output chip.
  - → Headers are in the right place. The output chip works at all different decimations.
- Worked on the Filter FPGA.
  - → Encountered problems running on the narrowest bandwidth to get the tone extractor value out.
- **Next**: Testing that the Station Board GUI is correct, including dump trig.

Zoran Ljusic

- Off last week.
- Doing Delay Module coding so that it can read from memory and to give more control to the person de-bugging.
  - → **Question** – Is there a RAM self-test on power up or is assumed that software will do it?
  - → Brent wants diagnostics to ensure proper operation.
  - → What is the repair philosophy for the Delay Module? Could build a stand-alone FPGA to determine JTAG.
  - → Gary H voiced a concern re: feature creep.
- **Next**: Documentation and some design.
  - → Brent would like a user manual for each board and each FPGA (could strip the applicable RFS and convert to the file to a user manual).
  - → Will need a documentation clean-up phase. Documentation requires a separate discussion.

Zhang Heng

- Keeping up with all the changes re: Baseline Board ECO items.
  → It is increasingly obvious that isolation of the ferrite bead before bypass capacitors is important.
- Completed an ECO for the RPMIB; which was forwarded to Ralph to add to the MITR dBase.
- **Next**: RXP chips and silk screens.

Ralph Webber

- Updated MITR dBase – everything is up to date.
  → The assembly workers will be able to enter items as appropriate.
- Brent reported that the pin on the replacement browser head on the Agilent scope does not work.
  → The scope is ready to be returned.
- Implemented changes re: ECO for the RPMIB.
- Procurement issues.
  → Received standoffs, SCSI cables and USB couplers. Waiting re: custom cables.
  → Triple E drawings arrived (converted from SolidWorks to AutoCAD) for review. Found many small errors.
  → Renewed Pete's contract for another 3 months.
  → Greg may not renew the current contract as he has asked Ralph for a reference.

Mark Halman

- Working on the design for the rack shipping containers.
  → Construction of a prototype container will be contracted out and delivered to DRAO in April.
  → Should be good for shipping eMERLIN racks.
  → There is a new regulation re: pest control and wood shipped to the UK.
  → Existing skids are not certified.
  → **Action** – Dave B to investigate possibilities.
- Did some re-work for the asic.
  → Brent ordered inter-poser pads. Important to have spare pads. Working on barrier strips.
- **Next**: A test rack will be shipped to the VLA in May with the 8 racks.

Project Management

Amy Fink

- Updated the schedule and forwarded it to Brent and Mark McK for comment.
- Received a proper quote for the Station Board.
- Submitted the Work Order for the SB with an amendment to delete Stage 3 items. Will do the same for the Baseline Board Work Order.
- Received 26 Common Backplane Boards.
- Procurement is up to date; in good shape for fiscal year end.
- Requested up to date invoices from BMS.
  → The issue of credits is not yet sorted out although Gary Lee believes it is sorted out.
- Encountered additional paperwork for the cable shipment re: country of origin.