Meeting Participants

Penticton	Amy, Brent, Dave F, Donna, Mark, Peter, Ralph, Sonja, Zhang, Zoran
Socorro	Bill, Bruce, Martin, Pete
Jodrell Bank	Bryan, Dave, Simon

Software Focus

Sonja Vrcic
- Working on the Station Board GUIs; still 2-3 items left to edit.
- Adding components and making changes to the GUI for the new format of CRC output from the Station Board.
  - → Zoran and Dave F. to test.
- Received information for and purchased Magic Drawer software but has not yet downloaded and installed it.
- Mark H. and Ralph W. have accounts in Jyra.

Bruce Rowen
- Finished the new CRC code; ready to upload to the test simulator.
  - → There are some inconsistencies re: CRC errors.
  - → The schema is updated to reflect the new format with data visible in a table. Will perform auto-scan of every wire.
  - → Still a labelling issue to sort out with Dave and Zoran.
- On vacation May 28 – June 1.

Martin Pokorny
- Worked on the design document for the backend; looking at config messages.
  - → Found a toolkit (open software library) that could be useful; indications are that it will give good performance.
  - → Martin plans to implement a prototype to see how it could be used for EVLA.

Pete Whiteis
- Working on delay model software.
  - → Developed files with tag value pairs with config and delay info to simulate external data at 10s/delay model.

New Software Action Items

- There are no new Software Action Items from this meeting.

Continuing Software Action Items

- Sonja to notify Tony H. re: communication problem experienced by Bruce.
- Sonja to prepare drawings re: auto-correlation products as requested by Michael R and publish in Memo #029.
- Michael to forward examples of typical, simple configurations re: auto-correlation products and Sonja will prepare the drawings to be included in Memo #029.
- Michael to forward the date for formal review of the Wiring Scheme Proposal when confirmed.
- Peter and Mark to discuss details for the formal review of the Wiring Scheme Proposal.
- Bill to write and distribute for comment an email explaining the possible use of Apache Tomcat for realtime

distribution of monitor and control products from the Station Board.

- Bruce to add memory dump definitions to schema.
- Bruce to freeze and release a software version as soon as the VSI MAH is completed – pending.
- In progress – Brent to forward pin numbers to Kevin.
- Long-term – Kevin to develop an RFS for RPMIB test software, which will be needed by summer 2007.
- Michael to send out email re: estimated dates for next steps as related to Binary Data Format document.
- When time, Dave DR and Bruce to discuss offline re: diagnostic display for different points on the Station Board.

Hardware Update

Brent Carlson
- Completely dedicated to testing the correlator chips.
  → The replacement cable for testing the correlator chips arrived.
  → The FPGAs have been reprogrammed and the chips returned from DATest have been tested resulting in almost the same numbers as those realized by DATest.
  → Of the 76 chips tested, 36 chips passed at room temperature and at 100°C; 19 chips did not pass at room temperature, but did pass at 100°C.
  → Used a programmable heat gun and a make shift oven.
  → Of the chips that passed at both room temperature and at 100°C, some chips reported an X IO error indicating an FPGA timing problem. Brent is investigating.
  → Almost completed extensive functional testing thanks to the GUIs.
  → Brent will write a test report and schedule a review of the test results. NRAO and Jodrell Bank folk will be invited to attend the (online) review.
  → Brent commented that the test results indicate good performance and is confident that he can sign-off for production once the review is complete.
- Brent will install on to a board the chip that previously indicated a RAM issue in 4 cells to demonstrate that the RAM issue is now a non-issue.
- The test socket is working well; it makes good contact with the BGAs.

Dave Fort
- Sorting out some document numbering issues and project code assignments.
- Still working on the Dump TRIG and encountering CRC errors.
- Working on Plan B of JTAG testing, that is, testing with the FPGA not programmed.
  → Encountering branching signals issues; 242 nodes are reporting errors.

Zoran Ljusic
- Returning from 1 week vacation.
- Working on JTAG testing with Dave.
- Not yet started the modifications to the Station Board.

Brent
  → It would be good to get started on the mods in parallel with other work.
Action
  → Zoran to purchase a 3 month Expedition PCB license.

Zhang Heng	• Working on changes to the Baseline Board design.
	→ Should be completed the high-speed traces by the end of this week.
	→ Will move on to the point-to-point clock, power supply press-fit pins, 200 traces between timing FPGAs and the PCMC connector.
Action	→ Discussion is required re: re-placement of power supplies.
Ralph Webber	• Working on Purchase Order Requisitions for the System BOM.
	→ Approximately 40% of COTS items are yet to be ordered. Ordering mechanical fasteners now.
	→ Not yet started ordering custom parts.
Mark Halman	• Working out the mechanics of re-arranging the Baseline Board and possibly shifting the heat sink to the top side.
Brent	→ A thermal foam could be placed under the heat sink as an alternative to thermal putty.
	→ Bergquist and Thermagon have similar products, but they are slightly tacky.
Action	→ Mark to investigate thermal foam as an alternative to thermal putty.
	• Updated the fan housing with indicator lights for fan rotation.
Action	→ Mark to pass on ordering information to Ralph.

Project Management

Amy Fink	• Sorting out BreconRidge's new billing system and the different assembly stages that will be needed.
	→ Scheduling BOMs and parts purchasing.
	• Re-organizing the procurement process.
	→ Updated the Procurement Request sheet and writing a set of instructions re: how to complete.
Brent	• The Fanout Board will probably be eliminated from the new design so a re-spin will not be required.