EVLA Weekly Meeting Notes

Meeting Date 2006October04

Meeting Participants

Penticton Brent, Dave DR, Dave F, Donna, Mark H, Peter, Ralph, Sonja, Zhang, Zoran

Socorro Bill, Bruce, Kevin, Mark M, Martin, Michael

Jodrell Bank Bryan

Software Focus

Sonja Vrcic

- Investigated Gbit Ethernet as per action from last meeting re: switches and protocol analysers.
  - → Found some sources for PAs which were forwarded to Ralph. Could not find a source for a rental PA.
  - → Auto negotiation done in transceivers should be okay.
  - → Spoke with Allied Telesyn rep who thought connections should be okay.
  - → Did not contact Cisco.

Brent

  - → Brent will review data sheets for transceivers; hopefully there will be no software involvement.
  - → The Gbit Ethernet Chip should capture frame exactly as sent to the transceiver; Brent is concerned re: CRC calculations are correct.
  - → Should be able to use ad hoc software to read the buffer.
  - → Decision: Not to purchase a PA at this point.
  - → HIA-Victoria may have an instrument DRAO could use.
- Question – Is there a need for Prototype Correlator Testing (OTS) meeting before the Oct 31 meeting in Socorro?
  - → Bill indicated that the meeting could be scheduled for after the Oct 31 meeting; possibly November 2.

Bill

  - → Bill to review material and make a decision.
- The updated Software Requirements for Testing of the Board Prototypes [RFS] document to be posted today.
- Sonja worked on the Action re: Network throughput and routing analysis.
  - → Output of backend performance estimates can be found in the CBE network drawings in the System directory on the WIDAR website.
  - → Summary table of CBE Network drawings are useful for SDM discussions.
  - → Need to wait for more refined results.

Action

  - → Peter to contact Mark McKinnon re: an idea regarding CBE.

Dave Del Rizzo

- Changed the plotting software; purchased the programmers' guide for the new software.

Bill

  - → Rick Moeser (NRAO) can be consulted for assistance if needed.
- Question – when will the CMIBs be available for testing again?

Kevin

  - → CMIBS were re-configured for GUI testing. Should get some more up and running.

Action

  - → Brent to get 3 CMIBs going at DRAO (test FPGA generator, Baseline Board, Station Board and 2 spare).

Action

  - → Bruce to copy root partitions for each board and forward to Brent.

Action

  - → Zhang to program the PCMC so Brent can get the CMIB going.

→ Sonja commented that it would be good to have seamless access to ports at both Socorro and DRAO.

Bill
→ NRAO is moving away from the VPN notion as a move towards greater security. Targeting specific solutions to specific services.
→ Need to consider access requirements as the project expands, e.g. streaming output through different ports, remote access, etc.

Kevin Ryan
- Hooked up the CMIB to the test fixture to test GUI which displaced Dave.
  → Set up an alternate CMIB in Socorro, but the ports didn't allow access.
- Kevin was unable to work on documentation this week but anticipates completing it next week.

Bruce Rowen
- Working on Station Board data products.
  → Taking data out of file handle from the operating system.

Martin Pokorny
- Working on CBE code optimization and documentation of code.
- Working on presentations for October 31 meeting.

Michael Rupen
- Been off sick for the last week.
- Sent email to Brent re: Phasing Board RFS.
  → Review to be scheduled for the week of October 16; Brent and Michael to sort out when and who should attend.
- Michael's top priority is sorting out the binary data format in consultation with Joe.
- Michael's second priority is the SDM for the Station Board data, in consultation with Joe and Bryan.
- This puts the Prototype Correlator Test Plan as a lower priority with a target date of 31December2006.
  → Need the Science Test Plan before integration and before the PCTP, possibly as early as mid-November.
  → Michael will check with Bryan B. re: UVFITS and the Science Test Plan.

Summary of Software Action Items

Action • Peter to contact Mark McKinnon re: an idea regarding CBE.
Action • Brent to get 3 more CMIBs going at DRAO (test FPGA generator, Baseline Board, Station Board and 2 spare.
Action • Bruce to copy root partitions for each board and forward to Brent.
Action • Zhang to program the PCMC so Brent can get the CMIB going.

Software Action Items Resulting from External Inputs

Action • Bryan B to produce report on Station Board data products; which ones go to the Monitor Archive (MA) and which go to the Science Data Model (SDM). This report will also treat data rate estimates in some detail, including examples for particular observing scenarios (2006Jun30 first draft).
Action • Michael to release report on where the ALMA Binary Data Format (ABDF) is insufficient for WIDAR output products (2006May19).
Action • Michael and Martin to release report on final Binary Data Format for EVLA. Hopefully in agreement (and

after consultation and iteration with) ALMA (2006Aug31).

Action • Sonja, Bryan, Bill to produce report on software integration test plan for the Prototype Correlator (PTC) tests (2006Dec31 Draft).

Action • Michael, Frazer, Rick to produce report on science test plan for the Prototype Correlator (PTC) tests (2006Oct31 Draft).

Action • Brent, Bryan, Michael to determine whether UVFITS is sufficient for all Prototype Correlator (PTC) tests (2006Dec31?).

Action • Sonja, Brent to network throughput and routing analysis of the 3 separate networks within the correlator subsystem (2006Oct31?).

Hardware Focus

Brent Carlson

- In a recent telecon with BMS, Brent learned that the Baseline Board is still scheduled to be shipped to DRAO October 16.
  - → The Baseline Board is currently undergoing "paperless" repair, then will proceed to flying probe testing.
  - → Coretec over-estimated shrinkage and the board was manufactured 10 thou oversize.
  - → There could be implications for the BGA socket fit and connections not lining up correctly.

Zoran

  - → Oversized board could have resulted in some shorts.
  - → Manufacturer is producing variable results in quality control; need to tighten up tolerances on the board.
- The Station Board is undergoing SMT (Service Mount Technology) and should be shipped to DRAO October 25.
- Brent is in the process of finalizing details re: Power Plant contract.
  - → Waiting for a response from NRAO re: training costs at installation, after installation or never.
- The Fanout Board is done; Konrad to let Brent know re: shipping date.
- The DFM for the Common Backplane is done.
  - → The quote for 100 quantity is $75.00/each.
  - → Press-fit holes are too big which have to be fixed as they may cause a problem down the road.
- Submitted a requisition to purchase an oven for testing.
- Looking at possibility of purchasing a freezer for low temperature testing.
- Chip MIL Standard Test with auto test is ~$30K.
  - → DATest have sub-contractors to do their testing.
  - → Brent is waiting for a cost/chip quote, if the quote is ~ $1.00 to $1.50/chip then will go with DATest. If it is as high as $5.00/chip, then it will be cheaper for DRAO to do the testing.
- Brent has forwarded questions re: Meritec Cables to Al Takasaki at PWGSC, who forwarded the questions to Meritec. Takasaki is waiting for a reply.

Dave Fort

- Updated the Programmers' Guide; changes are highlighted in yellow.
  - → Brent updated the tables re: memory map.
- Bringing the FPGAs up to the latest version of Xilinx.

- Adding detail to the Station Board Test Plan.

Zoran Ljusic

- The schematics for the new Delay Module are done.
  - → Started the layout, received the stack up from Coretec.
  - → Will take a break so that Zhang can use the software.
- Updated the Output FPGA RFS and released it to the web.
- Good news from Vicor; we should have the devices by Q1 2007 or earlier.

Action

- → Zoran to inquire re: longer pins.

Zhang Heng

- Completed the Correlator Chip Test Board schematic.
  - → Starting PAR; trying to use the auto-route to speed up the process.

Ralph Webber

- Working on the System BOM; identifying parts and getting pricing.
  - → System BOM Review scheduled for 2:00 pm (PDT) Tuesday, October 10.
  - → Mechanical/Electrical Rack Review scheduled for 9:30 am (PDT) Tuesday, October 10. NRAO to participate as interested.
- Spoke with Steve at Agilent re: testing with the scope. It should work but it doesn't.

Mark Halman

- Finished the BGA socket design.
  - → Visited ASDAC in Kelowna and delivered the drawings.
  - → The sub-section will be manufactured and DRAO charged only for time and materials.
  - → Mark to get a quote.
- Worked on preparing drawings for the racks.
  - → Triple E ejectors are not working as the racks are not built to spec (manufacturer added 40 thou slop).
  - → The dummy boards are exactly right.
  - → The guide rails are mis-machined by 20 thou.

Brent

- → Really need to tighten up on the specs and acceptance criteria in the RFP.
- → Mark is investigating the consequences of adding more weight to the rack overall.
- → Need a stronger front rail or move the front rail back ~1.5".
- → Ran an analysis for the section and found a slight bending on the sub-rack load bar.

Brent

- Need to consider the placement of the Phasing Board.
  - → Could make the duct shorter to allow for a 6U crate.

Project Management

Bryan Anderson

- Bryan retired Friday, September 29….Congratulations!
  - → No replacement in sight.
  - → Plans to stay on at Jodrell Bank with emeritus status.