EVLA Weekly Meeting Notes

Meeting Date 2005Oct12

Meeting Participants

Penticton Amy, Brent, Dave, Mark, Sonja, Zhang, Zoran

Socorro Kevin, Pat

Near-term Milestones and Target Dates

Please refer to the attached Gantt Chart for updates. Summary of significant changes are noted here.

- Circuit Board RFP – Phase II – All Bids Submitted: delete milestone
- Baseline Board BGA Socket Investigations – date is 16Sep, NOT complete.
- Reset Baseline Board PCB Place and Route complete to Oct.19
- Reset Baseline Board PCB Signal Integrity & Timing Analysis Complete to Nov. 5
  - → Cannot sign-off on Baseline Board until we get sign-off on correlator chip pinout.
  - → ModelSIM SE License expires Oct. 15. Getting another quote and another 2 month license.
- Reset Baseline Board Mechanical Design Complete to Nov. 5
- On-The-Sky Test Plan Complete to be pushed way out, date unknown.
- Final Correlator Chip ASIC Verification Testing Complete: latest Dec. 15
- Reset Station Board PCB Signal Integrity & Timing Analysis Complete to end of November

Penticton

Brent Carlson

- Correlator chip testing: full compile of gate-level testing.
- Appears the gate-level simulation is running for a different phase of time than the RTL simulation. This gives slightly different results which needs to be figured out.
- BreconRidge has asked for concept drawings for the baseline board (Brent) and station board (Dave) heat sinks.
- Had a telecon with BreconRidge yesterday about thermal mechanical analysis on the heat sinks. BreconRidge is going to quote us on an engineering study on the heat sinks.
- Had meeting yesterday to discuss software requirements and scheduling for prototype testing, came up with the idea of writing a programmers' guide. Will start working on it immediately.
- Worked on templates for assembly notes and release notes.
- Reminder that Amy is the point of contact for file transfers with BreconRidge.
- Working with Ralph to get ESD safety measures setup in the screened room. Want everything in place by the end of November.

Dave Fort

- Worked on programmers' guide.
- Worked on station board heat sink concept drawing.
- Working on delay module test vector environment. Wrote software for the outside information needed to create test vector sets.

→ Brent: Are you going to define format of file?
→ Dave: May write noise generator from scratch.

Zoran Ljusic
- Worked more on station board placement and fine tuning.
- Did some investigation of Artesyn modules. Need to find out how to ground these parts, the manufacturer's application note says it has to be grounded to the chassis.
- Waiting for stackup on station board from BreconRidge, then will get into more detail on station board again.

Zhang Heng
- Almost completed the baseline board place and route. About one week left, then will begin simulation.
- Have to put some voltage and temperature sensors in the right place.
- Today will give Mark hole locations so that he can continue with the mechanical design.

Sonja Vrcic
- Worked on station board GUI main display.
- Created a list of software tasks required for prototype testing.
- We reviewed this list in a meeting yesterday. The list has now been updated.
- Action: Send updated list to Kevin.
- Action: Update the schedule and the test plan document. Then get the test plan put on the web.

Mark Halman
- Was not here last week.
- Received rack drawings from Triple E for reviewing.
  → Brent: Thickness of boards is limited to 125 thou due to aspect ratio.
  → Dave: Need additional support for the heat sink on the station board. Requires further discussion.

Amy Fink
- Worked on baseline board BOM information to send to BreconRidge, some minor updates/fixes.
- Was away for a couple of days last week.
- BreconRidge phoned this morning, they want to take version control for the bare PCB and assembled PCB out of the WIDAR part number.
  → Brent: Ok, we have to do what they want. Maybe it can be in the manufacturer's part number.

Socorro

Kevin Ryan
- Got initial edition of correlator chip GUI done.
- Working on LTA Controller GUI now.
- Will miss the next two meetings, on vacation.

Pat Van Buskirk
- Bill/Brian going to call to discuss software requirements with Brent/Sonja. Need some changes to the CBE.
  → Sonja: Had meeting yesterday to discuss reorganization of software schedule.
  → Brent: Discussed defining output data format so we can get Dave Del Rizzo to make data graphs. So we need to find out CBE file formats.
- Action: Send latest CBE document to Sonja and Donna.
- Was told not to work on anything on the backend right now.

ID	Task Name	Resource	% Comp
311	Milestone: Enclosure Specs Document Complete	MH,RW	0%
1433	Milestone: Circuit Board RFP - Final Vendor Selected		100%
1431	Milestone: Circuit Board RFP - Site Visit		100%
1432	Milestone: Circuit Board RFP - Phase II - All Bids Submitted	BC	100%
251	Milestone: Baseline Board BGA Socket Investigations Complete	RW	0%
317	Milestone: 12U Sub-Rack Specs Document Complete		0%
315	Milestone: 6U Sub-Rack Specs Document Complete		0%
319	Milestone: 9U Duct Specs Document Complete	RW	0%
641	Milestone: Correlator Chip ASIC Post-Simulation Report Complete	RS	0%
243	Milestone: Baseline Board PCB Place and Route Complete	ZH	0%
313	Milestone: Memo 25 Complete		0%
759	Milestone: Station Board Prototype Test Interface Complete	SV	0%
517	Milestone: Station Board Test Case Verification Matrix Complete	DF	0%
523	Milestone: Baseline Board Test Case Verification Matrix Complete	BC	0%
245	Milestone: Baseline Board PCB Signal Integrity & Timing Analysis Complete	ZH	0%
247	Milestone: Baseline Board Mechanical Design Complete	MH	0%
646	Milestone: Correlator Chip Gate-Level Net List Received	EC	0%
1434	Milestone: Circuit Board RFP - Contract Signed		0%
529	Milestone: On-The-Sky Test Plan Complete	BC	0%
648	Milestone: Final Correlator Chip ASIC Verification Testing Complete	RS	0%
153	Milestone: Station Board PCB Signal Integrity & Timing Analysis Complete	ZL	0%
779	Milestone: Baseline Board Prototype Test Interface Complete	KR	0%
521	Milestone: Correlator Chip Test Case Verification Matrix Complete	BC	0%
1066	Milestone: Baseline Board In-House Test Software Complete	KR	0%
541	Milestone: 12U Test Beds Designed, Spec'd, and Built	RW,MH	0%
572	Milestone: Delay Module Prototype Assembly Complete	EC	0%
815	Milestone: CMIB Communication Infrastructure Complete	BR	0%
155	Milestone: Station Board Mechanical Design Complete	RW	0%
345	Milestone: Rack Electrical Design Complete	RW	0%
753	Milestone: Station Boards MAHs Complete		0%