EVLA Weekly Meeting Notes

Meeting Date: 31Mar2004
Meeting Participants:
Penticton: Amy, Brent, Dave, Rick, Sonja, Zhang, Zoran
Socorro: Tom, Bruce
Jodrell Bank: Simon

Schedule Discussion – Penticton:

Brent Carlson:
- What is the status of the Ethernet transmitter RFS? Right now the draft should be done but there is still 5h left.
  → It is in progress. 50% complete.
- Have you started re-design work on the recirculation controller? Supposed to start 2 weeks ago.
  → Have not started yet. Going to finish the Ethernet transmitter RFS first.
- The LTA Controller Pinout Definition task has 25h left, 0h done, and is supposed to be complete? Status?
  → Still working on final place and route, then will do pinout definition
- You have 18h left (7h done) on the Correlator Chip ASIC Verification Plan. Rick is finished. How much have you really done, what's left?
  →May have to modify test plan. No real answer given.

Dave Fort:
- You are scheduled to be working on the Autocorr FPGA right now, but are working on the FIR Filter still. Do you intend to finish the filter first then move on to the autocorr FPGA, should I rearrange the schedule?
  → Yes, working on finishing the filter first.

Zoran Ljusic:
- Station Board PCB Schematic Design & Preliminary PAR [BDP-2]: You should have about 25h left, correct?
  → Yes. Stuck right now waiting for Altera parts for ODA library.

Zhang Heng:
- The station data fanout board design review is still to be held today?
  → Yes
- Last week you said Lawrence was done working on the data feedthru backplane, but you wanted to change something. Did you change anything? What is his status?
  → Yes, changed things, he is finished with new changes too.

Sonja Vrcic:
- We will just continue schedule discussions offline.

Rick Smegal:
- Last week you said there was approximately 125h left on the Correlator Chip ASIC Functional Verification task instead of the 180h that was scheduled. You did 5h this pas week, so can I change it to 120h left now, or do you still want to leave it larger?
  → Yes you can change it.

General Discussion – Penticton:

DRAO:

Event	• Zoran brought cookies
Comments	• The correlator chip tendering process is closed. A few bids are in, none are compliant. Cannot discuss it much at

this stage.

- There is a big discrepancy in power dissipations estimates from different companies, one says 3 watts and one says 12 watts. Most likely this will result in descoping the chip: 5-level → 3-level phase rotator (2% sensitivity loss). The 4-bit multiplier also chews up a lot of power, however the dynamic range of the correlator requires a 4-bit multiplier therefore we may have to go to liquid cooling or consider cutting the number of lags in half.
- Big range in cost estimates.
- Companies suggested some changes on correlator chip tests.

Question (Tom)
- How many bids were there?

Answer (Brent)
- There were three companies that could possibly do it.

Brent Carlson:

Accomplishments
- Solved most of the problems with the LTA Controller DDR RAM controller.

Action
- Send out current draft of Gbit Ethernet RFS to Bruce and Tom so they can confirm the requirements before any further work is done.

Dave Fort:

Accomplishments
- Packaged up filter design and sent it off to Atmel and LSI Logic. Haven't heard anything back yet.
- Filter functional simulation continuing.

Comments
- Got Verilog 2001 book from the library. Will buy one when next fiscal year starts.
- Got list of prices from Xilinx on Pro series chips. The P-50 for the FIR is about $1200, therefore the prototype would be about $2400.

Zoran Ljusic:

Comments
- Didn't finish connector output pin assignment yet.
- Had to assign pins from Revnell's board. Decided on connectors. Still have to define some protocols.
- Going to play with placement before handing board off to Lawrence. This work will come under the PCB place and route task, not under the schematic design and preliminary PAR task.
- Will work on input chip in meantime while waiting for Altera parts.

Zhang Heng:

Accomplishments
- Finished Station Data Fanout Board Schematic Design.

Comments
- Will review Station Data Fanout Board design after this meeting before sending it off to Lawrence.
- Will start work on the baseline board PCB by the end of this week.

Sonja Vrcic:

Accomplishments
- Spend yesterday looking at schedule and changed some things. Seem to be going more or less according to plan. Separated tasks into prototype and production sections.
- Working on software model and configuration software more.

Question
- Regarding Station Board: How many ports are there going to be?

Answer (Dave)
- Think it's possible to have 2 instead of one, if it doesn't cost too much.

Related Comment (Brent)
- It's all a matter of pricing.

Rick Smegal:

Comments
- Assessing what order to run tests in.

Accomplishments
- Ran long test.

Schedule Discussion – Socorro:

Tom Morgan:

- Software Architecture Refinement, you were marked down for 25h, but have done 0h. Did you finish your additions? What is the status?
  → Was actually done in another way.
- Correlator Backend V1.0 Communication Infrastructure should be well underway. Schedule says 156h done, 194h remaining, but I haven't received any time updates this month.
  → Haven't spent any time on it in the last month. Numbers seem about right.

Bruce Rowen:

- CMIB Generic Prototype Software Development: 12% complete, 265h remaining? Do these numbers sound right? What is the status?
  →The estimates seem to be correct.
- TIMECODE Prototype Preliminary Driver supposed to be done. Only 10h done, 40h left! What is the status?
  → The numbers are correct. Need to set up test interface.
- What % of your time are you spending on the correlator? In the future?
  → Spending about 70% of time on correlator now. Don't predict it will go up to 100% any time soon.

General Discussion – Socorro:

Tom Morgan:

Comments	• Working full time on EVLA software design right now. Will continue to do so all the way into may. Won't be working on the backend until this is done. • Backend needs overall design to continue anyway.
Question (Dave)	• What will your backend look like physically?
Answer	• 64 computers, dual CPU (# computers may change in future). Right now in 2 racks, by 2007 may be one rack. With current technology it will use three switches

Bruce Rowen:

Comments	• Looking close at Linux 2.6 Kernel • Will start sending in time again this week