EVLA Weekly Meeting Notes

Meeting Date: 29SEP2004
Meeting Participants:
Penticton: Amy, Brent, Dave, Zoran, Mark
Socorro: Tom
Jodrell Bank: Bryan, Simon

Schedule Discussion – Penticton:

Zoran Ljusic:
- You have 0 hrs left for Station Board PCB Place & Route [BDP-3], is this ok, or do you want more hours?
  → Need 100h, won't work on it right now.

Mark Halman:
- You only marked down 10hrs worth of work last week. Were you busy doing other stuff outside of the project or do you need to have new tasks included in the schedule.
  → Neither, just entered times late…just before this meeting.

General Discussion – Penticton:

DRAO:

Event	• Mark brought donuts.
Absences	• Rick – On holiday. Ralph – On holiday.

Brent Carlson:

Comments	• Peter finished draft version of memo looking into correlator chip investigations. Faxed to P. Napier and to Simon. Waiting for some feedback. Then go to RFP & get it onto purchasing agent. • Will be having CDR of correlator chip once vendor is chosen because we want participation of vendor. •
Question (Tom)	• What are we looking at for date for prototypes?
Answer (Brent)	• Depends on vendor
Question (Tom)	• How much could it vary?
Answer (Brent)	• Could vary by a couple of months, earliest prototypes could be about mid-April next year.
Accomplishments	• Writing system level test & verification plan. Talking about various stages of the project. Discussing what the prototype correlator will look like. Want peer review of this before releasing. • Have updated prototype quantities, a bit different from what we decided last week. Amy will have to use the new numbers once this document is released.

Dave Fort:

Accomplishments	• Got stage I of Filter chip to place and route by itself but constrained to the area of the chip he wants to put it in. • Rest of the week was spent on stage II. Wouldn't place and route, so made some changes, basically daisy chained it and now it PAR's easily, but still constrained to a particular part of the chip. • Had to cut down slices because they were impeding things.
Comments	• Becoming more and more convinced this is like to be done. • Haven't seen any numbers from Altera yet.

Zoran Ljusic:

Accomplishments	• More input chip post place and route simulations • Did some station board placement and preparation for place and route by Lawrence.

- Started reading and thinking about output chip.

Comment
- Have to wait for Zhang to finish his board because only one Expedition PCB license, then can work on station board more.

Action
- Will talk to mentor guys to see if we can rent a license for a couple of months, as it is too expensive to buy a second license.

Zhang Heng:

Comments
- Finished SDFB PCB design.
- Lawrence finished final changes on SDFB except the art work.
- Continuing working on TGB PCB design now, need a few days to finish it.

Mark Halman:

Accomplishments
- Did some drawings – sent them out to vendors to get prices.
- Did some more boards up.
- Had review yesterday of thermal test rack document. Did some fixing up of that document.

General Discussion – Socorro:

Tom Morgan:

Comment
- Still working on the backend code.

Question (Brent)
- Are you working on the UVFITS writer?

Answer (Tom)
- Not yet, still reacquainting himself with backend code after being away from it for about 6 months

Comment (Brent)
- The writer needs the ability to look at raw data, plot lag data, and plot Fourier transform of that.

General Discussion – Jodrell Bank:

Simon Garrington:

Comment
- Received faxed document on correlator chip vendor selection process. Will look through it and provide feedback in the next couple of days.

Question
- Are the prototype chips included in the NRE?

Answer (Brent)
- Yes, sort of. We demanded 200 prototype chips but some vendors quoted differently, not all included in the NRE.

Related Comment
- This needs to be made clearer in a column in the spreadsheet.