EVLA Weekly Meeting Notes

Meeting Date: 24Nov2004
Meeting Participants:
Penticton: Amy, Brent, Dave, Mark, Peter, Ralph, Rick, Sonja, Zhang, Zoran
Socorro: Did Not Participate
Jodrell Bank: Bryan, Simon

General Discussion – Penticton:

DRAO:

Goodies	• Mark brought donuts
Status	• The correlator chip contract bidding has received only one question from bidders so far and no request for any extensions have been received.
Suggestion (Brent)	• Perhaps we should have a monthly meeting to go over everything we want to buy and what decisions need to be made or have changed in detail.
Action (Amy)	• Decide when this meeting should be and how it should run.

Brent Carlson:

Comments	• Working on gate level simulation of the recirculation controller in a Stratix II. It is misbehaving so sent it off to Altera to sort things out.
	• Finished coding the Gbit Ethernet Chip. Hopefully generated the final pinout file. Haven't tested anything yet.

Dave Fort:

Comments	• Don't know if the filter chip post place and route simulation will work yet, not finished. Have the model but have not actually tired it yet.
	• Switching time in schedule back to FPGAs, marked ASIC tasks down to 0 hrs.
	• When Xilinx ran stage II simulation they tried a bunch of different clock rates to see where things start to go wrong. It was at ~600MHz which should be ok since we are only going for 256MHz.
Question (Brent)	• Do you think it is a good use of your time to continue on the FIR chip right now still? Or is it better to work with Zoran on the station board?
Response (Dave)	• Things are going fine on the board and there is still a lot of simulation to do on the FIR chip. Also working on the wideband autocorr chip.
Question (Peter)	• What's Lawrence doing?
Answer (Zoran)	• Waiting for me.
Response (Dave)	• Don't think I can speed the PCB design process up.
Question (Brent)	• Do we want to have a preliminary review of the station board schematic before we send it to Lawrence?
Response (Zoran)	• Yes, seems like a good idea.

Zoran Ljusic:

Comments	• More work done on the station board schematics. Running Boardlink and swapping pins.

Zhang Heng:

Comments	• Baseline board schematic design: Built hierarchy and trying to connect together.
	• Next, choose what kind of heat sink we use and where to put it.
	• Need to know the hole locations for the monolithic heat sink.

Sonja Vrcic:

Comments	• Did some changes to Memo 18. Will incorporate Peter's suggestions and release it this week.
	• Development in CVS: Socorro is now trying to allow access to our server. Hopefully if they fix this, it will also fix the

access problem with project central.

Rick Smegal:

Comments

- Working on correlator chip test reports and updating test plans.
- Talked to Dave about FIR filter testing, sent test specification document.

Ralph Webber:

Comments

- Mostly worked on ACSIS this last week.
- Did some work on rework guideline document.
- Hopefully can start tests today with Mark. Waiting for Paul to hook up 100A supply.
- Logic Analyzer came in. Checking shipment later today.

Mark Halman:

Comments

- Yesterday made another jig up. Tests didn't turn out good, the large heat sink out-performs the individual heat sinks be ~10°C at the end (hottest heat sink).
- Did test and debug all the boards last week.

Peter Dewdney:

Comments

- Helped with Memo 18. Would be good to have a meeting to go over it.

Comment (Brent)

- Perhaps after the correlator chip CDR in January.

Action (Amy)

- Send out possible short software F2F notice.

Action (Rick)

- Should get Rick's document released and out there soon so everyone gets an idea of what is going to happen in the correlator chip CDR.