EVLA Weekly Meeting Notes

Meeting Date: 21Apr2004
Meeting Participants:
Penticton: Amy, Brent, Dave, Rick, Sonja, Zhang, Zoran
Socorro: Tom, Bruce
Jodrell Bank: Bryan, Simon

Face-To-Face Meeting – June 24/25:

- Brent has made a draft agenda and will be sending it out.
- The focus of this meeting will be mostly system issues.

Schedule Discussion – Penticton:

Brent Carlson:

- Is the LTA Controller Final Place and Route complete? It is marked as such in Project Central.
  →Yes.
- The correlator chip functional verification task has ~10h left for you. Does this seem ok?
  →Yes, keep this as it is.

Zoran Ljusic:

- I have transferred the remaining 16.25h of the Input Chip RFS from Dave to you, however nothing has been reported being done even though you have moved on to Coding & Preliminary PAR. Is this true?
  → Yes, no work done on the RFS yet.
- Station Board PCB Schematic Design & Preliminary PAR [BDP-2] has 0h left, is it really done?
  → No, still need FIR chip to be decided. Will be at least another week or two worth of work.

Zhang Heng:

- TIMECODE Generator Board PCB Schematic Design & Preliminary PAR [BDP-2] has 15h left on this task. Is this correct? Will you work on this after you have finished the mechanical design?
  → Actually more like one week. Yes it will be after the mechanical design.
- The TIMECODE Generator Board Mechanical design task has 15h left, does this seem correct?
  → Yes.

Sonja Vrcic:

- Already has 0h left on the Station Board Prototype Configuration Software, but you marked that last week you did 29h additional work on this task. Is it really complete now?
  →Probably done.

General Discussion – Penticton:

DRAO:

Comment
- Correlator chip is feasible to put in LSI Logic rapid chip. Unfortunately it is a $130 part (putting us $1.5M over budget). Going to issue a contract to work on dropping the gate count.

Brent Carlson:

Accomplishments
- LTA Controller place and route finished. Should be about 1.1W power dissipation.
- Finished GBit Ethernet Chip RFS.

- Ethernet Chip Preliminary design done. Will send out.

Comment
- Now working on Recirculation controller design changes.

Dave Fort:

Comments
- Talked to LSI Logic about going directly to structured ASIC with the filter chip. Therefore stripping down coding and reading up to see if it is possible. Got data sheets on their chips, reading through them.
- Saw quotes from the, the chip would still be over $100, which is budget price ($110 - $140 range) because of lower quantity.
- Talked to Xilinx guy, he was supposed to send code to Atmel. Didn't yet. Still waiting for response on whether or not we can go to FPGA, do they have direct conversion process or not?

Comment (Brent)
- Goal is to as soon as possible come up with a pinout definition for both filter chip and the correlator chip.

Zoran Ljusic:

Comments
- Making progress with the last chips on the station board and hooking up connectors
- Going to do initial placement (assign 1 month for now) before sending it to Lawrence.

Zhang Heng:

Accomplishment
- Finished Timecode cable specification

Comment
- Haven't got word back from Lawrence on Station Data Fanout Board

Sonja Vrcic:

Comments
- Was working on baseline board prototype software as well.
- Hoping to have all MCCC prototype stuff ready by June meeting

Rick Smegal:

Comments
- Didn't put time down because he was writing a number of functions to read output frames from correlator chip, which was not in schedule. This allows automation of process of looking at output frames.

Question (Brent)
- Are you going to have some sort of user manual for this code?

Answer
- Mostly commented scripts, but can make user manual if desired

Schedule Discussion – Socorro:

Bruce Rowen:

- Just need hours from last week and response to schedule changes.

General Discussion – Socorro:

Bruce Rowen:

Comments
- James was supposed to get back to him on Project Central but has not yet.
- Working on CVS. It is up and running. Checking initial software versions into it.
- Have CVS setup for DRAO. Can set up account to start using it now.
- Using Eclipse → works well for automating checkout of CVS. It is structured for Java development

Comment (Sonja)
- Will talk to Peter Cimbaro about setting everything up.