EVLA Weekly Meeting Notes

Meeting Date: 06Oct2004
Meeting Participants:
Penticton: Amy, Brent, Dave, Ralph, Mark, Sonja, Zhang, Zoran
Socorro: Tom, Bruce
Jodrell Bank: Bryan

Schedule Discussion:

- See Below

General Discussion – Penticton:

DRAO:

- Ralph brought treats.

Brent Carlson:

- Got the correlator chip Statement Of Work in a position to quantify risks very well. Thinking of having selection committee to evaluate bids. Individuals can then each put in their own judgment on the bids.
- Finished system test and development plan.

Dave Fort:

- Worked on the Station Board filter chip RFS more since the review.
- Have about 25 errors left in attempting to place and route the FIR in Virtex IV, however have had to give some things up. Suspect will get rid of errors but have to make sure to go back and check that nothing taken out was important.

Zoran Ljusic:

- Learning about station board output chip.
- Contacted guys from ODA about Virtex IV parts.

Zhang Heng:

- Finished TIMECODE Generator design and sent back to Lawrence yesterday.
- When Lawrence fixes it and sends it back will begin with Station Data Fanout Board simulation.

Sonja Vrcic:

- Working on memo 18 – created a couple diagrams. Hopefully finished soon.
- Received email from Bill Sahr that said they made decision to use message based architecture.
- Received transition plan (draft version).

Ralph Webber:

- Was on vacation last week.
- Got Hammond test rack. Can start putting some stuff in it.
- Nailed down requirements for rework/x-ray machine. Will send off to Kathy today.
- Work on thermal cooling document today.
- Hopefully telecon with liquid cooling guys.

Mark Halman:

- Same as Ralph. Chasing down Knuerr who is an alternate supplier of liquid cooling technology.
- Updating the rack enclosure cooling test and verification plan to include closed cycle cooling.
- Heat sinks arrived. Chopped down, ready to be put on board.
- Interface material showed up from Aavid. They left the manufacturers name on so we can look them up and order

rolls of the stuff directly and cut it ourselves. Hopefully this will reduce cost.

- One of the companies who have heavy duty test rack has a 6U rack we can borrow. Will also send section of T-bar front.
- Found reference from enclosure manufacturer giving rules of thumb on heat flow.

General Discussion – Socorro:

Tom Morgan:

- The backend is up and running. Giving correct output.
- Started yesterday working on FITS output problem. Making this priority for next little while.

Bruce Rowen:

- On vacation past 6-7 days and next week.
- Run into snag with module loading on 2.6 kernel.

Brent Carlson

Task Name	Start Date	Finish Date	% Comp.	Total Work	Remaining Work	Comments
FIR Filter RFS Design Review	13-Sep-2004	15-Sep-2004	100%	5 hrs	0 hrs	
MCB Interface & Clock Selector FPGA Preliminary Design [FDP-1]	2-Dec-2004	15-Dec-2004	0%	45 hrs	45 hrs	
MCB Interface & Clock Selector FPGA Milestone 1	15-Dec-2004	15-Dec-2004	0%	0 hrs	0 hrs	
MCB Interface & Clock Selector FPGA RFS Development [FDP-2]	15-Dec-2004	28-Dec-2004	0%	45 hrs	45 hrs	
MCB Interface & Clock Selector FPGA Milestone 2	28-Dec-2004	28-Dec-2004	0%	0 hrs	0 hrs	
Ethernet Transmitter FPGA Coding & Preliminary PAR [FDP-3]	17-May-2004	24-Nov-2004	15%	293 hrs	260.75 hrs	
Ethernet Transmitter FPGA Milestone 3a	8-Jul-2004	8-Jul-2004	0%	0 hrs	0 hrs	
Ethernet Transmitter FPGA Milestone 3b	24-Nov-2004	24-Nov-2004	0%	0 hrs	0 hrs	
MCB Interface & Clock Selector FPGA Coding & Preliminary PAR [FDP-3	28-Dec-2004	8-Feb-2005	0%	150 hrs	150 hrs	
MCB Interface & Clock Selector FPGA Milestone 3a	25-Jan-2005	25-Jan-2005	0%	0 hrs	0 hrs	
MCB Interface & Clock Selector FPGA Milestone 3b	8-Feb-2005	8-Feb-2005	0%	0 hrs	0 hrs	
LTA Controller FPGA Final Place & Route [FDP-4]	1-Mar-2004	15-Jul-2004	100%	73.5 hrs	0 hrs	
LTA Controller FPGA Milestone 4	17-Mar-2004	17-Mar-2004	100%	0 hrs	0 hrs	
Ethernet Transmitter FPGA Final Place & Route [FDP-4]	24-Nov-2004	1-Dec-2004	0%	25 hrs	25 hrs	
Ethernet Transmitter FPGA Milestone 4	1-Dec-2004	1-Dec-2004	0%	0 hrs	0 hrs	
Ethernet Transmitter FPGA Pinout Definition [FDP-5]	1-Dec-2004	2-Dec-2004	0%	5 hrs	5 hrs	
Ethernet Transmitter FPGA Milestone 5	2-Dec-2004	2-Dec-2004	0%	0 hrs	0 hrs	
Recirculation Controller FPGA RFS Update [FDP-6]	28-Apr-2004	10-Sep-2004	100%	22 hrs	0 hrs	
Recirculation Controller FPGA Milestone 6	10-Sep-2004	10-Sep-2004	100%	0 hrs	0 hrs	
Ethernet Transmitter FPGA RFS Update [FDP-6]	2-Dec-2004	3-Dec-2004	0%	5 hrs	5 hrs	
Ethernet Transmitter FPGA Milestone 6	3-Dec-2004	3-Dec-2004	0%	0 hrs	0 hrs	
GBit Data Cable Design & Specs	11-Nov-2002	14-Apr-2004	99%	76 hrs	10 hrs	
Gbit Data Cable Design & Specs Complete	14-Apr-2004	14-Apr-2004	0%	0 hrs	0 hrs	
Specify Rework Equipment	1-Jun-2001	24-Aug-2004	100%	2 hrs	0 hrs	
Specify Prototype Test Equipment	1-Jun-2001	30-Sep-2004	35%	25 hrs	10 hrs	Brent done his part.
Correlator Chip ASIC Acceptance Test & Verification Plan	15-Jun-2003	9-Sep-2004	92%	25 hrs	1.25 hrs	
Correlator Chip ASIC Functional Verification	5-Feb-2004	30-Nov-2004	50%	64.5 hrs	2 hrs	
Correlator Chip ASIC Critical Design Review	27-Oct-2004	3-Nov-2004	0%	25 hrs	25 hrs	Not until Dec. or maybe Jan.
Assemble Correlator Chip ASIC Design & Test-Bench Package for Manuf	12-Jul-2004	23-Jul-2004	100%	48 hrs	0 hrs	
Correlator Chip ASIC Design & Test-Bench Package Complete	14-Jul-2004	14-Jul-2004	100%	0 hrs	0 hrs	
Review and Acceptance of Correlator Chip ASIC Prototype	29-Mar-2004	14-Sep-2006	81%	15 hrs	6 hrs	
MCCC Prototype Test GUI Peer Review	17-Sep-2004	17-Sep-2004	0%	2 hrs	2 hrs	Should be complete
MCCC Design Document Review	17-Sep-2004	2-Nov-2004	33%	5 hrs	5 hrs	Hrs should be under GUI review.
Correlator Chip ASIC Contracting [CP]	8-Sep-2003	15-Oct-2004	39%	170 hrs	130 hrs	

Dave Fort

Task Name	Start Date	Finish Date	% Comp.	Total Work	Remaining Work	Comments
Input FPGA RFS Development [FDP-2]	2-Sep-2003	30-Sep-2004	51%	35.25 hrs	11.25 hrs	Leave for now.
Input FPGA Milestone 2	30-Sep-2004	30-Sep-2004	0%	0 hrs	0 hrs	
Output FPGA RFS Development [FDP-2]	2-Sep-2003	3-Dec-2003	63%	35 hrs	22.5 hrs	Give most hrs to Zoran.
Output FPGA Milestone 2	3-Dec-2003	3-Dec-2003	0%	0 hrs	0 hrs	
Autocorr FPGA Coding & Preliminary PAR [FDP-3]	12-Nov-2003	4-Nov-2004	36%	164.5 hrs	131 hrs	Wait until FIR chip decided.
Autocorr FPGA Milestone 3a	10-Dec-2003	10-Dec-2003	0%	0 hrs	0 hrs	
Autocorr FPGA Milestone 3b	4-Nov-2004	4-Nov-2004	0%	0 hrs	0 hrs	
Output FPGA Coding & Preliminary PAR [FDP-3]	5-Nov-2004	16-Dec-2004	0%	150 hrs	150 hrs	
Output FPGA Milestone 3a	2-Dec-2004	2-Dec-2004	0%	0 hrs	0 hrs	
Output FPGA Milestone 3b	16-Dec-2004	16-Dec-2004	0%	0 hrs	0 hrs	
Filter FPGA Milestone 4	21-May-2004	21-May-2004	25%	0 hrs	0 hrs	Set as complete
Autocorr FPGA Final Place & Route [FDP-4]	17-Dec-2004	20-Jan-2005	0%	125 hrs	125 hrs	
Autocorr FPGA Milestone 4	20-Jan-2005	20-Jan-2005	0%	0 hrs	0 hrs	
FIR Filter ASIC Conversion Work	7-Jun-2004	2-Jul-2004	100%	51.25 hrs	0 hrs	
FIR Filter ASIC Conversion Work Complete	2-Jul-2004	2-Jul-2004	100%	0 hrs	0 hrs	
FIR Filter Chip Virtex IV Investigations	26-Jul-2004	15-Oct-2004	74%	172 hrs	50 hrs	
FIR Filter Chip Virtex IV Investigations Complete	15-Oct-2004	15-Oct-2004	0%	0 hrs	0 hrs	
FIR Filter RFS Design Review	13-Sep-2004	15-Sep-2004	100%	10 hrs	0 hrs	
FIR Filter RFS Design Review Complete	15-Sep-2004	15-Sep-2004	0%	0 hrs	0 hrs	Mark as complete
FIR Filter Chip ASIC Consulation	30-Aug-2004	29-Sep-2004	9%	50 hrs	49 hrs	
FIR Filter Chip ASIC Acceptance Test & Verification Plan Complete	15-Dec-2004	15-Dec-2004	0%	0 hrs	0 hrs	
FIR Filter Chip ASIC Functional Verification	25-May-2004	11-Feb-2005	47%	250 hrs	95 hrs	
FIR Filter Chip ASIC Functional Verification Complete	11-Feb-2005	11-Feb-2005	0%	0 hrs	0 hrs	
Station Board PCB Schematic Design & Preliminary PAR [BDP-2]	13-Nov-2003	27-Jul-2004	96%	45 hrs	24.25 hrs	Cut down to 10 hrs.
Board Integration Test Plan	6-Sep-2004	31-May-2005	30%	25 hrs	23 hrs	
Board Integration Test Plan Complete	31-May-2005	31-May-2005	0%	0 hrs	0 hrs	
MCCC Prototype Test GUI Peer Review	17-Sep-2004	17-Sep-2004	0%	2 hrs	2 hrs	Mark as complete
MCCC Design Document Review	17-Sep-2004	2-Nov-2004	33%	5 hrs	3 hrs	Hrs should be under GUI review

Zoran Ljusic

Task Name	Start Date	Finish Date	% Comp.	Total Work	Remaining Work	Comments
Input FPGA RFS Development [FDP-2]	2-Sep-2003	30-Sep-2004	51%	32.5 hrs	2.5 hrs	About right
Input FPGA Milestone 2	30-Sep-2004	30-Sep-2004	0%	0 hrs	0 hrs	
VSI FPGA Phase I RFS Development [FDP-2]	22-Oct-2004	27-Oct-2004	0%	20 hrs	20 hrs	
VSI FPGA Phase I Milestone 2	27-Oct-2004	27-Oct-2004	0%	0 hrs	0 hrs	
Input FPGA Coding & Preliminary PAR [FDP-3]	5-Apr-2004	14-Sep-2004	100%	230 hrs	0 hrs	
Input FPGA Milestone 3a	21-Apr-2004	21-Apr-2004	100%	0 hrs	0 hrs	
Input FPGA Milestone 3b	27-Aug-2004	27-Aug-2004	75%	0 hrs	0 hrs	
VSI FPGA Phase I Coding & Preliminary PAR [FDP-3]	28-Oct-2004	1-Dec-2004	0%	125 hrs	125 hrs	Won't be doing any design on
VSI FPGA Phase I Milestone 3a	18-Nov-2004	18-Nov-2004	0%	0 hrs	0 hrs	this chip. Get rid of tasks.
VSI FPGA Phase I Milestone 3b	1-Dec-2004	1-Dec-2004	0%	0 hrs	0 hrs	
Input FPGA Final Place & Route [FDP-4]	15-Sep-2004	5-Oct-2004	0%	75 hrs	75 hrs	Mostly done. Leave hrs in case
Input FPGA Milestone 4	5-Oct-2004	5-Oct-2004	0%	0 hrs	0 hrs	of possible Virtex IV work.
Decode FPGA Final Place & Route [FDP-4]	23-Jun-2004	7-Jul-2004	100%	50 hrs	0 hrs	
Decode FPGA Milestone 4	7-Jul-2004	7-Jul-2004	45%	0 hrs	0 hrs	Mark milestone complete
VSI FPGA Phase I Final Place & Route [FDP-4]	2-Dec-2004	15-Dec-2004	0%	50 hrs	50 hrs	
VSI FPGA Phase I Milestone 4	15-Dec-2004	15-Dec-2004	0%	0 hrs	0 hrs	
Decode FPGA Pinout Definition [FDP-5]	7-Jul-2004	7-Jul-2004	100%	2.5 hrs	0 hrs	
Decode FPGA Milestone 5	7-Jul-2004	7-Jul-2004	100%	0 hrs	0 hrs	Mark milestone complete
VSI FPGA Phase I Pinout Definition [FDP-5]	16-Dec-2004	16-Dec-2004	0%	3.75 hrs	3.75 hrs	
VSI FPGA Phase I Milestone 5	16-Dec-2004	16-Dec-2004	0%	0 hrs	0 hrs	
Input FPGA RFS Update [FDP-6]	22-Jun-2004	23-Jun-2004	0%	5 hrs	5 hrs	
Input FPGA Milestone 6	23-Jun-2004	23-Jun-2004	0%	0 hrs	0 hrs	
Decode FPGA RFS Update [FDP-6]	8-Jul-2004	8-Jul-2004	0%	5 hrs	5 hrs	
Decode FPGA Milestone 6	8-Jul-2004	8-Jul-2004	0%	0 hrs	0 hrs	
VSI FPGA Phase I RFS Update [FDP-6]	16-Dec-2004	17-Dec-2004	0%	5 hrs	5 hrs	
VSI FPGA Phase I Milestone 6	17-Dec-2004	17-Dec-2004	0%	0 hrs	0 hrs	
Station Board PCB Schematic Design & Preliminary PAR [BDP-2]	13-Nov-2003	27-Jul-2004	96%	595 hrs	0 hrs	
Station Board PCB Milestone 2a	23-Jan-2004	23-Jan-2004	100%	0 hrs	0 hrs	
Station Board PCB Milestone 2b	27-Jul-2004	27-Jul-2004	100%	0 hrs	0 hrs	
Station Board PCB Place & Route [BDP-3]	2-Jun-2004	8-Dec-2004	7%	135 hrs	100 hrs	
Station Board Final PCB Timing & Signal Integrity Analysis [BDP-4]	8-Dec-2004	19-Jan-2005	0%	150 hrs	150 hrs	
Station Board PCB Milestone 4	19-Jan-2005	19-Jan-2005	0%	0 hrs	0 hrs	
Output Switch & Formatter FPGA Preliminary Design [FDP-1]	9-Jul-2004	21-Jul-2004	0%	45 hrs	45 hrs	
Output Switch & Formatter FPGA Milestone 1	21-Jul-2004	21-Jul-2004	0%	0 hrs	0 hrs	
Output Switch & Formatter FPGA RFS Development [FDP-2]	22-Jul-2004	10-Aug-2004	0%	70 hrs	70 hrs	
Output Switch & Formatter FPGA Milestone 2	10-Aug-2004	10-Aug-2004	0%	0 hrs	0 hrs	
Output Switch & Formatter FPGA Coding & Preliminary PAR [FDP-3]	11-Aug-2004	5-Oct-2004	0%	200 hrs	200 hrs	
Output Switch & Formatter FPGA Milestone 3a	15-Sep-2004	15-Sep-2004	0%	0 hrs	0 hrs	

Output Switch & Formatter FPGA Milestone 3b	5-Oct-2004	5-Oct-2004	0%	0 hrs	0 hrs
Output Switch & Formatter FPGA Final Place & Route [FDP-4]	6-Oct-2004	19-Oct-2004	0%	50 hrs	50 hrs
Output Switch & Formatter FPGA Milestone 4	19-Oct-2004	19-Oct-2004	0%	0 hrs	0 hrs
Output Switch & Formatter FPGA Pinout Definition [FDP-5]	20-Oct-2004	20-Oct-2004	0%	5 hrs	5 hrs
Output Switch & Formatter FPGA Milestone 5	20-Oct-2004	20-Oct-2004	0%	0 hrs	0 hrs
Output Switch & Formatter FPGA RFS Update [FDP-6]	21-Oct-2004	21-Oct-2004	0%	5 hrs	5 hrs
Output Switch & Formatter FPGA Milestone 6	21-Oct-2004	21-Oct-2004	0%	0 hrs	0 hrs

Additional Comments

Working on station board output chip now.

Zhang Heng

Task Name	Start Date	Finish Date	% Comp.	Total Work	Remaining Work	Comments
Baseline Board PCB Schematic Design & Preliminary PAR [BDP-2]	14-Jun-2004	8-Nov-2004	15%	225 hrs	193 hrs	
Baseline Board PCB Milestone 2a	20-Jul-2004	20-Jul-2004	0%	0 hrs	0 hrs	
Baseline Board PCB Milestone 2b	8-Nov-2004	8-Nov-2004	0%	0 hrs	0 hrs	
Mentor Graphics Training - Expedition PCB Introduction	20-Sep-2004	24-Sep-2004	100%	25 hrs	0 hrs	
Mentor Graphics Training - Expedition PCB Introduction Complete	24-Sep-2004	24-Sep-2004	100%	0 hrs	0 hrs	
Baseline Board PCB Place & Route [BDP-3]	8-Nov-2004	22-Mar-2005	0%	100 hrs	100 hrs	
Station Data Fanout Board Final PCB Timing & Signal Integrity Analysis [E	15-Jul-2004	8-Sep-2004	100%	90 hrs	0 hrs	
Station Data Fanout Board PCB Milestone 4	8-Sep-2004	8-Sep-2004	100%	0 hrs	0 hrs	
Station Data Fanout Board Assembly Notes	30-Apr-2004	3-May-2004	0%	10 hrs	10 hrs	
Station Data Fanout Board Design Complete	3-May-2004	3-May-2004	0%	0 hrs	0 hrs	
TIMECODE Generator Board PCB Schematic Design & Preliminary PAR	16-Jul-2003	2-Sep-2004	100%	150 hrs	0 hrs	
TIMECODE Generator Board PCB Milestone 2a	23-Jul-2003	23-Jul-2003	100%	0 hrs	0 hrs	
TIMECODE Generator Board PCB Milestone 2b	2-Sep-2004	2-Sep-2004	100%	0 hrs	0 hrs	
TIMECODE Generator Board Final PCB Timing & Signal Integrity Analysis	9-Sep-2004	28-Sep-2004	100%	30 hrs	0 hrs	
TIMECODE Generator Board PCB Milestone 4	28-Sep-2004	28-Sep-2004	0%	0 hrs	0 hrs	
TIMECODE Generator Board Assembly Notes	29-Sep-2004	30-Sep-2004	0%	10 hrs	10 hrs	
TIMECODE Generator Board Design Complete	30-Sep-2004	30-Sep-2004	0%	0 hrs	0 hrs	
Data Feedthru Backplane Assembly Notes	17-Mar-2004	19-Mar-2004	0%	10 hrs	10 hrs	
Data Feedthru Backplane Design Complete	21-May-2004	21-May-2004	0%	0 hrs	0 hrs	
Gbit Data Cable Design & Specs Complete	14-Apr-2004	14-Apr-2004	0%	0 hrs	0 hrs	Mark as complete?
TIMECODE Generator Board Prototype Test Plan	1-Oct-2004	1-Oct-2004	0%	5 hrs	5 hrs	
TIMECODE Generator Board Prototype Test Plan Complete	1-Oct-2004	1-Oct-2004	0%	0 hrs	0 hrs	

Sonja Vrcic

Task Name	Start Date	Finish Date	% Comp.	Total Work	Remaining Work	Comments
MCCC Prototype Test GUI [SWDP]	31-May-2004	3-Sep-2004	100%	444.2 hrs	0 hrs	Mark milestone complete
MCCC Prototype Test GUI Complete	3-Sep-2004	3-Sep-2004	0%	0 hrs	0 hrs	
MCCC Prototype Test GUI Peer Review	17-Sep-2004	17-Sep-2004	0%	2 hrs	2 hrs	Review is complete
MCCC Prototype Software Complete	17-Sep-2004	17-Sep-2004	0%	0 hrs	0 hrs	Complete?
Memo 18	8-Sep-2004	30-Sep-2004	65%	110.5 hrs	0 hrs	Need a little bit more hrs.
MCCC Design Document Development	17-Sep-2004	29-Oct-2004	0%	150 hrs	150 hrs	Yes this is next.
MCCC Design Document Review	17-Sep-2004	2-Nov-2004	33%	10 hrs	10 hrs	
MCCC Software Design Document Complete	2-Nov-2004	2-Nov-2004	0%	0 hrs	0 hrs	
MCCC Error Handling [SWDP]	2-Nov-2004	14-Dec-2004	0%	150 hrs	150 hrs	
MCCC Error Handling Complete	14-Dec-2004	14-Dec-2004	0%	0 hrs	0 hrs	
MCCC Alert Message Manager [SWDP]	14-Dec-2004	8-Feb-2005	0%	200 hrs	200 hrs	

Ralph Webber

Task Name	Start Date	Finish Date	% Comp.	Total Work	Remaining Work	Comments
Station Board Mechanical Design	22-Dec-2004	19-Jan-2005	0%	100 hrs	100 hrs	
GBit Data Cable Preliminary Prototype Test	30-Sep-2004	20-Jan-2005	0%	400 hrs	400 hrs	Can't do much until we get
GBit Data Cable Preliminary Prototype Test Physical Setup Complete	25-Nov-2004	25-Nov-2004	0%	0 hrs	0 hrs	boards. Shifted until receive
Gbit Data Cable Preliminary Prototype Test Complete	20-Jan-2005	20-Jan-2005	0%	0 hrs	0 hrs	PCMC, TGB, Bkpln, SDFB.
System Cooling Investigations	19-Aug-2004	6-Oct-2004	95%	40 hrs	3.5 hrs	
System Cooling Investigations Complete	6-Oct-2004	6-Oct-2004	0%	0 hrs	0 hrs	
Recalibrate Tektronix 610 Oscilloscope	15-Jul-2004	15-Jul-2004	100%	5 hrs	0 hrs	
Test Vicor Power Module	16-Jul-2004	16-Jul-2004	100%	5 hrs	0 hrs	
Thermal Test Document	23-Aug-2004	24-Aug-2004	40%	10 hrs	6 hrs	Mark is doing this.
Thermal Test Document Complete	24-Aug-2004	24-Aug-2004	0%	0 hrs	0 hrs	
12U Sub-Rack Design & Spec	12-Aug-2004	15-Feb-2005	34%	98 hrs	88.5 hrs	
12U Sub-Rack Design & Spec Complete	15-Feb-2005	15-Feb-2005	0%	0 hrs	0 hrs	
6U Sub-Rack Design & Spec	12-Aug-2004	10-Mar-2005	42%	100 hrs	84.5 hrs	
6U Sub-Rack Design & Spec Complete	10-Mar-2005	10-Mar-2005	0%	0 hrs	0 hrs	
Rack Mechanical Design	15-Jul-2004	25-Apr-2005	56%	94 hrs	63 hrs	
Rack Mechanical Design Complete	25-Apr-2005	25-Apr-2005	0%	0 hrs	0 hrs	
Rack Assembly Notes	20-Jul-2004	30-May-2005	36%	10 hrs	9 hrs	
Design & Specify Test Beds	16-Jul-2004	21-Sep-2004	64%	44 hrs	20 hrs	
Test Beds Design & Specification Complete	21-Sep-2004	21-Sep-2004	0%	0 hrs	0 hrs	
Specify Power Supplies and Logic Analysis Equipment for Test Beds	12-Jul-2004	20-Jul-2004	100%	25 hrs	0 hrs	
Specify Rework Equipment	1-Jun-2001	24-Aug-2004	100%	12.5 hrs	0 hrs	Order x-ray first. Can't order sole
Rework Equipment Specification Complete	21-Jul-2004	21-Jul-2004	100%	0 hrs	0 hrs	source. Give to Kathy today.
Rework/X-Ray Equipment Design Rules Document	2-Sep-2004	23-Sep-2004	0%	75 hrs	75 hrs	
Specify Prototype Test Equipment	1-Jun-2001	30-Sep-2004	35%	52 hrs	37.5 hrs	
Prototype Test Equipment Specification Complete	30-Sep-2004	30-Sep-2004	0%	0 hrs	0 hrs	
Procure Gbit Data Prototype Cable [PP-#]	20-Sep-2004	20-Sep-2004	0%	5 hrs	5 hrs	Complete yes?
ACSIS Project	**12-Aug-2004**	**20-Sep-2004**	**71%**	**61 hrs**	**30 hrs**	

Mark Halman

Task Name	Start Date	Finish Date	% Comp.	Total Work	Remaining Work	Comments
Building Thermal Test Rack	23-Aug-2004	20-Oct-2004	37%	104.5 hrs	53 hrs	
Thermal Test Rack Built	20-Oct-2004	20-Oct-2004	0%	0 hrs	0 hrs	
TIMECODE Generator Board Prototype Testing [BPTP]	12-Nov-2004	6-Jan-2005	0%	200 hrs	200 hrs	
GBit Timing Cable Prototype Testing	2-Aug-2004	13-Aug-2004	0%	50 hrs	50 hrs	
GBit Timing Cable Prototype Testing Complete	13-Aug-2004	13-Aug-2004	0%	0 hrs	0 hrs	
GBit Data Cable Prototype Testing	21-Sep-2004	4-Oct-2004	0%	50 hrs	50 hrs	
GBit Data Cable Prototype Testing Complete	4-Oct-2004	4-Oct-2004	0%	0 hrs	0 hrs	

Additional Comments

Added to Thermal Test Document task for 10 hrs.

Tom Morgan

Task Name	Start Date	Finish Date	% Comp.	Total Work	Remaining Work	Comments
Correlator Backend Version 1.0 Communications Infrastructure [SWDP]	15-Mar-2003	29-Oct-2004	66%	350 hrs	180 hrs	
Correlator Backend Version 1.0 Communications Infrastructure Complete	29-Oct-2004	29-Oct-2004	0%	0 hrs	0 hrs	
Correlator Backend Version 1.0 Test Frame Generator [SWDP]	1-Apr-2003	4-Jan-2005	45%	250 hrs	137 hrs	
Correlator Backend Version 1.0 Test Frame Generator Complete	4-Jan-2005	4-Jan-2005	0%	0 hrs	0 hrs	
Correlator Backend Version 1.0 User/Test Interface	1-May-2003	1-Apr-2005	51%	400 hrs	187 hrs	
Correlator Backend Version 1.0 User/Test Interface Complete	1-Apr-2005	1-Apr-2005	0%	0 hrs	0 hrs	
Correlator Backend Version 1.0 Output Data Formatter [SWDP]	9-Aug-2004	20-Jun-2005	8%	290 hrs	278 hrs	
Correlator Backend Version 1.0 Output Data Formatter Complete	20-Jun-2005	20-Jun-2005	0%	0 hrs	0 hrs	
Version 1.0 Backend Core DP Functional Implementation	15-May-2003	11-Aug-2005	46%	355 hrs	191 hrs	
Version 1.0 Backend Core DP Functional Implementation Complete	11-Aug-2005	11-Aug-2005	0%	0 hrs	0 hrs	

Bruce Rowen

Task Name	Start Date	Finish Date	% Comp.	Total Work	Remaining Work	Comments
TIMECODE Generator Board Prototype Testing [BPTP]	12-Nov-2004	6-Jan-2005	0%	200 hrs	200 hrs	
TIMECODE Generator Board Prototype Testing Complete	6-Jan-2005	6-Jan-2005	0%	0 hrs	0 hrs	
CMIB Generic Prototype Software Development - Phase I	10-Nov-2003	4-Nov-2004	20%	315 hrs	262 hrs	
CMIB Generic Prototype Software Development - Phase I Complete	2-Apr-2004	2-Apr-2004	100%	0 hrs	0 hrs	Should Milestone = 100%?
FO Receiver Module Access Handler [SWDP]	30-Jun-2004	24-Aug-2004	100%	54 hrs	0 hrs	
FO Receiver Module Access Handler Complete	6-Aug-2004	6-Aug-2004	100%	0 hrs	0 hrs	
Delay Module Access Handler [SWDP]	3-May-2004	1-Mar-2005	13%	40 hrs	35 hrs	
Delay Module Access Handler Complete	1-Mar-2005	1-Mar-2005	0%	0 hrs	0 hrs	
FIR Filter Module Access Handler [SWDP]	13-Jul-2004	22-Mar-2005	13%	40 hrs	35 hrs	
FIR Filter Module Access Handler Complete	22-Mar-2005	22-Mar-2005	0%	0 hrs	0 hrs	
Station Board Prototype Software RFS & Design Document Development	17-Feb-2003	1-Dec-2004	32%	140 hrs	95 hrs	
Station Board Prototype Software RFS & Design Document Development	1-Dec-2004	1-Dec-2004	0%	0 hrs	0 hrs	
Station Board Customization of CMIB Generic Software [SWDP];[BSCP]	4-May-2004	4-Mar-2005	10%	50 hrs	45 hrs	
Station Board Customization of CMIB Generic Software Complete	4-Mar-2005	4-Mar-2005	0%	0 hrs	0 hrs	
Correlator Chip Module Access Handler [SWDP]	5-Apr-2004	28-May-2004	91%	39 hrs	5 hrs	
Correlator Chip Module Access Handler Complete	28-May-2004	28-May-2004	0%	0 hrs	0 hrs	
Recirculation Controller Module Access Handler [SWDP]	6-Apr-2004	31-May-2004	83%	27 hrs	5 hrs	
Recirculation Controller Module Access Handler Complete	31-May-2004	31-May-2004	0%	0 hrs	0 hrs	
Ethernet Transmitter Module Access Handler [SWDP]	7-Apr-2004	1-Jun-2004	67%	13 hrs	5 hrs	
Ethernet Transmitter Module Access Handler Complete	1-Jun-2004	1-Jun-2004	0%	0 hrs	0 hrs	
LTA Controller Module Access Handler [SWDP]	8-Apr-2004	2-Jun-2004	80%	21 hrs	5 hrs	
LTA Controller Module Access Handler Complete	2-Jun-2004	2-Jun-2004	0%	0 hrs	0 hrs	
MCB Interface & Clock Selector Module Access Handler [SWDP]	28-Dec-2004	4-Jan-2005	0%	25 hrs	25 hrs	
MCB Interface & Clock Selector Module Access Handler Complete	4-Jan-2005	4-Jan-2005	0%	0 hrs	0 hrs	
Baseline Board Customization of CMIB Generic Software [SWDP];[BSCP]	29-Apr-2004	18-Jan-2005	39%	50 hrs	31 hrs	
Baseline Board Customization of CMIB Generic Software Complete	18-Jan-2005	18-Jan-2005	0%	0 hrs	0 hrs	
TIMECODE Generator Prototype Software RFS Update	16-Apr-2004	22-Apr-2004	0%	20 hrs	20 hrs	
TIMECODE Generator Prototype Software RFS Update Complete	22-Apr-2004	22-Apr-2004	0%	0 hrs	0 hrs	
TIMECODE Generator Prototype Test Interface [SWDP]	23-Feb-2004	14-May-2004	20%	50 hrs	40 hrs	
TIMECODE Generator Prototype Test Interface Complete	14-May-2004	14-May-2004	0%	0 hrs	0 hrs	
PCMC Module Handler	21-Jan-2004	2-Nov-2005	50%	40 hrs	20 hrs	
PCMC Module Handler Complete	2-Nov-2005	2-Nov-2005	0%	0 hrs	0 hrs	
PCMC Device Driver	19-Jul-2004	1-Dec-2005	16%	125 hrs	105 hrs	
PCMC Device Driver Complete	1-Dec-2005	1-Dec-2005	0%	0 hrs	0 hrs	
CMIB Communication Infrastructure	9-Feb-2004	5-Jun-2006	26%	200 hrs	158 hrs	
CMIB Communication Infrastructure Complete	5-Jun-2006	5-Jun-2006	0%	0 hrs	0 hrs	
CMIB Boot Configuration Software [SWDP]	4-Aug-2004	11-Jul-2006	24%	150 hrs	130 hrs	
CMIB Boot Configuration Software Complete	11-Jul-2006	11-Jul-2006	0%	0 hrs	0 hrs	

TIMECODE Generator Software RFS & Design Document	1-Jun-2003	29-Aug-2006	50%	100 hrs	50 hrs
TIMECODE Generator Software RFS & Design Document Complete	29-Aug-2006	29-Aug-2006	0%	0 hrs	0 hrs
TIMECODE Generator In-House Test Software [SWDP]	14-May-2004	28-May-2004	0%	50 hrs	50 hrs
TIMECODE Generator In-House Test Software Complete	28-May-2004	28-May-2004	0%	0 hrs	0 hrs
VLA Maintenance	**26-Jul-2004**	**15-Sep-2004**	**100%**	**87 hrs**	**0 hrs**
Other AOC Maintenance	**4-Aug-2004**	**16-Sep-2004**	**100%**	**36 hrs**	**0 hrs**