

<b>Meeting Date:</b>	<b>26-Mar-03</b>
<b>Meeting Attendants:</b>	
<b>Pentiction:</b>	Brent, Zoran, Zhang, Dave F, Amy
<b>Socorro:</b>	Tom, Bruce
<b>Jodrell Bank:</b>	Simon, Dave Brown, Roger (& Dave Brown again because I missed him last week!)

## Pentiction

<i>General Notes:</i>	
Events	<ul style="list-style-type: none"> <li>● Sonja Vrcic (s/w eng.) officially starting Mar.31/03</li> <li>● Possibly change correlator training meeting from Apr.23-25 to Apr.28-30???</li> <li>● Project Management consultant will be coming to DRAO again Mar. 27/28 to help begin preparing for re-planning and re-baselining the project.</li> </ul>
Comments	<ul style="list-style-type: none"> <li>● We will have a summer student arriving on May. 5 to do test case generation and verification and software analysis.</li> </ul>
New Development	<ul style="list-style-type: none"> <li>● Not going to be any more compact flash cards. May actually boot the entire system from the network</li> </ul>
<i>Brent:</i>	
Accomplishments	<ul style="list-style-type: none"> <li>● Has completed a lot of work on the recirculation controller. It is almost done except the recirculation part of the chip.</li> </ul>
<i>Dave F:</i>	
Comments	<ul style="list-style-type: none"> <li>● Hasn't really gotten anywhere of the filter chip in the last week.</li> <li>● Having trouble with signal vision, it keeps crashing the computer. (Probably something wrong with Dave's computer though, not a problem with the software).</li> <li>● Hoping to continue working on filter once signal vision problem sorted out.</li> </ul>
Accomplishments	<ul style="list-style-type: none"> <li>● Spent a lot of time looking into Altera chips and how they work this past week.</li> </ul>
New Development	<ul style="list-style-type: none"> <li>● Dave and Zoran looking into getting rid of 128MHz clock and going back to old idea of distributing clock on MDR-80 cable.</li> </ul>

<i>Zoran:</i>	
Comments	<ul style="list-style-type: none"> <li>Working with Dave on the clock (as mentioned above).</li> <li>Starting to read Altera stuff.</li> </ul>
Accomplishments	<ul style="list-style-type: none"> <li>Did more design on delay module board.</li> <li>Starting to update the delay module RFS.</li> </ul>
<i>Zhang:</i>	
Accomplishments	<ul style="list-style-type: none"> <li>Writing the second draft of the M/C mezzanine card RFS. Will be finished today.</li> </ul>

## Socorro

<i>Bruce</i>	
Accomplishments	<ul style="list-style-type: none"> <li>Still working on device driver for Zhang's mezzanine card PC-104 bridging function.</li> <li>Also doing the same thing for the delay module. Although only starting to because the RFS is changing.</li> </ul>
Comments	<ul style="list-style-type: none"> <li>Brent suggested starting working on the device driver for the correlator chip. Bruce says he's just waiting for the final word on the register pin set from the RFS documents.</li> </ul>
<i>Tom:</i>	
Event	<ul style="list-style-type: none"> <li>Was in Tucson first half of last week for the Alma software review.</li> </ul>
Idea	<ul style="list-style-type: none"> <li>The backend in the Alma correlator will be hung off of the M/C. This might be useful in EVLA as well. Might be good to have correlator M/C configure correlator and backend at the same time.</li> </ul>
Accomplishments	<ul style="list-style-type: none"> <li>Now at the point where software can handle memory buffer wrap-around and can handle an entire lag set going missing. Can't handle if an entire integration is missing. This is not tested yet (not enough data). Will be working on it this week.</li> </ul>
Comments	<ul style="list-style-type: none"> <li>Next step is to actually try and do some performance measurements.</li> </ul>

## Jodrell Bank

<i>General Notes:</i>	
Comments	● Generally looking at tenders for fibre connections. This is the main focus right now. It seems it will be dark fibre and the prices are not impossible.