

<b>Meeting Date:</b>	<b>23-Jul-03</b>
<b>Meeting Attendants:</b>	
<b>Penticton:</b>	Brent, Frances, Zhang, Amy, Dave, Sonja, Zoran
<b>Socorro:</b>	Bruce, Tom, Ken
<b>Jodrell Bank:</b>	Bryan

## Penticton

<i>General Notes:</i>	
Events	<ul style="list-style-type: none"> <li>Frances brought muffins. Next week is Zoran's turn to bring donuts (or some treat).</li> <li>Big media event last Monday. Positive response.</li> <li>Had meeting with PCB contractor to agree on methodology for communications.</li> </ul>
Comments	<ul style="list-style-type: none"> <li>There is no longer the possibility of the FIR chip and the correlator chip begin on the same day.</li> <li>Will have sub-band multi-beaming capability.</li> </ul>
<i>Brent:</i>	
Events	<ul style="list-style-type: none"> <li>Been away on vacation.</li> </ul>
Accomplishments	<ul style="list-style-type: none"> <li>Yesterday finished recirculation controller PAR in Altera EP1S10-5 at speed with 99% utilization of chip. This is a \$200,000 question on whether to use this chip or the next step up.</li> <li>Working on test bench for recirculation controller. Using correlator chip to test. Will get first results on how the recirculation works. Will take approximately 1 month to build the test bench &amp; test.</li> <li>Written a preliminary draft for testing correlator chip. Explained why he wants to go straight to full custom device.</li> </ul>
<i>Amy:</i>	
Comments	<ul style="list-style-type: none"> <li>Project management was put on hold for a while because of the media event last week.</li> <li>Just about finished reorganizing WBS</li> <li>Hope to get all info into database and start getting schedule info soon.</li> </ul>

<i>Dave F:</i>		
Events	●	On vacation recently.
Accomplishments	●	Final delay block done. Stage 1,2,3,4 done. Done = functionally tested.
Comments	●	Only tested up to 64 taps.
	●	Overall pieces do what he thinks they do. Smaller bits may cause quirks.
	●	Still working on Filter chip: few changes, some simplifications, things are starting to settle down. Still haven't done stage 1.
	●	Going to start with tone extractor in FIR chip
	●	Looks like this will fit into 25,000 logic slice FPGA (w/o Zoran's device included).
Action	●	Could do peer review of FIR chip at anytime.
<i>Zoran:</i>		
Accomplishments	●	Mostly worked with delay module PCB - changes some design.
New Projects	●	Worked with tools on constraints.
	●	Talked with Lawrence (PCB contractor) about his, decided not to put in net constraints for this board.
Deadline(s) Established	●	Hopefully will get files from Lawrence next week.
	●	Back to working on delay for filter chip.
<i>Zhang:</i>		
Accomplishments	●	Done PC/104 M/C board schematic design.
Event	●	Will have design review after this meeting.
Comments	●	Then will pass on to PCB contractor.
	●	Almost done TIMECODE Generator schematic. Will get new TIMECODE generator RFS put on web.
<i>Sonja:</i>		
Comments	●	Sent out memo 16 at end of June - haven't got much feedback yet (people on vacation).
	●	Had meeting last Friday (w/ Tom, Ken, Bruce) and discussed this document.
	●	Back to working on VCI
	●	Getting in closer contact with Ken to further identify requirements on VCI.

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<i>Frances:</i>	
Comments	<ul style="list-style-type: none"> <li>Working on correlator chip test analysis software - almost finished.</li> <li>Working on creating an installation CD.</li> <li>Going to develop some test cases and run them.</li> </ul>

## Socorro

<i>Tom:</i>	
Comments	<ul style="list-style-type: none"> <li>Busy testing and fixing a few things.</li> <li>Allowed himself a month to do backend tests. This means that they should be done by August 15, but probably will be done earlier.</li> </ul>
<i>Bruce:</i>	
Comments	<ul style="list-style-type: none"> <li>Taken a twist on driver document. Going to continue going from bottom up.</li> <li>Will have recirculation done soon.</li> <li>Will be device driver documentation for each board --&gt; but it will be a subset of a larger document. (Essentially an RFS).</li> </ul>
Action	<ul style="list-style-type: none"> <li>Will leave it up to the software group to decide what format to use for documentation and if necessary Sonja, Tom, and Bruce will make a software RFS template.</li> </ul>
<i>Ken:</i>	
Comment	<ul style="list-style-type: none"> <li>We talked with Sonja and said he'd look at how often we want to reconfigure the correlator: every 10 seconds (worst case).</li> <li>Guessing about 1 second to do the reconfiguration, seems reasonable spec.</li> </ul>
Comment (from Sonja)	<ul style="list-style-type: none"> <li>Also need to know, how far in advance we need to send out new configuration.</li> </ul>

## Jodrell Bank

<i>Bryan:</i>	
Events	<ul style="list-style-type: none"> <li>Have selected a provider for the fibre connections. It eats up a lot of the contingency money.</li> </ul>

Comments

- Will use dark fibre.
- Going to get first connection early next year.

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