NRC · CNRC

Transmission Line Topologies -Baseline Board

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Outline

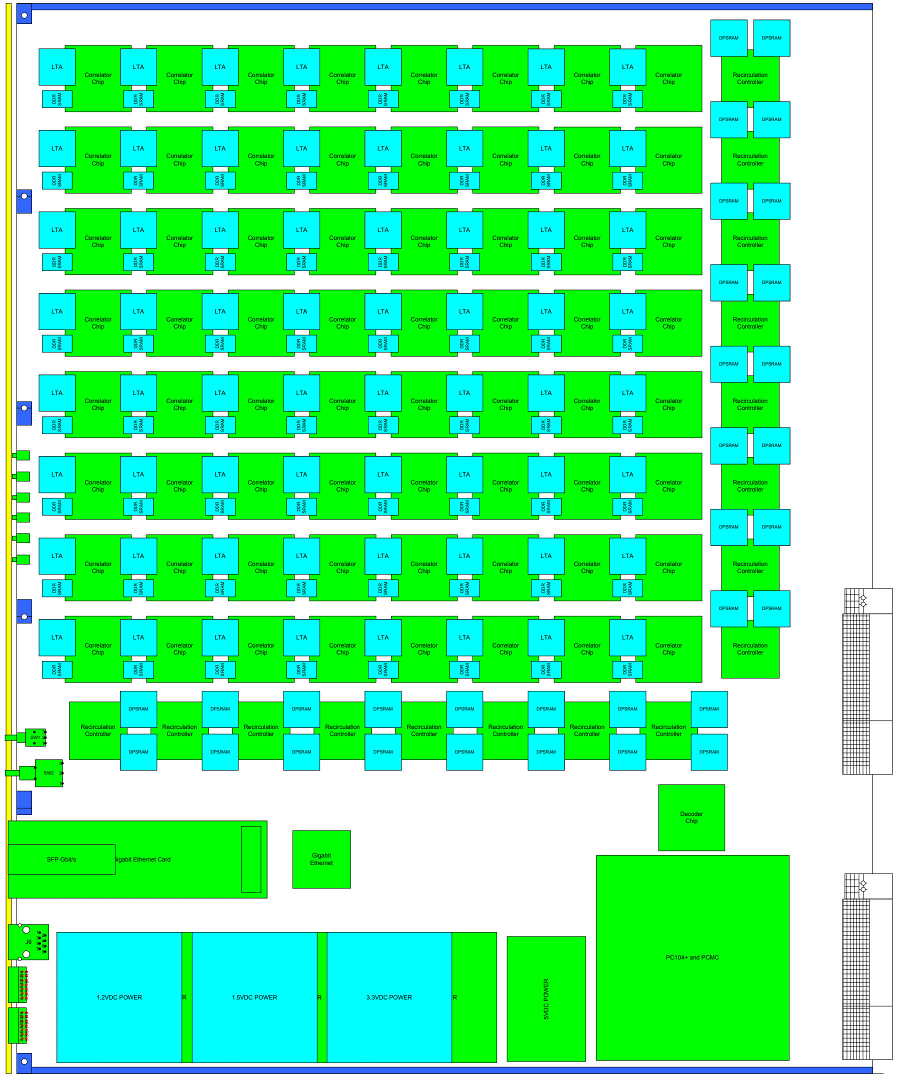
- Baseline Board Overview
- Transmission Line Topologies
- Simulation Waveforms

NRC · CNRC

Baseline Board Overview

- 64 correlator chips
- 64 LTA controllers
- 64 DDR SDRAM (each LTA controller has 1)
- 16 recirculation controllers
- 32 dual-port static RAM (each recirculation controller has 2)
- 1 Gigabit Ethernet chip
- 1 decoder chip
- 1 PC104+ and PCMC mezzanine card
- 2 HM connectors
- 5V, 3.3V, 2.5V, 1.5V, 1.2V power supplies
- LEDs, switches, capacitors, resistors…

Baseline Board Overview



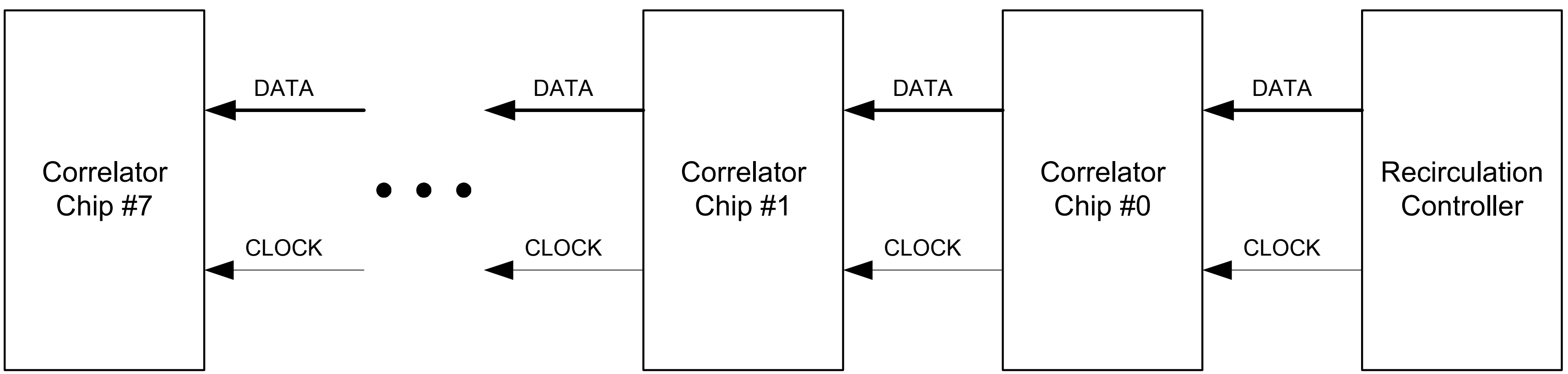
Transmission Line Topologies –

Recirculation Controller to Correlator Chip

- Data: 256 Mbits/sec
- Clock: 128 MHz
- Point-to-point bus chain
- 2.5V LVTTL I/Os
- Clock has a series terminator

Transmission Line Topologies –

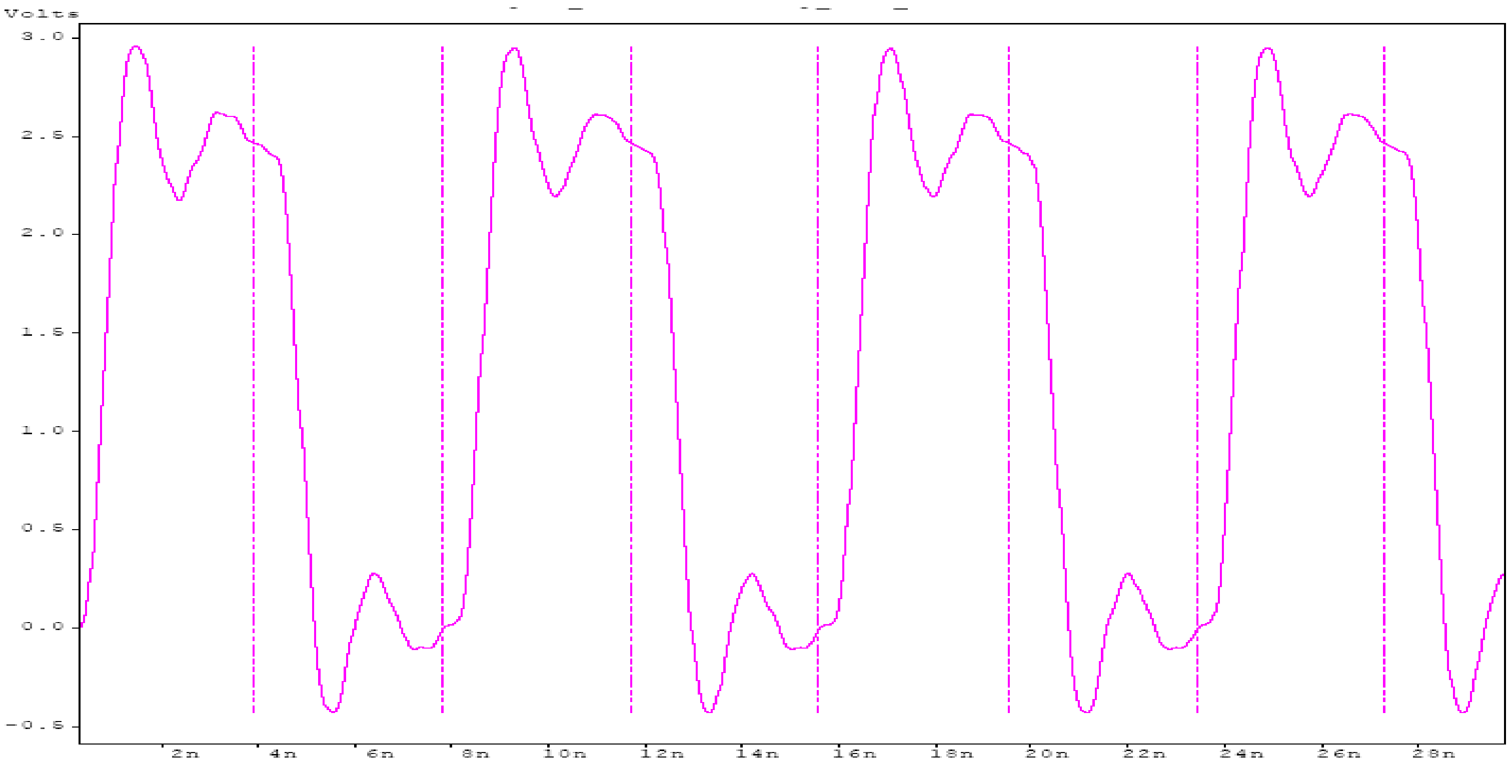
Recirculation Controller to Correlator Chip



Simulation Waveforms –

Recirculation Controller to Correlator Chip

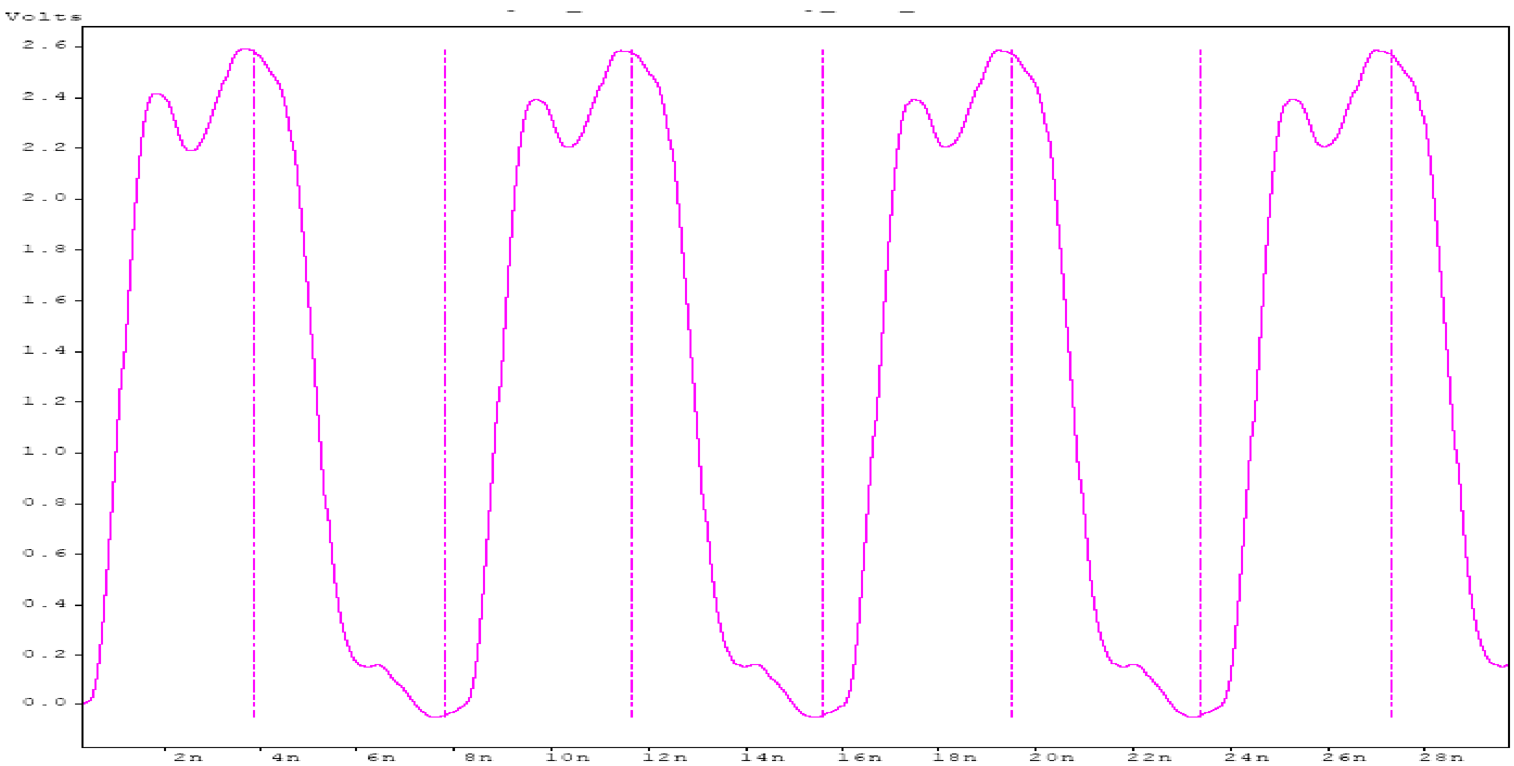
- Data (no termination)



Simulation Waveforms –

Recirculation Controller to Correlator Chip

- Clock (series termination)



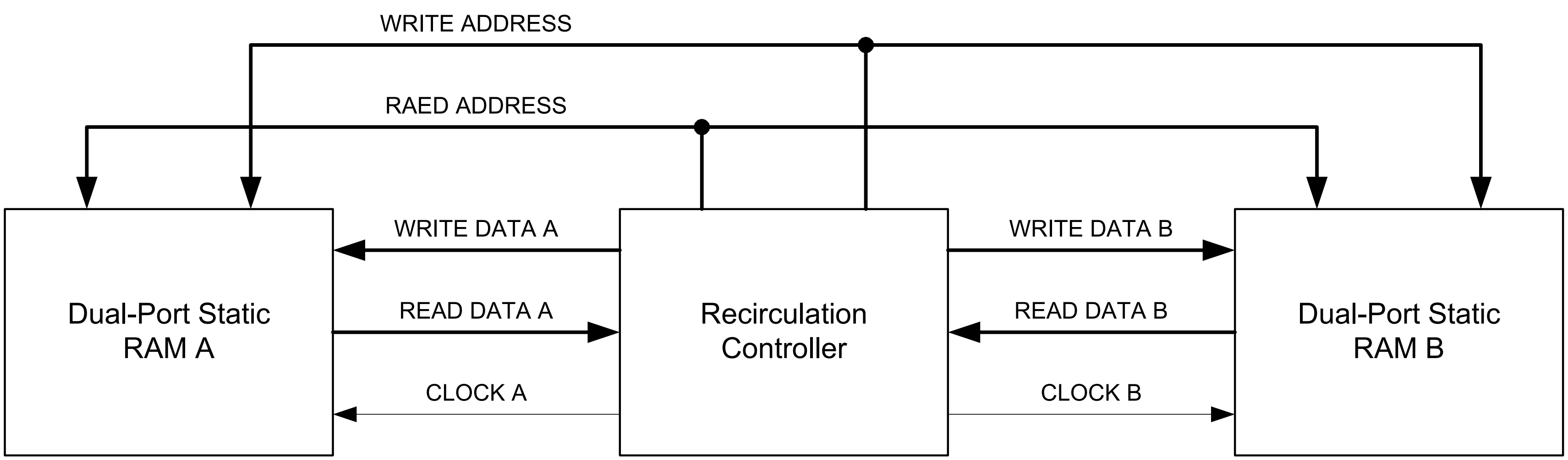
Transmission Line Topologies –

Recirculation Controller to DP-SRAMs

- Address and Data: 128 Mbits/sec
- Clock: 128 MHz
- Address 1-to-2 multi-drop
- Data and clock point-to-point
- 2.5V LVTTL I/Os

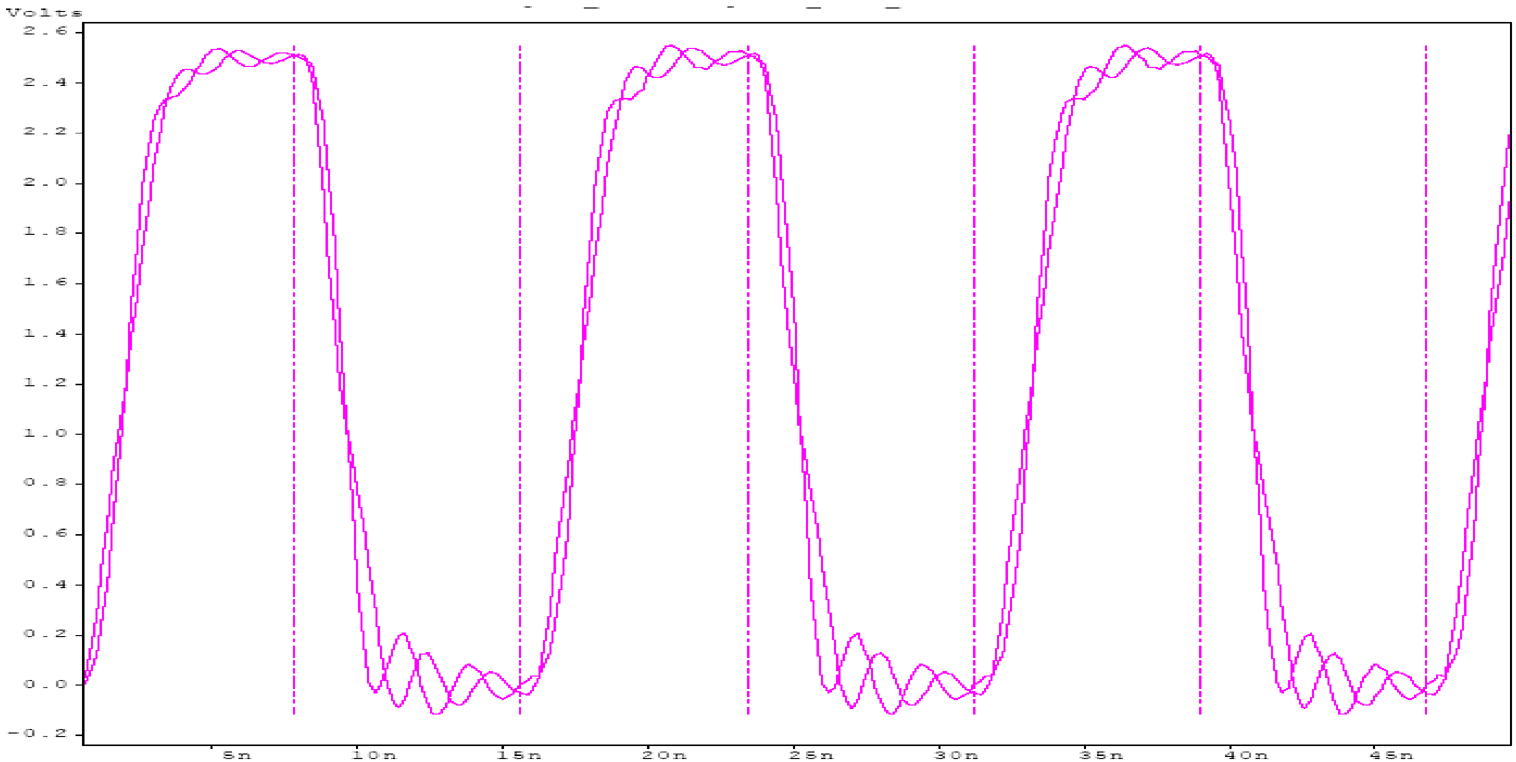
Transmission Line Topologies –

Recirculation Controller to DP-SRAMs



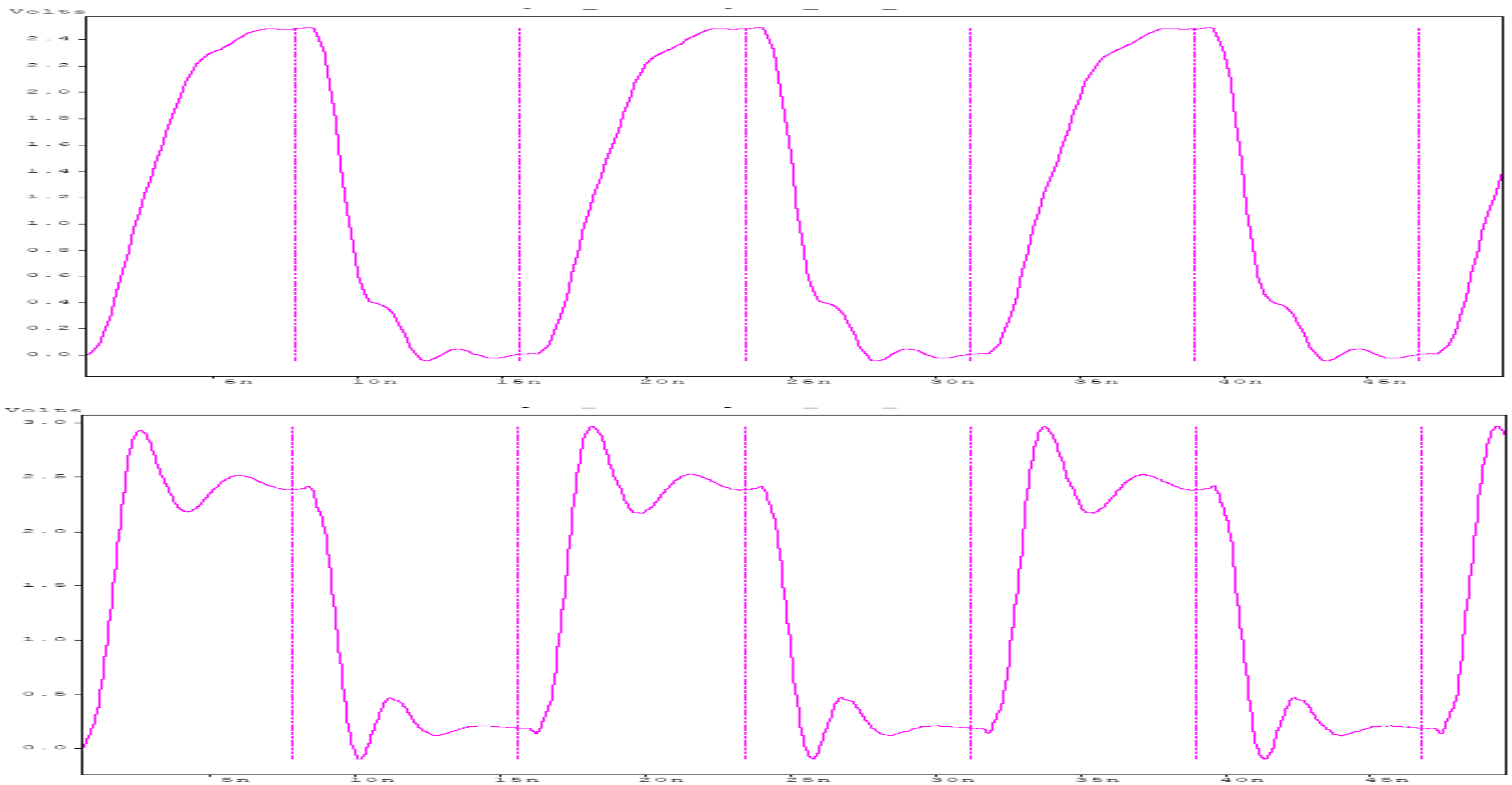
Simulation Waveforms –
Recirculation Controller to DP-SRAMs

- Address (1-to-2 no termination)



Simulation Waveforms –
Recirculation Controller to DP-SRAMs

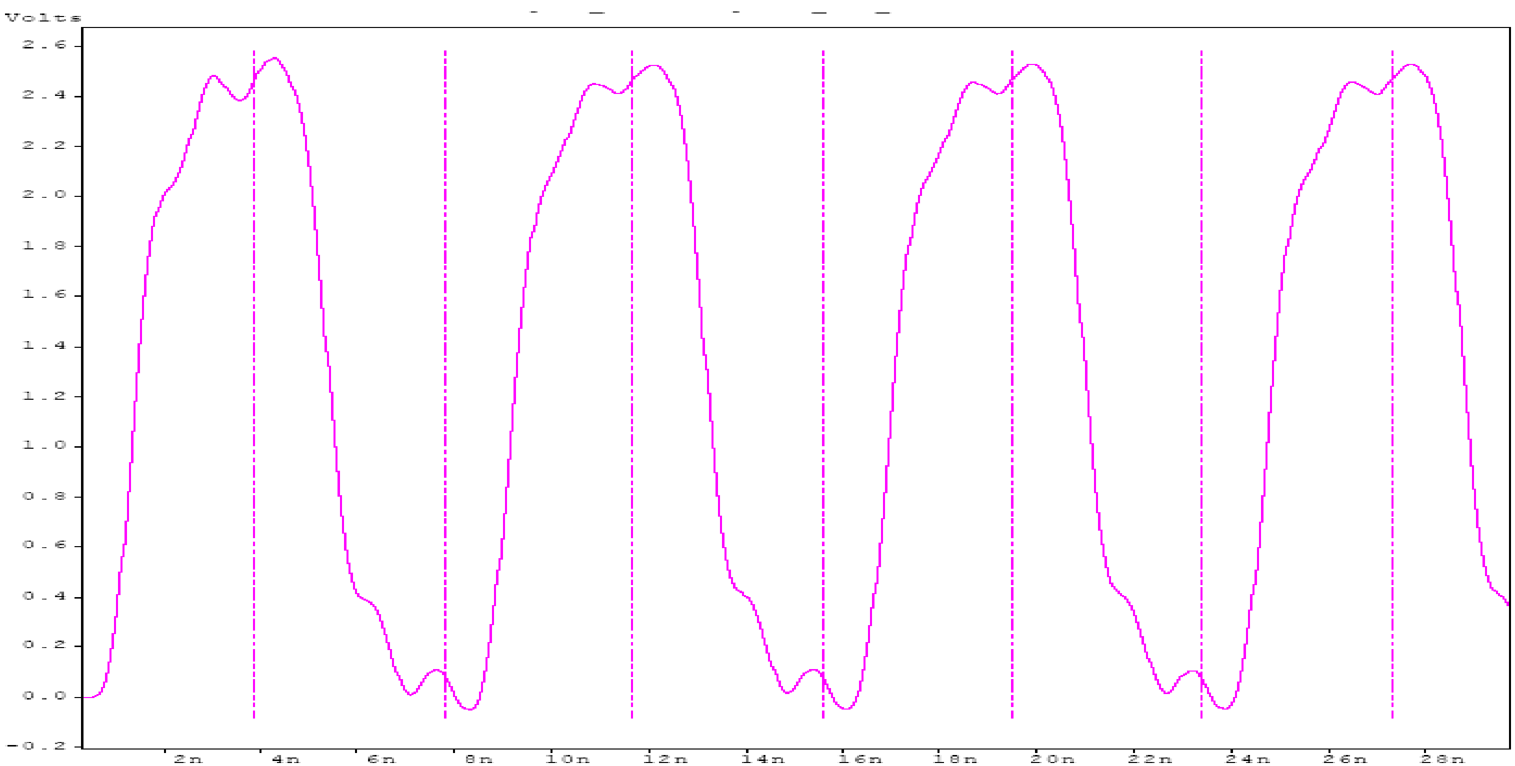
- Data (point-to-point no termination)



Simulation Waveforms –

Recirculation Controller to DP-SRAMs

- Clock (point-to-point series termination)



Transmission Line Topologies –

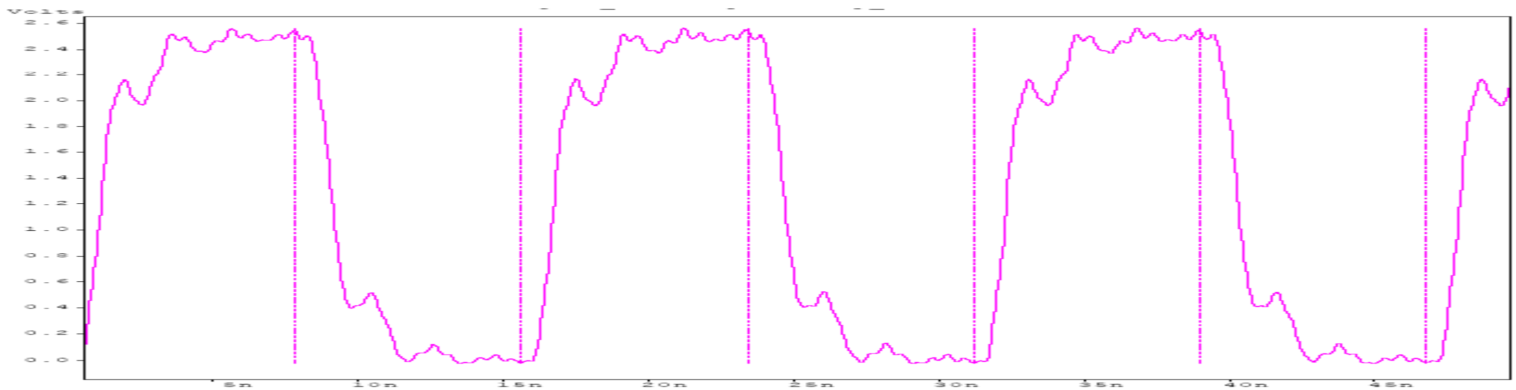
Correlator Chip to LTA Controller

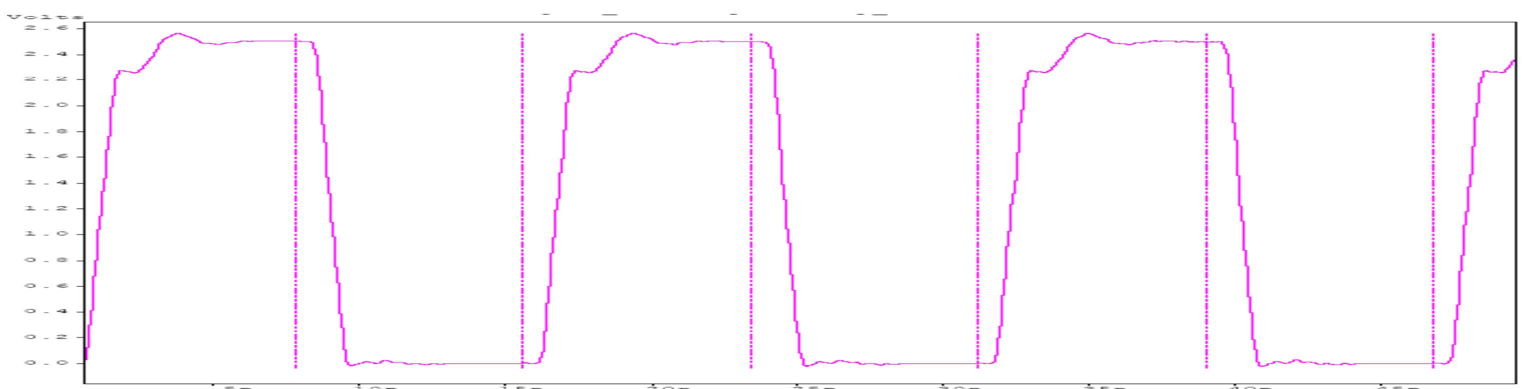
- Data: 128 Mbits/sec
- Clock: 128 MHz
- Data and clock: point-to-point
- 2.5V LVTTL I/Os

Simulation Waveforms –

Correlator Chip to LTA Controller

- Data (point-to-point no termination)

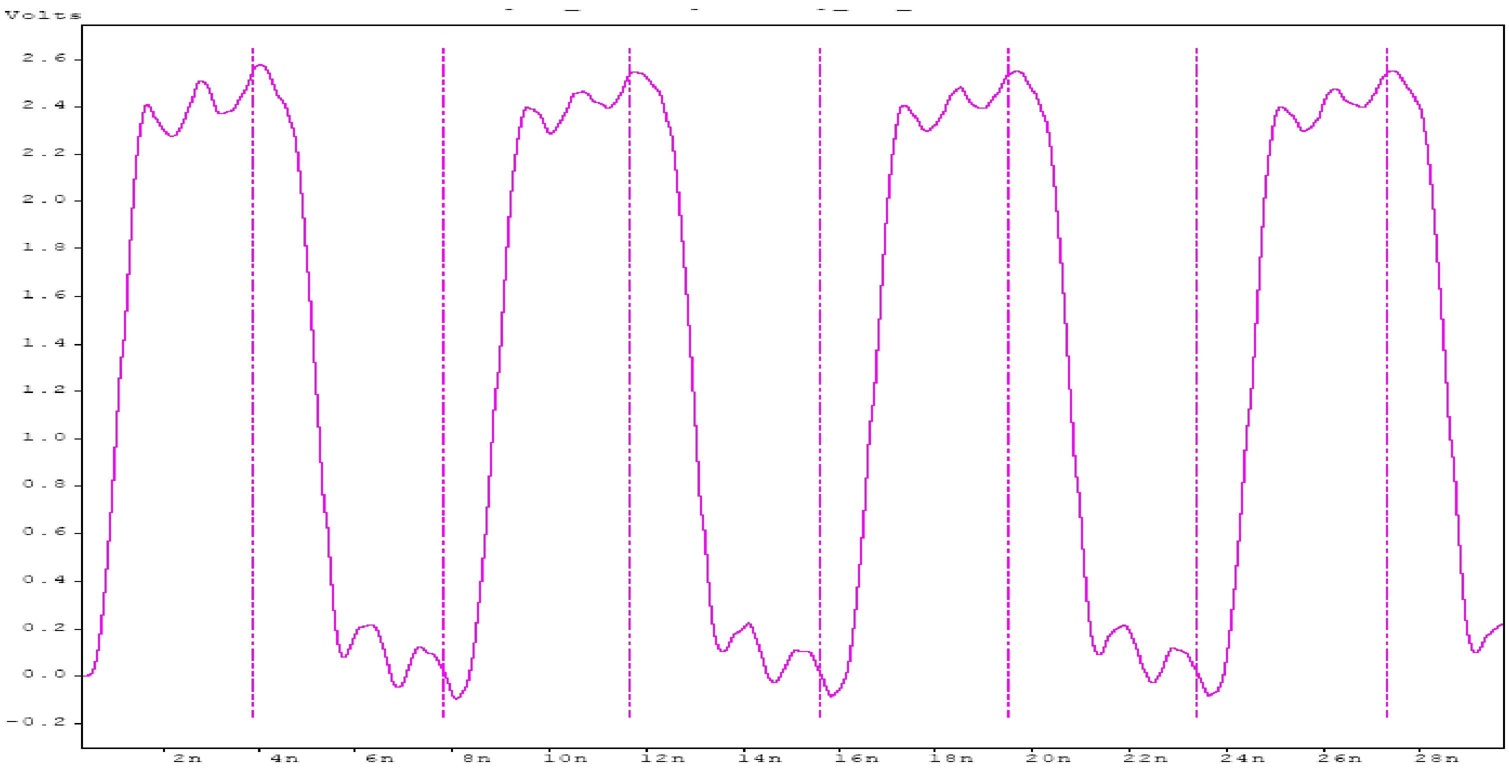




Simulation Waveforms –

Correlator Chip to LTA Controller

- Clock (point-to-point series termination)



Transmission Line Topologies –

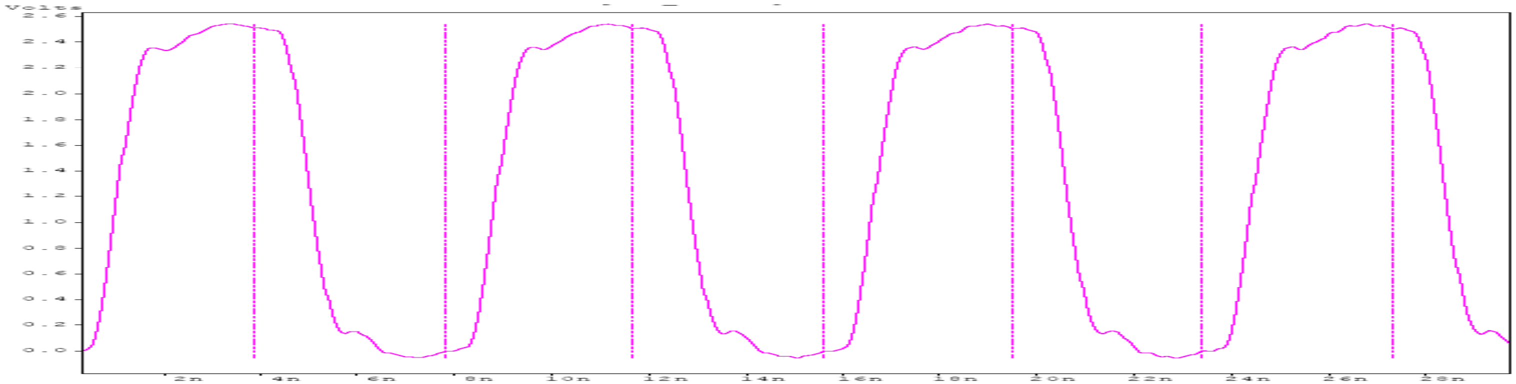
LTA Controller to DDR SDRAM

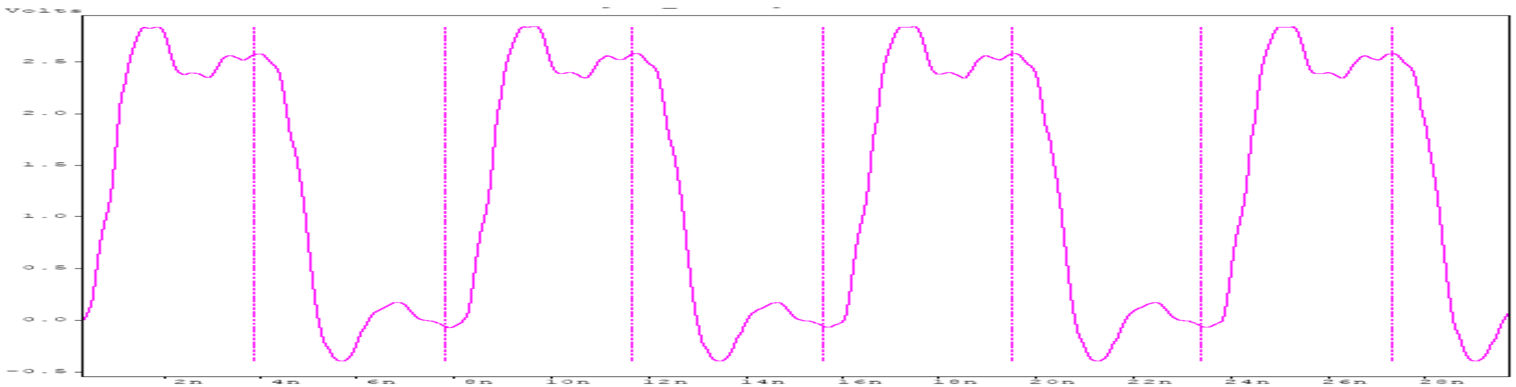
- Address and Data: 256 Mbits/sec
- Clock: 128 MHz
- All signals: point-to-point
- SSTL-2 Class 2 I/Os

Simulation Waveforms –

LTA Controller to DDR SDRAM

- Address, Data and Clock (point-to-point no termination)





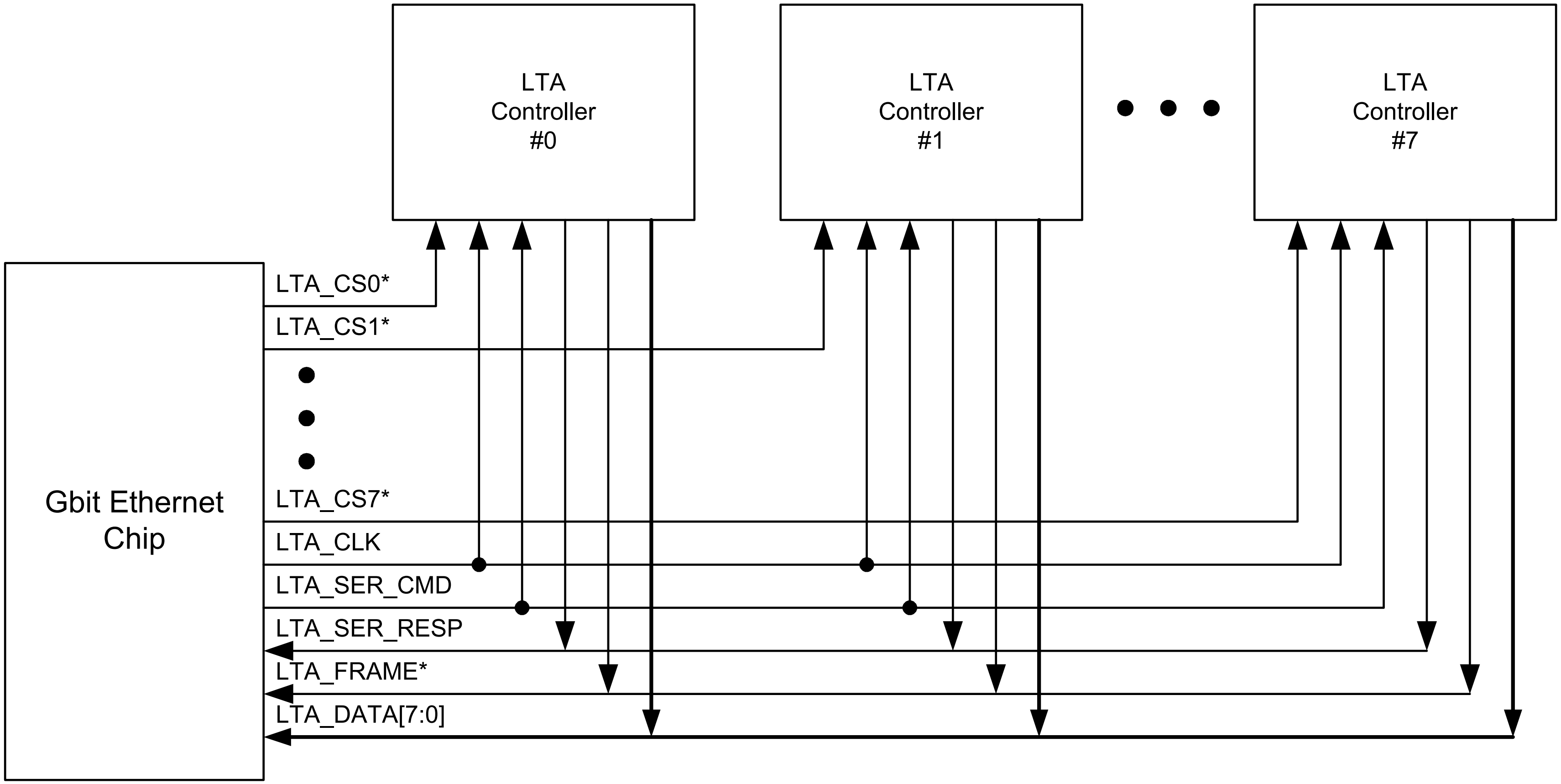
Transmission Line Topologies –

LTA Controller to Gbit Ethernet Chip

- Command, Response, Frame, Data: 125 Mbits/sec
- Clock: 31.25 MHz
- Clock, Command: 1-to-8 multi-drop
- Data, Frame, Response: 8-to-1 multi-driver
- SSTL-2 Class 2 I/Os

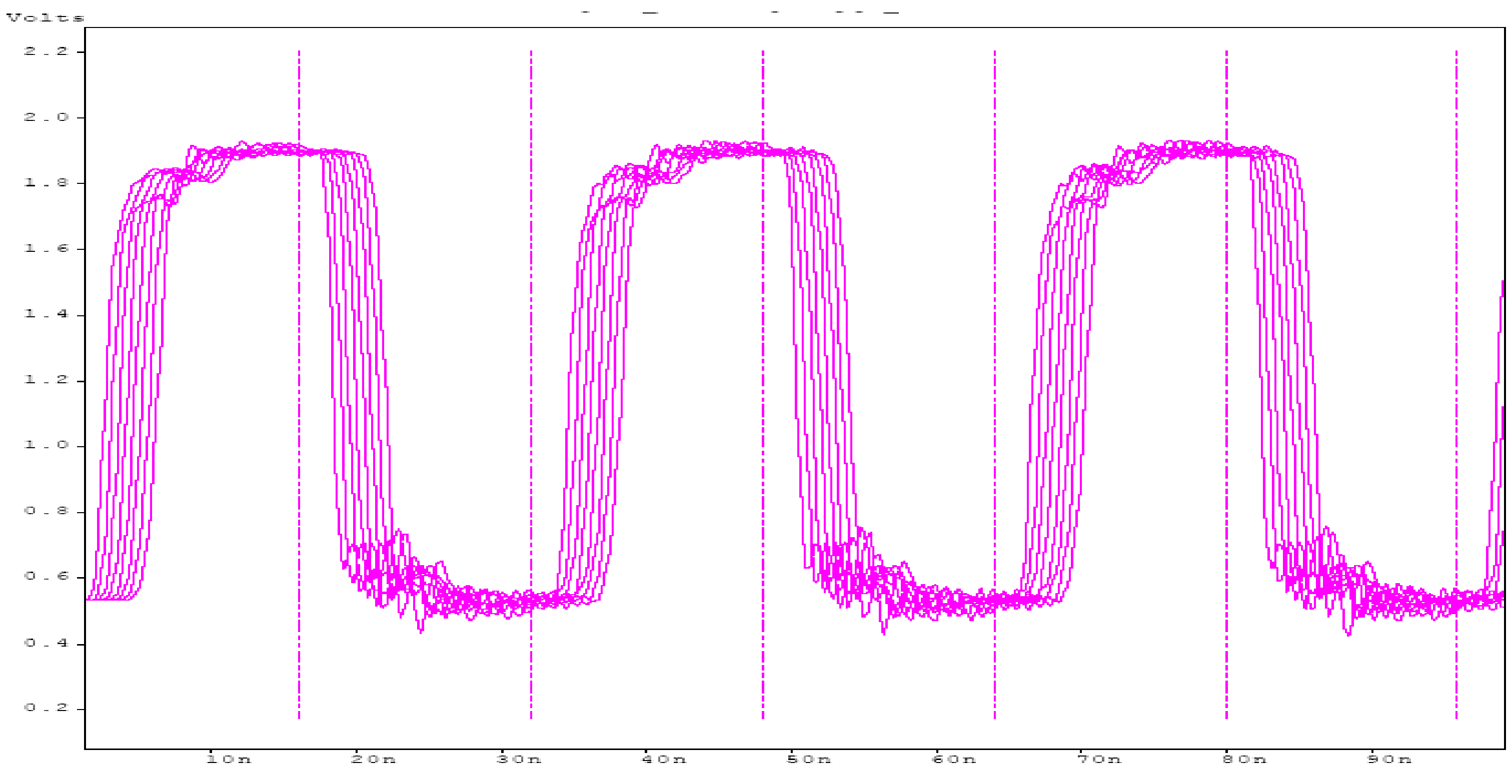
Transmission Line Topologies –

LTA Controller to Gbit Ethernet Chip



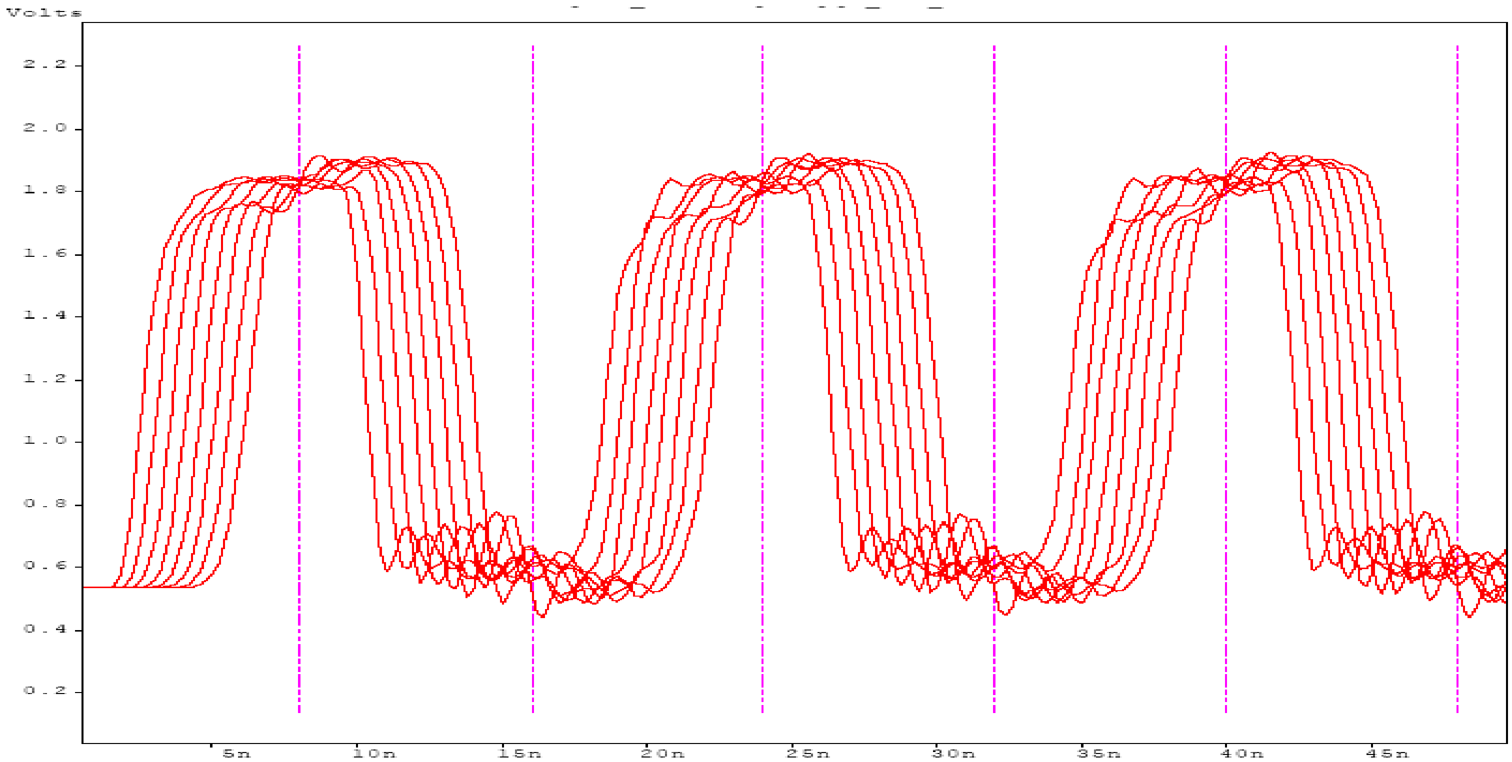
Simulation Waveforms –
LTA Controller to Gbit Ethernet Chip

- Clock (1-to-8 multi-drop with series and parallel termination)



Simulation Waveforms –
LTA Controller to Gbit Ethernet Chip

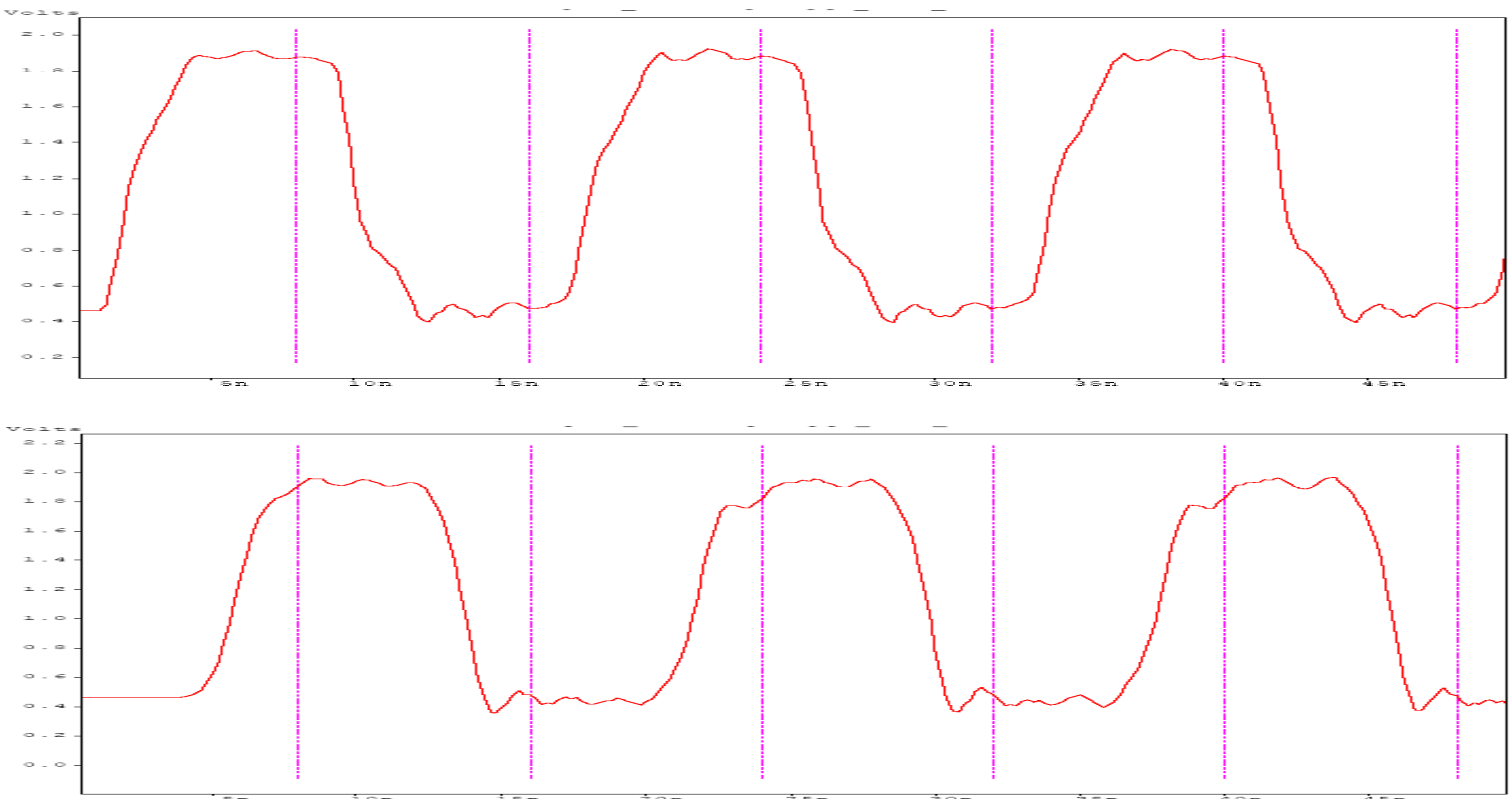
- Command (1-to-8 multi-drop, series and parallel termination)



Simulation Waveforms –

LTA Controller to Gbit Ethernet Chip

- Data (8-to-1 multi-driver, parallel termination on both ends)

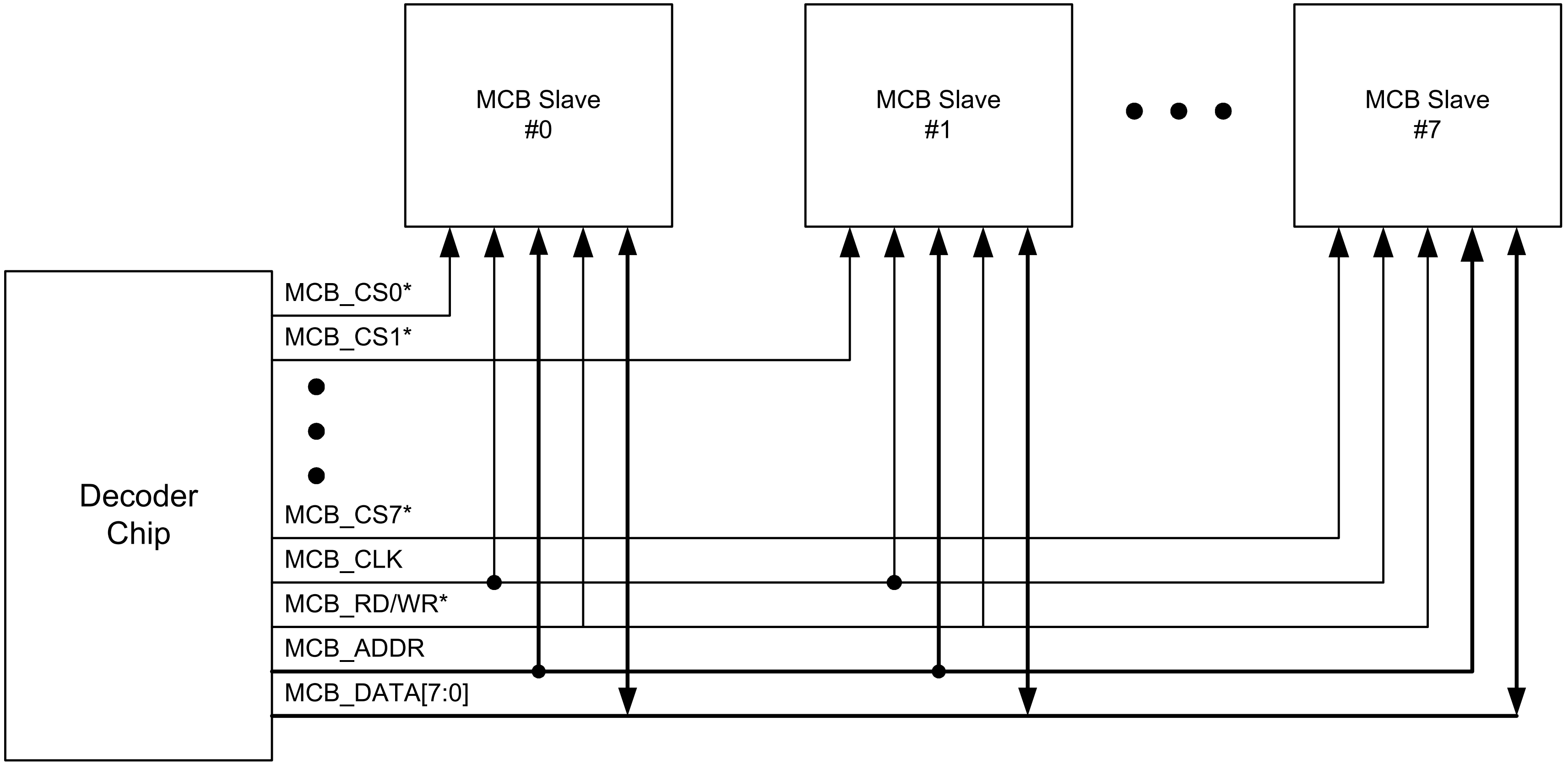


Transmission Line Topologies –
MCB Interface

- Control, Address, Data: 33 Mbits/sec
- Clock: 33 MHz
- Clock, Control, Address: 1-to-8 multi-drop
- Data: 1-to-8 and 8-to-1 multi-point
- SSTL-2 Class 2 I/Os

Transmission Line Topologies –

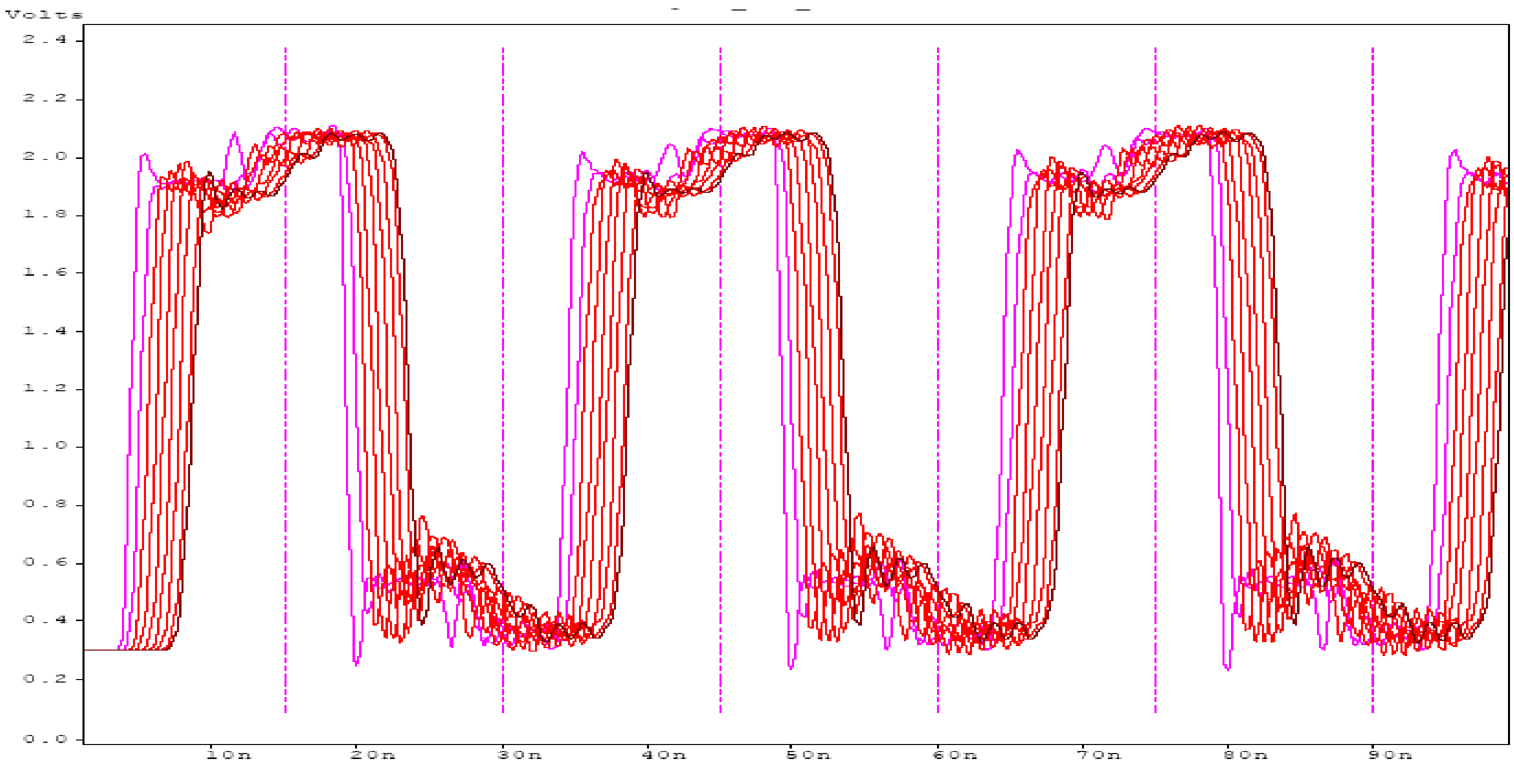
MCB Interface



Simulation Waveforms –

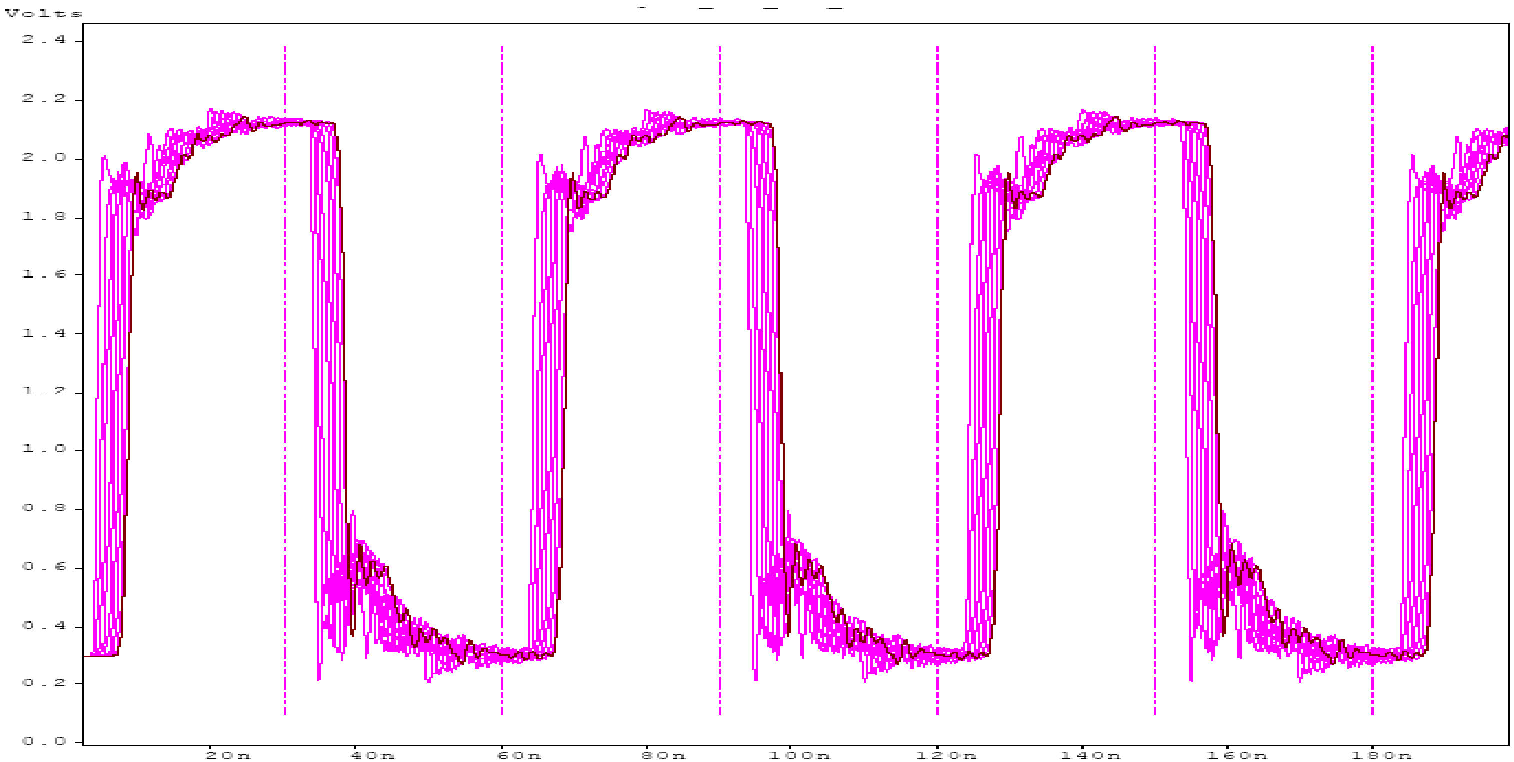
MCB Interface

- Clock (1-to-8 multi-drop, parallel termination)



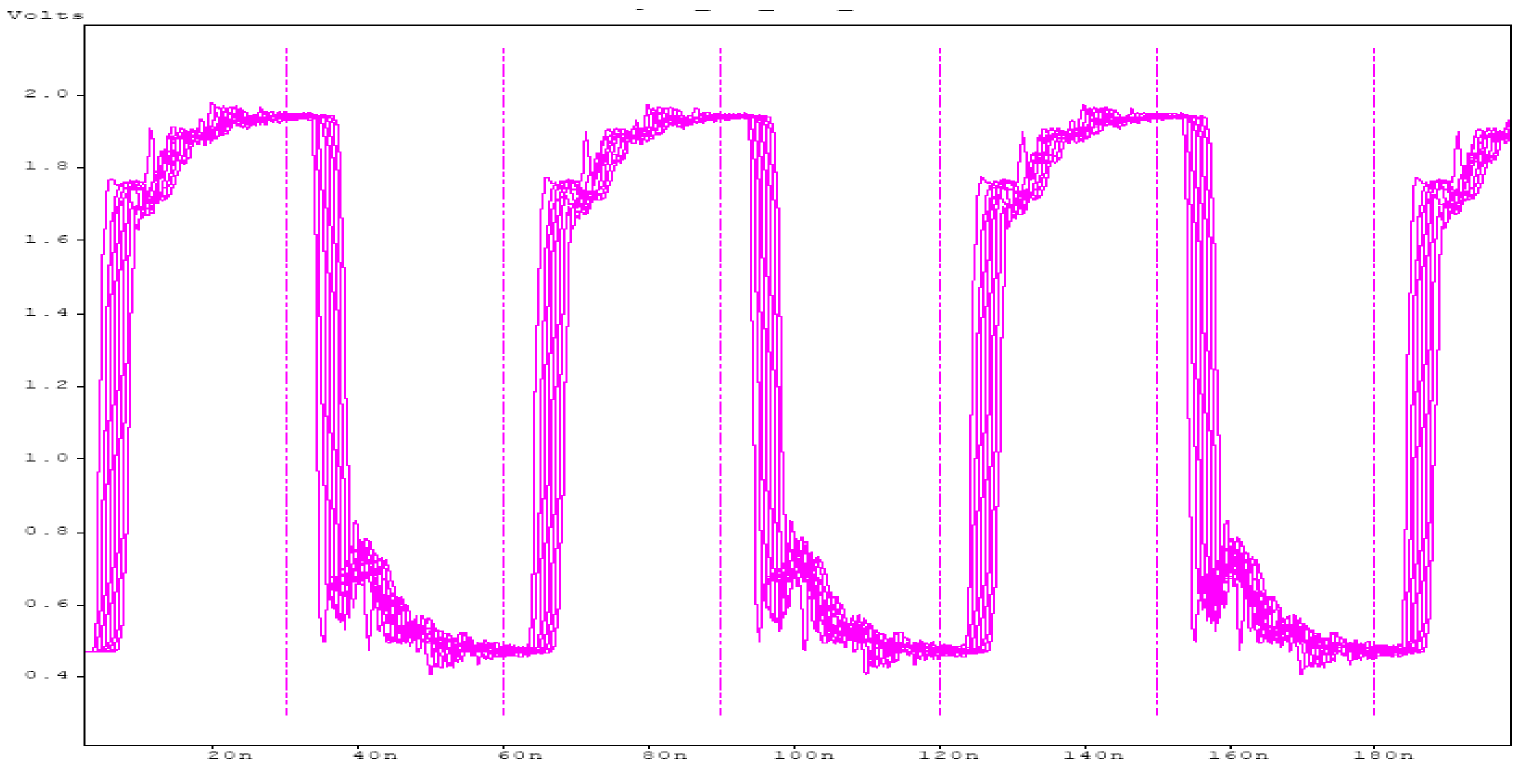
Simulation Waveforms –
MCB Interface

- Control (1-to-8 multi-drop, parallel termination)



Simulation Waveforms –
MCB Interface

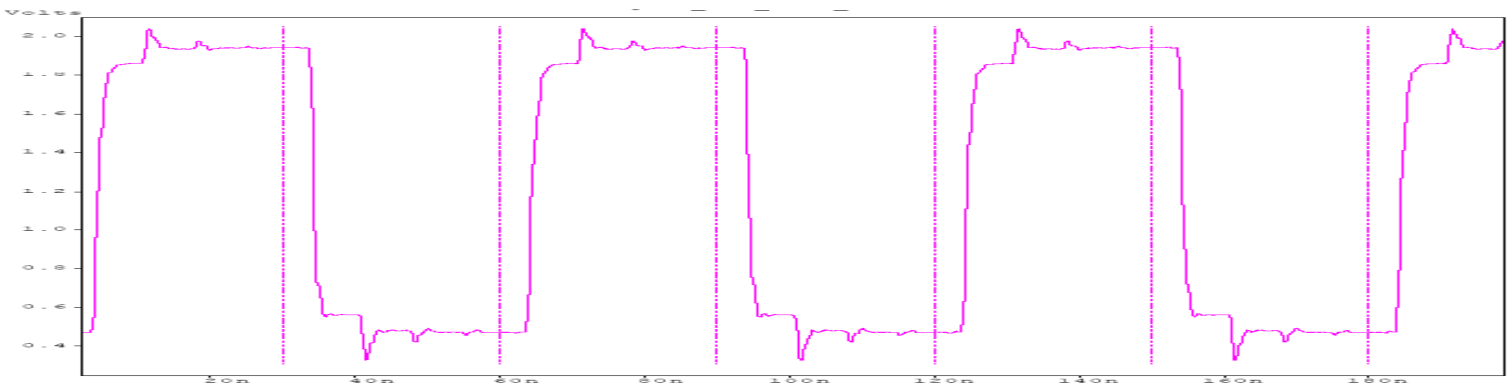
- Data (1-to-8, parallel termination on both ends)

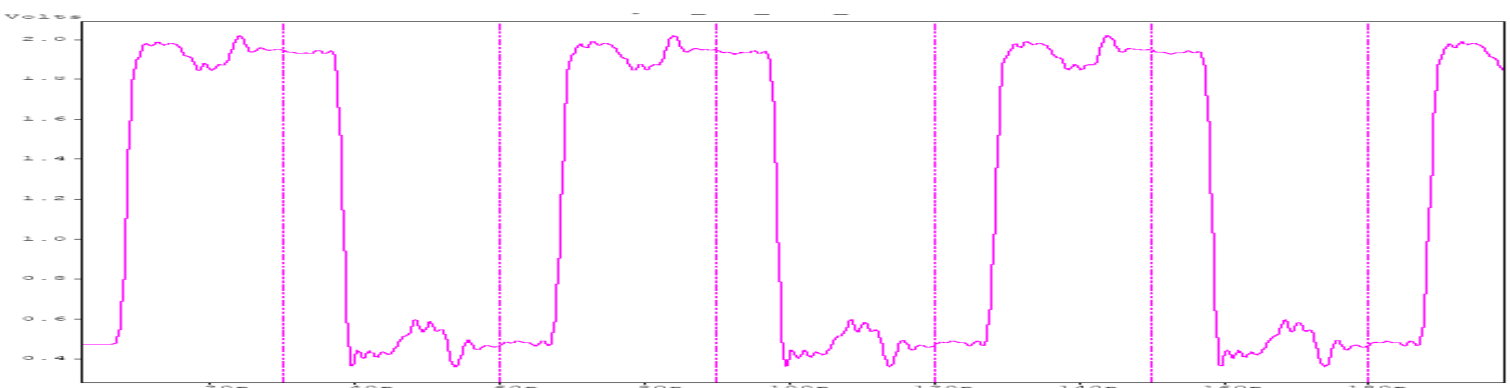


Simulation Waveforms –

MCB Interface

- Data (8-to-1, parallel termination on both ends)





Summary

- Post-layout simulation on high-speed Gbits/sec signals
- Many PCB layers to route signal traces
- SMT components on both sides, have to use micro-via, blind via technologies
- Use 5mil 50-ohm traces for all signals