EVLA Correlator Chip prototype verification matrix. C25082N0006 B. Carlson, VDRAFT April 18, 2006

Test Case Number	0	1	2	3	3a	4	5	5a	5b	6	6a	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	32a	33	34	35	36	37	38	40	41	50	50a	51	52	53	53a	52	53	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	80	81
Test Coverage Description																																																																										
NOTE: All tests run with 256 MHz clock, unless otherwise noted.																																																																										
I/O connectivity, timing, voltage, test vector mode																																																																										
X input test vector detection/sync with no errors generated or detected. TVEN=1		x																																																																							
Y input test vectors detection/sync with no errors generated or detected. TVEN=1		x																																																																							
X input test vectors with errors generated and detected on each X input line. TVEN=1			x																																																																						
Y input test vectors with errors generated and detected on each Y input line. TVEN=1			x																																																																						
X daisy-chain test vectors. Complete 8x8 array of chips active. No errors. TVEN=1				x																																																																					
Y daisy-chain test vectors. Complete 8x8 array of chips active. No errors. TVEN=1				x																																																																					
X daisy-chain test vectors. Complete 8x8 array of chips active. Errors. TVEN=1						x																																																																	
Y daisy-chain test vectors. Complete 8x8 array of chips active. Errors. TVEN=1						x																																																																	
X PLL output jitter, 1 chip, <150 ps pk-pk cycle-cycle, record stats.	x																																																																								
Y PLL output jitter, 1 chip, <150 ps pk-pk cycle-cycle, record stats.	x																																																																								
X PLL output jitter 8X daisy chain <150 ps pk-pk cycle-cycle, record stats.																																																																							x	
Y PLL output jitter 8X daisy chain <150 ps pk-pk cycle-cycle, record stats.																																																																							x	
Test Case Number	**0**	**1**	**2**	**3**	**3a**	**4**	**5**	**5a**	**5b**	**6**	**6a**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**32a**	**33**	**34**	**35**	**36**	**37**	**38**	**40**	**41**	**50**	**50a**	**51**	**52**	**53**	**53a**	**52**	**53**	**60**	**61**	**62**	**63**	**64**	**65**	**66**	**67**	**68**	**69**	**70**	**71**	**72**	**73**	**74**	**75**	**76**	**80**	**81**
The following measurements can be done in any one of several test cases. The test cases indicated are those which may most likely be used to make the measurements.																																																																										
XCLOCK_out to X data out, test vectors, tsu, record (>0.7 nsec)				x																																																																					
XCLOCK_out to X data out, test vectors, thold, record (>0.5 nsec)				x																																																																					
YCLOCK_out to Y data out, test vectors, tsu, record (>0.7 nsec)				x																																																																					
YCLOCK_out to Y data out, test vectors, thold, record (>0.5 nsec)				x																																																																					
X outputs: record voltage levels (must be within 2.5 V I/O standard)				x																																																																					
Y outputs: record voltage levels (must be within 2.5 V I/O standard)				x																																																																					
XCLOCK_O duty cycle: 47% < duty_cycle < 53%				x																																																																					
YCLOCK_O duty cycle: 47% < duty_cycle < 53%				x																																																																					
LCI clock to LCI data tco, record (max=1.5 nsec; min=-0.2 nsec)				x																																																																					
LCI inputs from LTA FPGA, tsu, record				x																																																																					
LCI inputs from LTA FPGA, thold, record				x																																																																					
LCI_DATA_CLKOUT, jitter < 150 ps, all chips daisy-chained, record.				x																																																																					
LCI interface signals: record voltage levels (must be within 2.5 V I/O standard)				x																																																																					
MCB clock to MCB_DATA, tco, record				x																																																																					
MCB clock tsu, record				x																																																																					
MCB clock thold, record				x																																																																					
MCB DATA out: record voltage levels (must be within 2.5 V I/O standard)				x																																																																					
LCI corr chip-to-LTA data interface, normal data transfer cycle							x																																																																	
LCI corr chip-to-LTA data interface, frame abort cycle.																																																	x			x																					
schid_frame sync with X-path > Y-path by ~10 m, test corr ok																																																																				x				
schid_frame sync with Y-path > X-path by ~10 m, test corr ok																																																																				x				
JTAG test ok. Conforms to IEEE-1149.1																																																																										
RESET_pad_ ok. Does not affect daisy-chain outputs.				x																																																																					
PLL_RESET_pad_ ok. Record lock time, if possible.				x																																																																					
Power dissipation, all I/Os active, 200 usec integration time, 256 Ms/s, all CCCs active, record																																																																									x
X input-to-final X output daisy chain delay, all 8 chips in column active; record; max=99.7 ns, including PCB wiring delays.				x																																																																					
Y input-to-final Y output daisy chain delay, all 8 chips in column active; record; max=99.7 ns, including PCB wiring delays.				x																																																																					
X/Y test vectors, all chips daisy-chained, no errors, 300 MHz. TVEN=1					x																																																																			
Normal operation, all CCCs independently correlate, all inputs active, all poln products, 300 MHz. Record core voltage and power required for this test.											x																																																												
Normal operation, all CCCs concatenated, inputs 0,1, 300 MHz.																																						x																																							
Normal operation, all CCCs concatenated, inputs X 6,7; Y 0,1, 300 MHz.																																						x																																							
Test Case Number	**0**	**1**	**2**	**3**	**3a**	**4**	**5**	**5a**	**5b**	**6**	**6a**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**32a**	**33**	**34**	**35**	**36**	**37**	**38**	**40**	**41**	**50**	**50a**	**51**	**52**	**53**	**53a**	**52**	**53**	**60**	**61**	**62**	**63**	**64**	**65**	**66**	**67**	**68**	**69**	**70**	**71**	**72**	**73**	**74**	**75**	**76**	**80**	**81**
Chaining configurations tests (a==all)																																																																										
CCC-0 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S			P		P	P	S	S		P	P	S	P	S		P	PS		PS		PS			P	S	P	P		A																												
CCC-0 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S			P		A	A	A	A		A	A	A	A	A		A	A		A		A			P	A	A	A		A																												
CCC-1 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S			P		A	A	A	A		A	A	A	A	A		A	A		A		A			P	A	A	A		A																												
CCC-1 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P			S		P	S	P	S		A	A	A	A	A		A	A		A		A			S	A	A	S		A																												
CCC-2 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P			S		S	S	P	P		A	A	A	A	A		A	A		A		A			S	A	A	S		A																												
CCC-2 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S			P		A	A	A	A		A	A	A	A	A		A	A		A		A			P	P	A	A		A																												
CCC-3 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P			S		A	A	A	A		A	A	A	A	A		A	A		A		A			S	P	A	A		A																												
CCC-3 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P			S		S	P	S	P		P	P	S	S	P		P	A		A		A			S	S	S	P		A																												
CCC-4 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					P	P	S	S		P	P	S	P	S		P	A		A		A			P	P	S	P		A																												
CCC-4 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					A	A	A	A		A	A	A	A	A		A	A		A		A			A	P	A	A		A																												
CCC-5 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					A	A	A	A		A	A	A	A	A		A	A		A		A			A	P	A	A		A																												
CCC-5 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					P	S	P	S		A	A	A	A	A		A	A		A		A			S	S	A	A		A																												
CCC-6 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					S	S	P	P		A	A	A	A	A		A	A		A		A			S	S	A	A		A																												
CCC-6 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					A	A	A	A		A	A	A	A	A		A	A		A		A			A	P	P	A		A																												
CCC-7 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					A	A	A	A		A	A	A	A	A		A	A		A		A			A	S	P	A		A																												
CCC-7 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					S	P	S	P		S	P	S	S	P		S	PS		PS		A			P	S	S	S		A																												
CCC-8 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					P	P	S	S		S	P	S	P	S		S	PS		PS		A			P	P	P	S		A																												
CCC-8 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					A	A	A	A		A	A	A	A	A		A	A		A		A			A	A	P	A		A																												
CCC-9 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					A	A	A	A		A	A	A	A	A		A	A		A		A			A	A	P	A		A																												
CCC-9 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					P	S	P	S		A	A	A	A	A		A	A		A		A			A	S	S	A		A																												
CCC-10 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					S	S	P	P		A	A	A	A	A		A	A		A		A			A	S	S	A		A																												
CCC-10 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					A	A	A	A		A	A	A	A	A		A	A		A		A			A	A	P	P		A																												
CCC-11 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					A	A	A	A		A	A	A	A	A		A	A		A		A			A	A	S	P		A																												
CCC-11 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					S	P	S	P		P	P	S	S	P		P	A		A		A			S	P	S	S		A																												
CCC-12 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					P	P	S	S		S	P	S	P	S		S	A		A		A			S	P	P	P		A																												
CCC-12 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					A	A	A	A		A	A	A	A	A		A	A		A		A			A	A	A	P		A																												
CCC-13 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					A	A	A	A		A	A	A	A	A		A	A		A		A			A	A	A	P		A																												
CCC-14 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					P	S	P	S		A	A	A	A	A		A	A		A		A			A	A	S	S		A																												
CCC-14 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					S	S	P	P		A	A	A	A	A		A	A		A		A			A	A	S	S		A																												
CCC-14 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			P		S			P	S					A	A	A	A		A	A	A	A	A		A	A		A		A			P	A	A	P		A																												
CCC-15 X: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					A	A	A	A		A	A	A	A	A		A	A		A		A			P	A	A	S		A																												
CCC-15 Y: A-adjacent; P-primary; S-seconday; U-undef. 256 Ms/s							U			S		P			S	P					S	P	S	P		S	P	S	S	P		S	PS		PS		PS			S	S	P	S		A																												

Note: Test #5 sequentially turns on each CCC, one at a time, to test for the correctness of the output frame and the accumulator values. As a consequence, each CCC will also be connected to the undefined (U) input, to deactivate it, thus resulting in testing each CCC for that "non-connection".

Test Case Number	0	1	2	3	3a	4	5	5a	5b	6	6a	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	32a	33	34	35	36	37	38	40	41	50	50a	51	52	53	53a	52	53	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	80	81
CCQ-0 X Switch 0 (P--Primary; S-Secondary) 256 Ms/s										P		P			P	P			S		P	P	P	P		P	P		P				P	P		P		PS			P	P	P	P																															
CCQ-0 X Switch 1 (P--Primary; S-Secondary) 256 Ms/s										P		P			P	P			S		P	P	P	P				P		P							PS			P	P		P																															
CCQ-0 Y Switch 0 (P--Primary; S-Secondary) 256 Ms/s; YS0 is no connect										P		P			P	P			P		P	P	P	P		P	P			P		P								P	P		P																												
CCQ-0 Y Switch 1 (P--Primary; S-Secondary) 256 Ms/s; YS1 is no connect										P		P			P	P			P		P	P	P	P				P	P											P	P	P	P																												
CCQ-1 X Switch 0 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P		S	P		P			S								P	P	P	P																												
CCQ-1 X Switch 1 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P				P		P										P	P	P																												
CCQ-1 Y Switch 0 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P			P			P			P		P					P	P	P																												
CCQ-1 Y Switch 1 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P		S		P	P			S								P	P	P	P																												
CCQ-2 X Switch 0 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P			P		P				PS		PS					P	P	P	P																												
CCQ-2 X Switch 1 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P		S		P		P		S	PS		PS						P	P	P																												
CCQ-2 Y Switch 0 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P		S	P			P		S									P	P	P																												
CCQ-2 Y Switch 1 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P				P	P											P	P	P	P																												
CCQ-3 X Switch 0 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P			P		P											P	P	P	P																												
CCQ-3 X Switch 1 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P		S		P		P		S								P		P	P																												
CCQ-3 Y Switch 0 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P			P			P			PS		PS		PS			P		P	P																												
CCQ-3 Y Switch 1 (P--Primary; S-Secondary) 256 Ms/s										P		P			S	S					P	P	P	P		S		P	P			S	PS		PS		PS			P	P	P	P																												

Test Case Number	0	1	2	3	3a	4	5	5a	5b	6	6a	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	32a	33	34	35	36	37	38	40	41	50	50a	51	52	53	53a	52	53	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	80	81
CCC-0 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S	P	PS					PS						PS			PS		PS			PS					PS		A																												
CCC-0 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S	P	PS					A						A			A		A			A					PS		A																												
CCC-1 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S	P	PS					A						A			A		A			A					PS		A																												
CCC-1 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P	S	PS					PS						A			A		A			A					SA		A																												
CCC-2 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P	S	PS					PS						A			A		A			A					SA		A																												
CCC-2 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S	P	PS					A						A			A		A			A					PA		A																												
CCC-3 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P	S	PS					A						A			A		A			A					a		A																												
CCC-3 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P	S	PS					PS						PS			A		A			A					PS		A																												
CCC-4 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					PS						PS			A		A			A					PS		A																												
CCC-4 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					A						A			A		A			A					PA		A																												
CCC-5 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					A						A			A		A			A					PA		A																												
CCC-5 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					PS						A			A		A			A					SA		A																												
CCC-6 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					PS						A			A		A			A					SA		A																												
CCC-6 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					A						A			A		A			A					PA		A																												
CCC-7 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					A						A			A		A			A					a		A																												
CCC-7 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					PS						PS			PS		PS			A					PS		A																												
CCC-8 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					PS						PS			PS		PS			A					PS		A																												
CCC-8 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					A						A			A		A			A					PA		A																												
CCC-9 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					A						A			A		A			A					PA		A																												
CCC-9 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					PS						A			A		A			A					SA		A																												
CCC-10 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					PS						A			A		A			A					SA		A																												
CCC-10 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					A						A			A		A			A					PA		A																												
CCC-11 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					A						A			A		A			A					a		A																												
CCC-11 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					PS						PS			A		A			A					PS		A																												
CCC-12 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					PS						PS			A		A			A					PS		A																												
CCC-12 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					A						A			A		A			A					PA		A																												
CCC-13 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					A						A			A		A			A					PA		A																												
CCC-14 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					PS						A			A		A			A					SA		A																												
CCC-14 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					PS						A			A		A			A					SA		A																												
CCC-14 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					P	S			P	S		PS					A						A			A		A			A					PA		A																												
CCC-15 X: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					A						A			A		A			A					a		A																												
CCC-15 Y: A-adjacent; P-primary; S-seconday. <256 Ms/s								U					S	P			S	P		PS					PS						PS			PS		PS			PS					PS		A																												

Test Case Number	0	1	2	3	3a	4	5	5a	5b	6	6a	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	32a	33	34	35	36	37	38	40	41	50	50a	51	52	53	53a	52	53	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	80	81
CCQ-0 X Switch 0 (P--Primary; S-Secondary) <256 Ms/s													P	P			P	P	S	a					P						P			P		P			PS					P																															
CCQ-0 X Switch 1 (P--Primary; S-Secondary) <256 Ms/s													P	P			P	P	S	a					P						P								PS					P																															
CCQ-0 Y Switch 0 (P--Primary; S-Secondary) <256 Ms/s; YS0 is no connect													P	P			P	P	P	P					P						P													P																												
CCQ-0 Y Switch 1 (P--Primary; S-Secondary) <256 Ms/s; YS1 is no connect													P	P			P	P	P	P					P						P													P																												
CCQ-1 X Switch 0 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P													P																												
CCQ-1 X Switch 1 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P													P																												
CCQ-1 Y Switch 0 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P			P		P									P																												
CCQ-1 Y Switch 1 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P													P																												
CCQ-2 X Switch 0 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P			PS		PS									P																												
CCQ-2 X Switch 1 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P			PS		PS									P																												
CCQ-2 Y Switch 0 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P													P																												
CCQ-2 Y Switch 1 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P													P																												
CCQ-3 X Switch 0 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P													P																												
CCQ-3 X Switch 1 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P													P																												
CCQ-3 Y Switch 0 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P			PS		PS			PS					P																												
CCQ-3 Y Switch 1 (P--Primary; S-Secondary) <256 Ms/s													P	P			S	S		a					P						P			PS		PS			PS					P																												

Note: Test# 15 is specifically designed to ensure that SE_CLK routing is correct in the chip, with no assumptions made. I.e. it assigns different sample rates to each input and ensures that SE_CLK routing is correct for each configuration in Tests 6-14. Test# 15 thus tests all (a) routing paths at sample rates <256 Ms/s.

Test Case Number	0	1	2	3	3a	4	5	5a	5b	6	6a	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	32a	33	34	35	36	37	38	40	41	50	50a	51	52	53	53a	52	53	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	80	81
Multiply, Phase-rotate, Accumulate tests.																																																																														
CCC-0: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																				
CCC-1: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-2: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-3: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-4: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-5: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-6: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-7: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-8: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-9: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-10: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-11: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-12: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			
CCC-13: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																			

CCC-14: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																		
CCC-15: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, 256 Ms/s.							x																																																																		
CCC-0: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																
CCC-1: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-2: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-3: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-4: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-5: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-6: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-7: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-8: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-9: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-10: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-11: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-12: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-13: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-14: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
CCC-15: all Re, Im accums ok, 500 usec, no OV, c/w full-cycle phase, <256 Ms/s.								x																																																																	
Test Case Number	**0**	**1**	**2**	**3**	**3a**	**4**	**5**	**5a**	**5b**	**6**	**6a**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**32a**	**33**	**34**	**35**	**36**	**37**	**38**	**40**	**41**	**50**	**50a**	**51**	**52**	**53**	**53a**	**52**	**53**	**60**	**61**	**62**	**63**	**64**	**65**	**66**	**67**	**68**	**69**	**70**	**71**	**72**	**73**	**74**	**75**	**76**	**80**	**81**
CCC-0: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-1: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-2: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-3: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-4: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-5: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-6: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-7: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-8: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-9: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-10: all Re, Im accums ok, >600 usec, OV									x																																																																		
CCC-11: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-12: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-13: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-14: all Re, Im accums ok, >600 usec, OV									x																																																																	
CCC-15: all Re, Im accums ok, >600 usec, OV									x																																																																	
Test Case Number	**0**	**1**	**2**	**3**	**3a**	**4**	**5**	**5a**	**5b**	**6**	**6a**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**32a**	**33**	**34**	**35**	**36**	**37**	**38**	**40**	**41**	**50**	**50a**	**51**	**52**	**53**	**53a**	**52**	**53**	**60**	**61**	**62**	**63**	**64**	**65**	**66**	**67**	**68**	**69**	**70**	**71**	**72**	**73**	**74**	**75**	**76**	**80**	**81**
Output frame contents (checked for each CCC):																																																																										
CMD--all bit combinations applicable: 000, 001, 010, 011, 100, 101.																																																																x										
CCC#--same as the CCC under test.							x	x	x																																																					x											
NUM_CLAGS=128							x	x	x																																																																
STATUS bits:																																																																											
OVR																																																	x																										
ACC_OV									x																																																																	
XSyncerr																																																									x																	
YSyncerr																																																									x																	
X_CCC_input																					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x	x	x	x	x	x	x															x													
Y_CCC_input																					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x	x	x	x	x	x	x															x													
SID-X: all bits exercised independently.																																																											x														
SBID-X: all bit combinations.																																																											x														
BBID-X: all bit combinations.																																																											x														
SID-Y: all bits exercised independently.																																																											x														
SBID-Y: all bit combinations.																																																											x														
BBID-Y: all bit combinations.																																																											x														
RECIRC_BLK-X: all bits exercised independently.																																																																x									
RECIRC_BLK-Y: all bits exercised independently.																																																																	x								
Phase Bin: bins 0-999 and banks 0,1																																																													x												
TIMESTAMP-0: all bits exercised independently.																																																																		x							
TIMESTAMP-1: all bits exercised independently.																																																																		x							
DVCOUNT-Center: exercised for range of integration times from 20 usec to 600 usec																																																																						x			
DVCOUNT-Edge: exercised for range of integration times from 20 usec to 600 usec																																																																					x			
DATA_BIAS: exercised for range of integration times from 20 usec to 600 usec																																																																						x			
Lag accumulators: bit exact with behavioural sim; minimum complete wrap of phase, range of integration times from 20 to 600 usec.																																																																						x			
START SYNC Word correct.							x																																																																		
END SYNC Word correct.							x																																																																		
CHECKSUM correct.							x																																																																		
Test Case Number	**0**	**1**	**2**	**3**	**3a**	**4**	**5**	**5a**	**5b**	**6**	**6a**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**32a**	**33**	**34**	**35**	**36**	**37**	**38**	**40**	**41**	**50**	**50a**	**51**	**52**	**53**	**53a**	**52**	**53**	**60**	**61**	**62**	**63**	**64**	**65**	**66**	**67**	**68**	**69**	**70**	**71**	**72**	**73**	**74**	**75**	**76**	**80**	**81**
Dump control parameters.																																																																										
NOTE: all bits exercised, to be considered tested.																																																																											
X-0 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C	R							H		
X-1 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C	R							H		
X-2 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C	R							H		
X-3 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C	R							H		
X-4 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C	R							H		
X-5 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C	R							H		
X-6 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C	R							H		
X-7 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C	R							H		
NOTE: all bits exercised, to be considered tested.																																																																											
Y-0 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C		R						H		
Y-1 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C		R						H		
Y-2 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C		R						H		
Y-3 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C		R						H		
Y-4 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C		R						H		
Y-5 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C		R						H		
Y-6 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C		R						H		
Y-7 input dump_en: F=function; C=CMD; P=Phase bin; R=Recirc block; H=holdof							F																																																					P		C		R						H		
X-Timestamp: all bits exercised.																																																																		x							
Y-Timestamp: all bits exercised.																																																																		x							
Test Case Number	**0**	**1**	**2**	**3**	**3a**	**4**	**5**	**5a**	**5b**	**6**	**6a**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**32a**	**33**	**34**	**35**	**36**	**37**	**38**	**40**	**41**	**50**	**50a**	**51**	**52**	**53**	**53a**	**52**	**53**	**60**	**61**	**62**	**63**	**64**	**65**	**66**	**67**	**68**	**69**	**70**	**71**	**72**	**73**	**74**	**75**	**76**	**80**	**81**
High performance dump and data integrity.																																																																										

Fast, burst-dump, all CCCs, no overruns (dump-save ~160 usec)																																															x																									
Fast, burst-dump, all CCCs, overruns (dump-save ~20 usec)																																																		x																					
Fast, burst-dump, all CCCs, overruns (dump-integrate-save ~20 usec)																																																x																								
Autocorrelator mode tests.																																																																								
Note: for autocorrelator mode tests, the Y_CLOCK input held low.																																																																								
Autocorrelator mode: X input 0 active, 256 Ms/s																																												x																												
Autocorrelator mode: X input 1 active, 256 Ms/s																																												x																												
Autocorrelator mode: X input 2 active, 256 Ms/s																																												x																												
Autocorrelator mode: X input 3 active, 256 Ms/s																																												x																												
Autocorrelator mode: X input 4 active, 256 Ms/s																																												x																												
Autocorrelator mode: X input 5 active, 256 Ms/s																																												x																												
Autocorrelator mode: X input 6 active, 256 Ms/s																																												x																												
Autocorrelator mode: X input 7 active, 256 Ms/s																																												x																												
Autocorrelator mode: X input 0 active, <256 Ms/s																																													x																											
Autocorrelator mode: X input 1 active, <256 Ms/s																																													x																											
Autocorrelator mode: X input 2 active, <256 Ms/s																																													x																											
Autocorrelator mode: X input 3 active, <256 Ms/s																																													x																											
Autocorrelator mode: X input 4 active, <256 Ms/s																																													x																											
Autocorrelator mode: X input 5 active, <256 Ms/s																																													x																											
Autocorrelator mode: X input 6 active, <256 Ms/s																																													x																											
Autocorrelator mode: X input 7 active, <256 Ms/s																																													x																											
Test Case Number	**0**	**1**	**2**	**3**	**3a**	**4**	**5**	**5a**	**5b**	**6**	**6a**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**32a**	**33**	**34**	**35**	**36**	**37**	**38**	**40**	**41**	**50**	**50a**	**51**	**52**	**53**	**53a**	**52**	**53**	**60**	**61**	**62**	**63**	**64**	**65**	**66**	**67**	**68**	**69**	**70**	**71**	**72**	**73**	**74**	**75**	**76**	**80**	**81**
MCB register bits.																																																																								
NOTE: all MCB control and status register tests must ensure the bit under test operates properly in both its set (1) and reset (0) state																																																																									
MCSR-CEN							x																																																																	
MCSR-TVEN		x	x	x		x																																																																		
MCSR-PhEN																																																									x																
MCSR-OVR																																																	x			x																					
MCSR-AOV									x																																																																
MCSR-TvER						x																																																																		
MCSR-SyncER																																																								x																	
MCSR-X/Y_DS																																																							x																		
NOTE: CCCSCR_0_1 … CCCSCR_14_15 functions tested with CCC input combinations. This tests the ability to set/reset each bit independently.																																																																					x					
NOTE: CCQR_1/2, CCQR_3/4 functions tested with CCC input combinations. This tests the ability to set/reset each bit independently.																																																																					x					
XYSSR: XAd, YAd: 0,1,2, …, C						x																																																	x																	
XSTATUS, all XAds, all bits						x																																																	x																	
YSTATUS, all YAds, all bits						x																																																	x																	
DESSR_0/7																																																										x															
DESSR_8/15																																																										x															
Miscl tests.																																																																								
Correlation, all CCCs in any chaining configuration, with no blanking time around the dump pulse. Statistical comparison with behavioural simulation.																																																																				x						