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Leaders in diagnostic services for microelectronics and photonics

Reliability Qualification Report on EVLA ASIC CA2048CL-F672C256-A WIDAR Correlator

Job No :	80013
Reference:	70573
Customer :	Brent Carlson
Company :	NRC
Author :	M. Simard-Normandin
Collaborators:	J. Woodward-Jack B. Oliver N. Tunca M. Beaulieu R. Sparks
Date :	August 29 2008
Problem Description :	Stress the devices according to a series of pre-set JEDEC conditions to evaluate the long term reliability of the product.

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1. Device Information

Device type : ASIC

Package : 672BGA

Qty received : 114

Branding : CA2048CL-F672C256-A
WIDAR Correlator
iSine, Inc.
N63944.12
0810
USA

Date received : April 4 2008

Parts received:

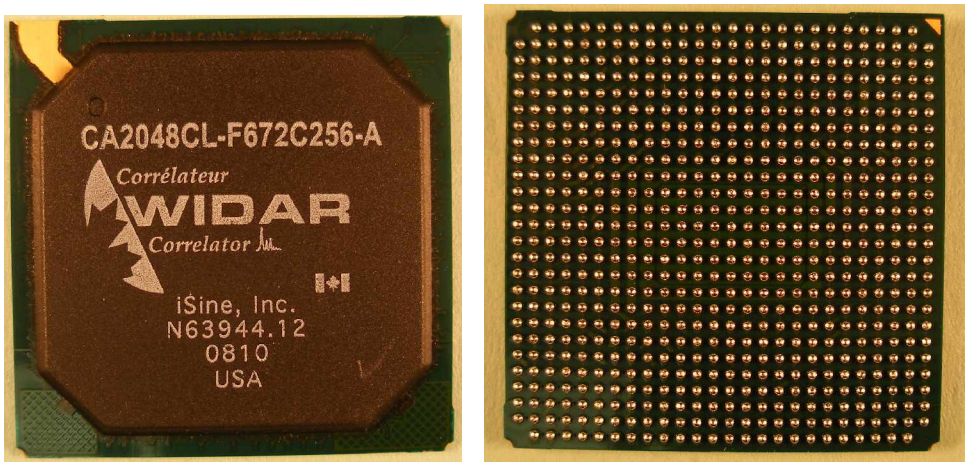

Figure 1. Appearance of the EVLA ASIC devices received.

In addition to devices, a stand alone tester was provided by NRC in order to verify the electrical integrity of the devices after each stress.

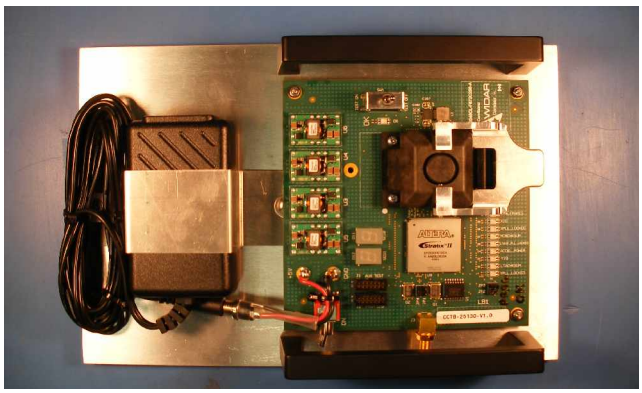

Figure 2. Appearance of the stand alone tester received.

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2. Results Summary

Tests	Results
ESD: Human body model testing per JESD 22-A114e	PASS
Latch-up testing per JESD78A	PASS
MSL per JEDEC J-STD-020d	PASS
HAST per JESD22-A118	PASS
TC per JESD22-A104c (conditions B&K1000 cycles)	PASS
HTS per JESD22-A103c	PASS

- The CA2048CL-F672C256-A WIDAR Correlator passes the JEDEC tests above, chosen for its qualification exercise.
    - Only one device failed electrically. It is suspected that mechanical damage to one corner was at the origin of the electrical failure.

- There is one small concern: the solder mask is open exposing the copper metallization between the solder balls. The exposed copper has not created any failures during the qualification tests but:

    - This could create issues when the devices are soldered to their boards if solder paste gets trapped there;

    - Over time, in a dry environment, conductive dust particles could accumulate there and create leakage between various signals.

- Another area of concern for long term reliability is the intermetallic formation at the bond pads. Over time these could increase the contact resistance of the bond wires. The problem can be reduced by keeping the part as cold as possible during operation.

- Because of these two concerns, it will be important to prepare test pieces of assembled devices for further tests.

- A screening test for devices should activate this bond pad concern without stressing the devices. It is suggested to submit the parts to 125ºC for 168 hours. This is a very standard burn-in condition for Si devices in BGA packages.

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3. Test Procedures

The exercise to be done here is to evaluate the quality of the product, which is to ensure that the die and the package will work well together for the full lifetime of the product.

The following tests and number of devices to be run have been chosen with this goal in mind.

Tests	No. devices
ESD: Human body model testing 1 voltage per device per JESD 22-A114e	6
Latch-up testing per JESD78A	6
MSL per JEDEC J-STD-020c with acoustic microscopy and electrical verification*	15
HAST per JESD22-A118 with acoustic microscopy and electrical verification*	25
TC per JESD22-A104c with acoustic microscopy and electrical verification*	25
HTS per JESD22-A103c with acoustic microscopy and electrical verification*	25

*All 102 chips in this exercise will be tested using the NRC provided stand alone tester before and after the tests, and at intermediate test points, as determined by the provisions of the standard used.

ESD: Electrostatic discharge is responsible for many early life failures in integrated circuits. It is important to characterize the device well in order to understand if there should be any particular precautions taken during its handling. Special hardware is needed to interface this ASIC to the ESD tester. It is included in the financial bid.

Latch-up (LU) : All CMOS devices are susceptible to latch-up. Latch-up can occur if there are transients in power or signals. Such transients often occur during re-start after a power outage. Observatories, being in remote locations, do suffer from power outages. The device needs to be properly characterized, so that if it exhibits any particular sensitivity, precautions can be taken to avoid catastrophes. Special hardware is needed to interface this ASIC to the LU tester. It is included in the financial bid. The same hardware will be used in the root cause FA later on.

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MSL: Moisture sensitivity level. Devices in plastic packages absorb moisture from the atmosphere. During soldering this moisture turns to steam and can damage the device. When the damage is severe the event is referred to as pop-corning, but this is generally avoidable. However subtle damage can occur, undetectable electrically, but it can lower the device life expectancy. Even subtle damage can be detected with acoustic microscopy and this is what is planned. Some devices may need to be replaced within the next twenty years. It will be important to fully comprehend the moisture sensitivity of the device in order to provide adequate instructions for future handling.

A subset of parts will be tested for Level 3, which is expected for such devices. If they do not pass level 3, we will use the remaining parts to assess into which MSL they fall, and issue recommendations for their future handling.

HAST: Highly accelerated stress test. BGA packages are more sensitive to humidity than one generally realizes. HAST is a short duration test that replaces the 1000 hrs at 85C 85%RH test. It is aggressive, but devices are intended to pass this test. If they fail, they have a weakness that will need to be recognized and addressed. If they pass, all is fine and one can be confident in long term longevity. Devices can pass electrical tests but still have suffered damage during the test. Acoustic microscopy is the technique of choice to reveal subtle issues. We will run the test unbiased, using Condition A, as defined by the standard.

TC: Temperature cycle. In BGAs there is a large mismatch of coefficient of thermal expansion between the package substrate and the silicon die. It is important to verify the robustness of devices, just as in HAST. With power ups and downs and system restarts, it is amazing how many temperature cycles a device can see in a 20 year lifetime. Again this is a test that devices should pass without any physical damage. Condition B of the standard (-55ºC, +125ºC; 1000 cycles) will be applied as dictated by JESD47. Interim tests will be done at 50,100 and 500 cycles. If there are significant fall-outs at 50 cycles, we will soften the condition to G (-40,+125) with notes to this effect in the report.

Since there were no failures with condition B after 250 cycles, and there were equipment concerns, in order to accelerate the test it was decided to use condition K (0ºC,+125ºC) for the remaining 750 cycles.

HTS: High Temperature storage. The most vulnerable part of the silicon chip is the bond pad-bond wire interface because it is exposed to the environment. Trace levels of contaminant in the package material, or left over from the etching or dicing process, can catalyze reactions that will take years to develop yet cause premature failures in the devices. This test aims at revealing this exposure. Condition B (150ºC for 1000hrs) does apply.

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4. Results

4.1 Initial tests and assignments

All devices were visually inspected and numbered. No 19 was found damaged.

All devices were tested electrically. No 23 failed initially, passed on re-test.

Devices 13-114 were tested by acoustic microscopy at 30MHz in C-Mode and through-scan. All passed. No 29 was scratched during test.

Devices 19, 23 and 29 were assigned to the role of profiling dummies.

Test	Sample #'s	Comment
ESD	1-6	
LU	7-12	
HTS	13-40 ex 19, 23, 29	Part 29 replaced with part 40 due to scratch during handling
MSL	41-45 (level 4) 46-55 106-110 (level 3)	
Preconditioning	56-105	Part 68 failed preconditioning. Mechanical damage upon retesting precluded further analysis.
TC	56-81, except 68	
HAST	82-105 +106 and 110 from MSL3	Part 105 scratched, replaced by part 106 but left in.

4.2 ESD test

The purpose of the assessment is to characterize Human Body Model ESD sensitivity of the EVLA device.

Samples were stressed applying one positive pulse and one negative pulse for each pin combination according to JEDEC JESD22-A114-E. Note: the ESD simulator has 256 channels. To test the complete device, the device was mapped into 4 orientations. Care was taken to ensure all pins were zapped and no pin was stressed more than once.

One device was stressed at each of 1000, 2000 and 4000 V. Three devices were stressed at 8000 V Human Body Model with no degradation observed.

A complete report is provided separately.

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4.3 LU test

The test was performed on the Ultra-Test International Multi-Trace tester according to JESD78A for each device in the following procedures:

The device under test was biased with power to the supply pins and 0 V to ground pins. Inputs are tied to a certain state, either high or low. The rise time on the pulse is approximately 50 microseconds. The pulse width remained constant at 10 ms. Cool down after the pulse was 100 ms. Delay before the post-pulse IDD measurement was 10 ms.

One device was stressed at 125ºC and 5 devices at 100ºC, with no indications of latch-up.

A complete report is provided separately.

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4.4 HTS test

Devices 13-40 except for devices 23 and 29 were tested for high temperature storage. The devices were put in a JEDEC tray and in an oven.

Stress duration 1002 hours per JESD22-A103c

Stress temperature: 150°C (+1. /-.5) on calibrated thermocouple gauge. The devices under test were not subjected to any voltage bias.

After stress inspection:

1. A few parts have scratches in the solder mask on the bottom, in the middle area. They are between and under balls, so cannot have happened any time after balling.

2. All parts are significantly discoloured after the HTS stress. This is normal and not a concern.

After stress test:

All devices passed first time, except for device #24 which failed first time and passed typically 50% of the time subsequently. Inspection located residue on two balls. After removal of the residue, the part passed consistently.

Acoustic microscopy was done on all devices after the HTS stress test. No delamination and significant difference from before the test and after the test were noted.

Electrical test: 25 of 25 tested good.

Device #15 was retained for cross-section analysis.

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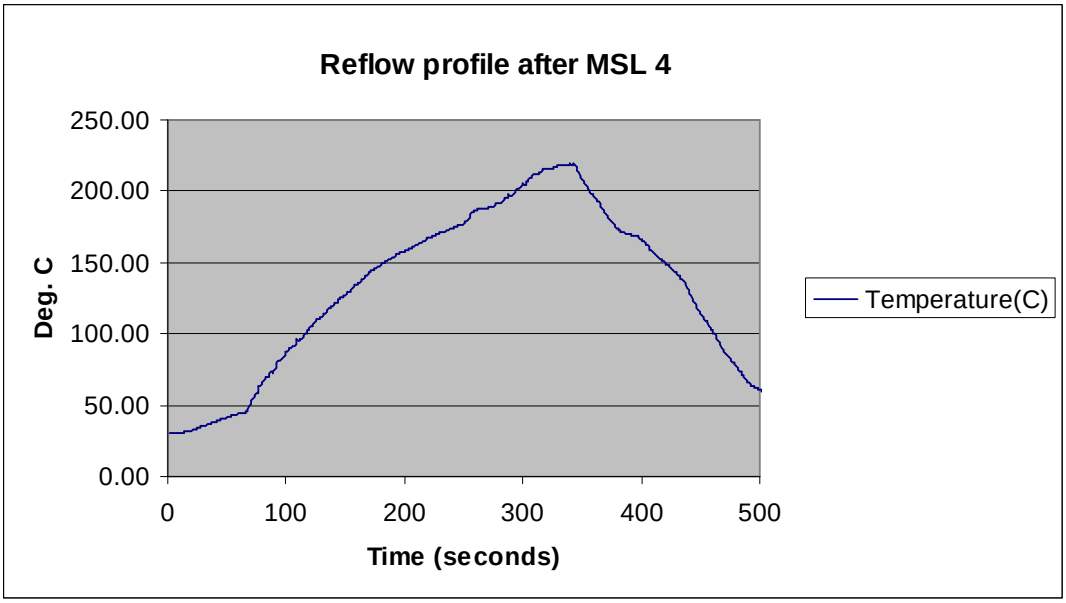
4.5 MSL determination and preconditioning

Devices 41-55 were tested to level 4 per JEDEC J-STD-020d.

Devices 46-55 and 106-110 were tested to level 3 per JEDEC J-STD-020d.

Devices 56-105 received Level 3 pre-conditioning.

Note**:** J-STD-020D specifies a user profile and a supplier profile. The supplier tin-lead profile was used for these devices. This means that for the tin-lead solder with the dimensions of the device, the peak temperature must be a minimum of 220ºC and the temperature within 5º of the peak must be attained for a minimum of 20 seconds.



Temp.(º C)	Time (s)	Specifications
100-150	66	60-120 s
>183	115	60-150 s
215-220	27	Min 20 s

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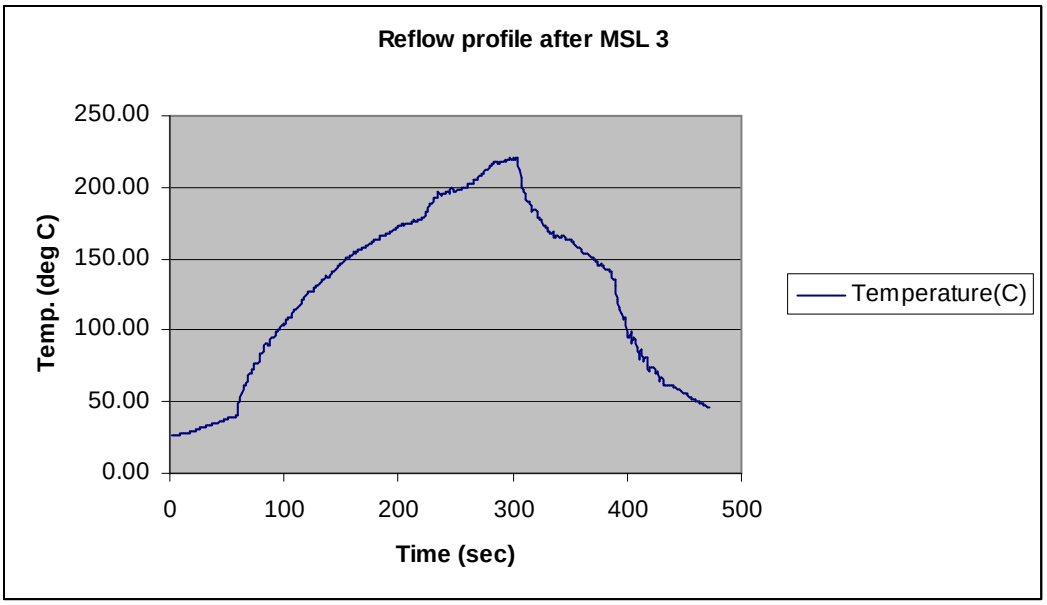

Temp. (ºC)	Time (s)	Specification
100-150	60	60-180 s
>183	91	60-150 s
215-220	23	Min 20 s

Acoustic microscopy was done on all devices, level 4 and level 3, after the reflow. No delamination and significant difference from before the test and after the test were observed.

Electrical test:

15 out of 15 parts submitted to MSL 4 passed.

64 out of 65 parts submitted to MSL 3 or preconditioning Level 3 (conditions are identical) passed.

One part (no. 68) failed LTACHKSUM, MCBCHKSUM, LTA_FRAMES

The device package became mechanically damaged and cracked in one corner upon a further attempt to retest. No further analysis was possible at this point. It is suspected that this mechanical damage was present in a latent stage and grew upon manipulation, and the cause of the electrical failure.

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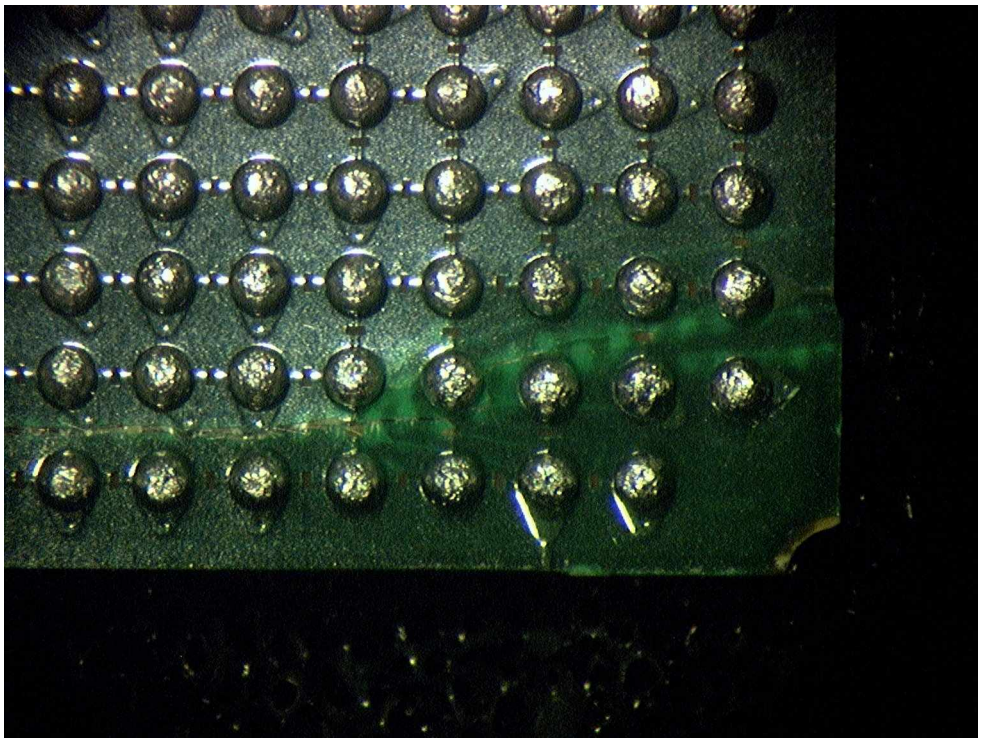

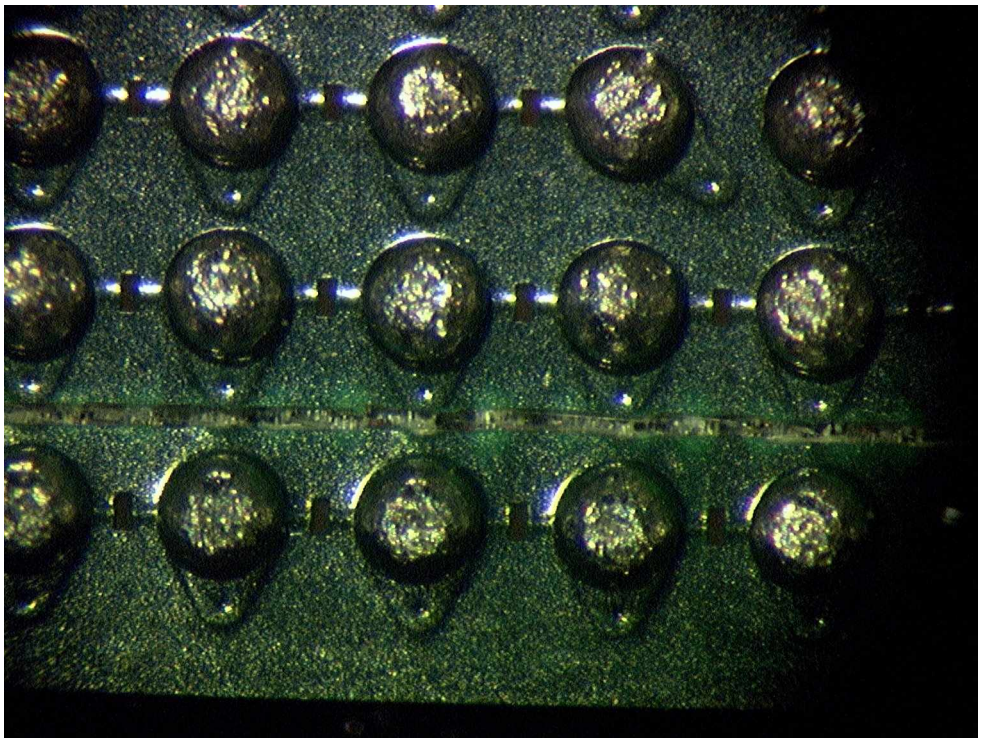

Broken corner from device 68.

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4.6 TC test

Devices 56-81 except 68 were tested for temperature cycling. The devices were put in a JEDEC tray and in an air-to-air temperature cycling chamber.

The TC was performed per JESD22-A104c.

For the first 250 cycles, condition B (-55°C to 125°C) was used. The instrument failed and could no longer reach -55C. The conditions were softened to K (0ºC to +125ºC). Condition K was selected because it maintains the 125ºC hot cycle, while softening only the cold part of the cycle. These parts are not destined for space or other harsh cold environments; the most likely temperature shock scenario for them is to cool from hot operation to near freezing temperature during a power outage.

Condition K (0ºC to 125°C) was used for the next 180 cycles. At that point we had instrument issues again. All parts passed electrically after the 430 cycles completed. No acoustic microscopy was performed on the 26 parts after the 430 cycles.

After the 430 cycles, all the devices (except for device #56) were put in storage at 85°C in an oven to prevent moisture to get into the devices, while the chamber was repaired. 85ºC was selected in order to avoid giving the parts an extra long hot duty cycle and to minimize intermetallic formation. Device #56 was retained for cross-section analysis.

For the remaining of the test (570 cycles), Condition K (0º to 125°C) was used.

All devices were tested electrically after the test was completed to 1000 cycles. All the devices passed electrically.

Acoustic microscopy was performed on the 25 devices after 1000 cycles. No delamination was seen on any device.

Condition	No of cycles	Range(ºC)
B	250	-55 to +125
K	180	0 to +125
Electrical test		All pass
K	500	0 to +125
Electrical test		All pass
K	70	0 to +125
Electrical test		All pass
CSAM		All pass

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A note of caution:

According to the JEDEC JESD47 guidelines, 3 lots of 25 devices each should be used.

For condition B, here should be no failures after 700 cycles.

For condition K, there should be no failures after 1500 cycles.

Due to the small number of devices, only 1 lot of 25 was stressed, with only 250 cycles at condition B and 750 cycles at condition K.

It has been understood from the start that this was a partial test, not meeting *all* the requirements of a full qualification.

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4.7 HAST test

Devices 82-106 and 110 were tested for Highly Accelerated Stress Testing.

The HAST was performed per JESD22-A118. Condition A (temperature 130°C and 85% RH for a duration of 96 hours) was used. No bias.

After stress inspection:

> All parts are significantly discoloured after HAST stress. This is normal and not a concern.

Alll parts passed electrically.

Acoustic microscopy after the HAST stress passed the test. No delamination and significant difference from before the test and after the test was noted.

Device #98 was retained for cross-section analysis.

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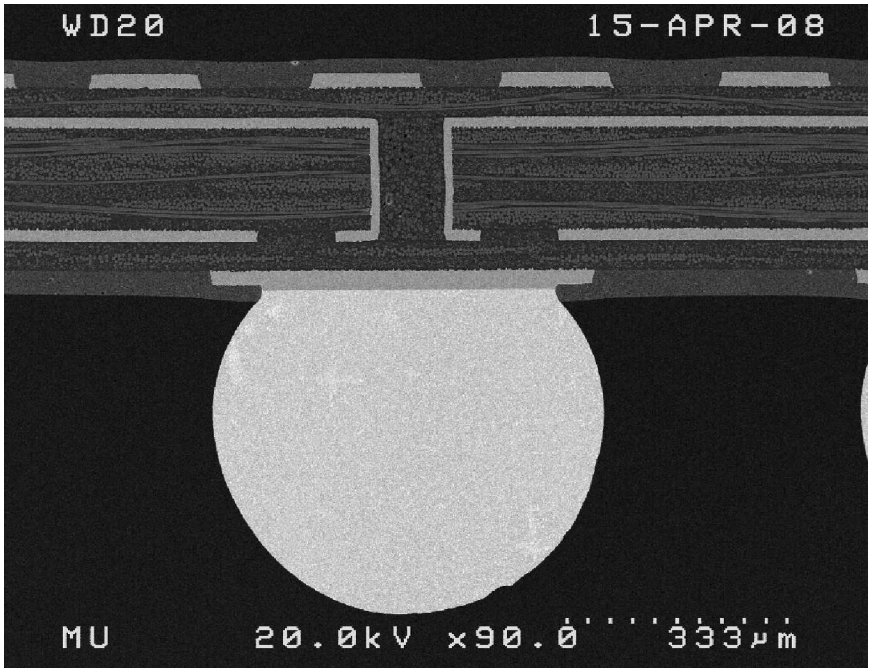
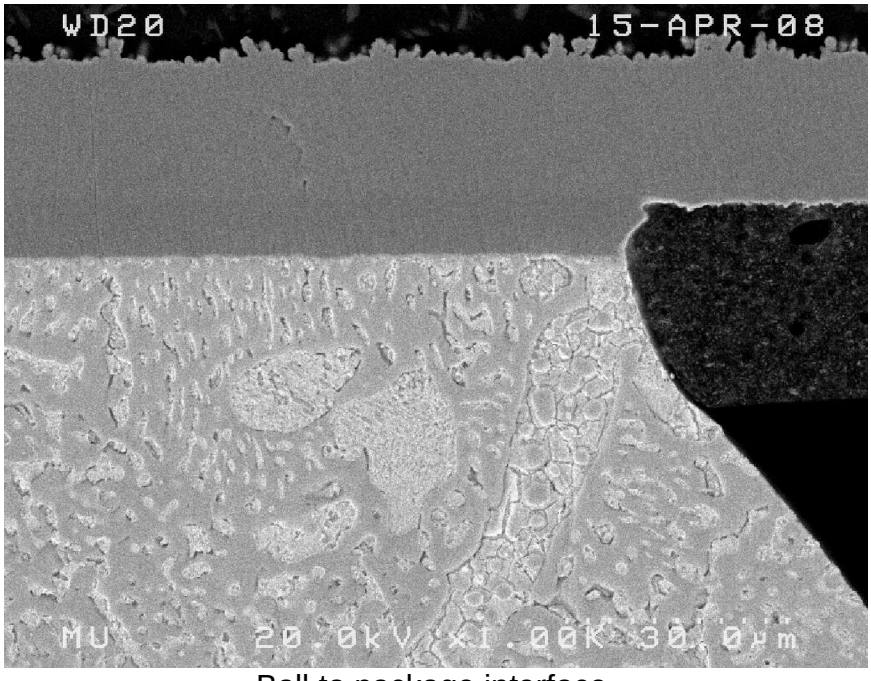
5. Cross-section analysis

5.1 Package construction.

The package appears well constructed.



Overview of package at ball location.



Ball to package interface.

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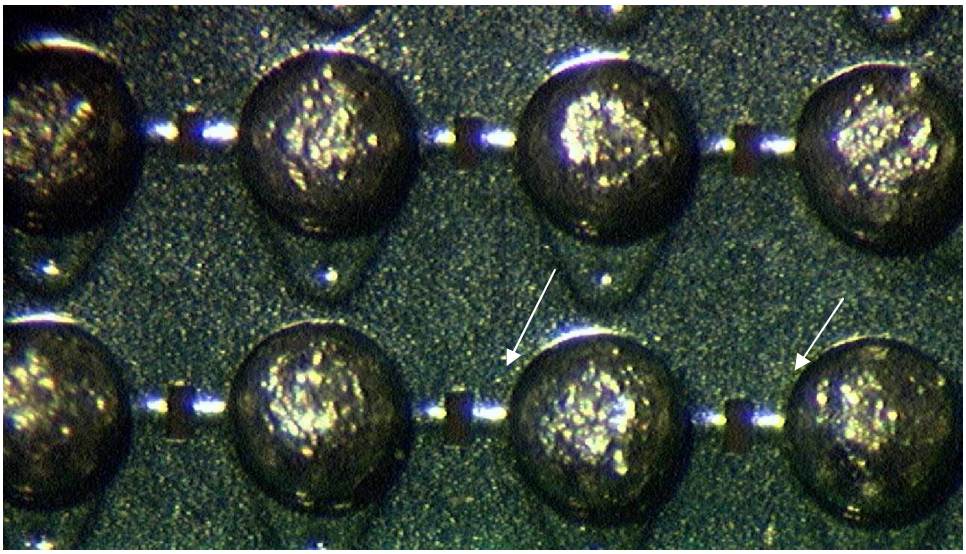
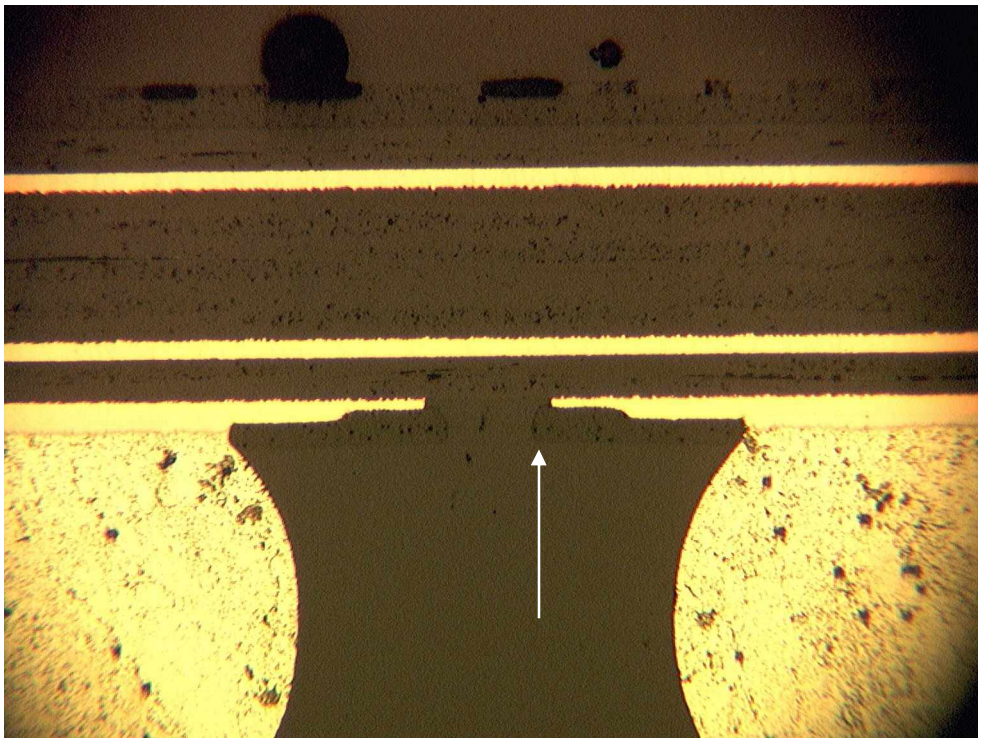


The solder mask is open exposing the ends of traces that connected the ball pads during plating.



Cross-section in the open solder mask area. The ends of the traces are exposed to elements. The spacing between different (exposed) signals is less than the pad to pad or ball to ball geometry.

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5.2 Bond-pad cross-section before and after tests.

There were no failure analysis to be done, the only failed device having suffered some very obvious mechanical damage. Instead one device from each stress test was cross-sectioned through the bond wires, the weaker part of the device, in order to determine the state of the joint after stress and to highlight any potential longer term reliability concerns.

The major concern in these devices is the formation of an intermetallic under the bond pad that consumes the Al layer. This intermetallic is brittle and subject to voiding, thus increasing the contact resistance of the bond wire.

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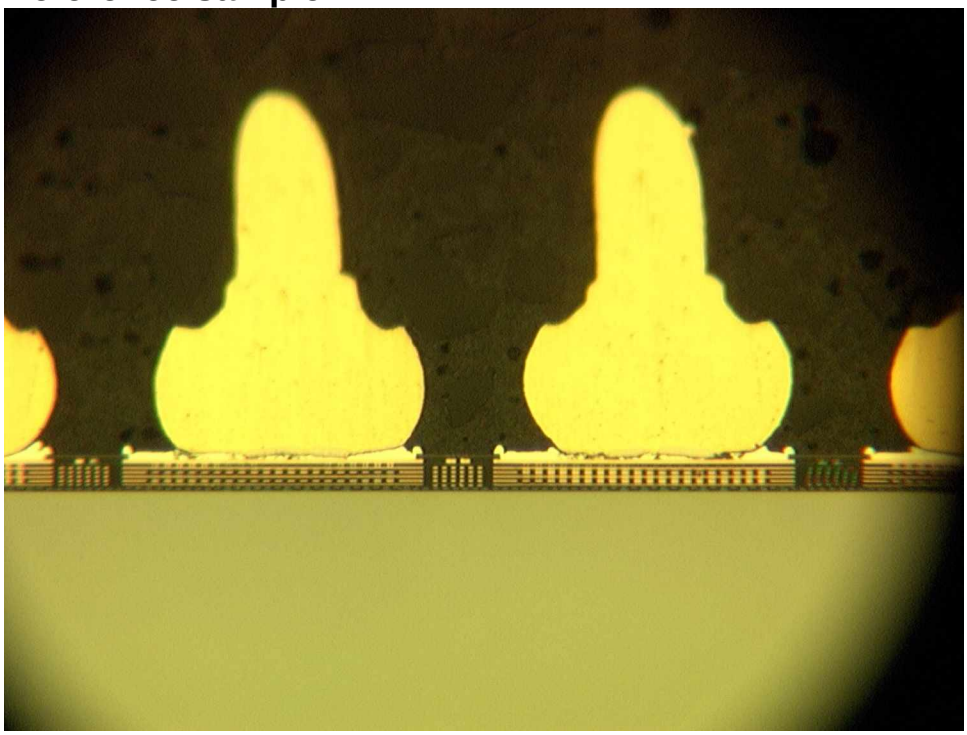
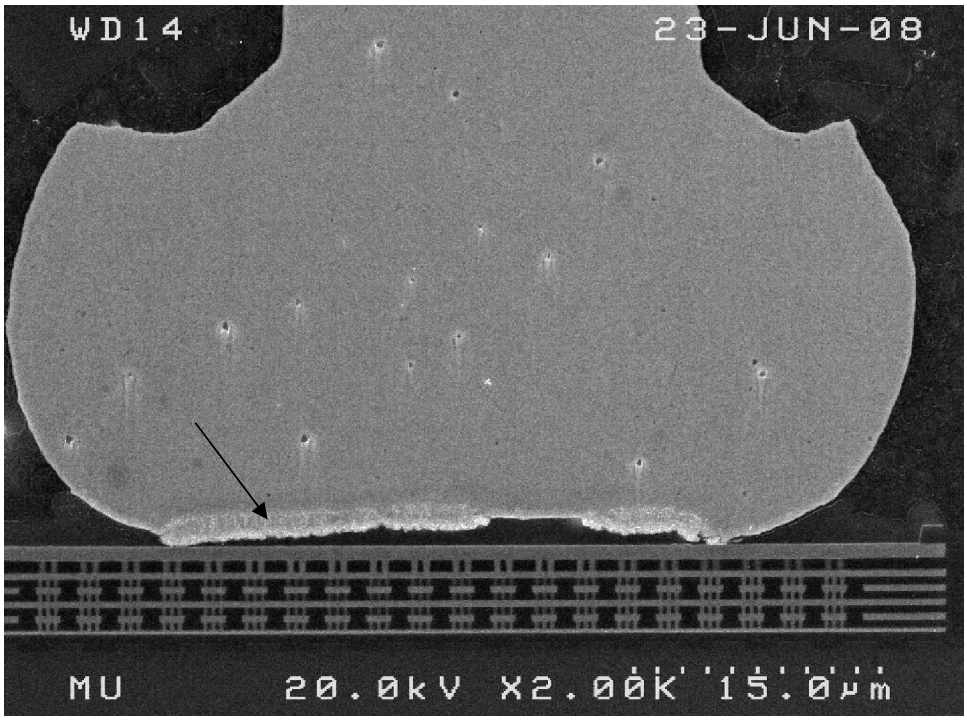
Reference sample:





The Al layer (bright under optical and dark under SEM) is continuous under the bond ball. The intermetallic layer (arrow) is uniform.

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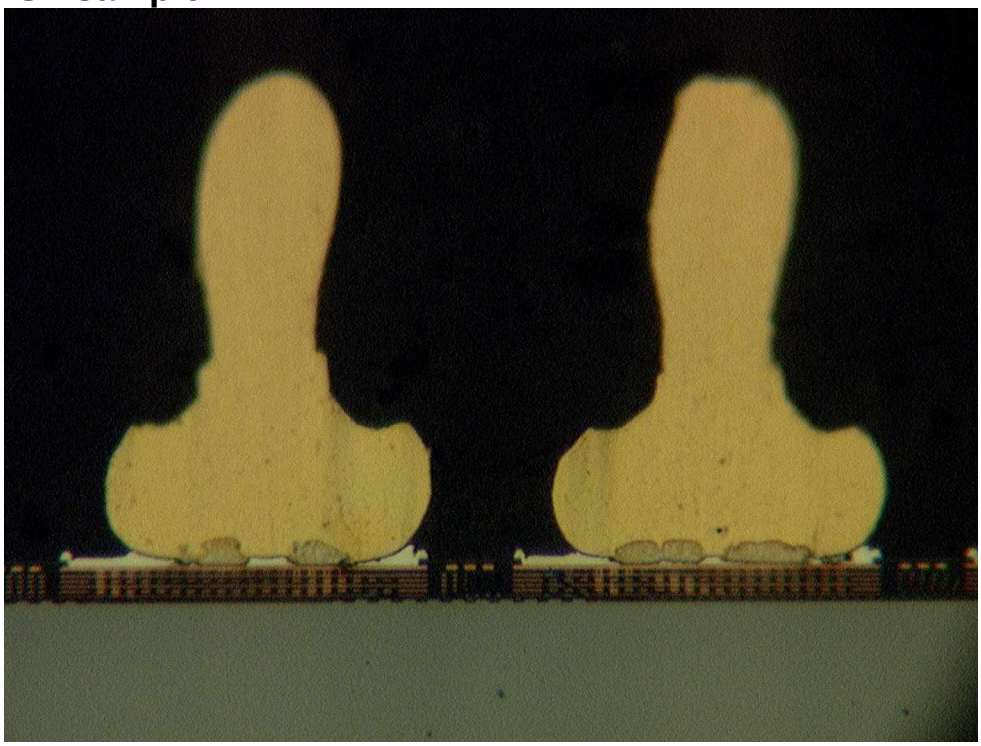
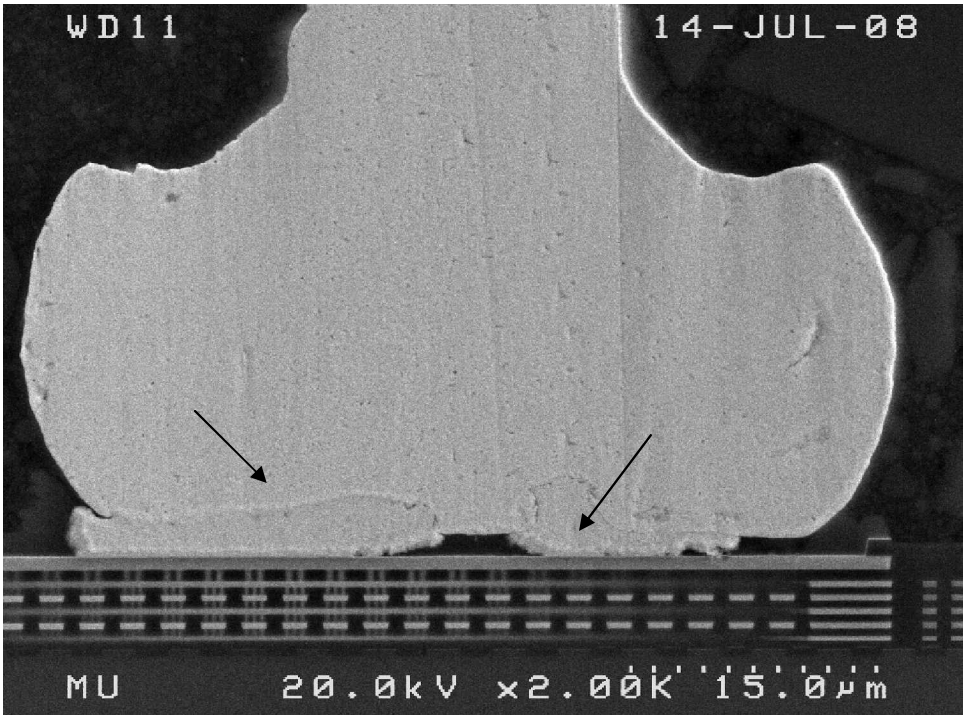
HAST sample





The intermetallic layer (arrows) has thickened and consumed most of the Al layer under the ball, stopping on the Cu layer.

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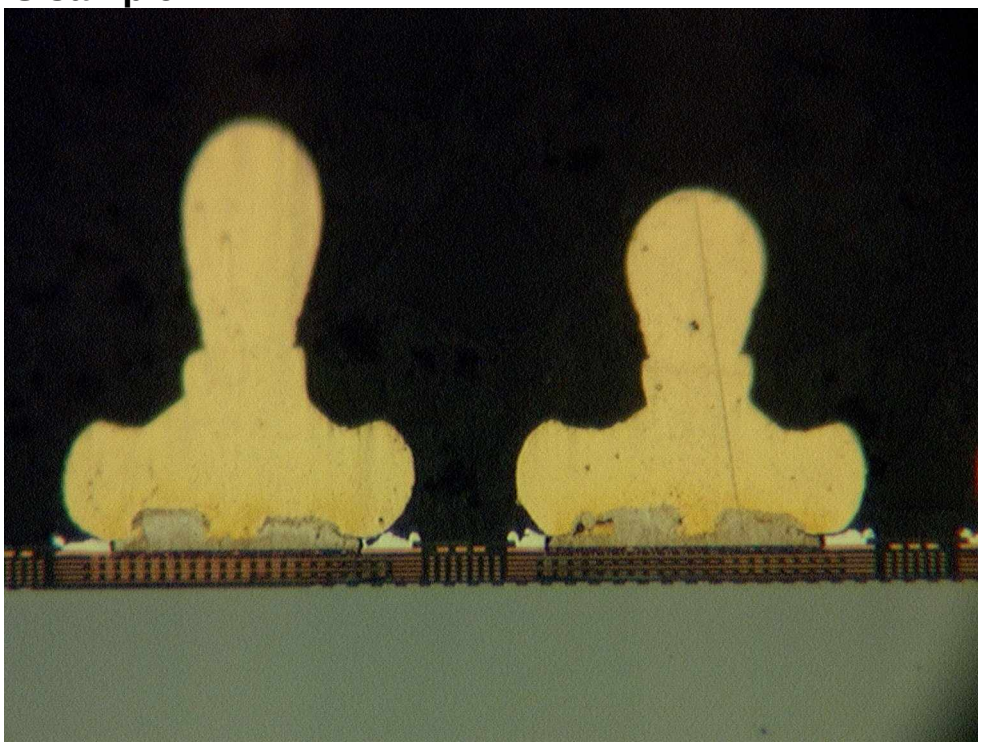
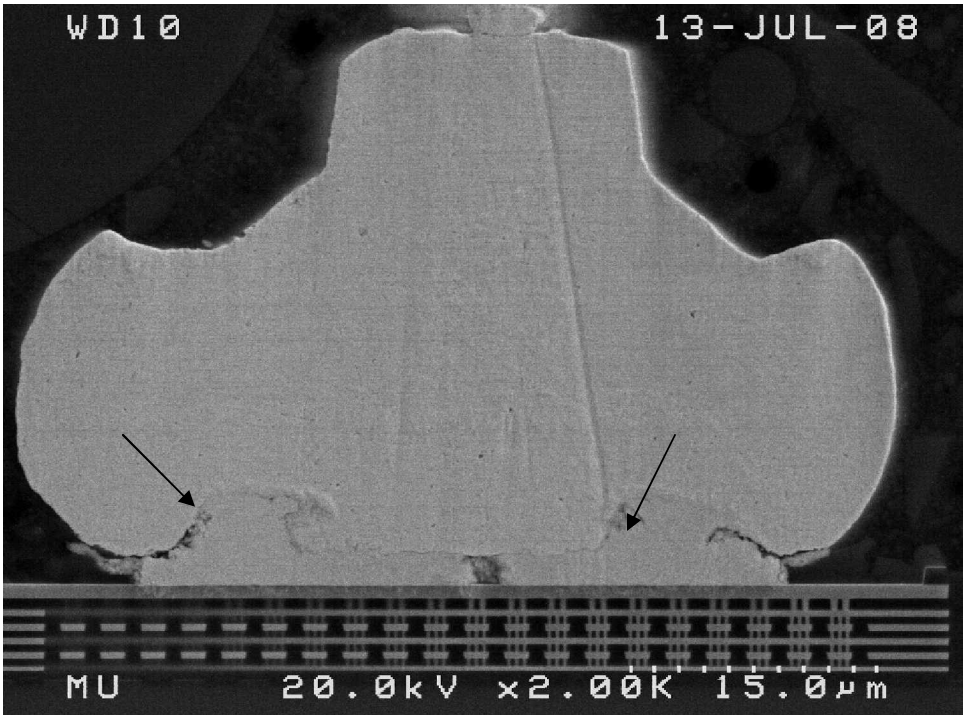
HTS sample





The intermetallic layer (arrows) is very thick and has consumed all of Al layer under the ball, stopping on the Cu layer.

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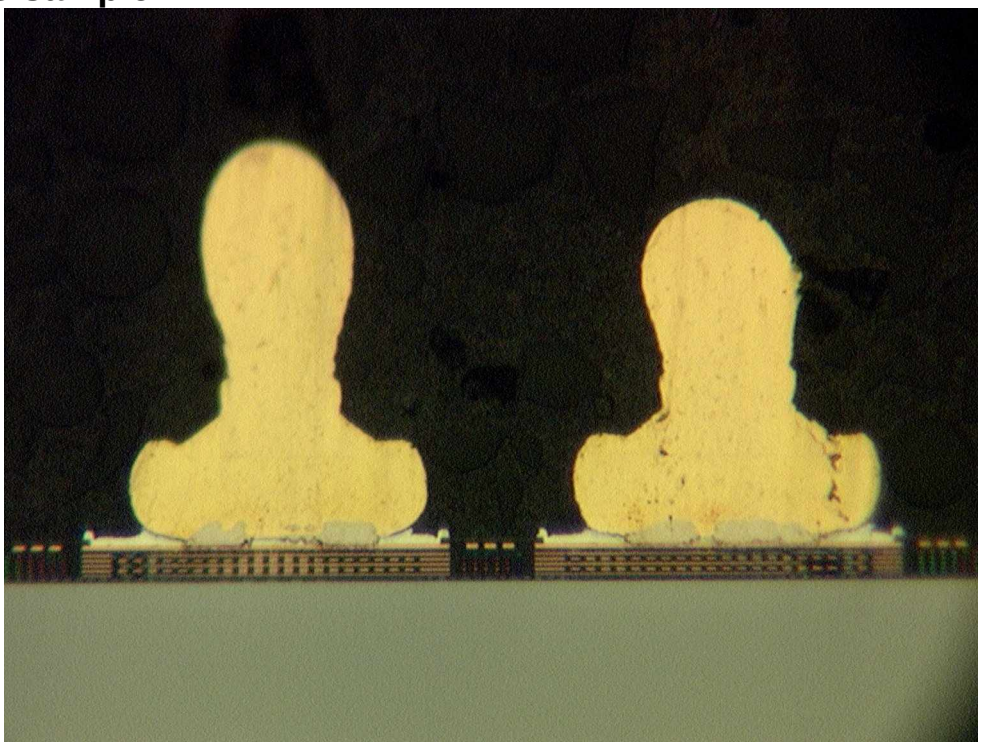
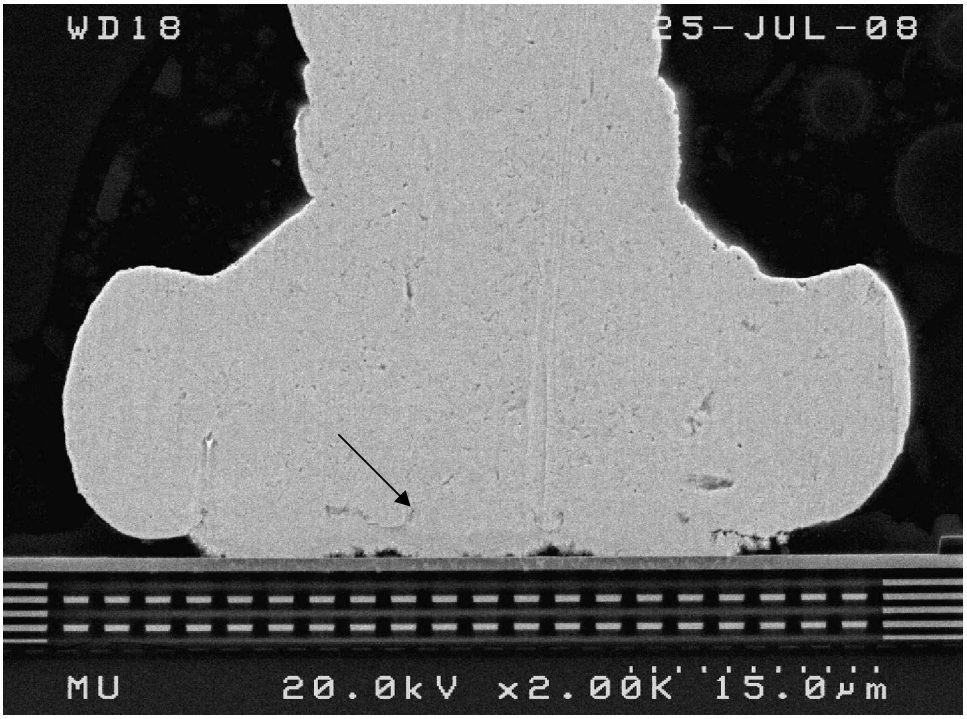
TC sample





The intermetallic layer (arrows) has thickened and consumed most of the Al layer under the ball, stopping on the Cu layer.

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5. Conclusion

- The CA2048CL-F672C256-A WIDAR Correlator passes the following JEDEC tests, chosen for its qualification exercise.
    - Only one device failed electrically. It is suspected that mechanical damage to one corner was at the origin of the electrical failure.

Tests	Results
ESD: Human body model testing per JESD 22-A114e	PASS
Latch-up testing per JESD78A	PASS
MSL per JEDEC J-STD-020d	PASS
HAST per JESD22-A118	PASS
TC per JESD22-A104c (conditions B&K1000 cycles)	PASS
HTS per JESD22-A103c	PASS

- There is one small concern: the solder mask is open exposing the copper metallization between the solder balls. The exposed copper has not created any failures during the qualification tests but:
    - This could create issues when the devices are soldered to their boards if solder paste gets trapped there;
    - Over time, in a dry environment, conductive dust particles could accumulate there and create leakage between various signals.
- Another area of concern for long term reliability is the intermetallic formation at the bond pads. Overtime these could increase the contact resistance of the bond wires. The problem can be reduced by keeping the part as cold as possible during operation.
- Because of these two concerns, it will be important to prepare test pieces of assembled devices for further tests.
- A screening test for devices should activate this bond pad concern without stressing the devices. **It is suggested to submit the parts to 125ºC for 168 hours before final test.** This is a very standard burn-in condition for Si devices in BGA packages.

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