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Latch-up Characterization Report for **NRC** **EVLA**

Job No : 80013
Customer : Brent Carlson
Company : NRC
Author : Joanne Woodward Jack
Date : July 31, 2008
Request : Characterize the latch-up sensitivity
of the EVLA in 672 BGA.

1. Purpose

The purpose of the assessment is to characterize latch-up sensitivity of EVLA in 672 BGA.

2. Results summary

One device was stressed at 125 deg. C, 5 at 100 deg. C, with no indications of latch-up.

3. Test method

3.1. Equipment

UTI Multi-Trace tester

3.2. Test method

The test was performed on the Ultra-Test International Multi-Trace tester according to JESD78A for each device in the following procedures:

The device under test was biased with power to the supply pins and 0 V to ground pins (more details below in the appendix). Inputs are tied to a certain state, either high or low. The rise time on the pulse is approximately 50 microseconds. The pulse width remained constant at 10 ms. Cool down after the pulse was 100 ms. Delay before the post-pulse IDD measurement was 10 ms. The vector (program in appendix) was sent for each pulse.

See Appendix for set-up

3.2.2. Overcurrent Test

During the overcurrent test, current pulses were applied to the pin tested to induce latch-up.

1. Constant steps of 25 milliamperes were applied to the pin under test (refer to table 3.2.2.). The supply currents (1.2V supply and 2.5V supply) of the device under test were measured 10 milliseconds after the end of the current pulse. Latch-up will be detected by a graphical output from the Multi-Trace and criterion for failure is an overcurrent of 10 mA or 1.4 times the supply current, whichever is greater. With inputs low, the current on +1.2V supply is approximately 1 mA, on the +2.5 V supply it is approximately 4 mA. With inputs high, the current on +1.2V supply is approximately 17 mA, on the +2.5V supply it is approximately 12 mA.

2. The current stimulation was repeated with negative current pulses.

3. To protect the device under test, the compliance voltage of the constant current pulses were limited to $-1.375/+4.1$ volts. The maximum constant trigger current was limited to ± 100 milliamperes. The supply currents were limited to 300 mA.

4. For device 8 the cooldown time between pulses was 100 ms. After the test of device 8 at 125 deg. C, the socket lost its travel and therefore connectivity. The socket manufacturer suggested a longer cooldown time, so this was increased to 300 ms between pulses. Also, the test temperature was reduced to 100 deg. C.

3.2.3. Supply Overvoltage test

The supplies of the device under test were increased in approximate steps of 0.1 volts. The supply currents were measured 10 milliseconds after the supply voltage was returned to the maximum operating voltage. The maximum supply stress for are presented in table 3.2.3. During the test, the device under test was set as indicated in table 3.2.1. The cooldown time was increased to 1 second between pulses to prevent socket damage as this was the highest current the device would see.

4. Test Samples Identification

Reference	80013
Brand	CA2048CL-F672C256-A WIDAR Correlator iSine, Inc. N63944.12 0810 USA Devices 1-6
Package type	672BGA



5. Results

5.1. Summary by Device

Table 5.1.1. Over/undercurrent test results.

Note: only 1 device was tested at 125 deg. C, as there was a problem with the socket. The socket was replaced, and the test temperature reduced and cooldown times increased for devices 7, 9-12

Max. Current pulse (mA)	Step (mA)	Dev. No.	Temp.	Input state	Pins Latching up	Current pulse where LU occurred (mA)	Voltage during pulse before LU (V)	1.2 V supply current (mA)	2.75 V supply current (mA)
100	25	8	125	Low	-	-	-	35	3
-100	-25	8	125	Low	-	-	-	34	4
100	25	8	125	High	-	-	-	44	12
-100	-25	8	125	High	-	-	-	44	12
100	25	7	100	Low	-	-	-	16	4
-100	-25	7	100	Low	-	-	-	16	4
100	25	7	100	High	-	-	-	26	9
-100	-25	7	100	High	-	-	-	26	9
100	25	9	100	Low	-	-	-	19	4
-100	-25	9	100	Low	-	-	-	19	6
100	25	9	100	High	-	-	-	29	16
-100	-25	9	100	High	-	-	-	29	16
100	25	10	100	Low	-	-	-	16	4
-100	-25	10	100	Low	-	-	-	16	5
100	25	10	100	High	-	-	-	25	12
-100	-25	10	100	High	-	-	-	26	12
100	25	11	100	Low	-	-	-	16	4
-100	-25	11	100	Low	-	-	-	16	4
100	25	11	100	High	-	-	-	27	11
-100	-25	11	100	High	-	-	-	27	11
100	25	12	100	Low	-	-	-	18	4
-100	-25	12	100	Low	-	-	-	18	5
100	25	12	100	High	-	-	-	29	17
-100	-25	12	100	High	-	-	-	29	17

-Notes

1. Dev 7 undercurrent ip low pin 534 Y_DUMP_EN_I_pad[6] showed high current before and after pulse – the test was repeated and the current looked normal.
2. Dev 7 Overcurrent ip high pin 102 HIZ_pad showed variable current, probably due to the fact that it was no longer held low during its trigger. Pin 208 MCB_CS_pad_ also showed variable current, pin 314 X_CLOCK_O_pad shows variable current when being triggered
3. Dev 10 undercurrent ip low showed some high current on several pins. Test was repeated and most pins showed lower current. This is possibly a device state issue and not latch-up as the same current level is seen before and after latch-up pulse.
4. Dev 11 pin 236 Y_CLOCK_O_pad shows variable current during trigger in overcurrent ip high.

Table 5.1.2. Supply overvoltage test results.

Supply Tested	Max. Voltage (V)	Step (mV) Approx.	Temp.	Dev. No.	Input State	Voltage pulse where LU occurred (V)	1.2 V supply current (mA)	3.3 V supply current (mA)
+1.2 V 1.2 VDD DVDD_PLL	1.98	100	125	8	low	-	34	3
	1.98	100	125	8	high	-	43	13
	1.98	220	100	7	low	-	15	3
	1.98	220	100	7	high	-	25	9
	1.98	220	100	9	low	-	19	4
	1.98	220	100	9	high	-	29	15
	1.98	220	100	10	low	-	16	4
	1.98	220	100	10	high	-	27	15
	1.98	220	100	11	low	-	16	4
	1.98	220	100	11	high	-	26	11
	1.98	220	100	12	low	-	18	4
	1.98	220	100	12	high	-	28	12

Note: the 3.3 V supply current shows a slight increase in the last 2 steps with inputs high, but is not high enough to fail latch-up criteria and the device is not damaged.

Supply Tested	Max. Voltage (V)	Step (mV) Approx.	Temp.	Dev. No.	Input State	Voltage pulse where LU occurred (V)	1.2 V supply current (mA)	3.3 V supply current (mA)
2.5 V supply AHVDD_PLL AHVDD_PLL_AHVDD G_PLL	4.1	100	125	8	low	-	33	3
	4.1	100	125	8	high	-	43	11 to 17 (gradual increase)
	4.1	350	100	7	low	-	15	3
	4.1	350	100	7	high	-	25	8
	4.1	350	100	9	low	-	18	3
	4.1	350	100	9	high	-	28	13
	4.1	350	100	10	low	-	16	3
	4.1	350	100	10	high	-	26	15 (slight increase at last step)
	4.1	350	100	11	low	-	16	3
	4.1	350	100	11	high	-	26	11
	4.1	350	100	12	low	-	18	4
	4.1	350	100	12	high	-	29	13

Notes:

Table 5.1.3. Stand alone tester results

Device	Point of test	Results
7	Pre latch-up and post latch-up test	Pass
8	Pre latch-up and post latch-up test	Pass
9	Pre latch-up and post latch-up test	Pass
10	Pre latch-up and post latch-up test	Pass
11	Pre latch-up and post latch-up test	Pass
12	Pre latch-up and post latch-up test	pass

6. Conclusion

Under the conditions stated in this report, no latch-up was observed on the EVLA at room temperature or at 125 deg. C up to +/- 100 mA. With inputs low, the currents were stable; however with the inputs high condition, some pins show some variability in the currents, but does not indicate latch-up.

7. Appendix

No more than 50 mA of the trigger current could be injected or removed, given the voltage clamps. See individual raw data for current injected for each pin.

Device set-up

NC		means not connected in the socket					
UTi pin	SIGNAL	BALL	BALL	ip high voltage	ip low voltage	ip high drive	ip low drive
62	DVDD_PLL	G	13	1.32	1.32	4	4
413	DVDD_PLL	Y	14	1.32	1.32	4	4
139	1.2V VDD	K	15	1.32	1.32	4	4
141	1.2V VDD	K	17	1.32	1.32	4	4
212	1.2V VDD	K	11	1.32	1.32	4	4
213	1.2V VDD	K	13	1.32	1.32	4	4
229	1.2V VDD	K	8	1.32	1.32	4	4
257	1.2V VDD	L	8	1.32	1.32	4	4
283	1.2V VDD	N	8	1.32	1.32	4	4
286	1.2V VDD	K	9	1.32	1.32	4	4
293	1.2V VDD	L	18	1.32	1.32	4	4
294	1.2V VDD	N	18	1.32	1.32	4	4
328	1.2V VDD	R	8	1.32	1.32	4	4
342	1.2V VDD	R	18	1.32	1.32	4	4
388	1.2V VDD	U	14	1.32	1.32	4	4
394	1.2V VDD	U	18	1.32	1.32	4	4
406	1.2V VDD	U	10	1.32	1.32	4	4
408	1.2V VDD	U	8	1.32	1.32	4	4
416	1.2V VDD	U	16	1.32	1.32	4	4
437	1.2V VDD	U	12	1.32	1.32	4	4
563	1.2V VDD	U	13	1.32	1.32	4	4
NC	1.2V VDD	K	10	1.32	1.32	4	4
NC	1.2V VDD	K	12	1.32	1.32	4	4
NC	1.2V VDD	K	14	1.32	1.32	4	4
NC	1.2V VDD	K	16	1.32	1.32	4	4
NC	1.2V VDD	K	18	1.32	1.32	4	4
NC	1.2V VDD	M	8	1.32	1.32	4	4
NC	1.2V VDD	M	18	1.32	1.32	4	4
NC	1.2V VDD	P	8	1.32	1.32	4	4
NC	1.2V VDD	P	18	1.32	1.32	4	4
NC	1.2V VDD	T	8	1.32	1.32	4	4
NC	1.2V VDD	T	18	1.32	1.32	4	4

NC	1.2V VDD	U	9	1.32	1.32	4	4
NC	1.2V VDD	U	11	1.32	1.32	4	4
NC	1.2V VDD	U	15	1.32	1.32	4	4
NC	1.2V VDD	U	17	1.32	1.32	4	4
63	2.5 V VCC	H	14	2.75	2.75	2	2
105	2.5 V VCC	H	8	2.75	2.75	2	2
112	2.5 V VCC	H	12	2.75	2.75	2	2
166	2.5 V VCC	H	16	2.75	2.75	2	2
167	2.5 V VCC	H	17	2.75	2.75	2	2
184	2.5 V VCC	H	9	2.75	2.75	2	2
192	2.5 V VCC	H	18	2.75	2.75	2	2
202	2.5 V VCC	K	6	2.75	2.75	2	2
211	2.5 V VCC	H	10	2.75	2.75	2	2
221	2.5 V VCC	J	19	2.75	2.75	2	2
245	2.5 V VCC	K	20	2.75	2.75	2	2
253	2.5 V VCC	M	6	2.75	2.75	2	2
256	2.5 V VCC	L	6	2.75	2.75	2	2
259	2.5 V VCC	J	7	2.75	2.75	2	2
261	2.5 V VCC	H	11	2.75	2.75	2	2
264	2.5 V VCC	H	15	2.75	2.75	2	2
291	2.5 V VCC	M	20	2.75	2.75	2	2
292	2.5 V VCC	L	20	2.75	2.75	2	2
298	2.5 V VCC	N	20	2.75	2.75	2	2
346	2.5 V VCC	R	20	2.75	2.75	2	2
350	2.5 V VCC	P	20	2.75	2.75	2	2
362	2.5 V VCC	W	12	2.75	2.75	2	2
373	2.5 V VCC	T	20	2.75	2.75	2	2
395	2.5 V VCC	U	20	2.75	2.75	2	2
396	2.5 V VCC	W	19	2.75	2.75	2	2
414	2.5 V VCC	W	15	2.75	2.75	2	2
424	2.5 V VCC	V	20	2.75	2.75	2	2
431	2.5 V VCC	V	8	2.75	2.75	2	2
436	2.5 V VCC	W	11	2.75	2.75	2	2
442	2.5 V VCC	W	17	2.75	2.75	2	2
443	2.5 V VCC	W	18	2.75	2.75	2	2
542	2.5 V VCC	W	16	2.75	2.75	2	2
162	AHVDD_PLL	H	13	2.75	2.75	2	2
513	AHVDD_PLL_AHVDDG_PLL	V	14	2.75	2.75	2	2
137	AHVSS_PLL	J	13	0	0	3	3
613	AHVSS_PLL_AHVSSG_PLL	W	14	0	0	3	3
163	DVSS_PLL	J	14	0	0	3	3
338	DVSS_PLL	V	13	0	0	3	3
114	VSS	M	15	0	0	3	3
214	VSS	N	14	0	0	3	3
239	VSS	L	16	0	0	3	3
262	VSS	L	12	0	0	3	3
263	VSS	L	14	0	0	3	3
280	VSS	N	10	0	0	3	3
281	VSS	M	9	0	0	3	3
285	VSS	L	10	0	0	3	3
287	VSS	M	13	0	0	3	3

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289	VSS	N	16	0	0	3	3
290	VSS	M	17	0	0	3	3
307	VSS	N	12	0	0	3	3
312	VSS	M	11	0	0	3	3
316	VSS	R	16	0	0	3	3
334	VSS	T	9	0	0	3	3
335	VSS	R	10	0	0	3	3
336	VSS	P	11	0	0	3	3
337	VSS	P	9	0	0	3	3
341	VSS	T	17	0	0	3	3
343	VSS	P	17	0	0	3	3
354	VSS	T	11	0	0	3	3
363	VSS	P	13	0	0	3	3
365	VSS	P	15	0	0	3	3
439	VSS	T	15	0	0	3	3
463	VSS	R	12	0	0	3	3
488	VSS	R	14	0	0	3	3
588	VSS	T	13	0	0	3	3
NC	VSS	L	9				
NC	VSS	L	11				
NC	VSS	L	13				
NC	VSS	L	15				
NC	VSS	L	17				
NC	VSS	M	10				
NC	VSS	M	12				
NC	VSS	M	14				
NC	VSS	M	16				
NC	VSS	N	9				
NC	VSS	N	11				
NC	VSS	N	13				
NC	VSS	N	15				
NC	VSS	N	17				
NC	VSS	P	10				
NC	VSS	P	12				
NC	VSS	P	14				
NC	VSS	P	16				
NC	VSS	R	9				
NC	VSS	R	11				
NC	VSS	R	13				
NC	VSS	R	15				
NC	VSS	R	17				
NC	VSS	T	10				
NC	VSS	T	12				
NC	VSS	T	14				
NC	VSS	T	16				
18	VSSPST	J	17	0	0	3	3
22	VSSPST	A	25	0	0	3	3
27	VSSPST	A	2	0	0	3	3
41	VSSPST	G	16	0	0	3	3
48	VSSPST	B	26	0	0	3	3
51	VSSPST	B	1	0	0	3	3

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64	VSSPST	J	15	0	0	3	3
104	VSSPST	G	5	0	0	3	3
106	VSSPST	D	5	0	0	3	3
128	VSSPST	F	5	0	0	3	3
131	VSSPST	J	10	0	0	3	3
152	VSSPST	J	8	0	0	3	3
156	VSSPST	E	5	0	0	3	3
187	VSSPST	J	11	0	0	3	3
190	VSSPST	J	16	0	0	3	3
217	VSSPST	J	18	0	0	3	3
226	VSSPST	M	7	0	0	3	3
237	VSSPST	J	12	0	0	3	3
255	VSSPST	J	9	0	0	3	3
258	VSSPST	K	7	0	0	3	3
267	VSSPST	K	19	0	0	3	3
295	VSSPST	M	19	0	0	3	3
347	VSSPST	P	19	0	0	3	3
369	VSSPST	T	19	0	0	3	3
387	VSSPST	V	11	0	0	3	3
393	VSSPST	V	18	0	0	3	3
397	VSSPST	V	19	0	0	3	3
412	VSSPST	V	12	0	0	3	3
433	VSSPST	V	9	0	0	3	3
467	VSSPST	V	17	0	0	3	3
477	VSSPST	AE	1	0	0	3	3
491	VSSPST	V	16	0	0	3	3
515	VSSPST	V	15	0	0	3	3
538	VSSPST	Y	13	0	0	3	3
550	VSSPST	AF	25	0	0	3	3
575	VSSPST	AE	26	0	0	3	3
579	VSSPST	AE	2	0	0	3	3
601	VSSPST	AA	7	0	0	3	3
602	VSSPST	AF	2	0	0	3	3
603	VSSPST	AC	5	0	0	3	3
NC	VSSPST	L	7				
NC	VSSPST	L	19				
NC	VSSPST	N	19				
NC	VSSPST	R	19				
NC	VSSPST	U	19				
1	NOCONNECT	B	2				
3	NOCONNECT	B	5				
4	NOCONNECT	E	6				
9	NOCONNECT	A	4				
10	NOCONNECT	B	4				
23	NOCONNECT	A	23				
29	NOCONNECT	C	4				
30	NOCONNECT	F	7				
35	NOCONNECT	C	2				
50	NOCONNECT	C	24				
53	NOCONNECT	D	3				
54	NOCONNECT	G	8				

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60	NOCONNECT	C	5				
76	NOCONNECT	D	2				
78	NOCONNECT	C	1				
85	NOCONNECT	D	4				
103	NOCONNECT	G	7				
123	NOCONNECT	D	26				
130	NOCONNECT	D	1				
149	NOCONNECT	B	25				
179	NOCONNECT	J	6				
376	NOCONNECT	AD	3				
426	NOCONNECT	AB	5				
451	NOCONNECT	AC	1				
476	NOCONNECT	AB	1				
478	NOCONNECT	AE	3				
486	NOCONNECT	AC	11				
496	NOCONNECT	AD	26				
503	NOCONNECT	AC	2				
506	NOCONNECT	AF	3				
520	NOCONNECT	AE	20				
521	NOCONNECT	AD	21				
523	NOCONNECT	AC	25				
524	NOCONNECT	AC	26				
530	NOCONNECT	AE	5				
541	NOCONNECT	AF	21				
547	NOCONNECT	AB	20				
548	NOCONNECT	AC	24				
549	NOCONNECT	AD	25				
552	NOCONNECT	AC	3				
553	NOCONNECT	AD	2				
554	NOCONNECT	AD	5				
555	NOCONNECT	AE	4				
557	NOCONNECT	AF	5				
566	NOCONNECT	AF	22				
571	NOCONNECT	AC	21				
572	NOCONNECT	AC	20				
576	NOCONNECT	AC	4				
577	NOCONNECT	AD	4				
578	NOCONNECT	AD	1				
581	NOCONNECT	AF	4				
590	NOCONNECT	AD	20				
591	NOCONNECT	AC	23				
595	NOCONNECT	AF	24				
596	NOCONNECT	AE	22				
597	NOCONNECT	AC	22				
600	NOCONNECT	AE	25				
604	NOCONNECT	AB	6				
615	NOCONNECT	AF	20				
616	NOCONNECT	AB	21				
619	NOCONNECT	AD	22				
620	NOCONNECT	AF	23				
621	NOCONNECT	AE	21				

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622	NOCONNECT	AE	23				
624	NOCONNECT	W	20				

BGA	PGA	UTI pin	SIGNAL	BALL	BALL	PAD CELL		ip high voltage	ip low voltage	ip high drive	ip low drive
C03	A02	2	TESTMODE_1_pad	C	3	PDIDGZ	I	0	0	5	5
B03	B03	28	TESTMODE_0_pad	B	3	PDIDGZ	I	0	0	5	5
A20	B20	45	TESTMODE_pad	A	20	PDIDGZ	I	0	0	5	5
D22	C24	74	SCAN_EN_pad	D	22	PDIDGZ	I	0	0	5	5
E22	D22	97	SCAN_CLK_pad	E	22	PDIDGZ	I	0	0	5	5
G06	E02	102	HIZ_pad	G	6	PDIDGZ	I	0	0	5	5
AD24	AE17	617	TMS_pad	AD	24	PDUWDGZ	I	2.75	2.75	6	6
AD23	AE18	618	TCK_pad	AD	23	PDIDGZ	I	vector low to high 8 times	vector low to high 8 times	5 to 6	5 to 6
E02	B01	26	MCB_ADDR_pad[1]	E	2	PDIDGZ	I	2.75	0	6	5
E04	B06	31	MCB_ADDR_pad[3]	E	4	PDIDGZ	I	2.75	0	6	5
E21	B24	49	LCI_DATA_OE_pad	E	21	PDIDGZ	I	2.75	0	6	5
F03	C06	56	MCB_DATA_pad[2]	F	3	PDB16DGZ	B	2.75	0	6	5
D20	C20	70	LCI_DATA_CS_pad	D	20	PDIDGZ	I	2.75	0	6	5
E03	D02	77	MCB_ADDR_pad[2]	E	3	PDIDGZ	I	2.75	0	6	5
B20	D21	96	PLL_RESET_pad	B	20	PDIDGZ	I	2.75	0	6	5
H04	E01	101	X_DUMP_EN_I_pad[0]	H	4	PDIDGZ	I	2.75	0	6	5
G03	F01	126	MCB_DATA_pad[6]	G	3	PDB16DGZ	B	2.75	0	6	5
G04	F02	127	MCB_DATA_pad[7]	G	4	PDB16DGZ	B	2.75	0	6	5
G01	F04	129	MCB_DATA_pad[4]	G	1	PDB16DGZ	B	2.75	0	6	5
C20	F18	143	RESET_pad	C	20	PDIDGZ	I	2.75	0	6	5
H07	G01	151	X_PHASE2_I_pad[3]	H	7	PDIDGZ	I	2.75	0	6	5
H06	G03	153	X_SDATA3_I_pad[2]	H	6	PDIDGZ	I	2.75	0	6	5
G02	G04	154	MCB_DATA_pad[5]	G	2	PDB16DGZ	B	2.75	0	6	5
F02	G05	155	MCB_DATA_pad[1]	F	2	PDB16DGZ	B	2.75	0	6	5
K05	H01	176	X_SE_CLK_I_pad[1]	K	5	PDIDGZ	I	2.75	0	6	5
J03	H02	177	X_SE_CLK_I_pad[5]	J	3	PDIDGZ	I	2.75	0	6	5
H05	H03	178	X_DUMP_EN_I_pad[7]	H	5	PDIDGZ	I	2.75	0	6	5
F01	H05	180	MCB_DATA_pad[0]	F	1	PDB16DGZ	B	2.75	0	6	5
E01	H06	181	MCB_ADDR_pad[0]	E	1	PDIDGZ	I	2.75	0	6	5
F04	H07	182	MCB_DATA_pad[3]	F	4	PDB16DGZ	B	2.75	0	6	5
L03	J01	201	X_PHASE1_I_pad[1]	L	3	PDIDGZ	I	2.75	0	6	5
K01	J03	203	X_SDATA4_I_pad[3]	K	1	PDIDGZ	I	2.75	0	6	5
J04	J04	204	X_SE_CLK_I_pad[2]	J	4	PDIDGZ	I	2.75	0	6	5
J01	J05	205	X_SCHID_FRAME_I_pad	J	1	PDIDGZ	I	2.75	0	6	5
H01	J06	206	MCB_RD_WR_pad	H	1	PDIDGZ	I	2.75	0	6	5
J02	J07	207	X_SDATA0_I_pad[3]	J	2	PDIDGZ	I	2.75	0	6	5

H02	J08	208	MCB_CS_pad	H	2	PDIDGZ	I	2.75	0	6	5
L02	K02	227	X_SDATA1_I_pad[1]	L	2	PDIDGZ	I	2.75	0	6	5
L04	K03	228	X_TIMESTAMP_I_pad	L	4	PDIDGZ	I	2.75	0	6	5
K02	K05	230	X_SDATA3_I_pad[1]	K	2	PDIDGZ	I	2.75	0	6	5
K03	K06	231	X_PHASE4_I_pad[1]	K	3	PDIDGZ	I	2.75	0	6	5
J05	K07	232	X_SDATA6_I_pad[0]	J	5	PDIDGZ	I	2.75	0	6	5
K04	K08	233	X_SDATA3_I_pad[3]	K	4	PDIDGZ	I	2.75	0	6	5
H03	K09	234	MCB_CLK_pad	H	3	PDIDGZ	I	2.75	0	6	5
C25	K25	250	LCI_FRAME_ABORT_pad	C	25	PDIDGZ	I	2.75	0	6	5
M03	L01	251	X_DVALID_I_pad[3]	M	3	PDIDGZ	I	2.75	0	6	5
M05	L02	252	X_SDATA6_I_pad[3]	M	5	PDIDGZ	I	2.75	0	6	5
L01	L04	254	X_DVALID_I_pad[2]	L	1	PDIDGZ	I	2.75	0	6	5
L05	L10	260	X_SE_CLK_I_pad[6]	L	5	PDIDGZ	I	2.75	0	6	5
N05	M01	276	X_SDATA7_I_pad[3]	N	5	PDIDGZ	I	2.75	0	6	5
M01	M02	277	X_PHASE0_I_pad[2]	M	1	PDIDGZ	I	2.75	0	6	5
M02	M03	278	X_DUMP_EN_I_pad[3]	M	2	PDIDGZ	I	2.75	0	6	5
N06	M04	279	X_SE_CLK_I_pad[4]	N	6	PDIDGZ	I	2.75	0	6	5
M04	M07	282	X_PHASE4_I_pad[3]	M	4	PDIDGZ	I	2.75	0	6	5
N07	M09	284	X_DUMP_EN_I_pad[6]	N	7	PDIDGZ	I	2.75	0	6	5
G14	M13	288	X_CLOCK_I_pad	G	14	PDIDGZ	I	2.75	0	6	5
P04	N01	301	X_SDATA2_I_pad[1]	P	4	PDIDGZ	I	2.75	0	6	5
P01	N02	302	X_PHASE1_I_pad[3]	P	1	PDIDGZ	I	2.75	0	6	5
N01	N03	303	X_SDATA5_I_pad[2]	N	1	PDIDGZ	I	2.75	0	6	5
N02	N04	304	X_SDATA0_I_pad[0]	N	2	PDIDGZ	I	2.75	0	6	5
P05	N05	305	X_PHASE2_I_pad[1]	P	5	PDIDGZ	I	2.75	0	6	5
P02	N06	306	X_PHASE6_I_pad[0]	P	2	PDIDGZ	I	2.75	0	6	5
N03	N08	308	X_SDATA7_I_pad[0]	N	3	PDIDGZ	I	2.75	0	6	5
P06	N09	309	X_SE_CLK_I_pad[0]	P	6	PDIDGZ	I	2.75	0	6	5
P03	N10	310	X_SDATA4_I_pad[2]	P	3	PDIDGZ	I	2.75	0	6	5
N04	N11	311	X_DVALID_I_pad[4]	N	4	PDIDGZ	I	2.75	0	6	5
R02	P01	326	X_DUMP_EN_I_pad[4]	R	2	PDIDGZ	I	2.75	0	6	5
R05	P02	327	X_PHASE7_I_pad[2]	R	5	PDIDGZ	I	2.75	0	6	5
P07	P04	329	X_SDATA7_I_pad[1]	P	7	PDIDGZ	I	2.75	0	6	5
R03	P05	330	X_SE_CLK_I_pad[7]	R	3	PDIDGZ	I	2.75	0	6	5
R07	P06	331	X_PHASE7_I_pad[3]	R	7	PDIDGZ	I	2.75	0	6	5
R06	P07	332	X_SDATA2_I_pad[0]	R	6	PDIDGZ	I	2.75	0	6	5
T06	P08	333	X_SDATA0_I_pad[2]	T	6	PDIDGZ	I	2.75	0	6	5
AC14	P14	339	Y_PHASE7_I_pad[0]	AC	14	PDIDGZ	I	2.75	0	6	5
Y02	R01	351	X_SDATA1_I_pad[2]	Y	2	PDIDGZ	I	2.75	0	6	5

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Y05	R02	352	X_PHASE5_I_pad[1]	Y	5	PDIDGZ	I	2.75	0	6	5
U01	R03	353	X_SDATA1_I_pad[0]	U	1	PDIDGZ	I	2.75	0	6	5
T02	R05	355	X_SE_CLK_I_pad[3]	T	2	PDIDGZ	I	2.75	0	6	5
T03	R06	356	X_SDATA5_I_pad[3]	T	3	PDIDGZ	I	2.75	0	6	5
T07	R07	357	X_SDATA2_I_pad[2]	T	7	PDIDGZ	I	2.75	0	6	5
R01	R08	358	X_DVALID_I_pad[7]	R	1	PDIDGZ	I	2.75	0	6	5
U02	R09	359	X_DVALID_I_pad[0]	U	2	PDIDGZ	I	2.75	0	6	5
T05	R10	360	X_DUMP_EN_I_pad[5]	T	5	PDIDGZ	I	2.75	0	6	5
R04	R11	361	X_DUMP_EN_I_pad[2]	R	4	PDIDGZ	I	2.75	0	6	5
AE15	R14	364	Y_SDATA3_I_pad[0]	AE	15	PDIDGZ	I	2.75	0	6	5
W09	T02	377	Y_SE_CLK_I_pad[4]	W	9	PDIDGZ	I	2.75	0	6	5
AA03	T03	378	X_PHASE5_I_pad[0]	AA	3	PDIDGZ	I	2.75	0	6	5
Y01	T04	379	X_PHASE7_I_pad[1]	Y	1	PDIDGZ	I	2.75	0	6	5
U03	T05	380	X_SDATA3_I_pad[0]	U	3	PDIDGZ	I	2.75	0	6	5
U04	T06	381	X_PHASE4_I_pad[2]	U	4	PDIDGZ	I	2.75	0	6	5
T01	T07	382	X_PHASE7_I_pad[0]	T	1	PDIDGZ	I	2.75	0	6	5
T04	T08	383	X_SDATA6_I_pad[1]	T	4	PDIDGZ	I	2.75	0	6	5
U05	T09	384	X_PHASE6_I_pad[1]	U	5	PDIDGZ	I	2.75	0	6	5
V03	T10	385	X_PHASE3_I_pad[3]	V	3	PDIDGZ	I	2.75	0	6	5
Y10	T11	386	Y_DVALID_I_pad[4]	Y	10	PDIDGZ	I	2.75	0	6	5
AB15	T14	389	Y_SDATA5_I_pad[1]	AB	15	PDIDGZ	I	2.75	0	6	5
AC16	T15	390	Y_PHASE2_I_pad[0]	AC	16	PDIDGZ	I	2.75	0	6	5
AC17	T16	391	Y_DVALID_I_pad[6]	AC	17	PDIDGZ	I	2.75	0	6	5
Y08	U01	401	X_PHASE3_I_pad[0]	Y	8	PDIDGZ	I	2.75	0	6	5
V04	U02	402	X_DUMP_SYNC_I_pad	V	4	PDIDGZ	I	2.75	0	6	5
V01	U03	403	X_PHASE2_I_pad[2]	V	1	PDIDGZ	I	2.75	0	6	5
U06	U04	404	X_SDATA2_I_pad[3]	U	6	PDIDGZ	I	2.75	0	6	5
V02	U05	405	X_PHASE6_I_pad[3]	V	2	PDIDGZ	I	2.75	0	6	5
U07	U07	407	X_DVALID_I_pad[1]	U	7	PDIDGZ	I	2.75	0	6	5
V06	U09	409	X_DUMP_EN_I_pad[1]	V	6	PDIDGZ	I	2.75	0	6	5
AC09	U10	410	Y_SDATA1_I_pad[1]	AC	9	PDIDGZ	I	2.75	0	6	5
Y11	U11	411	Y_SDATA2_I_pad[0]	Y	11	PDIDGZ	I	2.75	0	6	5
Y16	U15	415	Y_PHASE3_I_pad[3]	Y	16	PDIDGZ	I	2.75	0	6	5
AD17	U17	417	Y_PHASE5_I_pad[3]	AD	17	PDIDGZ	I	2.75	0	6	5
W01	V02	427	X_PHASE0_I_pad[1]	W	1	PDIDGZ	I	2.75	0	6	5
V07	V03	428	X_SDATA5_I_pad[1]	V	7	PDIDGZ	I	2.75	0	6	5
W05	V04	429	X_SDATA6_I_pad[2]	W	5	PDIDGZ	I	2.75	0	6	5
W02	V05	430	X_DVALID_I_pad[5]	W	2	PDIDGZ	I	2.75	0	6	5
V05	V07	432	X_PHASE6_I_pad[2]	V	5	PDIDGZ	I	2.75	0	6	5

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AA09	V09	434	Y_SDATA4_I_pad[3]	AA	9	PDIDGZ	I	2.75	0	6	5
AD10	V10	435	Y_PHASE1_I_pad[3]	AD	10	PDIDGZ	I	2.75	0	6	5
W13	V13	438	Y_CLOCK_I_pad	W	13	PDIDGZ	I	2.75	0	6	5
AC15	V15	440	Y_PHASE6_I_pad[2]	AC	15	PDIDGZ	I	2.75	0	6	5
AD16	V16	441	Y_DUMP_EN_I_pad[1]	AD	16	PDIDGZ	I	2.75	0	6	5
W07	W02	452	X_PHASE5_I_pad[2]	W	7	PDIDGZ	I	2.75	0	6	5
W04	W03	453	X_DVALID_I_pad[6]	W	4	PDIDGZ	I	2.75	0	6	5
W08	W04	454	X_PHASE3_I_pad[2]	W	8	PDIDGZ	I	2.75	0	6	5
W03	W05	455	X_PHASE5_I_pad[3]	W	3	PDIDGZ	I	2.75	0	6	5
W06	W06	456	X_PHASE2_I_pad[0]	W	6	PDIDGZ	I	2.75	0	6	5
V10	W07	457	Y_SE_CLK_I_pad[0]	V	10	PDIDGZ	I	2.75	0	6	5
AA08	W08	458	Y_SDATA3_I_pad[3]	AA	8	PDIDGZ	I	2.75	0	6	5
Y09	W09	459	Y_SDATA6_I_pad[3]	Y	9	PDIDGZ	I	2.75	0	6	5
AB10	W10	460	Y_DUMP_EN_I_pad[3]	AB	10	PDIDGZ	I	2.75	0	6	5
AB12	W11	461	Y_DUMP_EN_I_pad[4]	AB	12	PDIDGZ	I	2.75	0	6	5
Y12	W12	462	Y_DUMP_EN_I_pad[2]	Y	12	PDIDGZ	I	2.75	0	6	5
AA14	W14	464	Y_PHASE3_I_pad[2]	AA	14	PDIDGZ	I	2.75	0	6	5
Y15	W15	465	Y_PHASE6_I_pad[3]	Y	15	PDIDGZ	I	2.75	0	6	5
AA16	W16	466	Y_PHASE0_I_pad[3]	AA	16	PDIDGZ	I	2.75	0	6	5
AE17	W18	468	Y_DVALID_I_pad[5]	AE	17	PDIDGZ	I	2.75	0	6	5
AA19	W19	469	Y_SDATA4_I_pad[0]	AA	19	PDIDGZ	I	2.75	0	6	5
Y06	Y04	479	X_PHASE3_I_pad[1]	Y	6	PDIDGZ	I	2.75	0	6	5
Y03	Y05	480	X_PHASE1_I_pad[2]	Y	3	PDIDGZ	I	2.75	0	6	5
Y04	Y06	481	X_SDATA7_I_pad[2]	Y	4	PDIDGZ	I	2.75	0	6	5
AD06	Y07	482	Y_SDATA0_I_pad[3]	AD	6	PDIDGZ	I	2.75	0	6	5
AD07	Y08	483	Y_DUMP_EN_I_pad[7]	AD	7	PDIDGZ	I	2.75	0	6	5
AE08	Y09	484	Y_SDATA3_I_pad[1]	AE	8	PDIDGZ	I	2.75	0	6	5
AA10	Y10	485	Y_DVALID_I_pad[3]	AA	10	PDIDGZ	I	2.75	0	6	5
AE13	Y12	487	Y_SDATA6_I_pad[1]	AE	13	PDIDGZ	I	2.75	0	6	5
AD14	Y14	489	Y_SDATA2_I_pad[2]	AD	14	PDIDGZ	I	2.75	0	6	5
AA15	Y15	490	Y_PHASE5_I_pad[2]	AA	15	PDIDGZ	I	2.75	0	6	5
Y17	Y17	492	Y_PHASE7_I_pad[1]	Y	17	PDIDGZ	I	2.75	0	6	5
Y18	Y18	493	Y_SDATA0_I_pad[1]	Y	18	PDIDGZ	I	2.75	0	6	5
AD19	Y20	495	Y_SDATA5_I_pad[2]	AD	19	PDIDGZ	I	2.75	0	6	5
AA01	AA01	501	X_PHASE0_I_pad[3]	AA	1	PDIDGZ	I	2.75	0	6	5
AA04	AA02	502	X_SDATA0_I_pad[1]	AA	4	PDIDGZ	I	2.75	0	6	5
Y07	AA04	504	X_PHASE1_I_pad[0]	Y	7	PDIDGZ	I	2.75	0	6	5
AA02	AA05	505	X_SDATA1_I_pad[3]	AA	2	PDIDGZ	I	2.75	0	6	5
AE06	AA07	507	Y_SCHID_FRAME_I_pad	AE	6	PDIDGZ	I	2.75	0	6	5

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AC07	AA08	508	Y_SDATA3_I_pad[2]	AC	7	PDIDGZ	I	2.75	0	6	5
AD09	AA09	509	Y_DVALID_I_pad[2]	AD	9	PDIDGZ	I	2.75	0	6	5
AE10	AA10	510	Y_SDATA7_I_pad[1]	AE	10	PDIDGZ	I	2.75	0	6	5
AA11	AA11	511	Y_PHASE2_I_pad[1]	AA	11	PDIDGZ	I	2.75	0	6	5
AC13	AA12	512	Y_SDATA2_I_pad[3]	AC	13	PDIDGZ	I	2.75	0	6	5
AF15	AA14	514	Y_DVALID_I_pad[0]	AF	15	PDIDGZ	I	2.75	0	6	5
AB16	AA16	516	Y_PHASE5_I_pad[1]	AB	16	PDIDGZ	I	2.75	0	6	5
AB17	AA17	517	Y_PHASE1_I_pad[0]	AB	17	PDIDGZ	I	2.75	0	6	5
AC18	AA18	518	Y_PHASE3_I_pad[1]	AC	18	PDIDGZ	I	2.75	0	6	5
AB18	AA19	519	Y_SDATA1_I_pad[3]	AB	18	PDIDGZ	I	2.75	0	6	5
AB02	AB01	526	X_SDATA5_I_pad[0]	AB	2	PDIDGZ	I	2.75	0	6	5
AA06	AB02	527	X_SDATA4_I_pad[1]	AA	6	PDIDGZ	I	2.75	0	6	5
AA05	AB03	528	X_PHASE0_I_pad[0]	AA	5	PDIDGZ	I	2.75	0	6	5
AB04	AB04	529	X_SDATA4_I_pad[0]	AB	4	PDIDGZ	I	2.75	0	6	5
AB09	AB06	531	Y_PHASE1_I_pad[1]	AB	9	PDIDGZ	I	2.75	0	6	5
AC08	AB07	532	Y_TIMESTAMP_I_pad	AC	8	PDIDGZ	I	2.75	0	6	5
AF06	AB08	533	Y_DUMP_EN_I_pad[0]	AF	6	PDIDGZ	I	2.75	0	6	5
AE09	AB09	534	Y_DUMP_EN_I_pad[6]	AE	9	PDIDGZ	I	2.75	0	6	5
AC10	AB10	535	Y_PHASE0_I_pad[2]	AC	10	PDIDGZ	I	2.75	0	6	5
AE12	AB11	536	Y_SDATA4_I_pad[2]	AE	12	PDIDGZ	I	2.75	0	6	5
AA13	AB12	537	Y_PHASE2_I_pad[2]	AA	13	PDIDGZ	I	2.75	0	6	5
AB14	AB14	539	Y_DVALID_I_pad[1]	AB	14	PDIDGZ	I	2.75	0	6	5
AF16	AB15	540	Y_DUMP_SYNC_I_pad	AF	16	PDIDGZ	I	2.75	0	6	5
AF19	AB18	543	Y_PHASE0_I_pad[0]	AF	19	PDIDGZ	I	2.75	0	6	5
AE19	AB19	544	Y_SDATA4_I_pad[1]	AE	19	PDIDGZ	I	2.75	0	6	5
AC19	AB20	545	Y_SDATA5_I_pad[0]	AC	19	PDIDGZ	I	2.75	0	6	5
AB19	AB21	546	Y_PHASE4_I_pad[0]	AB	19	PDIDGZ	I	2.75	0	6	5
AB03	AC01	551	X_PHASE4_I_pad[0]	AB	3	PDIDGZ	I	2.75	0	6	5
AC06	AC06	556	Y_SE_CLK_I_pad[5]	AC	6	PDIDGZ	I	2.75	0	6	5
W10	AC08	558	Y_SDATA7_I_pad[3]	W	10	PDIDGZ	I	2.75	0	6	5
AF09	AC09	559	Y_SE_CLK_I_pad[1]	AF	9	PDIDGZ	I	2.75	0	6	5
AF11	AC10	560	Y_SDATA0_I_pad[2]	AF	11	PDIDGZ	I	2.75	0	6	5
AC12	AC11	561	Y_DVALID_I_pad[7]	AC	12	PDIDGZ	I	2.75	0	6	5
AF13	AC12	562	Y_SDATA5_I_pad[3]	AF	13	PDIDGZ	I	2.75	0	6	5
AE14	AC14	564	Y_PHASE6_I_pad[1]	AE	14	PDIDGZ	I	2.75	0	6	5
AE16	AC15	565	Y_SDATA6_I_pad[2]	AE	16	PDIDGZ	I	2.75	0	6	5
AA17	AC17	567	Y_PHASE3_I_pad[0]	AA	17	PDIDGZ	I	2.75	0	6	5
AA18	AC18	568	Y_PHASE5_I_pad[0]	AA	18	PDIDGZ	I	2.75	0	6	5
AF18	AC19	569	Y_SDATA1_I_pad[2]	AF	18	PDIDGZ	I	2.75	0	6	5

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AE24	AC24	574	TDI_pad	AE	24	PDUWDGZ	I	2.75	0	6	5
AB07	AD05	580	Y_PHASE2_I_pad[3]	AB	7	PDIDGZ	I	2.75	0	6	5
AE07	AD07	582	Y_SDATA6_I_pad[0]	AE	7	PDIDGZ	I	2.75	0	6	5
AF08	AD08	583	Y_PHASE4_I_pad[3]	AF	8	PDIDGZ	I	2.75	0	6	5
AF10	AD09	584	Y_PHASE7_I_pad[3]	AF	10	PDIDGZ	I	2.75	0	6	5
AB11	AD10	585	Y_SDATA2_I_pad[1]	AB	11	PDIDGZ	I	2.75	0	6	5
AD12	AD11	586	Y_PHASE7_I_pad[2]	AD	12	PDIDGZ	I	2.75	0	6	5
AD13	AD12	587	Y_DUMP_EN_I_pad[5]	AD	13	PDIDGZ	I	2.75	0	6	5
AF14	AD14	589	Y_SDATA1_I_pad[0]	AF	14	PDIDGZ	I	2.75	0	6	5
AF17	AD17	592	Y_PHASE0_I_pad[1]	AF	17	PDIDGZ	I	2.75	0	6	5
AD18	AD18	593	Y_SDATA7_I_pad[2]	AD	18	PDIDGZ	I	2.75	0	6	5
AE18	AD19	594	Y_PHASE1_I_pad[2]	AE	18	PDIDGZ	I	2.75	0	6	5
AD08	AE05	605	Y_PHASE4_I_pad[1]	AD	8	PDIDGZ	I	2.75	0	6	5
AB08	AE06	606	Y_SE_CLK_I_pad[6]	AB	8	PDIDGZ	I	2.75	0	6	5
AF07	AE07	607	Y_SE_CLK_I_pad[2]	AF	7	PDIDGZ	I	2.75	0	6	5
AE11	AE08	608	Y_SDATA0_I_pad[0]	AE	11	PDIDGZ	I	2.75	0	6	5
AD11	AE09	609	Y_SDATA7_I_pad[0]	AD	11	PDIDGZ	I	2.75	0	6	5
AF12	AE10	610	Y_PHASE6_I_pad[0]	AF	12	PDIDGZ	I	2.75	0	6	5
AA12	AE11	611	Y_SE_CLK_I_pad[7]	AA	12	PDIDGZ	I	2.75	0	6	5
AB13	AE12	612	Y_SE_CLK_I_pad[3]	AB	13	PDIDGZ	I	2.75	0	6	5
AD15	AE14	614	Y_PHASE4_I_pad[2]	AD	15	PDIDGZ	I	2.75	0	6	5
E07	A05	5	Y_SE_CLK_O_pad[2]	E	7	PDB12DGZ	O	floating	floating	-	-
A07	A06	6	Y_SDATA3_O_pad[3]	A	7	PDB12DGZ	O	floating	floating	-	-
A06	A07	7	Y_PHASE2_O_pad[3]	A	6	PDB12DGZ	O	floating	floating	-	-
A05	A08	8	Y_SE_CLK_O_pad[5]	A	5	PDB12DGZ	O	floating	floating	-	-
C07	A11	11	Y_DUMP_EN_O_pad[7]	C	7	PDB12DGZ	O	floating	floating	-	-
E12	A12	12	Y_SDATA2_O_pad[1]	E	12	PDB12DGZ	O	floating	floating	-	-
D13	A13	13	Y_SDATA6_O_pad[1]	D	13	PDB12DGZ	O	floating	floating	-	-
B14	A14	14	Y_SDATA1_O_pad[0]	B	14	PDB12DGZ	O	floating	floating	-	-
F15	A15	15	Y_SDATA3_O_pad[0]	F	15	PDB12DGZ	O	floating	floating	-	-
A15	A16	16	Y_PHASE6_O_pad[3]	A	15	PDB12DGZ	O	floating	floating	-	-
B16	A17	17	Y_PHASE3_O_pad[2]	B	16	PDB12DGZ	O	floating	floating	-	-
A18	A19	19	Y_SDATA0_O_pad[1]	A	18	PDB12DGZ	O	floating	floating	-	-
D19	A20	20	Y_SDATA5_O_pad[2]	D	19	PDB12DGZ	O	floating	floating	-	-
F19	A21	21	Y_PHASE0_O_pad[0]	F	19	PDB12DGZ	O	floating	floating	-	-
A24	A24	24	LCI_ACCDATA_pad[10]	A	24	PDB12DGZ	O	floating	floating	-	-
B22	A25	25	LCI_ACCDATA_pad[5]	B	22	PDB12DGZ	O	floating	floating	-	-
B08	B07	32	Y_SE_CLK_O_pad[6]	B	8	PDB12DGZ	O	floating	floating	-	-
A08	B08	33	Y_SE_CLK_O_pad[4]	A	8	PDB12DGZ	O	floating	floating	-	-

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D10	B09	34	Y_DUMP_EN_O_pad[3]	D	10	PDB12DGZ	O	floating	floating	-	-
G09	B11	36	Y_SE_CLK_O_pad[1]	G	9	PDB12DGZ	O	floating	floating	-	-
G12	B12	37	Y_SDATA0_O_pad[2]	G	12	PDB12DGZ	O	floating	floating	-	-
A13	B13	38	Y_PHASE6_O_pad[1]	A	13	PDB12DGZ	O	floating	floating	-	-
A14	B14	39	Y_PHASE3_O_pad[3]	A	14	PDB12DGZ	O	floating	floating	-	-
C15	B15	40	Y_DVALID_O_pad[1]	C	15	PDB12DGZ	O	floating	floating	-	-
F17	B17	42	Y_PHASE5_O_pad[3]	F	17	PDB12DGZ	O	floating	floating	-	-
D17	B18	43	Y_PHASE2_O_pad[0]	D	17	PDB12DGZ	O	floating	floating	-	-
D18	B19	44	Y_PHASE0_O_pad[3]	D	18	PDB12DGZ	O	floating	floating	-	-
E20	B21	46	LCI_DATA_RDY_pad	E	20	PDB12DGZ	O	floating	floating	-	-
C23	B22	47	LCI_ACCDATA_pad[8]	C	23	PDB12DGZ	O	floating	floating	-	-
A03	C02	52	SENSEOUT_pad	A	3	PDB12DGZ	O	floating	floating	-	-
B06	C05	55	Y_SDATA0_O_pad[3]	B	6	PDB12DGZ	O	floating	floating	-	-
D07	C07	57	Y_SDATA6_O_pad[0]	D	7	PDB12DGZ	O	floating	floating	-	-
D09	C08	58	Y_SDATA1_O_pad[1]	D	9	PDB12DGZ	O	floating	floating	-	-
B10	C09	59	Y_DVALID_O_pad[4]	B	10	PDB12DGZ	O	floating	floating	-	-
A11	C11	61	Y_SE_CLK_O_pad[0]	A	11	PDB12DGZ	O	floating	floating	-	-
D15	C15	65	Y_PHASE6_O_pad[2]	D	15	PDB12DGZ	O	floating	floating	-	-
A16	C16	66	Y_SDATA5_O_pad[1]	A	16	PDB12DGZ	O	floating	floating	-	-
A17	C17	67	Y_PHASE7_O_pad[1]	A	17	PDB12DGZ	O	floating	floating	-	-
B18	C18	68	Y_PHASE5_O_pad[0]	B	18	PDB12DGZ	O	floating	floating	-	-
A19	C19	69	Y_SDATA4_O_pad[0]	A	19	PDB12DGZ	O	floating	floating	-	-
A21	C21	71	LCI_ACCDATA_pad[0]	A	21	PDB12DGZ	O	floating	floating	-	-
A22	C22	72	LCI_ACCDATA_pad[4]	A	22	PDB12DGZ	O	floating	floating	-	-
B24	C23	73	LCI_ACCDATA_pad[11]	B	24	PDB12DGZ	O	floating	floating	-	-
D25	C25	75	LCI_ACCDATA_VALID_pad	D	25	PDB12DGZ	O	floating	floating	-	-
F06	D04	79	TDO_pad	F	6	PDB12DGZ	O	floating	floating	-	-
C06	D05	80	Y_SCHID_FRAME_O_pad	C	6	PDB12DGZ	O	floating	floating	-	-
B07	D06	81	Y_SDATA3_O_pad[2]	B	7	PDB12DGZ	O	floating	floating	-	-
B09	D07	82	Y_SDATA4_O_pad[3]	B	9	PDB12DGZ	O	floating	floating	-	-
C09	D08	83	Y_PHASE1_O_pad[1]	C	9	PDB12DGZ	O	floating	floating	-	-
A09	D09	84	Y_SDATA6_O_pad[3]	A	9	PDB12DGZ	O	floating	floating	-	-
E11	D11	86	Y_SDATA0_O_pad[0]	E	11	PDB12DGZ	O	floating	floating	-	-
F13	D12	87	Y_PHASE7_O_pad[2]	F	13	PDB12DGZ	O	floating	floating	-	-
E14	D13	88	Y_SDATA5_O_pad[3]	E	14	PDB12DGZ	O	floating	floating	-	-
C14	D14	89	Y_SE_CLK_O_pad[3]	C	14	PDB12DGZ	O	floating	floating	-	-
B15	D15	90	Y_PHASE2_O_pad[2]	B	15	PDB12DGZ	O	floating	floating	-	-
G17	D16	91	Y_DVALID_O_pad[5]	G	17	PDB12DGZ	O	floating	floating	-	-
E17	D17	92	Y_PHASE5_O_pad[1]	E	17	PDB12DGZ	O	floating	floating	-	-

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E18	D18	93	Y_PHASE1_O_pad[0]	E	18	PDB12DGZ	O	floating	floating	-	-
C19	D19	94	Y_SDATA5_O_pad[0]	C	19	PDB12DGZ	O	floating	floating	-	-
B19	D20	95	Y_PHASE4_O_pad[0]	B	19	PDB12DGZ	O	floating	floating	-	-
E24	D23	98	LCI_ACCDATA_pad[14]	E	24	PDB12DGZ	O	floating	floating	-	-
D23	D24	99	LCI_ACCDATA_pad[9]	D	23	PDB12DGZ	O	floating	floating	-	-
E23	D25	100	LCI_ACCDATA_pad[13]	E	23	PDB12DGZ	O	floating	floating	-	-
D08	E07	107	Y_PHASE4_O_pad[1]	D	8	PDB12DGZ	O	floating	floating	-	-
F08	E08	108	Y_PHASE4_O_pad[3]	F	8	PDB12DGZ	O	floating	floating	-	-
C10	E09	109	Y_DVALID_O_pad[3]	C	10	PDB12DGZ	O	floating	floating	-	-
A10	E10	110	Y_SDATA7_O_pad[3]	A	10	PDB12DGZ	O	floating	floating	-	-
A12	E11	111	Y_SDATA4_O_pad[2]	A	12	PDB12DGZ	O	floating	floating	-	-
E13	E13	113	Y_DVALID_O_pad[7]	E	13	PDB12DGZ	O	floating	floating	-	-
E16	E15	115	Y_DUMP_SYNC_O_pad	E	16	PDB12DGZ	O	floating	floating	-	-
B17	E16	116	Y_PHASE3_O_pad[0]	B	17	PDB12DGZ	O	floating	floating	-	-
C18	E17	117	Y_SDATA1_O_pad[3]	C	18	PDB12DGZ	O	floating	floating	-	-
G19	E18	118	Y_SDATA1_O_pad[2]	G	19	PDB12DGZ	O	floating	floating	-	-
E19	E19	119	Y_SDATA4_O_pad[1]	E	19	PDB12DGZ	O	floating	floating	-	-
C21	E20	120	LCI_ACCDATA_pad[2]	C	21	PDB12DGZ	O	floating	floating	-	-
F23	E21	121	LCI_ACCDATA_pad[19]	F	23	PDB12DGZ	O	floating	floating	-	-
F21	E22	122	LCI_ACCDATA_pad[17]	F	21	PDB12DGZ	O	floating	floating	-	-
E25	E24	124	LCI_ACCDATA_pad[15]	E	25	PDB12DGZ	O	floating	floating	-	-
F24	E25	125	LCI_ACCDATA_pad[20]	F	24	PDB12DGZ	O	floating	floating	-	-
C08	F07	132	Y_TIMESTAMP_O_pad	C	8	PDB12DGZ	O	floating	floating	-	-
E08	F08	133	Y_SDATA3_O_pad[1]	E	8	PDB12DGZ	O	floating	floating	-	-
B11	F09	134	Y_PHASE6_O_pad[0]	B	11	PDB12DGZ	O	floating	floating	-	-
D11	F10	135	Y_PHASE2_O_pad[1]	D	11	PDB12DGZ	O	floating	floating	-	-
C12	F11	136	Y_SE_CLK_O_pad[7]	C	12	PDB12DGZ	O	floating	floating	-	-
B13	F13	138	Y_SDATA2_O_pad[3]	B	13	PDB12DGZ	O	floating	floating	-	-
C16	F15	140	Y_DUMP_EN_O_pad[1]	C	16	PDB12DGZ	O	floating	floating	-	-
G18	F17	142	Y_SDATA7_O_pad[2]	G	18	PDB12DGZ	O	floating	floating	-	-
D21	F19	144	LCI_ACCDATA_pad[3]	D	21	PDB12DGZ	O	floating	floating	-	-
G23	F20	145	LCI_ACCDATA_pad[25]	G	23	PDB12DGZ	O	floating	floating	-	-
G24	F21	146	LCI_ACCDATA_pad[26]	G	24	PDB12DGZ	O	floating	floating	-	-
F22	F22	147	LCI_ACCDATA_pad[18]	F	22	PDB12DGZ	O	floating	floating	-	-
B23	F23	148	LCI_ACCDATA_pad[7]	B	23	PDB12DGZ	O	floating	floating	-	-
F26	F25	150	LCI_ACCDATA_pad[22]	F	26	PDB12DGZ	O	floating	floating	-	-
D06	G07	157	Y_DUMP_EN_O_pad[0]	D	6	PDB12DGZ	O	floating	floating	-	-
E10	G08	158	Y_PHASE0_O_pad[2]	E	10	PDB12DGZ	O	floating	floating	-	-
C11	G09	159	Y_SDATA2_O_pad[0]	C	11	PDB12DGZ	O	floating	floating	-	-

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F11	G10	160	Y_PHASE7_O_pad[3]	F	11	PDB12DGZ	O	floating	floating	-	-
D12	G11	161	Y_DUMP_EN_O_pad[4]	D	12	PDB12DGZ	O	floating	floating	-	-
G15	G14	164	Y_DVALID_O_pad[0]	G	15	PDB12DGZ	O	floating	floating	-	-
E15	G15	165	Y_PHASE4_O_pad[2]	E	15	PDB12DGZ	O	floating	floating	-	-
F20	G18	168	Y_PHASE1_O_pad[2]	F	20	PDB12DGZ	O	floating	floating	-	-
G22	G19	169	LCI_ACCDATA_pad[24]	G	22	PDB12DGZ	O	floating	floating	-	-
G21	G20	170	LCI_ACCDATA_pad[23]	G	21	PDB12DGZ	O	floating	floating	-	-
G20	G21	171	Y_PHASE0_O_pad[1]	G	20	PDB12DGZ	O	floating	floating	-	-
H25	G22	172	LCI_ACCDATA_pad[31]	H	25	PDB12DGZ	O	floating	floating	-	-
H23	G23	173	LCI_ACCDATA_pad[29]	H	23	PDB12DGZ	O	floating	floating	-	-
H24	G24	174	LCI_ACCDATA_pad[30]	H	24	PDB12DGZ	O	floating	floating	-	-
E26	G25	175	LCI_ACCDATA_pad[16]	E	26	PDB12DGZ	O	floating	floating	-	-
F09	H08	183	Y_DUMP_EN_O_pad[6]	F	9	PDB12DGZ	O	floating	floating	-	-
B12	H10	185	Y_DUMP_EN_O_pad[2]	B	12	PDB12DGZ	O	floating	floating	-	-
F12	H11	186	Y_SDATA7_O_pad[0]	F	12	PDB12DGZ	O	floating	floating	-	-
F14	H13	188	Y_SDATA2_O_pad[2]	F	14	PDB12DGZ	O	floating	floating	-	-
D14	H14	189	Y_PHASE7_O_pad[0]	D	14	PDB12DGZ	O	floating	floating	-	-
C17	H16	191	Y_PHASE5_O_pad[2]	C	17	PDB12DGZ	O	floating	floating	-	-
H19	H18	193	X_SCHID_FRAME_O_pad	H	19	PDB12DGZ	O	floating	floating	-	-
J20	H19	194	X_PHASE4_O_pad[3]	J	20	PDB12DGZ	O	floating	floating	-	-
J22	H20	195	X_SE_CLK_O_pad[2]	J	22	PDB12DGZ	O	floating	floating	-	-
H20	H21	196	X_SDATA3_O_pad[1]	H	20	PDB12DGZ	O	floating	floating	-	-
H22	H22	197	X_SE_CLK_O_pad[5]	H	22	PDB12DGZ	O	floating	floating	-	-
J23	H23	198	X_SDATA6_O_pad[0]	J	23	PDB12DGZ	O	floating	floating	-	-
H21	H24	199	X_SDATA0_O_pad[3]	H	21	PDB12DGZ	O	floating	floating	-	-
D24	H25	200	LCI_ACCDATA_pad[12]	D	24	PDB12DGZ	O	floating	floating	-	-
E09	J09	209	Y_DVALID_O_pad[2]	E	9	PDB12DGZ	O	floating	floating	-	-
G10	J10	210	Y_SDATA7_O_pad[1]	G	10	PDB12DGZ	O	floating	floating	-	-
F16	J15	215	Y_DVALID_O_pad[6]	F	16	PDB12DGZ	O	floating	floating	-	-
F18	J16	216	Y_PHASE3_O_pad[1]	F	18	PDB12DGZ	O	floating	floating	-	-
K24	J18	218	X_SDATA3_O_pad[3]	K	24	PDB12DGZ	O	floating	floating	-	-
K23	J19	219	X_SE_CLK_O_pad[6]	K	23	PDB12DGZ	O	floating	floating	-	-
K25	J20	220	X_SE_CLK_O_pad[1]	K	25	PDB12DGZ	O	floating	floating	-	-
J26	J22	222	X_PHASE2_O_pad[3]	J	26	PDB12DGZ	O	floating	floating	-	-
J24	J23	223	X_DUMP_EN_O_pad[7]	J	24	PDB12DGZ	O	floating	floating	-	-
J21	J24	224	X_PHASE4_O_pad[1]	J	21	PDB12DGZ	O	floating	floating	-	-
C26	J25	225	LCI_DATA_CLKOUT_pad	C	26	PDB12DGZ	O	floating	floating	-	-
F10	K10	235	Y_PHASE1_O_pad[3]	F	10	PDB12DGZ	O	floating	floating	-	-
G11	K11	236	Y_CLOCK_O_pad	G	11	PDB12DGZ	O	floating	floating	-	-

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C13	K13	238	Y_DUMP_EN_O_pad[5]	C	13	PDB12DGZ	O	floating	floating	-	-
D16	K15	240	Y_SDATA6_O_pad[2]	D	16	PDB12DGZ	O	floating	floating	-	-
J25	K16	241	X_SDATA3_O_pad[2]	J	25	PDB12DGZ	O	floating	floating	-	-
K22	K17	242	X_TIMESTAMP_O_pad	K	22	PDB12DGZ	O	floating	floating	-	-
L22	K18	243	X_SDATA4_O_pad[3]	L	22	PDB12DGZ	O	floating	floating	-	-
L25	K19	244	X_PHASE7_O_pad[3]	L	25	PDB12DGZ	O	floating	floating	-	-
K26	K21	246	X_DUMP_EN_O_pad[6]	K	26	PDB12DGZ	O	floating	floating	-	-
G26	K22	247	LCI_ACCDATA_pad[28]	G	26	PDB12DGZ	O	floating	floating	-	-
F25	K23	248	LCI_ACCDATA_pad[21]	F	25	PDB12DGZ	O	floating	floating	-	-
C22	K24	249	LCI_ACCDATA_pad[6]	C	22	PDB12DGZ	O	floating	floating	-	-
L21	L15	265	X_SDATA1_O_pad[1]	L	21	PDB12DGZ	O	floating	floating	-	-
L24	L16	266	X_SE_CLK_O_pad[4]	L	24	PDB12DGZ	O	floating	floating	-	-
M23	L18	268	X_DVALID_O_pad[4]	M	23	PDB12DGZ	O	floating	floating	-	-
M25	L19	269	X_SE_CLK_O_pad[0]	M	25	PDB12DGZ	O	floating	floating	-	-
M26	L20	270	X_SDATA0_O_pad[2]	M	26	PDB12DGZ	O	floating	floating	-	-
L23	L21	271	X_SDATA6_O_pad[3]	L	23	PDB12DGZ	O	floating	floating	-	-
L26	L22	272	X_SDATA7_O_pad[1]	L	26	PDB12DGZ	O	floating	floating	-	-
K21	L23	273	X_PHASE1_O_pad[1]	K	21	PDB12DGZ	O	floating	floating	-	-
G25	L24	274	LCI_ACCDATA_pad[27]	G	25	PDB12DGZ	O	floating	floating	-	-
H26	L25	275	X_DUMP_EN_O_pad[0]	H	26	PDB12DGZ	O	floating	floating	-	-
M21	M21	296	X_PHASE0_O_pad[2]	M	21	PDB12DGZ	O	floating	floating	-	-
N21	M22	297	X_PHASE1_O_pad[3]	N	21	PDB12DGZ	O	floating	floating	-	-
M22	M24	299	X_DUMP_EN_O_pad[3]	M	22	PDB12DGZ	O	floating	floating	-	-
M24	M25	300	X_SDATA7_O_pad[3]	M	24	PDB12DGZ	O	floating	floating	-	-
B21	N13	313	LCI_ACCDATA_pad[1]	B	21	PDB12DGZ	O	floating	floating	-	-
P21	N14	314	X_CLOCK_O_pad	P	21	PDB12DGZ	O	floating	floating	-	-
P24	N15	315	X_SDATA4_O_pad[2]	P	24	PDB12DGZ	O	floating	floating	-	-
N22	N17	317	X_DVALID_O_pad[3]	N	22	PDB12DGZ	O	floating	floating	-	-
P22	N18	318	X_DVALID_O_pad[2]	P	22	PDB12DGZ	O	floating	floating	-	-
P25	N19	319	X_PHASE7_O_pad[2]	P	25	PDB12DGZ	O	floating	floating	-	-
N25	N20	320	X_SDATA2_O_pad[1]	N	25	PDB12DGZ	O	floating	floating	-	-
N23	N21	321	X_SDATA0_O_pad[0]	N	23	PDB12DGZ	O	floating	floating	-	-
P23	N22	322	X_PHASE6_O_pad[0]	P	23	PDB12DGZ	O	floating	floating	-	-
P26	N23	323	X_SDATA2_O_pad[0]	P	26	PDB12DGZ	O	floating	floating	-	-
N26	N24	324	X_PHASE2_O_pad[1]	N	26	PDB12DGZ	O	floating	floating	-	-
N24	N25	325	X_SDATA7_O_pad[0]	N	24	PDB12DGZ	O	floating	floating	-	-
R24	P15	340	X_DUMP_EN_O_pad[4]	R	24	PDB12DGZ	O	floating	floating	-	-
R25	P19	344	X_SE_CLK_O_pad[7]	R	25	PDB12DGZ	O	floating	floating	-	-
R22	P20	345	X_SDATA6_O_pad[1]	R	22	PDB12DGZ	O	floating	floating	-	-

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R23	P23	348	X_DVALID_O_pad[7]	R	23	PDB12DGZ	O	floating	floating	-	-
R21	P24	349	X_SDATA5_O_pad[3]	R	21	PDB12DGZ	O	floating	floating	-	-
U23	R16	366	X_SDATA3_O_pad[0]	U	23	PDB12DGZ	O	floating	floating	-	-
U26	R17	367	X_DVALID_O_pad[1]	U	26	PDB12DGZ	O	floating	floating	-	-
T22	R18	368	X_DVALID_O_pad[0]	T	22	PDB12DGZ	O	floating	floating	-	-
U24	R20	370	X_PHASE4_O_pad[2]	U	24	PDB12DGZ	O	floating	floating	-	-
T25	R21	371	X_PHASE6_O_pad[1]	T	25	PDB12DGZ	O	floating	floating	-	-
T23	R22	372	X_DUMP_EN_O_pad[5]	T	23	PDB12DGZ	O	floating	floating	-	-
T21	R24	374	X_SDATA1_O_pad[0]	T	21	PDB12DGZ	O	floating	floating	-	-
R26	R25	375	X_DUMP_EN_O_pad[2]	R	26	PDB12DGZ	O	floating	floating	-	-
V22	T17	392	X_DUMP_SYNC_O_pad	V	22	PDB12DGZ	O	floating	floating	-	-
U22	T23	398	X_SE_CLK_O_pad[3]	U	22	PDB12DGZ	O	floating	floating	-	-
T26	T24	399	X_SDATA2_O_pad[2]	T	26	PDB12DGZ	O	floating	floating	-	-
T24	T25	400	X_SDATA2_O_pad[3]	T	24	PDB12DGZ	O	floating	floating	-	-
Y22	U18	418	X_SDATA1_O_pad[2]	Y	22	PDB12DGZ	O	floating	floating	-	-
W22	U19	419	X_DVALID_O_pad[6]	W	22	PDB12DGZ	O	floating	floating	-	-
W24	U20	420	X_PHASE2_O_pad[0]	W	24	PDB12DGZ	O	floating	floating	-	-
W26	U21	421	X_PHASE3_O_pad[0]	W	26	PDB12DGZ	O	floating	floating	-	-
V23	U22	422	X_SDATA6_O_pad[2]	V	23	PDB12DGZ	O	floating	floating	-	-
V21	U23	423	X_PHASE3_O_pad[3]	V	21	PDB12DGZ	O	floating	floating	-	-
U25	U25	425	X_PHASE6_O_pad[2]	U	25	PDB12DGZ	O	floating	floating	-	-
AB24	V19	444	X_SDATA5_O_pad[0]	AB	24	PDB12DGZ	O	floating	floating	-	-
AB25	V20	445	X_PHASE4_O_pad[0]	AB	25	PDB12DGZ	O	floating	floating	-	-
AA22	V21	446	X_SDATA1_O_pad[3]	AA	22	PDB12DGZ	O	floating	floating	-	-
Y26	V22	447	X_PHASE1_O_pad[0]	Y	26	PDB12DGZ	O	floating	floating	-	-
V25	V23	448	X_SDATA5_O_pad[1]	V	25	PDB12DGZ	O	floating	floating	-	-
V24	V24	449	X_DUMP_EN_O_pad[1]	V	24	PDB12DGZ	O	floating	floating	-	-
U21	V25	450	X_PHASE7_O_pad[0]	U	21	PDB12DGZ	O	floating	floating	-	-
AB23	W20	470	X_SDATA5_O_pad[2]	AB	23	PDB12DGZ	O	floating	floating	-	-
Y24	W21	471	X_SDATA7_O_pad[2]	Y	24	PDB12DGZ	O	floating	floating	-	-
AA26	W22	472	X_SDATA4_O_pad[1]	AA	26	PDB12DGZ	O	floating	floating	-	-
W23	W23	473	X_PHASE5_O_pad[1]	W	23	PDB12DGZ	O	floating	floating	-	-
W25	W24	474	X_PHASE5_O_pad[2]	W	25	PDB12DGZ	O	floating	floating	-	-
V26	W25	475	X_PHASE3_O_pad[2]	V	26	PDB12DGZ	O	floating	floating	-	-
Y19	Y19	494	X_PHASE2_O_pad[2]	Y	19	PDB12DGZ	O	floating	floating	-	-
Y25	Y22	497	X_PHASE3_O_pad[1]	Y	25	PDB12DGZ	O	floating	floating	-	-
AB26	Y23	498	X_SDATA4_O_pad[0]	AB	26	PDB12DGZ	O	floating	floating	-	-
AA24	Y24	499	X_SDATA0_O_pad[1]	AA	24	PDB12DGZ	O	floating	floating	-	-
AA25	Y25	500	X_PHASE0_O_pad[0]	AA	25	PDB12DGZ	O	floating	floating	-	-

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AA23	AA22	522	X_PHASE5_O_pad[0]	AA	23	PDB12DGZ	O	floating	floating	-	-
Y23	AA25	525	X_PHASE1_O_pad[2]	Y	23	PDB12DGZ	O	floating	floating	-	-
AB22	AC20	570	X_PHASE0_O_pad[3]	AB	22	PDB12DGZ	O	floating	floating	-	-
AA21	AC23	573	X_DVALID_O_pad[5]	AA	21	PDB12DGZ	O	floating	floating	-	-
Y20	AD23	598	X_PHASE7_O_pad[1]	Y	20	PDB12DGZ	O	floating	floating	-	-
Y21	AD24	599	X_PHASE6_O_pad[3]	Y	21	PDB12DGZ	O	floating	floating	-	-
AA20	AE23	623	X_PHASE0_O_pad[1]	AA	20	PDB12DGZ	O	floating	floating	-	-
W21	AE25	625	X_PHASE5_O_pad[3]	W	21	PDB12DGZ	O	floating	floating	-	-

Vector program

```

'
'
'
'This vector file is used to send a sequence of reset to the
'NRC EVLA. These vectors place the device in
'reset mode initially. Bus 5 is the low bus, Bus 6 is the high bus,
'Bus 3 is the Ground bus, and Bus 2 is the Vdd2.5 bus, Bus 4 is VDD12 bus.
' File:NRC_EVLA.VC0
'
#SaveResults
C:\WINDOWS\desktop\VECOUT.VC0, EchoCommand
#Vector
NRC_EVLA Reset Sequence,ResetOn
#SetBus
5,6,3,4      'low, high, Gnd, Vdd2.75
#Group
Inputs1,"618"
#GroupOrder
"Inputs1"
#InitPinByGroup
Inputs1,"1"
#PatternStart
"0"
"1"
"0"
"1"
"0"
"1"
"0"
"1"
"0"
"1"

```

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```
"0"  
"1"  
"0"  
"1"  
"0"  
"1"  
#PatternEnd  
#End  
NRC_EVLA Reset Sequence
```