TEST AND VERIFICATION PLAN

EVLA Baseline Board Prototypes

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List of Abbreviations and Acronyms

ASIC – Application Specific Integrated Circuit. Refers to the correlator chip here.

BE – BackEnd. Refers to computers that process correlator output data.

BGA – Ball Grid Array.

EMI – Electro-Magnetic Interference.

EVLA – Expanded Very Large Array.

e-MERLIN – MERLIN radio telescope upgrade in the UK.

FPGA – Field Programmable Gate Array.

GigE – Gbit/sec Ethernet.

GUI – Graphical User Interface.

HM Gbps – Refers to time-multiplexed 1.024 Gbps signals that are used for signal transport from Station Boards to Baseline Boards in the correlator.

JTAG – Used for connectivity testing of chips on a PCB.

LTA – Long-Term Accumulator.

PCB – Printed Circuit Board.

PCMC – PC/104+ mezzanine card. The PC/104+ module plugs into this, that then plugs into the motherboard.

PC/104+ – Small form-factor embedded PC with ISA and PCI bus interfaces.

R2 – Refers to "recirculation 2" in the RC. R2 supports recirculation on all 8 streams.

RC – Recirculation Controller.

TGB – Timecode Generator Board.

UDP/IP – User Datagram Protocol over Internet Protocol.

UUT – Unit Under Test.

VLA – Very Large Array radio telescope in New Mexico.

1 Revision History

Revision	Date	Changes/Notes	Author
DRAFT	March 17, 2005	Initial DRAFT release	B. Carlson

2 Introduction

This document defines the baseline test and verification plan for the EVLA correlator Baseline Board. This plan encompasses all testing requirements and activities for the board from initial prototypes up to, but not including, prototype on-the-sky testing at the VLA and e-MERLIN sites.

The functionality and performance of the Baseline Board is largely determined by the functionality and performance of FPGAs and correlator chips on the board, and these are defined in detail in associated RFS documents. Refer to the RFS documents for the Recirculation Controller [1], Correlator Chip [2], LTA Controller [3], and Gbit Ethernet chip [4] for further detailed information on the operation of the Baseline Board, in lieu of a Baseline Board RFS document that does not yet exist at the time of this writing.

This document describes in some detail software requirements for GUI (Graphical User Interface) screens that will provide essential facilities to expedite testing and provide feedback for design verification. If these are not available, some bare bones ability to read and write registers in a reasonably easy fashion is essential. However, it cannot be stressed enough the effect on testing that powerful user interface software will have on the speed with which tests can be performed, and the additional integrity that this software will add to the entire testing process. Indeed, this GUI software will likely exist and provide powerful testing and debug capability on through to full operations. As such, considerable effort is given to describing the functionality of these GUI screens in this document.

There are three important classes of testing that will need to be performed:

1. Verification that the Printed Circuit Board (PCB) is functioning as designed. This involves functionality/connectivity, timing and signal integrity verification, power/heat testing (including stress testing), and EMI testing mostly to ensure proper function.

2. Testing of the functionality and performance of FPGAs. Much testing of these designs has been performed in simulations, and board-level testing will be used to verify functionality and run tests that could not be run in simulations because of excessive simulation times.

3. Verification of the correlator chip ASIC prototypes. The Baseline Board will act as a test bed for testing the correlator chips, and this is the highest priority for testing.

An understanding of the context of Baseline Board testing defined by this document within the overall framework of the test plan for the entire project, as well as the test plan for the correlator chip ASIC is essential. Refer to [5] for a complete overview of test plan for the entire project and [6] for the test plan for the correlator chip ASIC.

3 Overview

This section presents a brief overview of the plan for testing and verifying the functionality and performance of the Baseline Board.

The main phases/steps in testing are envisioned to be as follows:

1. First prototype tests. This is testing of the first board built, and is a special build of the board to focus efforts on correlator chip ASIC testing. There will be several BGA sockets mounted in some correlator chip locations on the board and these will be used to allow easy testing of correlator chips (the first batch of prototype correlator chips are untested, and the yield is expected to be 60-70%). The rest of the correlator chip locations *may*—if footprint compatibility is possible—be populated with Altera Stratix-II FPGAs, to allow the board interconnects to be fully tested as well—although this is not the first priority. Nevertheless, when this testing is complete, there should be a high degree of confidence in the function of the board, the correlator chips, and the FPGAs and there should be minimum risk in the next stage of construction and test.

2. Prototype correlator board tests. Prototype chips are tested with the first prototype board and good chips are used to fully populate two additional Baseline Boards. To fully populate two boards requires a yield of about 64% (128 required good out of 200 prototype chips). These boards will be fully tested with Station Boards and are the boards that will be shipped to the VLA site, and the UK for on-the-sky tests. If a full complement of correlator chips is not available, some reduced bandwidth in the on-the-sky tests will be the result, but it will not otherwise hamper testing. Refer to [5] for more information on prototype correlator on-the-sky test configurations.

4 First Prototype Tests

The first Baseline Board prototype's primary function will be to act as a test bed for the correlator chip ASIC. Nevertheless, significant functionality of the board and its FPGAs will be necessary to properly test the ASIC. Additionally, if the ASIC turns out to be footprint compatible with an FPGA (the Altera Stratix-II EP2S15F672C3), then the board can be fully populated and all data paths tested. This is the secondary goal of the first prototype test.

The prototype ASICs that are delivered are untested and the expected yield is 60-70%. Thus, it is desirable to socket some locations on the board for ASIC test. Sockets should have little if no impact on the performance of the chip since all high-speed connections are point-to-point over short distances. All locations *could* have sockets, however the cost of this is excessive since sockets cost about $260 each. It is believed that a sufficiently rigorous level of testing of the ASIC can be performed by only socketing some locations.

The test setup for the first prototype is shown in Figure 1. In this setup, the following items are of note:

- The board is populated with 16 BGA sockets (at $260 each the cost is $4100) for correlator chip prototypes as indicated in the figure (these are labeled with the "CCS" boxes in the figure).

- The rest of the correlator chip locations are populated with FPGAs—labeled with the "FP" boxes in the figure. If the FPGAs are not footprint compatible, then these locations are left blank. The basic daisy-chain operation of LTA Controller FPGAs (as far as readout communication and control is concerned) is not affected by missing chips in the correlator chip locations. The LTA Controllers are on the reverse side of the board and are not shown in the figure.

- One Timecode Generator Board, and 2 Fanout Boards are required to generate the signals to stimulate the board. The Timecode Generator Board has a 128 MHz local oscillator and an FPGA with enough outputs to fully stimulate 4 complete wafers with test signals. These go through 2 stages of Fanout Boards to generate the necessary 16 x 4-wafer outputs that can fully stimulate the Baseline Board.

- Qty=19, 1 m x 4-wafer cables, 8 common backplanes, and an 800 W –48 VDC power supply are needed for power and connection of high-speed signals.

- A test backend (BE) computer with Gbit/sec Ethernet, a host computer running Linux with the GUI test software (or the GUI software could be run on another machine, remotely), and a 10/100 Mbps switch are needed to complete the test setup.

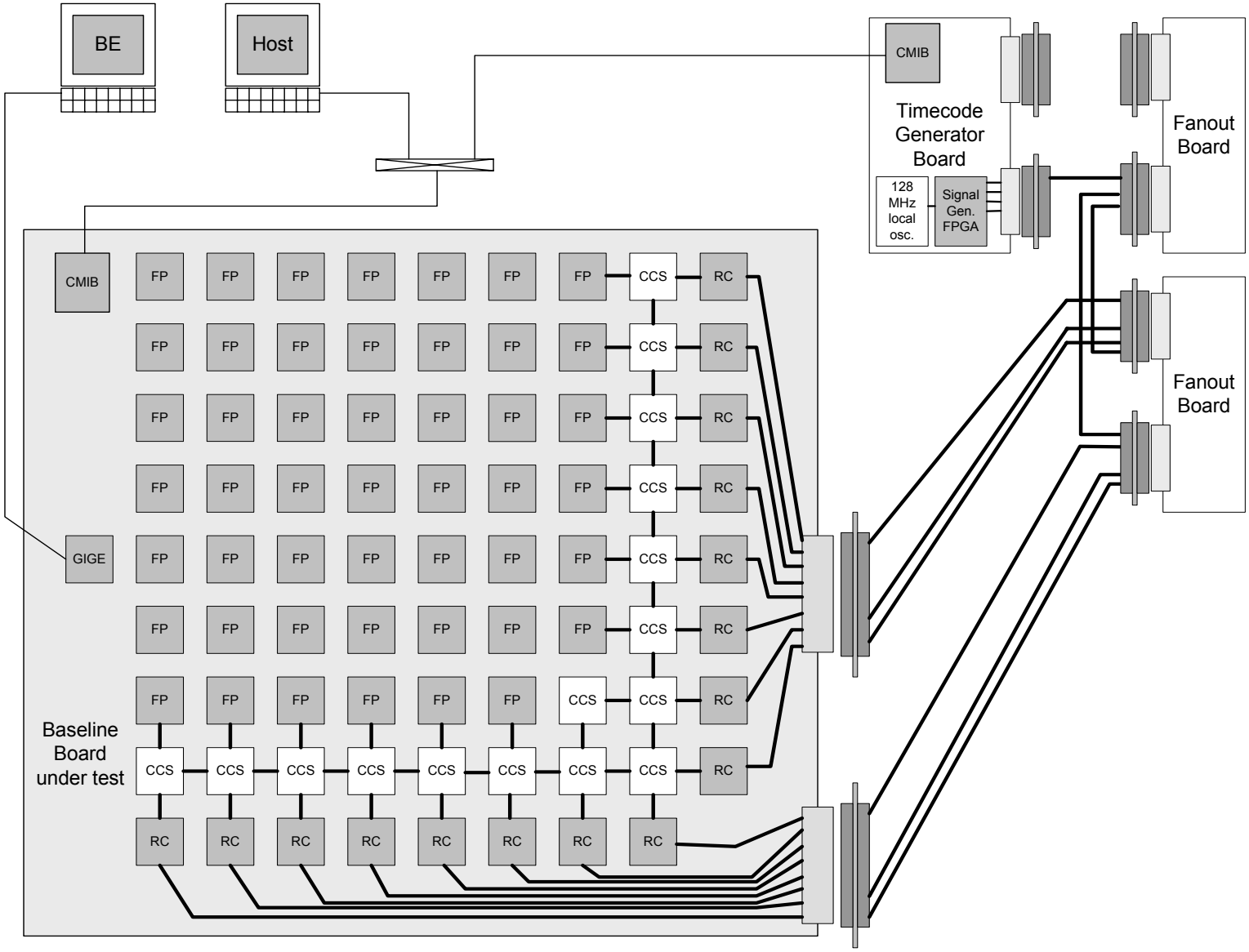

Figure 1 First Baseline Board prototype test setup. Power supplies and test bed not shown.

- The Gbit Ethernet output of the Baseline Board is untested and if the BE computer cannot detect frames from the chip, it will be necessary to lease or buy a Gbit Ethernet protocol analyzer to check the output and diagnose problems. It is not possible to look at raw correlator output data frames without a BE computer, since it will be necessary to use the "speed dump" mode of the LTA to access these raw frames.

- Additional test equipment and test techniques that will likely be utilized include the following:

    - High-speed digital storage oscilloscope with at least a 2 GHz input bandwidth and a single-shot sample rate of at least 4 Gs/s. The existing Tektronics DSA 602 lab scope and active FET probe meet these requirements (I believe so anyway). This scope and probe is capable of observing basic eye diagrams on the 1 Gbps signals into the board. Lower-bandwidth probes can be used for probing the 256 Mbps signals on the board.

    - The board is equipped with land pads on the PCB to accept the Agilent "soft-touch" connectorless probes at the output of Recirculation Controllers ("RC" boxes in the figure), and these can be used with our recently purchased Agilent 16900A logic analyzer to look at critical signals traveling to the correlator chips.

    - There is no such land pad between correlator chips or to the LTA FPGA, and so it is likely prudent, if possible, to acquire one signal breakout socket for the correlator chip so that signals can be probed directly since many correlator chip BGA pads go to blind vias and cannot, in any way, be accessed directly.

    - The RC and LTA FPGAs contain 4 test points each, and these can be connected to internal nodes. However, relative timing of these signals are subject to the vagaries of FPGA routing and can only be used for basic signal sanity checks if necessary.

    - The FPGAs have the ability to instantiate internal logic analysis probe points that are accessed externally via the JTAG interface. This ability is not built into the existing designs, however, it can be added if it is found to be necessary since all chips will be connected to JTAG.

4.1 Test Signal Generation and Verification

To properly test the correlator chip, the following signal generation and testing is envisioned:

- Load the Timecode Generator Board (TGB) FPGA with a design that stimulates all of the signals on one 4x4-wafer cable. This design contains repetitive deterministic signals for making the Recirculation Controller generate repetitive deterministic signals to the correlator chip.

- Feed the TGB output to all of the inputs of the Baseline Board as shown in Figure 1.

- The repetitive signals are on a timescale such that it is possible to perform a direct comparison of frames produced by the actual correlator chip (via "speed dump" frames routed to the backend computer) with frames produced by an RTL simulation of the TGB FPGA, the Recirculation Controller, and the correlator chip.

- The generated repetitive signals do not have to contain data to produce fringes. Verification of the correlator chip is the only requirement.

- The generated repetitive signals must have short time scales to make RTL simulation feasible. The suggest time between Timecode ticks is 10 usec for this reason.

- The signals generated for this purpose, and for the Gbit/sec end-to-end test can be identical. Thus, only one TGB FPGA test design is required for this purpose.

As a matter of course, the major functions and data paths on the Baseline Board will be tested by testing the correlator chip as described above. If the correlator chip locations containing FPGAs are populated, then it will be possible to test all signal paths on the board. If not, some signal paths will be untested although these signal paths are, in principle, identical to paths that will undergo tests and so there should be a high confidence factor established.

4.2 Prototype Test Bed Requirements

The requirements for the prototype test bed are as follows:

- Slots for the components and Baseline Board under test as shown in Figure 1. Insertion and ejection capability for all boards.
- Easy access to the front and back side of the Baseline Board for probe testing, especially with the logic analyzer and with an oscilloscope on the connector pins.
- It may be necessary, and it is acceptable, if the Baseline Board and the other plug-in boards (TGB, Fanout Board) are in separate test beds. This may make access to the Baseline Board easier.
- Adequate fan cooling for the Baseline Board, even with no heat-spreader installed.
- At least a 1 kW, -48 VDC power supply. This will likely be fed from a breaker panel that sources from a lab power supply with 100 A total capacity. It is essential that power to *each* large board under test uses a separate (~15 A) breaker.

A simplified diagram of the Baseline Board test bed, with the Baseline Board UUT (Unit Under Test) is shown in Figure 2. It is likely that a sub-rack used for the rack thermal tests can be modified and used for this purpose. In this diagram, there is enough room for the Fanout Boards and TGB, although they should likely be mounted in a separate, similarly constructed 6U test bed to allow for complete access to the UUT.

Refer to section 7 for more information on lab power supply and networking requirements.

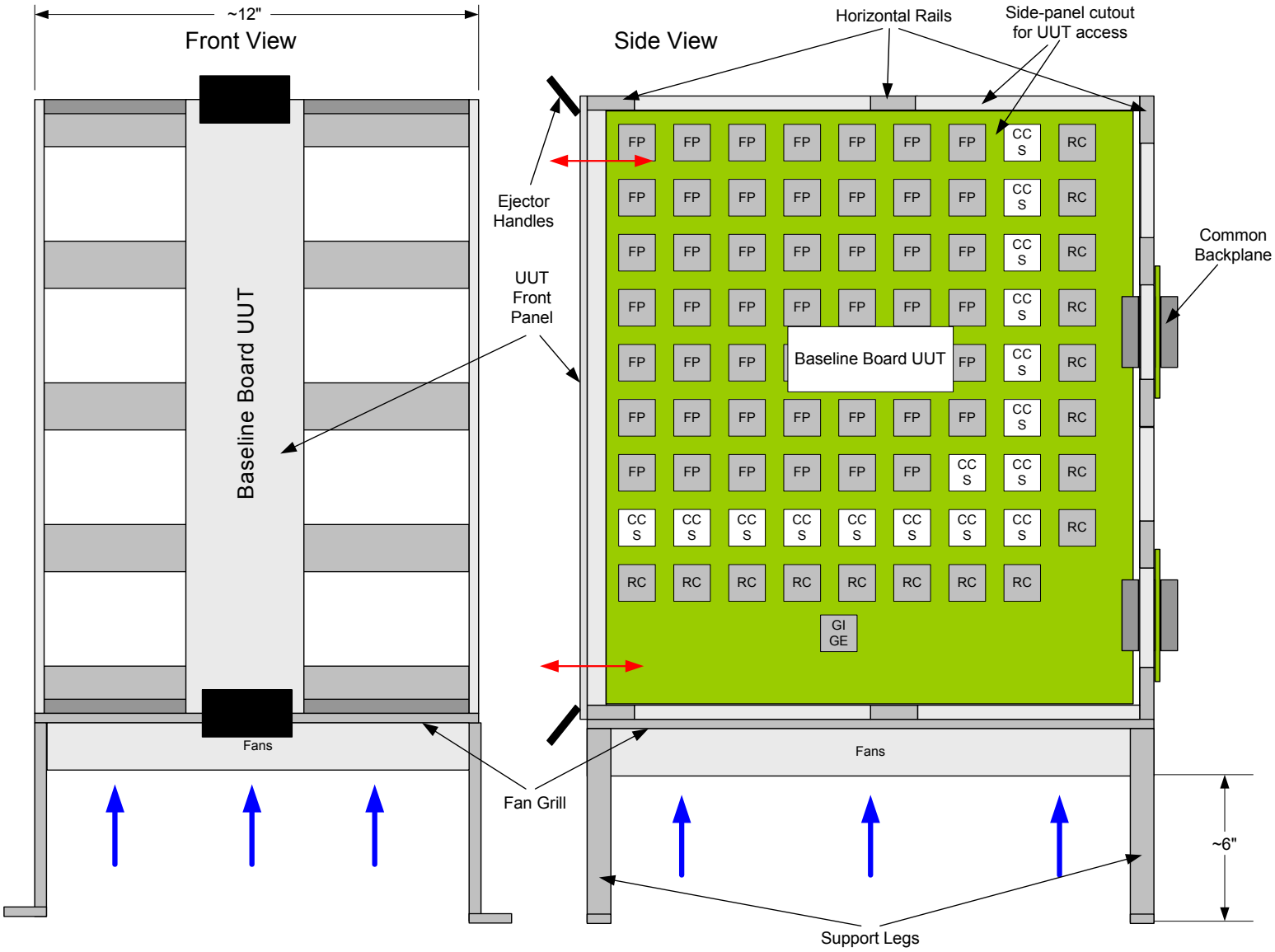

Figure 2 Baseline Board test bed concept.

4.3 First Prototype Testing Activities

The following testing activities are envisioned to occur in the tests of the first prototype Baseline Board (UUT), roughly in chronological order:

- The first prototype Baseline Board should be populated with EP2S30F672C3 FPGAs for RCs, and all 256k x 18 DPSRAMs for the RCs to test all data paths on the board. The 2S30 device is required for R2 (recirculation-2) capability, and is footprint compatible with the 2S15 device that will likely be the device used in production unless the cost of the 2S30 and DPSRAMs drops.

- Inspect the board and ensure that all devices are installed with the proper polarity. Do not install any correlator chips in sockets at this time. Perform a continuity test across the 48 VDC power lines and low-voltage power lines to ensure there are no short circuit conditions. If FPGAs are installed in places where there are no correlator chip sockets, ensure that the Accel regulator chips are programmed to supply the correct voltage to the FPGAs (1.2 V). This is possible to do on a serial command line via the LTA FPGA, although there is no support for doing it at this time. Ensure that the FPGAs are not supplied with core voltages exceeding their specifications!

- Install the PCMC and PC/104+ boards and power-up the board. The only cable connections at this point are the power supply lines and a network connection to the PC/104+ board. Check power supply voltages to the chips…this should be a matter of observing the power-ok LEDs on the board, that are driven by window comparators. Check for any overheating components. This is the "smoke test".

- Work with software engineers to get the PC/104+ board booting, c/w a shell, and talking to the PCMC. rlogin access to the PC/104+ board can be via any computer on the network. Refer to section 7.2 for the preferred setup whereby there is a laptop computer in the lab that can be used to access the PC/104+ board via the network.

- Connect the Timecode Generator Board and Fanout Boards to the UUT as shown in Figure 1. Power-up and boot the Timecode Generator Board, load the FPGA with the test program to generate signal stimulus as described in section 4.1. This should be easy to do, since this is the same FPGA program and basic setup as the Gbit/sec end-to-end test. If necessary, verify that the signals are being generated by looping back into the TGB.

- Download the bitstreams for the Recirculation Controller (RC) FPGAs on the UUT. Ensure the RCs are programmed…this should be a matter of checking status information in the PCMC. Ensure that each of the 16 RCs can synchronize and lock to the input signals—this is a simple process whereby receiver locking is turned on, and status registers are checked for lock indication. Refer to the Recirculation Controller RFS, and the GUI screen in section 6.2.

- It should be possible for the Gbit Ethernet (GigE) FPGA to talk to the LTA Controller FPGAs without installation of the correlator chips, and it should be possible to send frames from the LTA Controller to the backend via the direct memory access feature of the LTA (see the LTA GUI of section 6.4). Thus, download the bitstream for the LTA FPGA and the GigE FPGA, write a frame into each LTA RAM, and try to transfer this frame to the backend (BE).

- If there are problems transferring frames to the BE, the problem can be in one of several locations, and it should be possible to nail down the problem by reading the LTA and GigE status registers via their GUIs. If there are no problems on the board, then it is possible that the Ethernet frame format is incorrect, and if the BE's GigE card gives no indication as to cause of no frames, it will be necessary to lease or purchase a GigE tester to diagnose the problem. There is no testing of the GigE FPGA Ethernet frame format yet, and so it is entirely possible that there errors that need to be corrected.

- Once it is possible to send frames from the LTA to the BE, and the RCs all lock on their inputs, it is time to test the first correlator chip.

- Install the first correlator chip in the socket in location X0, Y0. Double-check its polarity. Power up and boot the board including downloading bitstreams into all of the FPGAs. Check for overheating. Turn-on test signal generation in the TGB test FPGA. Ensure the RCs are locked and generating normal data to the correlator chip row and columns.

- Use the LTA in location X0, Y0 GUI to power-up the correlator chip. Check for power good status from the Accel chip via the LTA. Remove the "PLL Reset" and then the "Reset" lines to the correlator chip.

- Use the correlator chip GUI to check status. It should be possible to talk to the chip, and it should not be reporting errors. With the correlator chip, LTA and GigE so enabled, the correlator chip should be producing frames to go to the BE, where raw frames can be captured and compared directly with the frames produced by the RTL sim. Configure the correlator chip in a number of different lag chaining configurations and test output for compliance with the RTL sim. Use the test cases developed for correlator chip validation as a guide for the kinds of tests to be run.

- As the prototype correlator chips have only a 60-70% expected yield, it is entirely possible that the first chip is defective without it being a design problem. If necessary, swap out the correlator chip with different ones until a chip is found that at least produces frames. Continue testing.

- Using the appropriate GUIs, set the RCs and correlator chip for test vector mode. Note that this mode still requires detection and locking of the signal from the TGB test FPGA. Ensure that the correlator chip is detecting no errors from the RCs. This is an indication that the data path to the correlator chip is functioning

properly. Use the RC's GUI to force bitstream errors on every input to see if the correlator chip detects the error.

- Install correlator chips in the remaining sockets and test accordingly. Swap out chips if necessary to eliminate bad ones. Ensure that known good chips are marked as such.

- Run the correlator chips at elevated temperature (need recommendations from the chip manufacturer for this, could be 100 ^{o}C max chip temperature) and let the chip run in normal mode producing frames to the BE. If possible, also temperature-shock the chip to see if there are any hiccups in its operation (likely using heat-gun/cold-spray, but a recommendation from the chip manufacturer on how extreme this could be needs to be followed).

- It may be necessary to modify, or allow the modification of how often the correlator chip produces a frame (by controlling how often DUMPTRIGs are produced in the program in the TGB test FPGA) so that overrun conditions are not produced. This can be done by interleaving the occasional speed-dump frame with a bunch of "dump/clear" frames to throttle the frame rate from the correlator chip. It is desirable to capture frames into the BE from the correlator chip over a long period of time so that comparison of a large number of frames with frames produced by the RTL sim is possible to try to find intermittent problems. This will require some auxiliary software to perform an exhaustive comparison of frames captured by the BE.

- Once the correlator chip produces error-free frames and expected status reads for 100 hours at elevated temperature with a few low-temperature shocks thrown in, then 1st prototype testing is complete and there is a high probability that the correlator chip and the Baseline Board itself is functioning properly.

- Use the sockets on this first prototype to qualify all of the correlator chips for fabrication of the 2nd two prototype boards required for on-the-sky testing. Each chip should run at elevated temperature for at least 24 hours, with no failures, to be fully qualified. This, followed by fabrication of the next 2 fully populated boards, should be done soon after the 100 hour test is complete. These new boards should have the RCs and DPSRAMs populated identically to the first board.

At this point, the majority of the Baseline Board (all of it if FPGAs are installed where there are no correlator chip sockets) has been tested. It is now necessary to connect the board to the Station Board output to see if the locking to the Station Board's output signal is possible, and to see if fringes can be detected for simulated astronomical test vector signals. This testing is described in the next sub-section. The signal-generation setup as shown in Figure 1 should not be permanently dismantled, as that signal-generation setup will still be used for testing the next 2 boards that are fabricated.

4.4 Testing with Station Board Outputs

Once first prototype testing, as described in the previous section, is complete, it is time to connect the first Baseline Board under test to the Station Board. While this test is underway, two more Baseline Boards, fully populated with tested correlator chips are fabricated.

The following testing activities are envisioned for this stage of testing:

- Connect the Baseline Board UUT to Station Board outputs using Fanout Boards in a manner similar to that shown in Figure 1 to stimulate all inputs.

- Power-up, boot, and configure FPGAs and try to lock to the signal from the Station Boards.

- The Station Board should be producing test vectors, TIMECODE, PHASEMOD, and PHASERR for simulated astronomical signals so that fringes can be obtained. Basic DUMPTRIG ability should be in place to dump correlator chip frames, accumulate in the LTA, and output to the BE.

- Put the correlator chip in a number of different configuration modes and check the output with BE software by comparing with simulations of the same test vectors using the C simulator. The test vector generator must be upgraded to insert delay into the signal as well as frequency shift. The correlator C simulator will need significant upgrade to encompass the critical signal processing functions of delay tracking, digital filtering, sub-sample delay tracking, and correlation. This upgrade is required to test to ensure that the test vector generator is functioning properly and these results can be used for statistical comparison with the BE.

- Set the RC for "static recirculation" mode, whereby the recirculation memory is used to introduce a delay offset in the data path. This exercises the recirculation functions and memory on the RC FPGA, and once working, will engender a high degree of confidence that recirculation will work. This requires only standard, simple DUMPTRIG generation capability.

- Acquire a quantity of long (10 m) Meritec, equalized high-speed data cables and put these, along with short cables, in the data path from the Station Board to the Fanout Board. This will test a variety of cable configurations, as well as the synchronization FIFO buffer range on the correlator chip.

This testing is complete once fringes are detected in a number of different correlator chip configurations, these are compared with C simulator results, and the HM Gbps receivers lock and stay locked with no errors for extended time periods. Use the facilities of the FPGA and correlator chip GUIs described in section 6 and the RFS documents for long-term error monitoring.

5 Prototype Correlator Board Tests

This stage involves bench testing of the 2 fully populated Baseline Boards that will eventually be used for one-the-sky testing at the VLA and e-MERLIN sites. Once testing is complete at this stage, boards are ready for integration and testing in the prototype correlator crates in preparation for on-the-sky testing. Each board is tested individually, and the following testing activities are envisioned:

- Test boards and chips for correct operation with the test setup of Figure 1, and follow similar procedures and perform similar tests as described in the previous section.

- Run at elevated temperature (100 ^{o}C max chip temperature) for 100 hours, under different configurations and ensure that the results are correct by comparing with RTL sim results.

- Connect to the Station Board outputs and run similar tests to that described in the previous section, and compare results with previous tests and the C simulator output.

- It is important to run the correlator chip(s) in all of the possible modes that it will see in its lifetime since this is the final qualification test for the correlator chips. Refer to [8] for an exhaustive list of tests that should be performed. On-the-sky testing is believed not to be necessary for correlator chip prototype qualification, and so exhaustive testing at this stage is essential.

6 Baseline Board GUI Screens

This section contains straw-man designs for GUI screens for the Baseline Board. These GUIs, and the software functionality behind them will facilitate powerful and flexible testing of the board, FPGAs, and the correlator chip. It is likely that these GUI screens will continue to find extensive use beyond this stage of testing and will live on into normal operations.

6.1 Top-level Baseline Board GUI

This GUI is shown in Figure 3. The functionality of the GUI is more-or-less straightforward, however, the following descriptive notes on its operation may be of use.

- One or two default configurations of all chips should be made available via the "Config…" button.

- The user can double-click on any chip to see its current status and configuration (screens for these are in following figures). Configurations can be changed, applied to other chips, and then stored. This allows any number of configurations to be built and stored for future recall and use.

- More general software capabilities such as "Error and Status Reporting…" are used to set levels of reporting that will likely have system defaults. This functionality is not explicitly described here.

- If a chip on the board is operating normally and not reporting errors or warnings, its colour is green. If a chip is reporting warnings, it is yellow. If it is reporting/detecting errors, it is red. There may need to be a global "clear alarm status" button (not shown) so that software status indicators catch even short term events. These conditions can propagate to higher levels of the system.

- This GUI does not represent the top-level hierarchy for the system. It is likely that eventually GUI capability on top of this will be built so that the user could see/access any board down to any chip in the system in a hierarchical fashion.

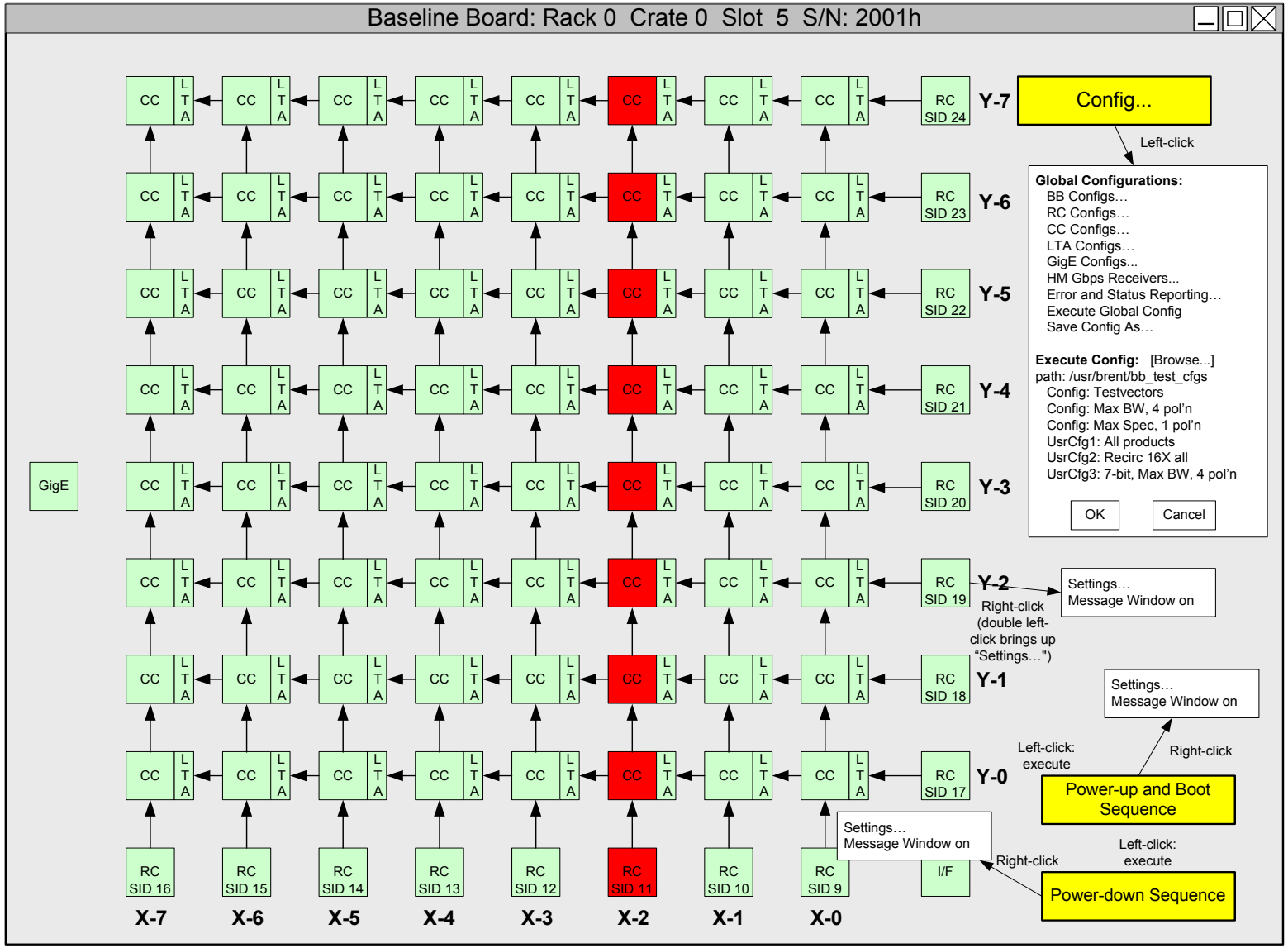

Figure 3 Baseline Board top-level GUI.

6.2 Recirculation Controller GUI

Some notable aspects of the Recirculation Controller FPGA GUI shown in Figure 4 are as follows:

- A graphical representation of data routing in the chip is provided in a manner that does not require software to change/re-draw lines when configuration changes occur. Settings can be changed by clicking on check boxes or entering settings in applicable boxes.
- "BB-0…7" refers to pins on the HM Gbps signaling cable according to [7]. Each of these refers to a 4-bit data stream that can contain 4-bit, or 7-bit samples.
- On the GUI screen there is mixture of configuration and status information. If any status indicator is reporting error conditions it is red, if warnings yellow, and if no problems green.
- In the lower-right of the screen, there is information on detection of control signals from the originating Station Boards. Some of this information requires software to accumulate status information read from chips.
- In the upper left corner is status information on the HM Gbps input. This too requires software accumulation of status read from hardware registers. This status information will be critical in prototype and on through system testing to allow evaluation of error statistics on the data link from the Station Boards to the Baseline Boards.
- In the bottom-middle of the screen is a box for recirculation operation and configuration. If the chip supports "R2" then another similar box will have to be built into the GUI.
- There is a direct read/write register capability to be used for low-level debugging.
- It may be desirable to show actively-correlated data paths in bold blue (not shown).
- There is a "SAFE MODE" that allows the chip status registers to be read, but no configuration changes to occur.
- All of the config and status information shown in the GUI accesses registers on the chip. Refer to the Recirculation Controller RFS document register description for more detailed information.
- If not in safe mode, the configuration can be changed and then applied to this, some, or all chips on the board by hitting the "Write Config" button. Once this happens, it is possible via the top-level board GUI to save this configuration to a file for future use.
- VIEW RAW REGISTERS button allows the view to change to raw register view (Figure 8).

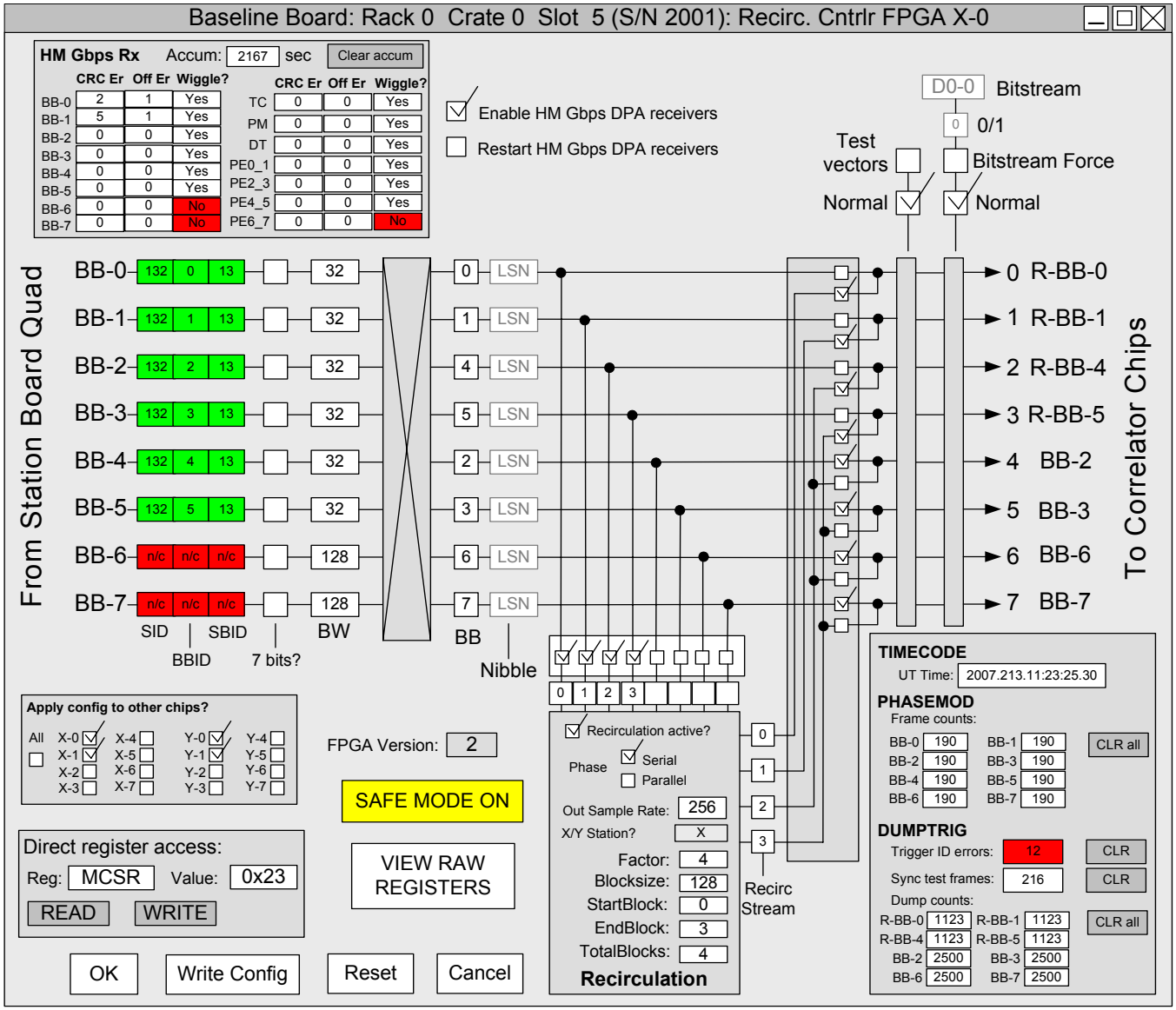

Figure 4 Recirculation Controller GUI

6.3 Correlator Chip GUI

Some notable aspects of the Correlator Chip GUI shown in Figure 5 are as follows:

- The graphics are arranged so that the X and Y inputs are on the same sides of the diagram as in the board-level GUI of Figure 3.
- Active data paths, including chaining of lag sections and active inputs, are shown in highlighted bold blue.
- Same status colour coding as the other GUIs (red—error; yellow—warning; green—ok).
- Data routing switches can be changed by clicking on appropriate boxes (these are not shown as check boxes, but could be check boxes).
- As with the RC GUI, there is a SAFE MODE, VIEW RAW REGISTERS, and direct register R/W access.

6.4 LTA Controller GUI

The LTA Controller GUI shown in Figure 6 contains some notable features:

- There are no graphics to show data paths in the chip. While this is possible it likely does not provide any useful information.
- The "CCC frame control/status" box in the upper-left corner provides configuration and status information for each CCC of the correlator chip the LTA is connected to. Software accumulation and colour-coded boxes are applicable here.
- The "LTA statistics for specified corr chip CCC" provides detailed frame status information for one selected CCC in the correlator chip. Software accumulation is necessary for desired functionality. It is also possible to provide information at this level of detail for all CCCs, on a software time-multiplex basis, but there may not be much need for such, given the box immediately above it.
- The "General register control/status" box covers miscellaneous control and status information provided by the chip, including power-up and reset control of the correlator chip.
- The "Direct LTA RAM Access" box allows direct read/write access to the LTA RAM. This can be used for correlator chip frame capture, or to test the LTA-to-BE (backend) data path without a correlator chip.
- SAFE MODE, VIEW RAW REGISTERS, and direct register access are as described for other GUIs.

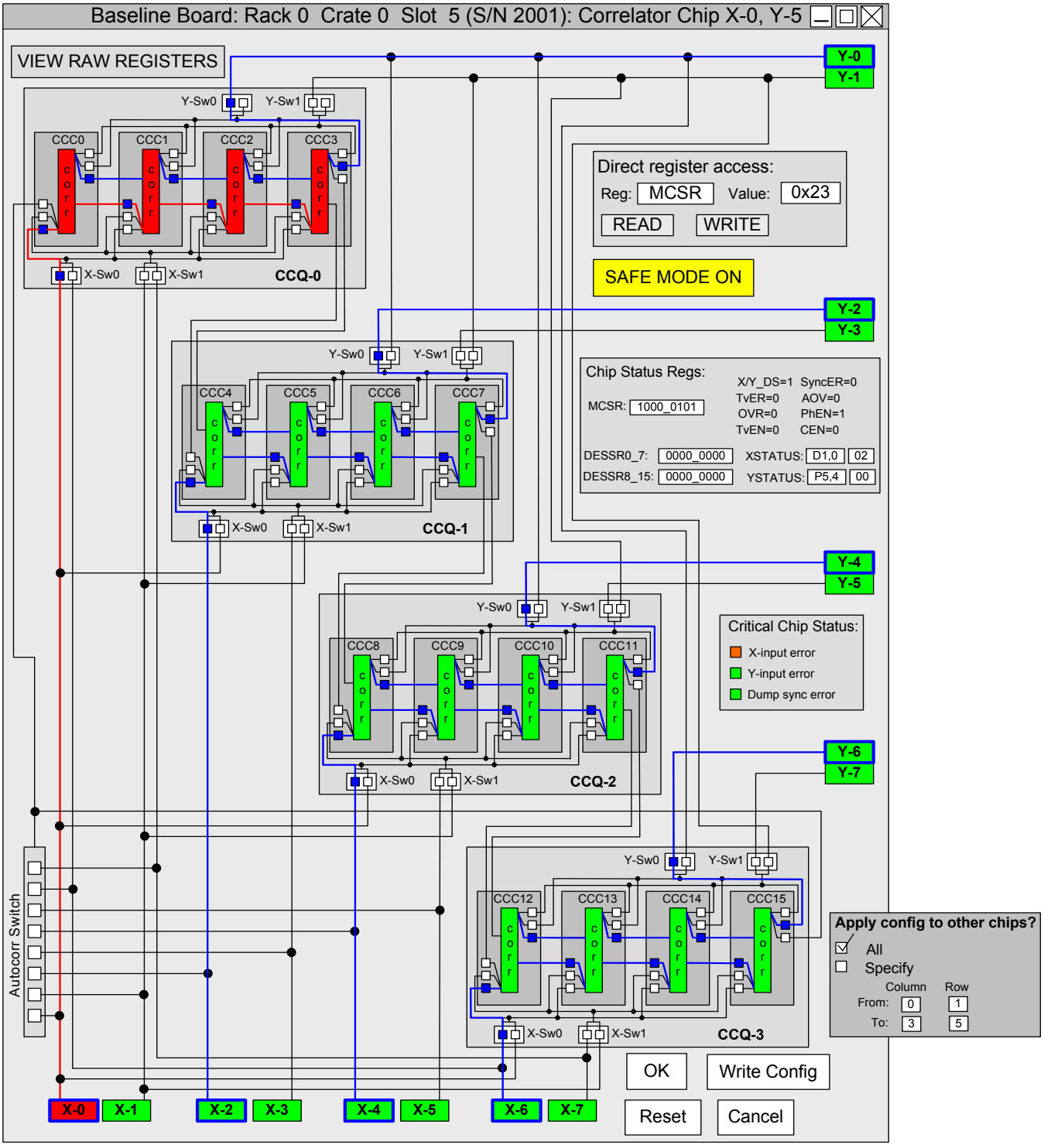

Figure 5 Correlator Chip GUI.

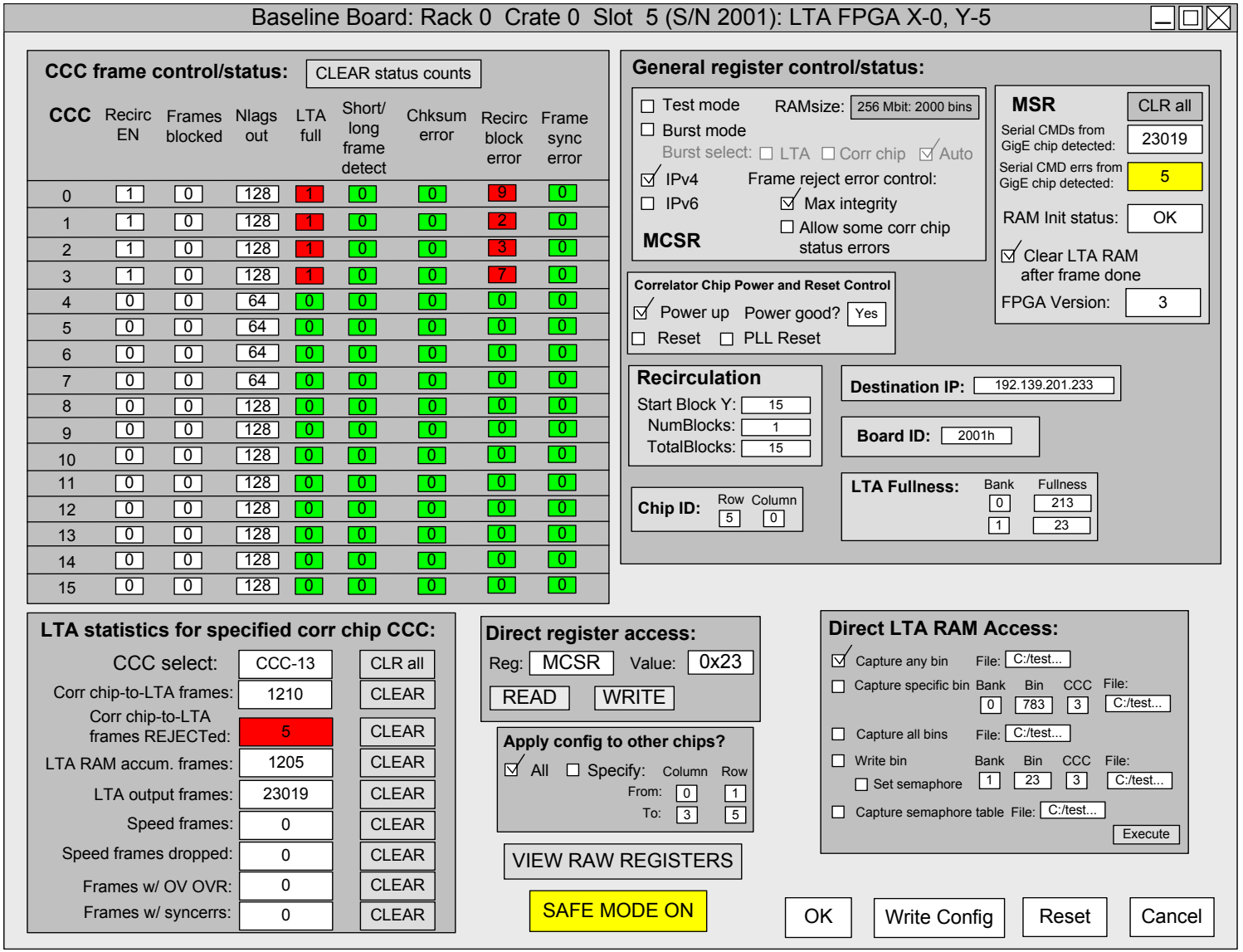

Figure 6 LTA Controller GUI.

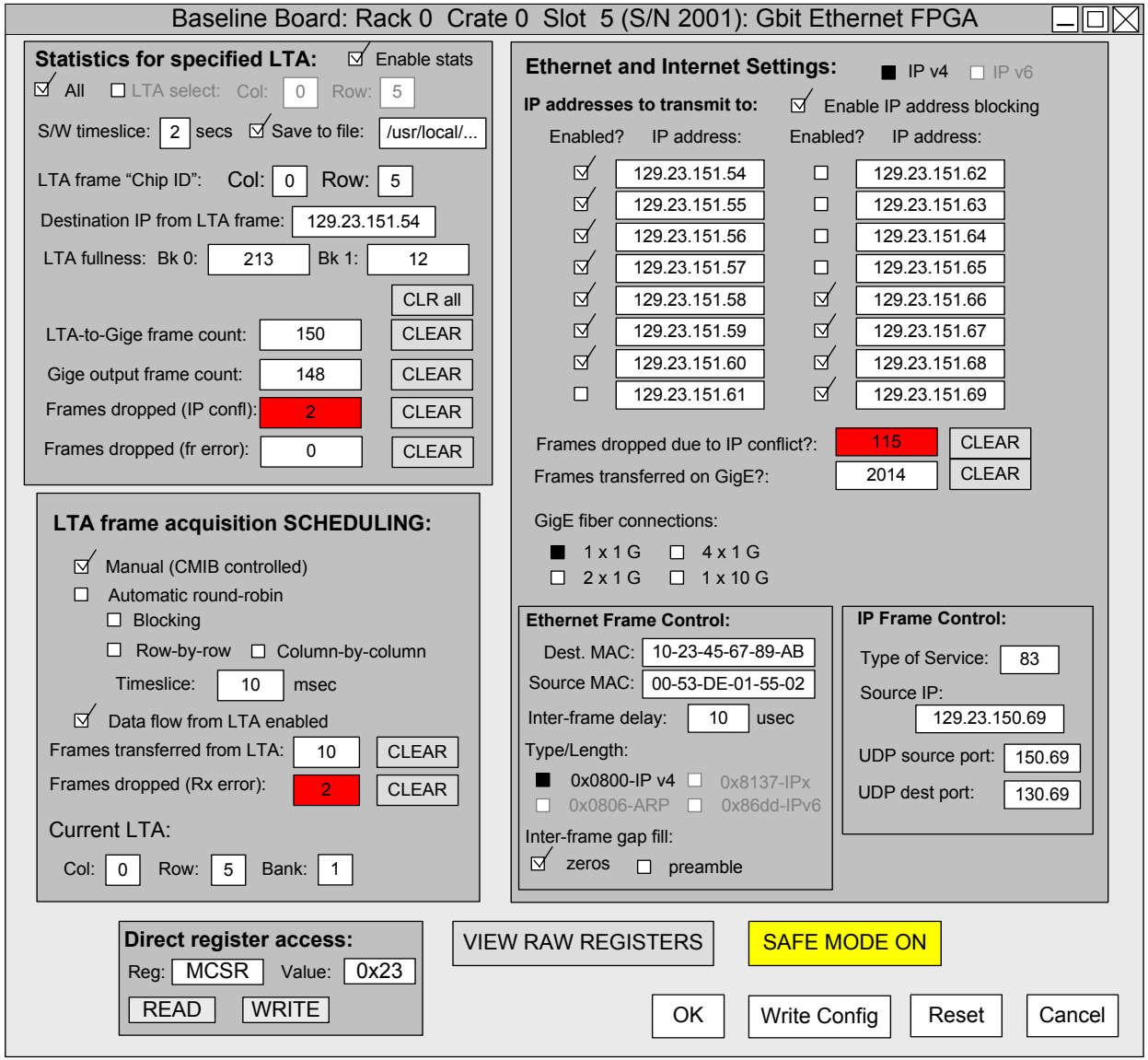

Figure 7 Gigabit Ethernet Chip GUI

6.5 Gbit/sec Ethernet (GigE) GUI

This GUI is used to provide frame reception, handling, and transmission statistics for the GigE chip, as well as Ethernet/IP/UDP control and status information. Some points to note on the GUI:

- The "LTA frame acquisition SCHEDULING" box allows the scheduling algorithm whereby the GigE chip visits each LTA looking for frames to transfer to the Backend (BE). If there is no manual mode built into software initially, then manual mode can be controlled by the GUI, or just not allowed at all. This box also provides some status information.

- The "Statistics for specified LTA" box allows the acquisition of frame statistics from a selected LTA to be acquired. There is also a software time-multiplexing feature that requires software support to implement.

- The "Ethernet and Internet Settings" box allows various fields in the Ethernet, IP, and UDP frames and headers to be set. It also allows configuration and monitoring of IP address blocking that is in place to minimize frame collision and dropped frames in external switches.

- SAFE MODE, VIEW RAW REGISTERS, and direct register access are also features of this GUI.

6.6 RAW REGISTER Display GUIs

It is often useful during debugging to be able to see raw displays of chip status and configuration information, and thus each chip has a raw GUI display as well. Figure 8 through Figure 11 are examples of these displays. The format of each is different since the output was taken from test bench data from chip testing—a consistent format should be developed for these displays. There is no direct register write capability in these GUIs, although this functionality might be useful.

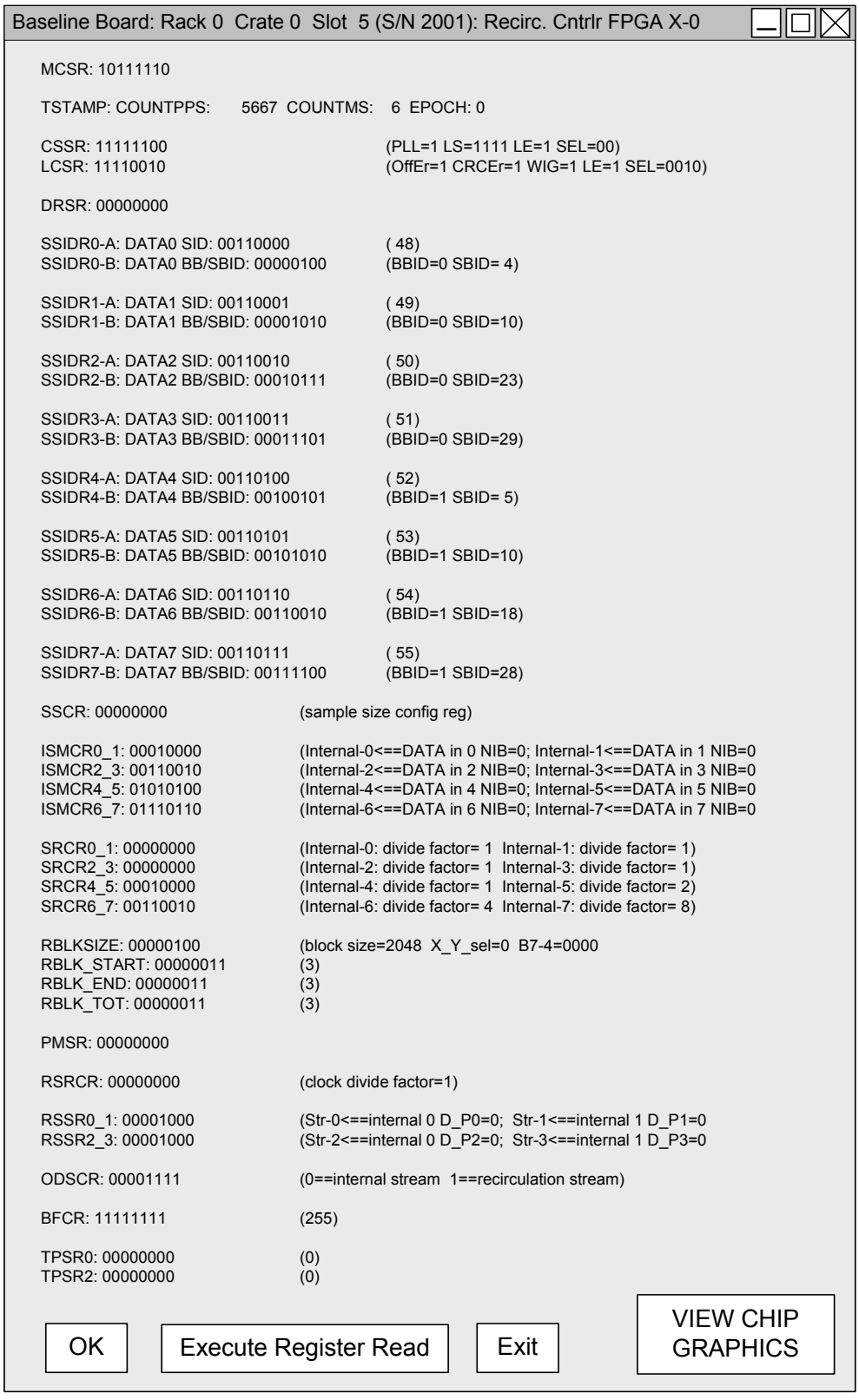

Figure 8 Recirculation Controller raw GUI display.

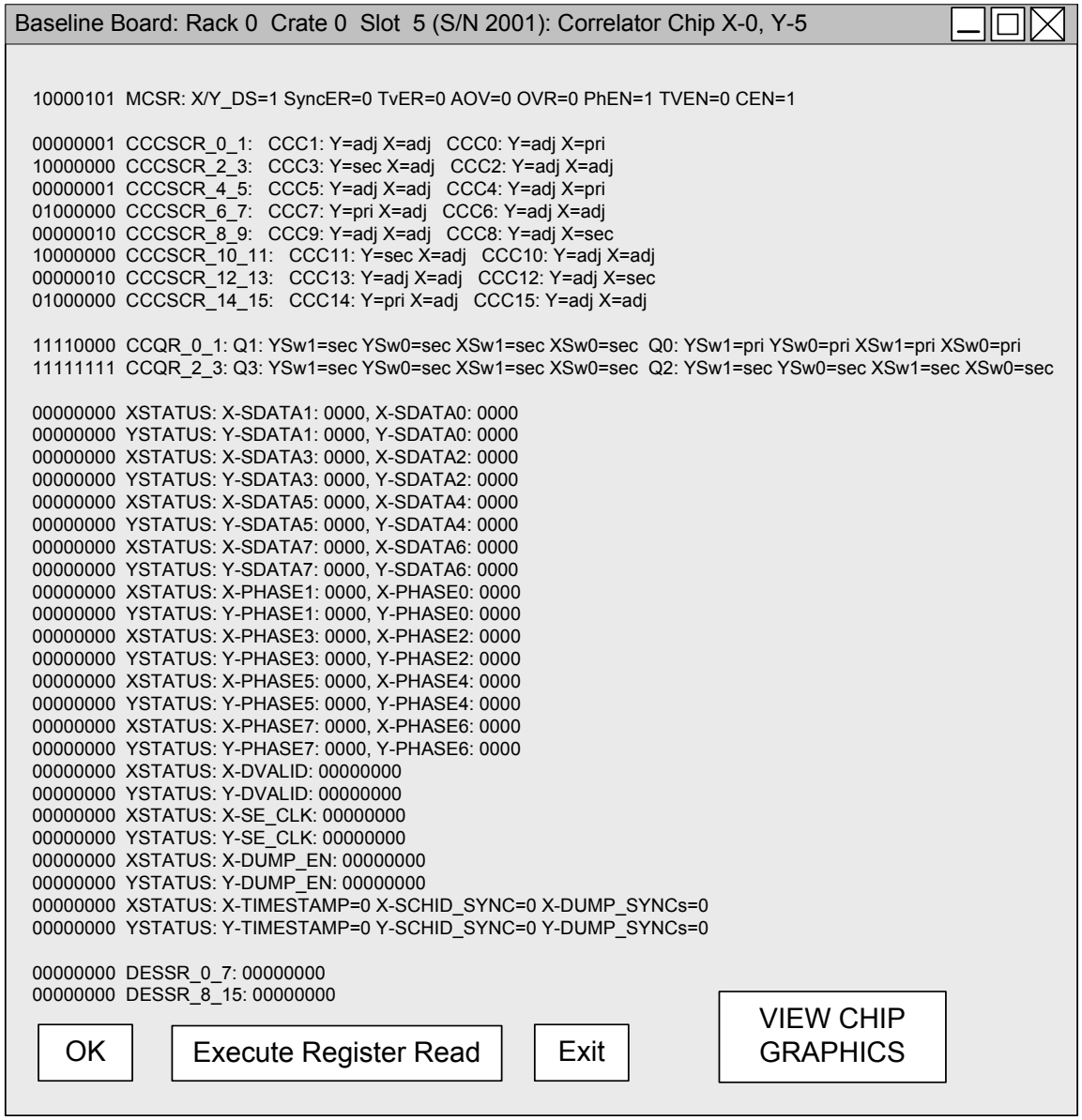

Figure 9 Correlator chip raw register GUI.

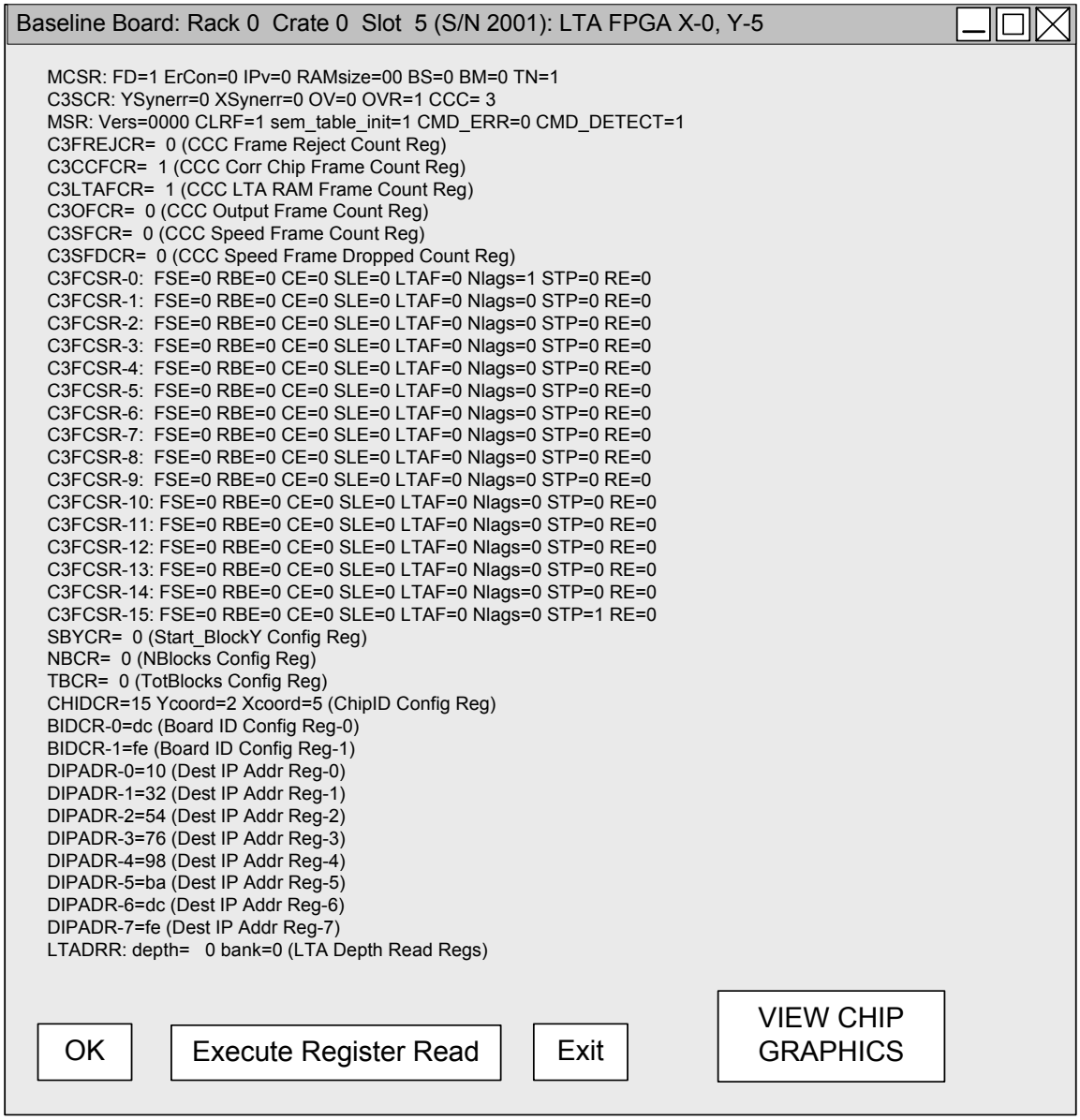

Figure 10 LTA Controller raw register GUI.

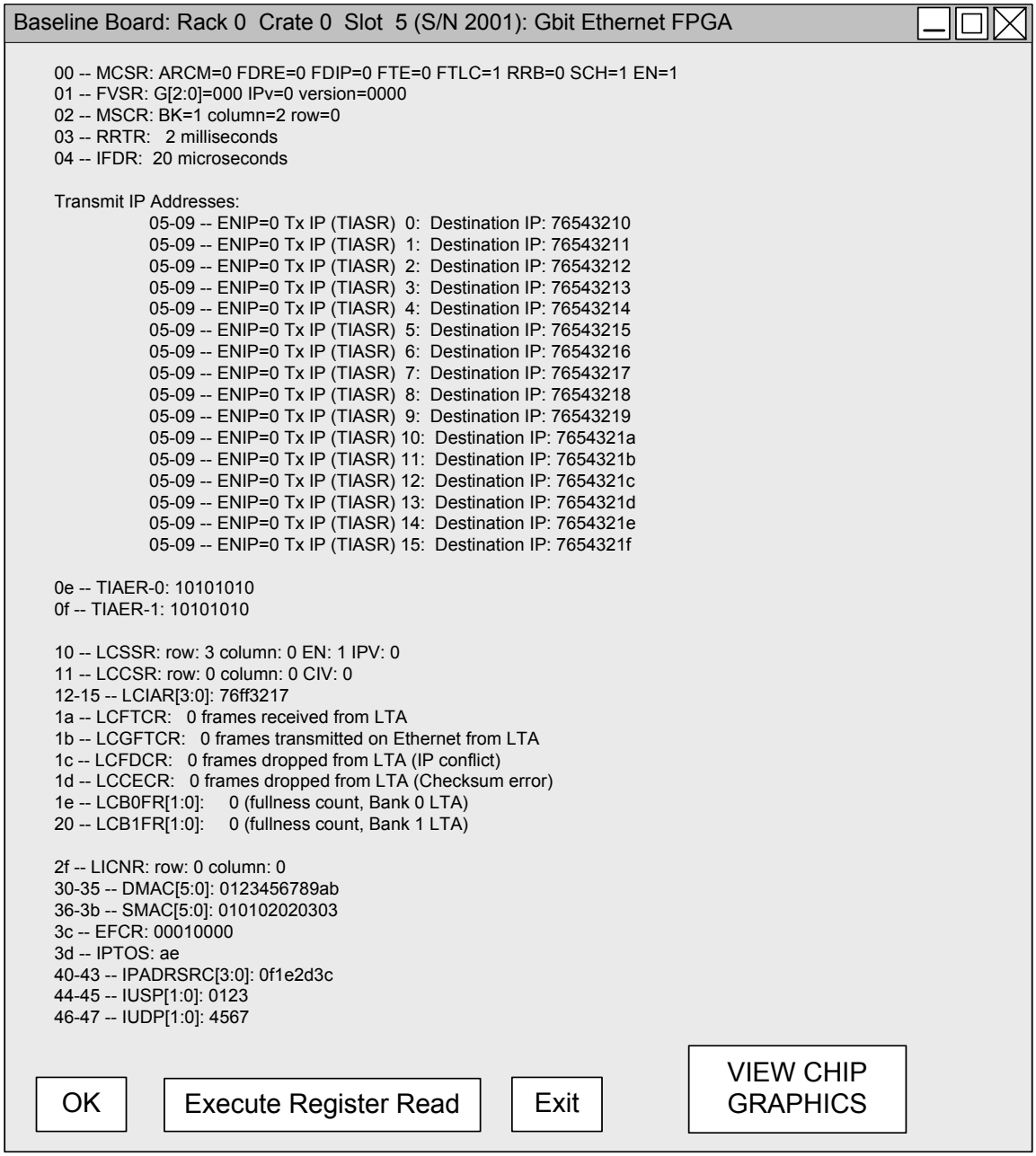

Figure 11 GigE chip raw register GUI.

6.7 General Board-wide GUIs

There are a few more GUIs that are accessible through the board-level "Config…" button. These are the "BB Configs…" and "HM Gbps Receivers…" GUIs. These are shown in Figure 12 and Figure 13.

The "BB Configs…" GUI is shown in Figure 12. This GUI is used to, in a manner similar to what the EVLA monitor and control might do across the VCI, set the BB configurations, polarization, and number of correlator channels. This GUI would thus be used to configure the Recirculation Controllers, and the correlator chips in one fell swoop. Note that integration time, number of bins, and pulsar binning are not set here because these parameters are a function of settings on the Station Board. "BB-0…7" refer to particular inputs to the board as per [7].

The HM Gbps receiver GUIs shown in Figure 13 are used, along with support software, to acquire accumulated status information for one receiver chip (Recirculation Controller) or all receiver chips on the board. It is possible with these GUIs to obtain long-term status information on the receivers—extremely useful during testing—as well as make some basic configuration settings. There is some overlap in functionality between these GUIs and similar functions provided on the Recirculation Controller GUI of Figure 4.

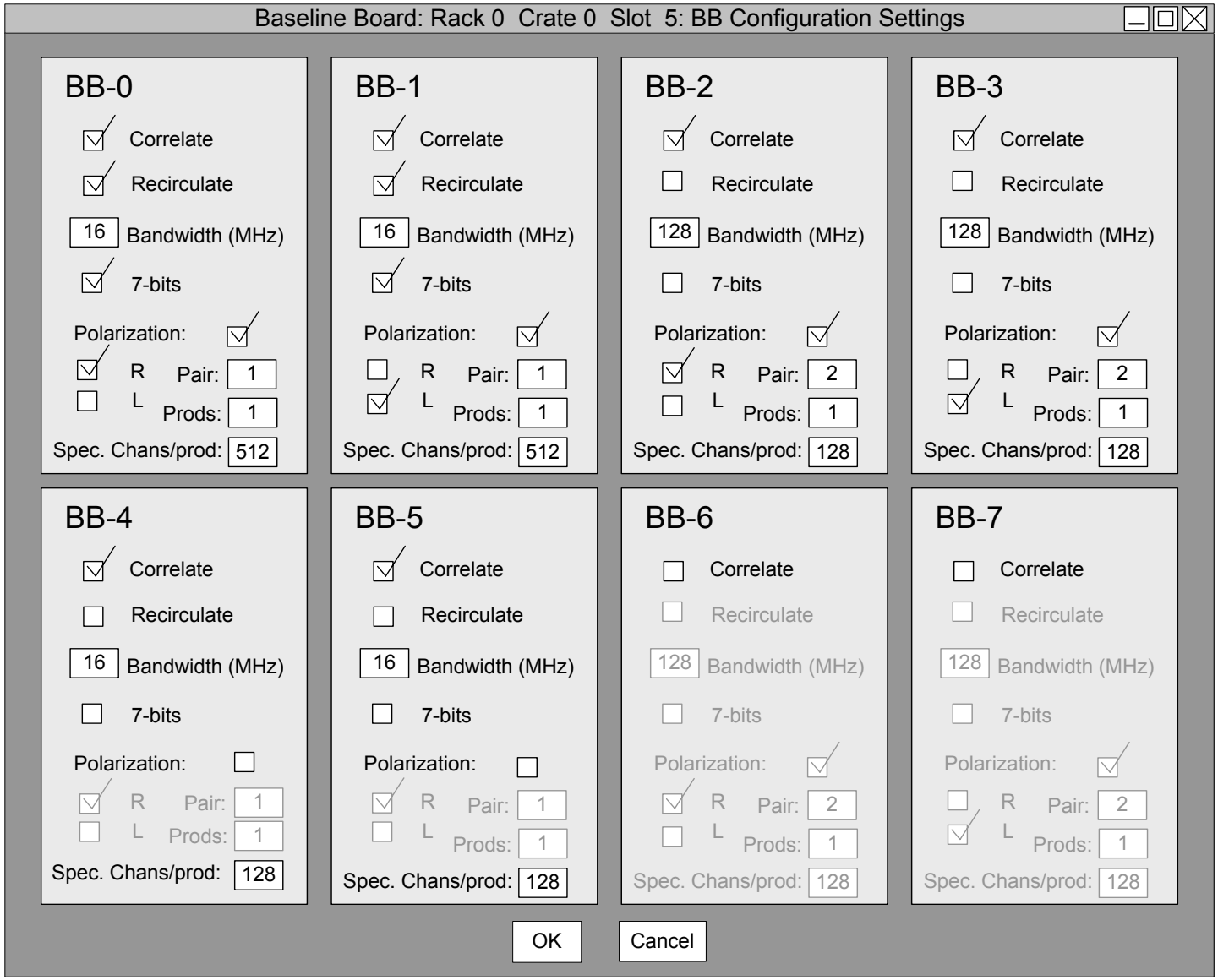

Figure 12 BB Configs GUI screen.

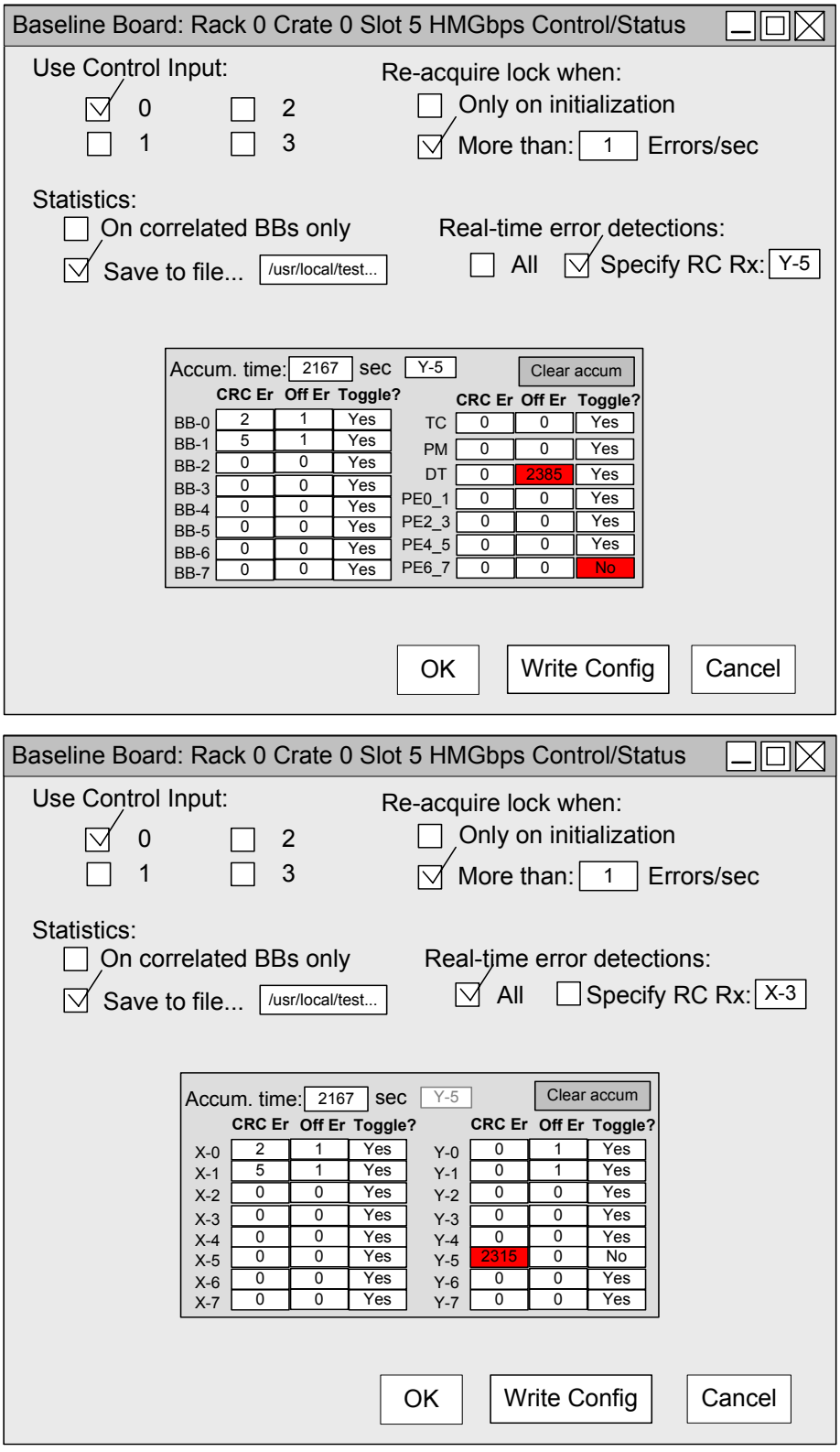

Figure 13 HM Gbps Receiver GUIs. Individual receiver chip (top) and all receivers on board.

7 Lab Power Supplies and Networking

7.1 Power Supplies

It will be necessary to supply –48 VDC power to the Baseline Board test bed for testing. This section presents a straw-man concept for supplying power to this test bed and other test beds in the lab.

The basic power supply setup is shown in Figure 14. A –48 VDC 100 A supply provides power to all test beds via a breaker panel. 15 A breakers in this panel allow one board to be powered off each breaker. In total, there should be ~10 breakers in the panel (not all boards will use the full 720 W capability of a breaker).

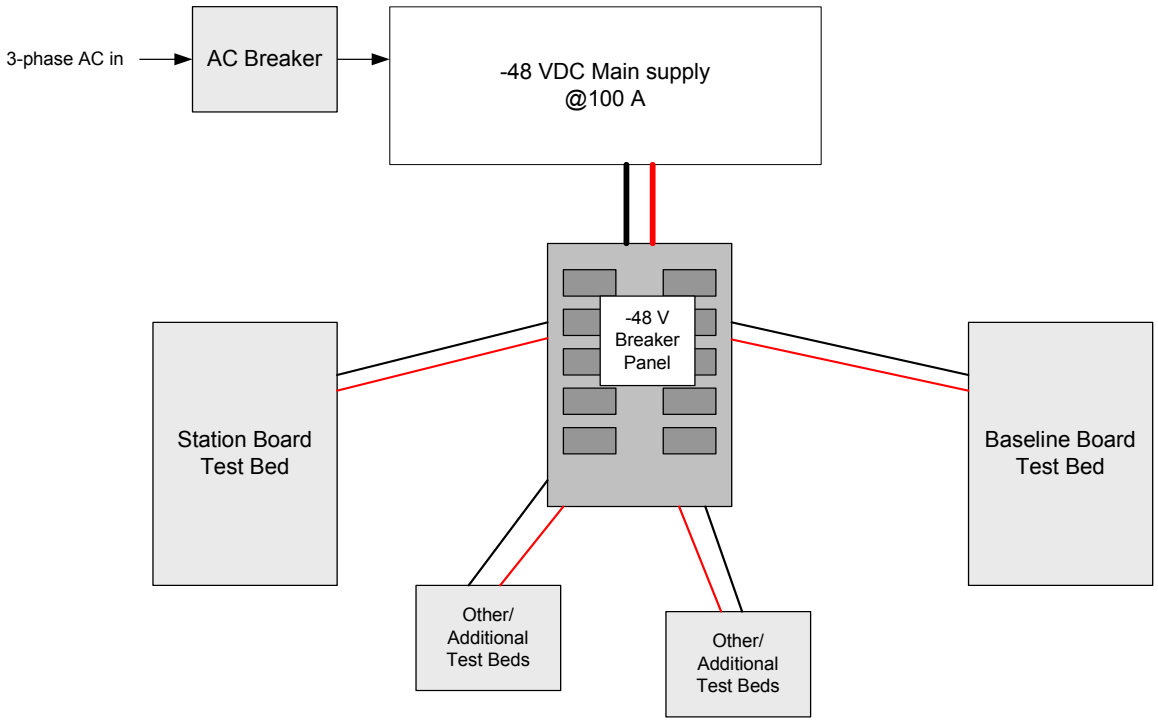

Figure 14 Straw-man concept for lab –48 VDC supplies to board test beds.

The power supply and breaker panel should be mounted in a quasi-permanent fashion near the center of the lab benches in the lab. If possible some standard 48 VDC keyed socket and plug should be used so that each board plugs into the breaker panel as an "appliance".

7.2 Networking

Notwithstanding other network diagrams in this document, a network diagram for the lab setup that encompasses more than the Baseline Board is shown in Figure 15. The following items in the diagram are of note:

- UUTs (Units Under Test) with 100M (100 Mbit/sec Ethernet on RJ-45) network connections can be one or more of Station Boards, NRAO-supplied Fiber-Optic Receiver Modules, or Timecode Generator Boards (TGBs).

- UUTs with 100M and 1G (1 Gbit/sec Ethernet on fiber) are Baseline Boards.

- The IP address for UUT is set partially in software and partially in hardware via the UUT "Common Backplane". Refer to [9] for more detailed information on board IP addressing.

- The SERVER Linux PC contains the PC/104+ boot files and FPGA bitstream files. When the PC/104+ CPUs boot, they will get all necessary boot files from this server.

- The SERVER Linux PC monitors and controls power for all of the UUTs. This CPU is thus functioning in a simple capacity as the CPCC (Correlator Power Control Computer). These lines are shown in red in the diagram.

- The SERVER Linux PC has a 1G backbone to the switch, although there are no extreme performance requirements for this test. A 100M connection would be fine, although it may be useful to gain some performance experience in the configuration shown.

- Three laptops are shown and these are to be used in the lab for rlogin and GUI access to UUTs. There may be a few more laptops than shown—perhaps up to 5.

- The "backend" Linux PC contains a 1G Ethernet card and is used for backend testing and reception of UDP/IP frames from Baseline Boards. The 1G switch does not need to be the highest performance switch available. A total aggregate throughput of a minimum of 1 Gbps, with a minimum of 4 ports is the requirement. A switch that blocks or drops frames if it is overloaded is acceptable since there are algorithms in the correlator that will work around these problems, and it is desired to test these algorithms in addition to flat-out performance capabilities.

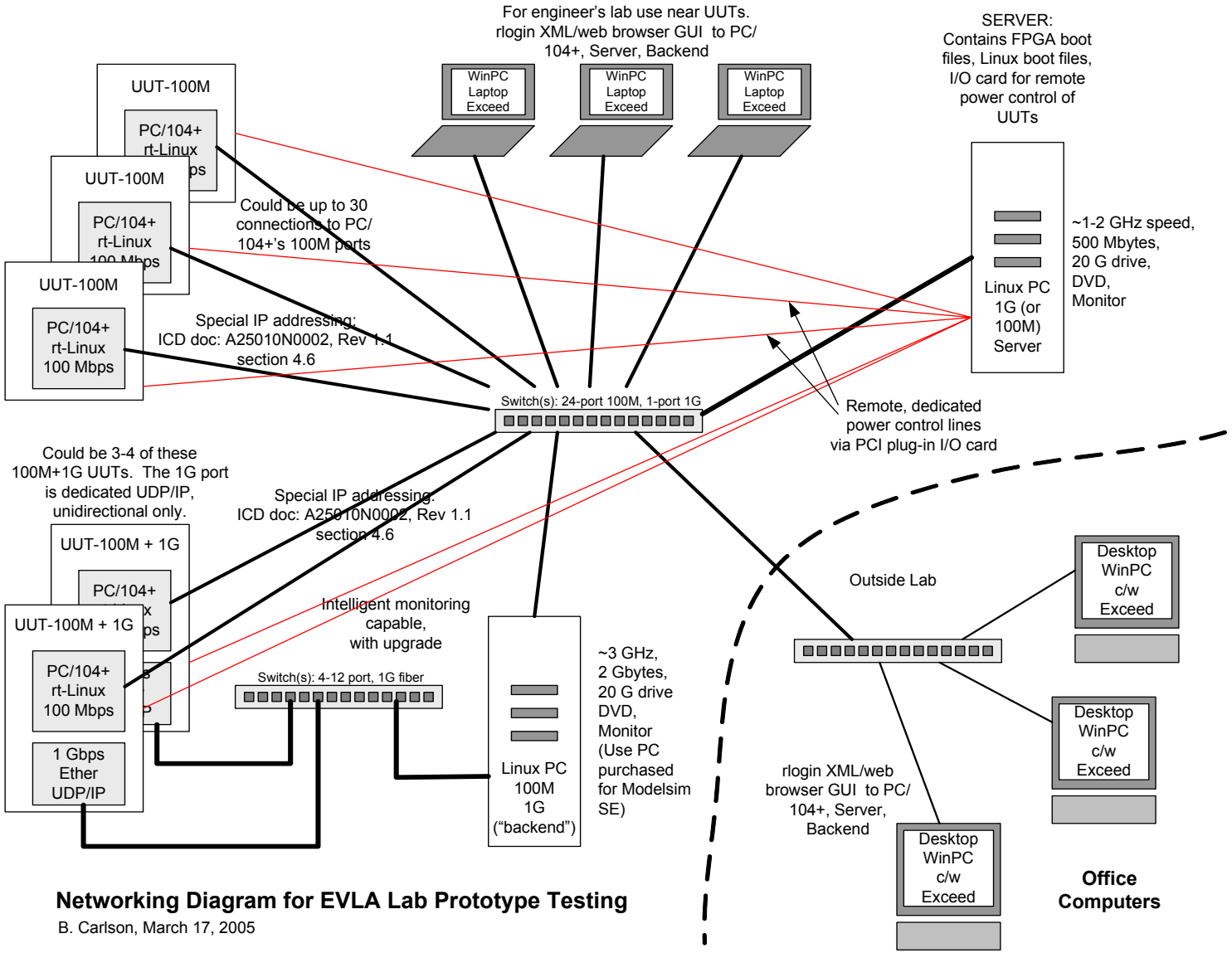

Figure 15 EVLA Correlator Lab Prototype Network Diagram.

8 References

All of these documents are available on the web at http://www.drao.nrc.ca/science/widar

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[5] Carlson, Brent, EVLA Correlator Project Development and Test Plan, TVP document A25010N0001, Rev. DRAFT, October 1, 2004.

[6] Carlson, Brent, EVLA Correlator Chip, TVP document A25082N0001, Rev. DRAFT, Aug. 26, 2004.

[7] Heng, Zhang, HM Gbps Cable Physical Specification, ICD document A25022N0040, Rev. Draft, April 13, 2004. Also, refer to: Carlson, Brent, HM Gbps Cable Signaling Specification, Protocol document A25022N0041, Rev. 1.1, Feb. 24, 2005.

[8] Smegal, Rick, EVLA Correlator Chip Functional Test Cases, TVP document A25082N0002, Rev. DRAFT 2.0, January 14, 2005.

[9] Carlson, Brent, EVLA Correlator System Numbering Plan, ICD document A25010N0002, Rev. 1.1, Feb. 24, 2005.