USER MANUAL

EVLA Correlator Baseline Board

User Manual Document: **A25080N0001**

Revision: 1.1

B. Carlson, February 10, 2012

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Table of Contents

List of Figures

List of Tables

List of Abbreviations, Acronyms, and Definitions

100Base-T – Refers to 100 Mbps ("Fast") Ethernet, running on twisted pair, using an RJ-45 connector.

1000Base-T – Refers to 1 G Ethernet, running on twisted pair, using an RJ-45 connector.

ASIC – Application Specific Integrated Circuit. In this document, it often refers to the Correlator Chip.

BGA – Ball Grid Array. Refers to the package/pin arrangement of integrated circuit chips.

BlB – Short form for "Baseline Board".

BlB Pair – Baseline Board Pair. In the EVLA, a pair of Baseline Boards are required to correlate all polarization products, for 32 antennas, 128 MHz/pol'n.

BB0, BB1 – The HM Gbps code stream which carries sampled DATA streams to the Baseline Boards.

CBE – Correlator Back End. Refers to the cluster of computers which accept and process Ethernet "lag frames" from Baseline Boards.

CMIB – Correlator Monitor Interface Board.

CompactPCI – An *n* x 3U Eurocard-based industrial computer standard. "U" refers to a standard rack vertical occupancy and is 1.75".

COTS – Commercial Off-The-Shelf.

CPCC – Correlator Power Control Computer.

DDR – Double Data Rate. Data is transferred on both the rising and falling edges of a clock.

DPA – Dynamic Phase Alignment. The Altera-FPGA scheme for automatically selecting and tracking the clock edge, in source-synchronous clocking/communication.

DUMPTRIG – The HM Gbps code stream which controls Correlator Chip integration.

Dynamic recirculation – When the Recirc FPGA recirculation "Start Block" and "End Block" are not equal, dynamic delays are put into the data stream path, which requires close control and synchronization with DUMPTRIG.

ERNI – One manufacturer of "2 mm Hard Metric" connectors.

FPGA -- Field Programmable Gate Array. XBB functions are implemented in FPGAs.

FPGA boot binary – Binary file generated by FPGA compile software, which gets loaded (booted) into the FPGA to enable the FPGA to perform designed functions. Also known as a "configuration" file or a "personality" file.

HM Gbps – Refers to the inter-board data transmission protocol used in the EVLA correlator system. Refer to A25022N0041.

IEEE 802.3 – The Ethernet frame standard, which defines the Ethernet frame (preamble, start, addresses, payload, FCS).

IST – Interconnect Stress Test.

jitter – Refers to randomization of arrival time of waveform edges from where they ideally should be.

JTAG – Joint Test Action Group, developer of IEEE Standard 1149.1-1990, a board connectivity test scheme, which does not require normal functioning of chips.

LISN – Line Impedance Stabilization Network. A standard power-line circuit to allow for standardized conducted EMI testing.

LED – Light Emitting Diode.

LTA – Long-Term Accumulator.

MCB – Monitor Control Bus. Refers to the simplified synchronous read/write CPU interface, used on the Baseline Board.

MCCC – Master Correlator Control Computer.

NVRAM – Non-Volatile RAM.

PHASEMOD – The HM Gbps code stream which carries antenna-based phase models to the Baseline Boards.

PHASERR – The HM Gbps code stream which carries phase corrections to the Baseline Boards, to implement sub-sample delay tracking.

PC/104+ -- Refers to an industry-standard embedded CPU form factor, which is a PC on a 3.5" x 3.5" card.

PCMC – PC/104+ Mezzanine Card. This card is part of the CMIB stack, and is sandwiched between the COTS PC/104+ CPU card and the motherboard.

RAM – Random Access Memory.

Recirc -- Refers to the Recirculation FPGAs on the board.

RFS – Requirements and Functional Specification.

RJ-45 – Registered Jack – 45. Standard 8-wire connector used in networking.

RXP -- Refers to one of two RXP FPGAs on the Baseline Board. "Re-timing", "X-bar", and "Phasing".

SDRAM – Synchronous Dynamic RAM.

SFP – Small Form Factor Pluggable.

Static recirculation – When the Recirc FPGA recirculation "Start Block" and "End Block" are equal, the recirculation memory introduces a static memory delay which does not require any interaction or synchronization with DUMPTRIG.

TIMECODE – The HM Gbps code stream which carries the current time epoch.

TSSOP – Refers to an integrated circuit package type, "Thin Shrink Small Outline Package".

UDP/IP – User Datagram Protocol/Internet Protocol. A connectionless, packet-based protocol defined by RFC 791 and RFC 768.

VDIF – VLBI Data Interchange Format. Refer to the GigE FPGA RFS A25092N0001 for more information.

W0/W1 – A distinct pattern inserted in the BB0, BB1 sampled DATA streams to help with receiver synchronization.

XAUI – Refers to a 10G Attachment Unit Interface, consisting of 4, 3.125 Gbps serial lanes.

XPAK – Expansion Pack; industry-standard form factor, for 10G Ethernet.

XML – Extensible Markup Language. ASCII-encoded messaging used for peer-to-peer communications.

1 Revision History

Revision	Date	Changes/Notes	Author
1.0	January 27, 2011	Initial release.	B. Carlson
1.1	February 10, 2012	Fix some bugs/typos. Add better description for D and P recirculation streams in the Recirc GUI. Also, add description for lag/lead lag acquisition using the Upper and Lower diagonals of the board (Recirculation FPGA GUI description).	B. Carlson

2 Introduction

This document is the User Manual for the EVLA correlator Baseline Board. This User Manual contains all relevant information necessary to understand the operation and behaviour of various board functions, determine various jumper settings and configurations, and understand in detail connector I/O, power requirements, cooling requirements, and physical attributes.

The functionality, register sets, pin-outs, and pin descriptions of the majority of custom-designed FPGA and ASIC chips that provide board functions are detailed in separate RFS documents, and most of this information will not be repeated here. These documents are:

- **RXP FPGA**: A25093N0000, Revision 2.1c or higher.
- **Recirculation Controller FPGA**: A25090N0000, Revision 3.1a or higher.
- **Correlator Chip ASIC**: A25082N0000, Revision 2.5 or higher.
- **LTA Controller FPGA**: A25091N000, Revision 2.3a or higher.
- **GBit Ethernet V2 FPGA**: A25092N0001, Revision 1.6 or higher.

These documents will be referenced heavily throughout this document, and only a relatively simplified description of each device will be provided.

The Baseline Board (**BlB** for short) is a double-sided surface-mount 12U x 400 mm card containing 87 FPGAs (F250 and F672 BGA packages), 64 standard-cell ASICs (F672 BGA), 32 dual-port static RAMs (DPSRAMs) (F256 packages), 64 512 Mbit DDR SDRAMs (in TSSOP-64 packages), as well as 12 48 VDC to LVDC ¼-brick power supply modules, a PC/104+ CPU mezzanine card, 2 SFP (or 1 XPAK) modules, and temperature and voltage monitor circuitry. The card is built to be mounted in a 24” (or 19”) rack-mount CompactPCI style card cage. The complete assembly also includes a monolithic heatsink weighing ~13.5 lbs, and so only card cages built to house this and the board load of ~8 lbs may be used.

The purpose of the BlB is to cross-correlate a sub-band pair, where each sub-band pair has a bandwidth up to 128 MHz per polarization, for up to 32 antennas. A single board can only cross-correlate ½ the number of polarization products required for 32 antennas, and so a pair of BlBs, fed with the same data in a daisy-chain fashion, is required to obtain all four polarization products. The board is not restricted to correlating just 32 antennas; for example, a pair of boards could correlate 1 polarization product for 64 antennas (same polarization hands both sides, for cross-hands, the Y-ERNI connector must be set for inputs—see section 8.6), 128 MHz bandwidth, or a board could correlate 16 antennas (1 board correlates all polarization products), or 8 antennas (1 board correlates all polarization products, at 4X bandwidth).

The board, using a pair of RXP FPGAs on each board, is able to produce phased-array (a.k.a. "tied-array") output, concurrently with cross-correlation, using *exactly* the same delay and phase models used for cross-correlation. Thus, when phasing-up the array, the solutions produced by the correlator on a calibrator source can be used directly to adjust delays and phases to get coherent phasing. The phased output may be routed to the on-board Correlator Chip array for auto-correlation or cross-correlation, at the same time routed to the X-ERNI connector for use by external hardware, and at the same time built into VDIF (a short description and reference on VDIF can be found in the GigE FPGA RFS A25092N0001) frames exclusively routed to the SFP2 Gigabit Ethernet port, or optionally, the SFP1 Gigabit Ethernet port.

Normally SFP1 and SFP2 ports contain COTS 1000BASE-T SFP modules, but could contain fiber SFP modules if desired. The GBit Ethernet FPGA does not support auto-negotiation, and is a fixed design for GigaBit Ethernet. There is an optional upgrade path to a single 10 Gigabit Ethernet port, and the board contains the XPAK cage to allow for this upgrade. The upgrade entails removing 8 resistors on the board, installing a 10G XPAK module in the XPAK cage, and using a separate 10G Ethernet FPGA binary, and slightly modified M&C software.

The board contains a "CMIB stack", consisting of a COTS PC/104+ (3.5" x 3.5") embedded CPU card running a real-time Linux OS mated with a PC104 Mezzanine Card (PCMC). This CMIB CPU provides an on-board intelligent monitor and control of the board, and communicates with the outside world using the XML protocol on Ethernet TCP/IP via an RJ-45 connector, currently set (by the choice of CPU card) for 100Base-T (100 Mbps). The PCMC, sandwiched between the PC/104+ and the BlB motherboard, provides a simple synchronous bus interface to 4 "MCB FPGAs" (U150-U153) on the board, which provide address decoding and bus fan-in/fan-out to allow the CPU read/write access to all read/writable chips on the board. The design of the chips, data paths, and signaling protocols do not require high performance from the CMIB or connections to the board; all correlation coefficient and phased-array data products are not handled by the CPU, and are transferred to the SFP (or XPAK) outputs without CPU intervention. This ensures minimal bottlenecks to output data flow such that using the 1 Gigabit SFP port allows all correlation products to be output for 10 msec integrations, and fewer correlation products to be output for even smaller integration times. The XPAK field upgrade path allows for even higher performance output.

The BlB power dissipation is 500 W maximum, all chips operating at the maximum bandwidth. The board is powered by dual independent -48 VDC inputs, although both inputs must supply power for full board operation. The inputs are each protected with 60 WVDC 1500 W transorbs, crow-bar protected with on-board 10 A fuses, to prevent voltage spikes from damaging the board's power supplies. Most board power-supplies are plug-replaceable ¼-brick Artesyn DC-DC converters, and contain integrated thermal overload and over-current protection. The board contains integral, redundant, dead man thermal-overload protection, and will automatically shutdown if the monolithic heat sink temperature exceeds 65 ^{o}C. The board requires sufficient airflow to keep it from reaching shutdown temperature, and with such airflow, can operate at an ambient temperature in the range from 0 to 40 ^{o}C.

2.1 Acknowledgements

The design, construction, test, and deployment of the Baseline Board has depended on the efforts of many people. Zhang Hang built the 100+ page schematic, spent long hours laying out the board, and always cheerfully responded to my requests to drill down to look at layers and make changes when requested. There were many challenges to successful layout, in particular dealing with all of the 1 Gbps differential lines, the 90 or so wires running from chip-to-chip in both horizontal and vertical directions, and just dealing with the shear complexity of the board. In the end, the design "just barely" fit and due to PCB mechanical limitations it is not possible to add a single layer of copper to the design. Mark Halman expertly designed the front panel, and heatsink, and ensured that the sub-rack and rack design could handle the mechanical load.

Kevin Ryan and Bruce Rowen (NRAO Socorro) are responsible for the successful GUI and CMIB code design and implementation respectively, and to do so required reading and digesting many pages of FPGA and ASIC design documentation, not to mention a huge number of hours of writing code, and iterating with the hardware designers and testers to get it working reliably. Bruce Rowen also contributed important information regarding CPU boot procedures to this document.

iSine Inc. was the specialty design house that implemented the ASIC design from RTL code. Their unique "specialty" approach, Lou Morales' and Gary Stevens' depth of expertise, and their patented Accel regulator technology, all fed in to make the ASIC low-power, affordable, and most of all, work as designed!

The PCB manufacturer, Merix, and the contract manufacturer, BreconRidge (now Sanmina-SCI), were essential to turn the design and vision of the board into reality. This is no small feat when you consider that the board has over 100,000 solder points, 28 layers, and 0.0035" "trace and space". Any single broken wire or bad solder joint could result in a non-working board.

Then there is the entire final assembly and test crew at DRAO in Penticton. Led by Ralph Webber, Dale Basnett, Pete Pelletier, and Shelley Deakin patiently and expertly ran all ~150 boards through the final assembly and test procedure, and so far, only a small number have had field defects that have had to be returned. Amy Fink's impeccable attention to detail when it came to working with BreconRidge to get orders placed, credit notices handled etc. ensured timely delivery of raw assembled boards.

Michael Rupen and Ken Sowinski (NRAO Socorro) have spent many hours working with the boards in the correlator at the VLA, patiently tracking down problems and providing feedback to the engineers to get bugs solved. Kerry Shores' (NRAO Socorro), patient and diligent installation and handling of the boards continues to ensure successful operation. Finally, there are many others who played important roles in helping to get the board to a final working state (or, asymptotically approaching a "final state"), the names of which are too numerous to mention here.

3 Context

A greatly simplified block diagram of the Baseline Board is shown in Figure 3-1 below:

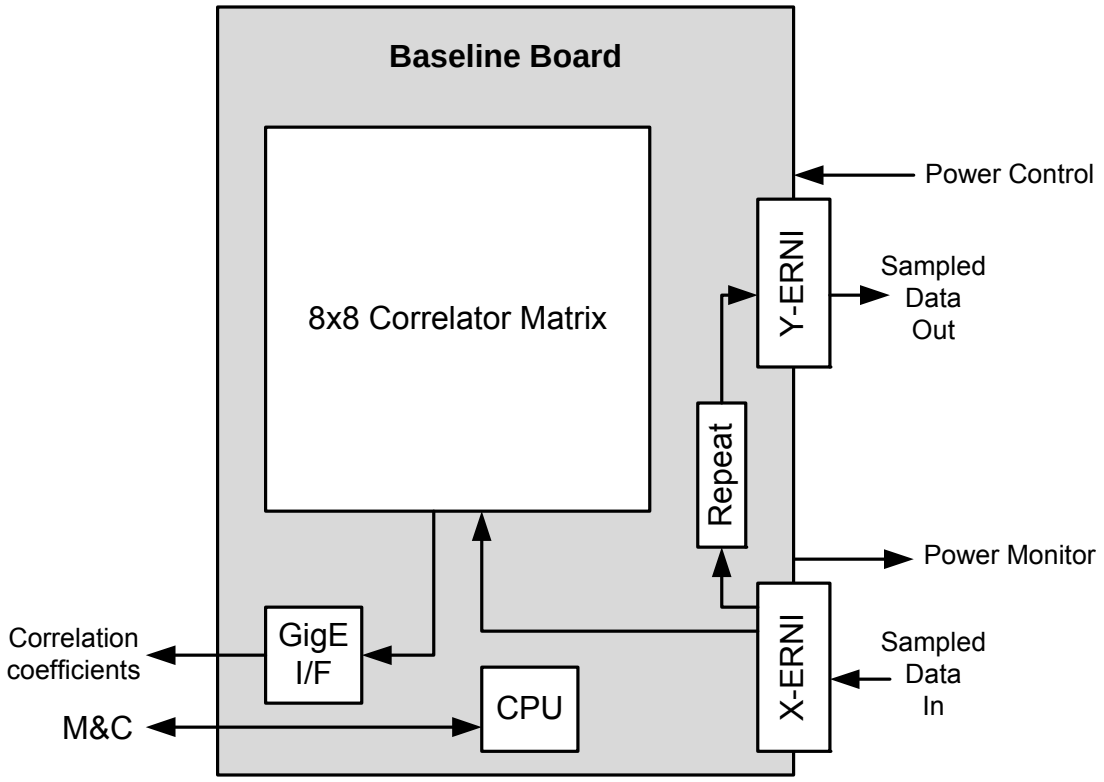

Figure 3-1 Greatly simplified block diagram of the Baseline Board.

There are 64 Correlator Chip ASICs on the board, 87 FPGAs, 32 static RAM chips, 64 DDR SDRAM chips, power supplies, and an embedded CPU module.

The X-ERNI connector is where real-time sampled data, clock, and control signals (on "wafers" using the "HM Gbps" protocol [1]) for 32 antennas enters the board, gets routed to the Correlator Matrix, and gets repeated out the Y-ERNI connector for use by a downstream daisy-chained board.

Correlation coefficients from the Correlator Matrix exit the board as IEEE 802.3 UDP/IP frames on Gigabit Ethernet. The embedded CPU runs a real-time Linux operating system, communicating with the outside world via TCP/IP and XML, and communicating with chips on the board via a simple synchronous "MCB bus" interface.

3.1 Simplified EVLA System Context

A simplified context diagram of the Baseline Board (BlB) within the EVLA system is shown in Figure 3-2 below:

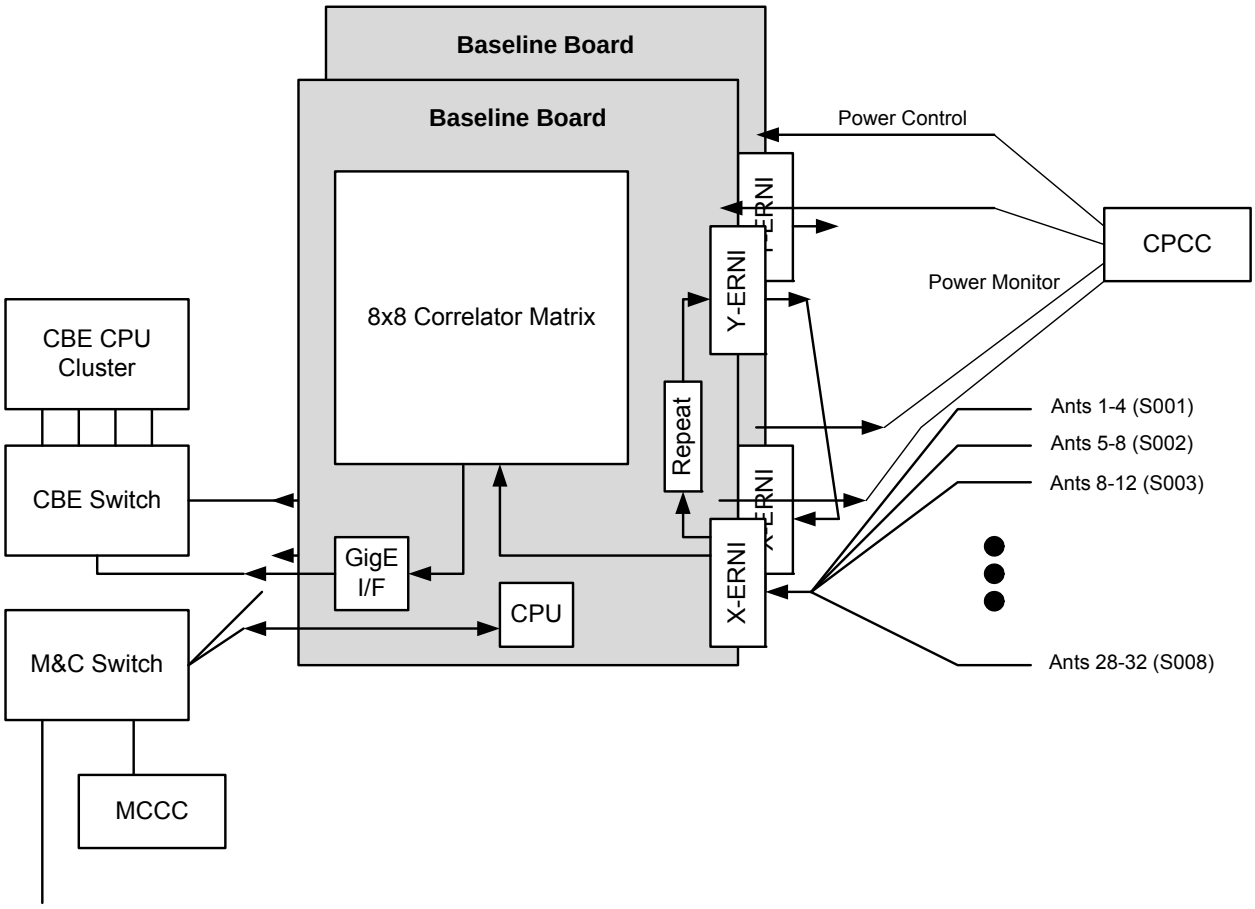

Figure 3-2 Simplified EVLA system context diagram. This shows a Baseline Board pair (BLB pair) fed with the same data from 32 antennas in a daisy-chained fashion. Not shown are the RXP/phasing connections or outputs.

Antenna data fed into the board, sources from Cross-Bar Boards [3] located in Station racks (S00x) numbered as shown. A BlB pair is fed the same data, in a daisy-chained fashion, and performs all cross-correlations, all polarization products, for a sub-band pair, where each sub-band can range from 31.25 kHz bandwidth to 128 MHz bandwidth.

The MCCC (Master Correlator Control Computer) sends configurations, and monitors status via the M&C Switch. The CBE (Correlator Back End) cluster receives and processes correlated data frames, distributed via the CBE Switch.

The CPCC (Correlator Power Control Computer) provides remote power monitor and control via TTL lines.

3.2 Simplified eMERLIN System Context

A simplified context diagram of the Baseline Board (BlB) within the eMERLIN system is shown in Figure 3-3 below:

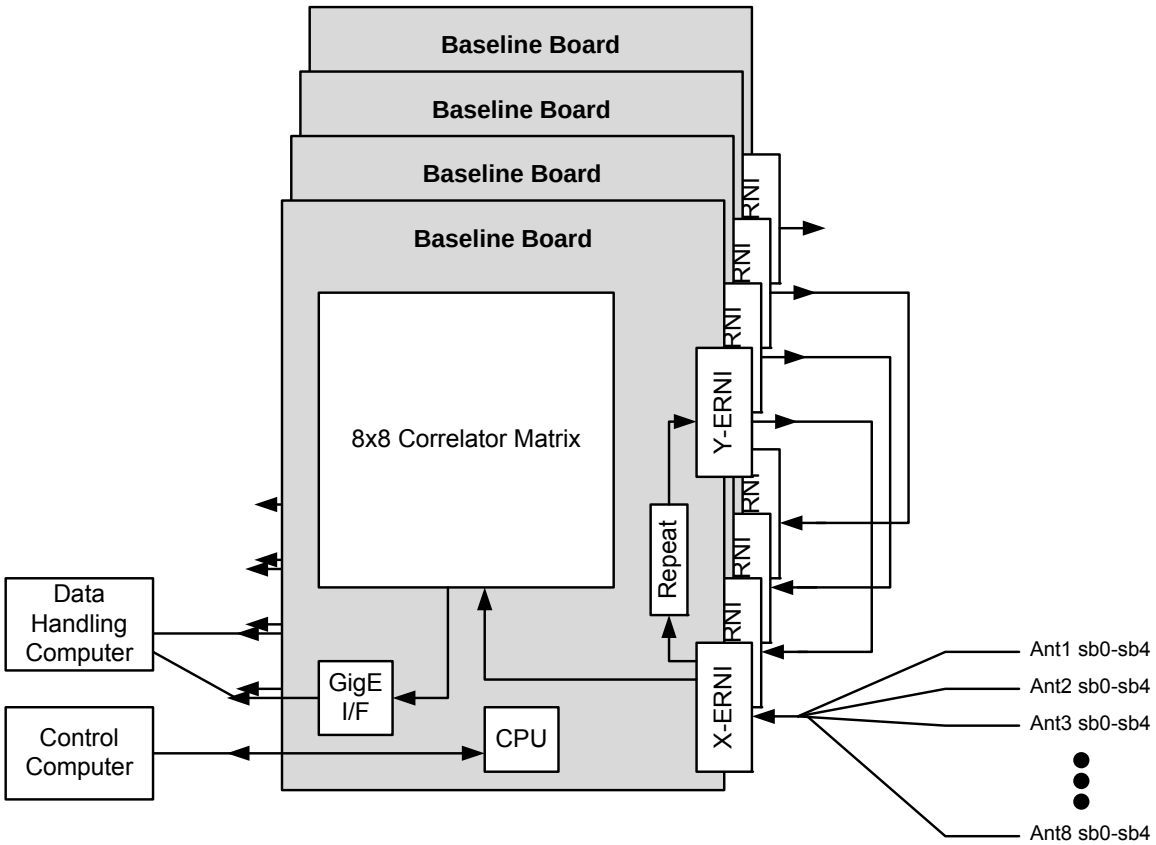

Figure 3-3 Simplified eMERLIN system context diagram. There are 4 boards in a daisy-chain, each fed with the same data, consisting of 4 sub-bands from 8 antennas. The total eMERLIN configuration consists of 4 sets of 4 boards configured this way. This configuration is used to provide 4X spectral channels compared to using just 1 board for 8 antennas, 4 sub-bands.

4 Overview

A simplified block/signal flow diagram of the BlB is shown in Figure 4-1 below:

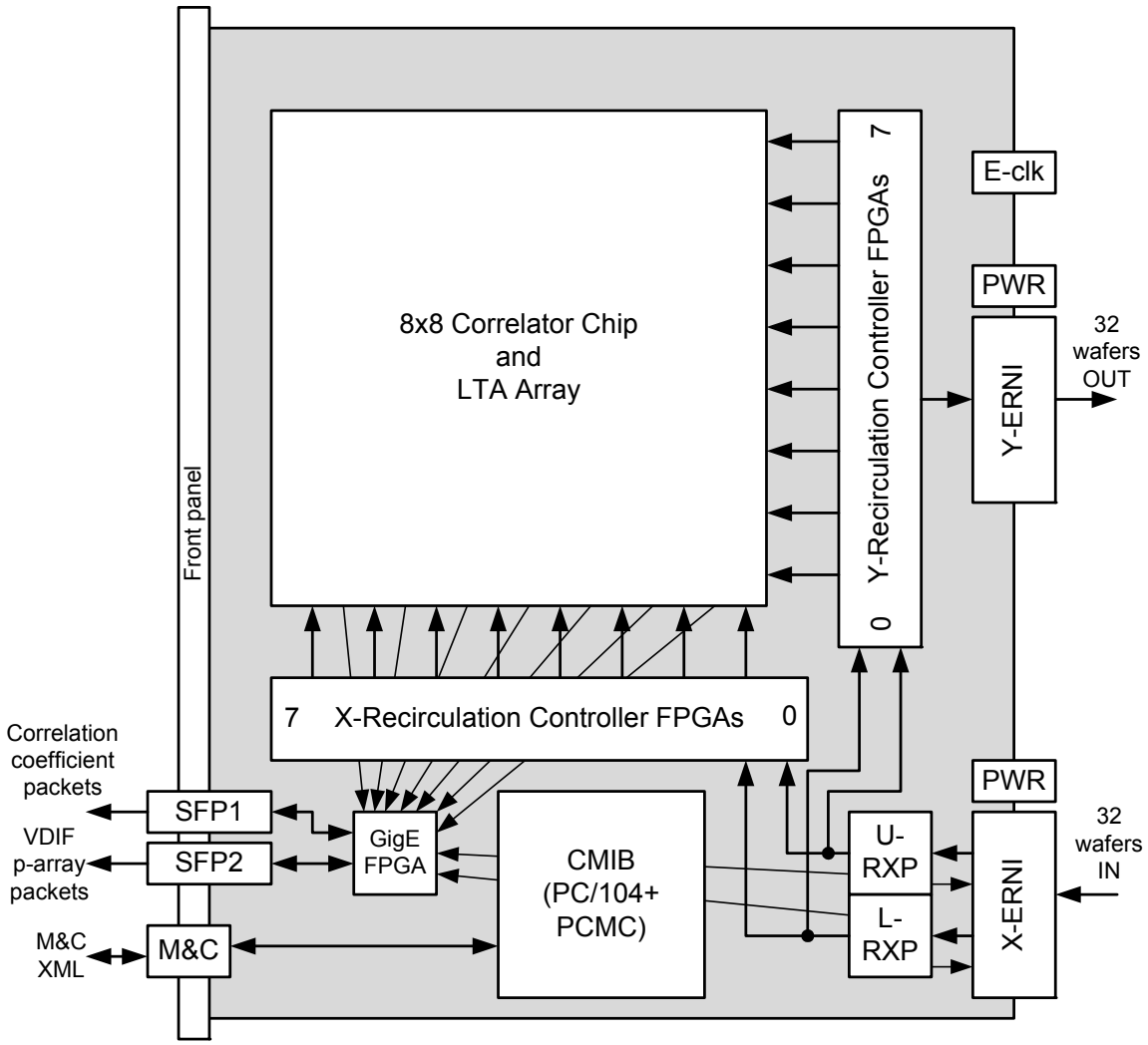

Figure 4-1 Greatly simplified Baseline Board layout/block diagram showing all major blocks/functions and data paths.

The functional blocks and data flow paths are as follows:

1) 32 wafers of data, control, and clock enter via the "X-ERNI" connector on the board and terminate at the U-RXP and L-RXP FPGAs. All these inputs are DC-coupled with single-leg 1 k-ohm bias resistors to 1.2 V. Each wafer contains a 128 MHz clock, a 1.024 Gbps control (CTRL) signal, and two 1.024 Gbps sampled data streams (BB0, BB1). The "**HM Gbps**" protocol describing the contents of these wafer signals can be found in [1]. The U-RXP FPGA gets its clock from input wafer 0 (top wafer of the X-ERNI connector), or the External

Clock ("E-clk" in the figure) input. The L-RXP FPGA gets its clock from input wafer 16 or the External Clock. All other wafer input clocks are ignored.

2) The U-RXP and L-RXP FPGAs, together, allow each FPGA access to all 32 wafers. Each RXP contains a full cross-bar switch to allow any of the 32 X-ERNI incoming wafers to be routed to any output, in the same 1.024 Gbps HM Gbps format, destined for the 8 X and 8 Y Recirculation Controller FPGAs. The U-RXP routes signals to X, Y Recirculation FPGAs 0-3, and the L-RXP routes signals to X, Y Recirculation FPGAs 4-7. Each X/Y FPGA of the same number gets identical data, since signal fanout is performed using 1:2 buffers on the board.

   Each RXP is also capable of phasing-up one sampled data stream of any or all of the 32 wafer inputs. Phased outputs can be concurrently routed to the Correlator Chip array (X/Y 3, 7); out two reserved wafers in the X-ERNI connector; and to the GigE FPGA using VDIF frames destined for the SFP2 (or optionally SFP1) GigE ports.

3) Each Recirculation Controller FPGA gets 4 wafers from either the U-RXP or the L-RXP. The Recirculation FPGA decodes the incoming signals, contains a full cross-bar switch to allow any incoming stream to be routed to any output data path, generates real-time phase coefficients for the Correlator Chips, performs any required recirculation functions (using external and internal RAM), decodes and generates dump control and timestamp information, and formats the data for transmission to the Correlator Chip array. There are approximately 90 wires leaving each Recirculation FPGA, destined for a Correlator Chip array row or column; data and phase wires operate at 256 Mbps each, and control wires operate at 128 Mbps each. For more information on this protocol, refer to the Correlator Chip ASIC RFS A25082N0000.

   The Recirculation FPGA also generates 8 phase-controlled, 32 MHz clocks, one clock for each Correlator Chip in the row or column. A clock phase calibration step is required to set the phases of these clocks for correct board operation.

   Additionally, Y-Recirculation FPGAs re-time the incoming 1.024 Gbps signals, and re-transmit them out the Y-ERNI connector for use (i.e. routing to X-ERNI connectors) by one or more companion boards connected in a daisy-chain[1]. With this mechanism, it is possible to stack boards in a daisy-chain for higher spectral-channel capability, as is done with the e-MERLIN system. All outputs are AC-coupled, with chip-side 1 k-ohm DC biasing to 1.2 V for the possibility that they might be used as inputs (see section 8.6).

[1] But note that there is a reversal of wafer numbers entering the second board in the daisy chain, due to routing restrictions on the interconnecting "Patch Board". For example, Y-7 Recirculation FPGA output, sourcing from the Lower RXP, routes to wafers 0-3 input of the Upper RXP in the second board.

4) Each of the 64 Correlator Chips performs up to 16 independent cross-correlations (128 lags per cross-correlation), with integration times up to 500 μsec before being sent to a companion LTA (Long Term Accumulator) FPGA for further integration. For more details on Correlator Chip and LTA operation and interfaces, refer to the Correlator Chip ASIC RFS and the LTA FPGA RFS. Each LTA FPGA is connected to a companion 512 Mbit DDR SDRAM, allowing for 2 banks of 2000 bins each for every correlation product. These banks are used as integration buffers for normal integrate-dump operation (and the more that are used, the more latency is allowed, and a bins for pulsar phase binning).

5) The GigE FPGA queries each LTA, via 8 serial daisy-chained, command/response lines to determine if data is ready for output. If so, the LTA transmits an "LTA Frame" to the GigE FPGA, which encapsulates it in an IEEE 802.3 frame within the UDP/IP V4 protocol, and transmits it out the SFP1 Gigabit Ethernet port. For details on these mechanisms, protocols, and frame formats, refer to the LTA FPGA and GBit Ethernet FPGA RFS documents (A25091N0000, A25092N0001).

6) The CMIB "stack" is an intelligent embedded PC/104+ CPU running a real-time Linux operating system, mated with the PCMC card providing an interface to the motherboard. It communicates with the outside world via a 100Base-T (RJ-45) connection, using the XML protocol. The CMIB in-system programs all of the on-board FPGAs via the PCMC, and communicates with all FPGAs via the 4 "MCB FPGAs" on the motherboard (not shown), using a simple address/data/control synchronous read/write interface running at 33 MHz. Each FPGA or ASIC on the board thus has a very simple 8-bit DATA interface, with varying numbers of address bits depending on addressing requirements.

   The PCMC card contains a multi-channel 8-bit A-to-D converter, to allow the CPU to monitor board voltages and temperatures. For further details on the PCMC card, refer to the PCMC RFS [2].

Not shown in Figure 4-1 is all of the ¼-brick power supplies needed for all the chips. The board contains power supplies providing, +5V, +3.3V, +2.5V, +1.8V, +1.5V, +1.2V, and +1.02V. All FPGAs are provided bulk power (i.e. multiple FPGAs hang off a single power supply), however each Correlator Chip ASIC has its own POL (Point of Load) regulator, called the "Accel" regulator chip. There is a closed-loop connection between the Accel chip and the ASIC, such that the ASIC is provided only with enough voltage to maintain required speed operation, and this voltage is nominally +1.02 V, but ranges from ~0.95V to 1.10 V, depending on each ASICs inherent process speed. All bulk power supplies can be remotely controlled (and monitored) with TTL-level signals via contacts in the "PWR" connectors, so it is possible to remotely power-cycle the board. Accel regulators are controlled via LTA FPGAs.

A photograph of the FRONT of Baseline Board, without the heatsink attached, with annotation showing major components/blocks is shown in Figure 4-2:

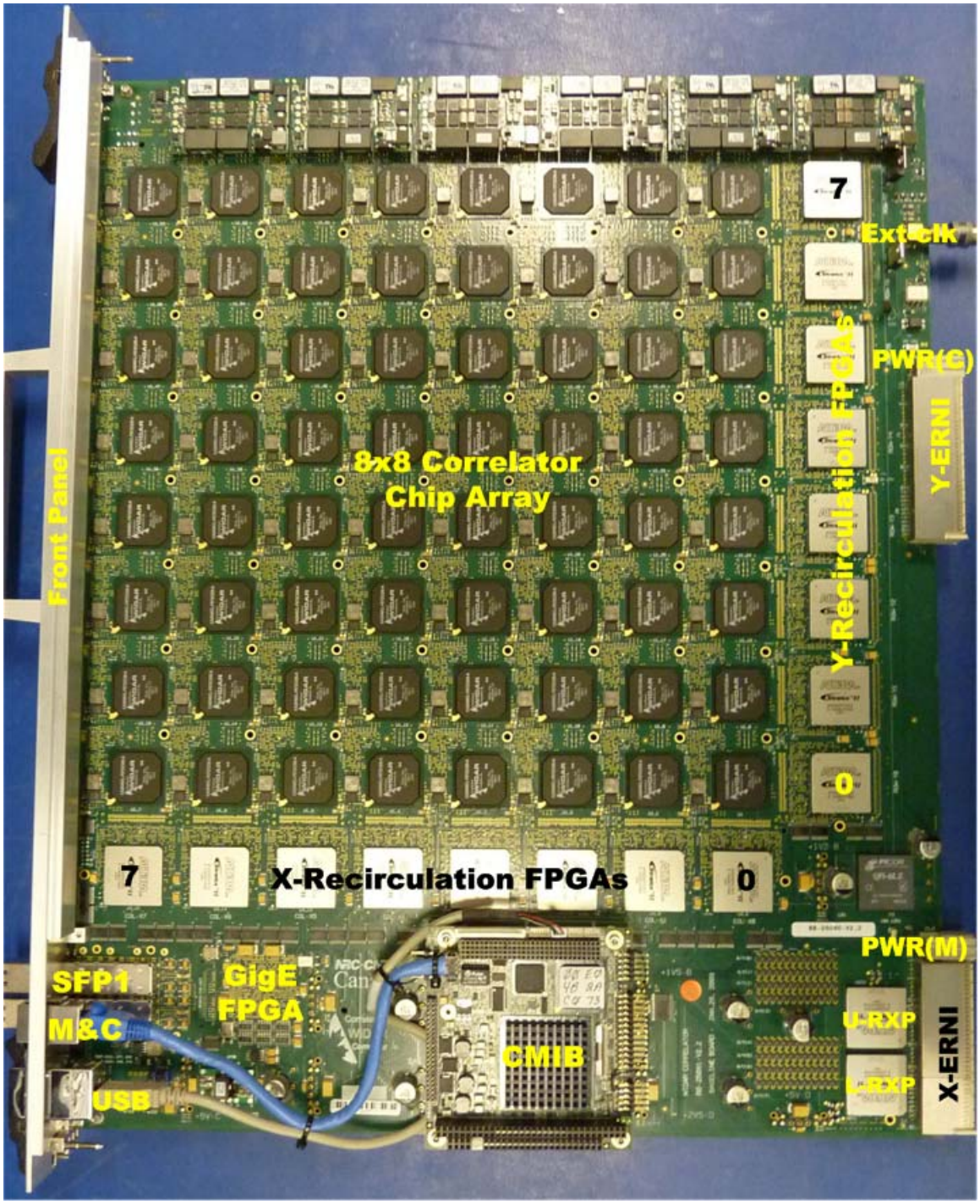

Figure 4-2 Photograph of the FRONT side of the Baseline Board, without heatsink.

A photograph of the REAR of Baseline Board, with annotation showing major components/blocks is shown in Figure 4-3:

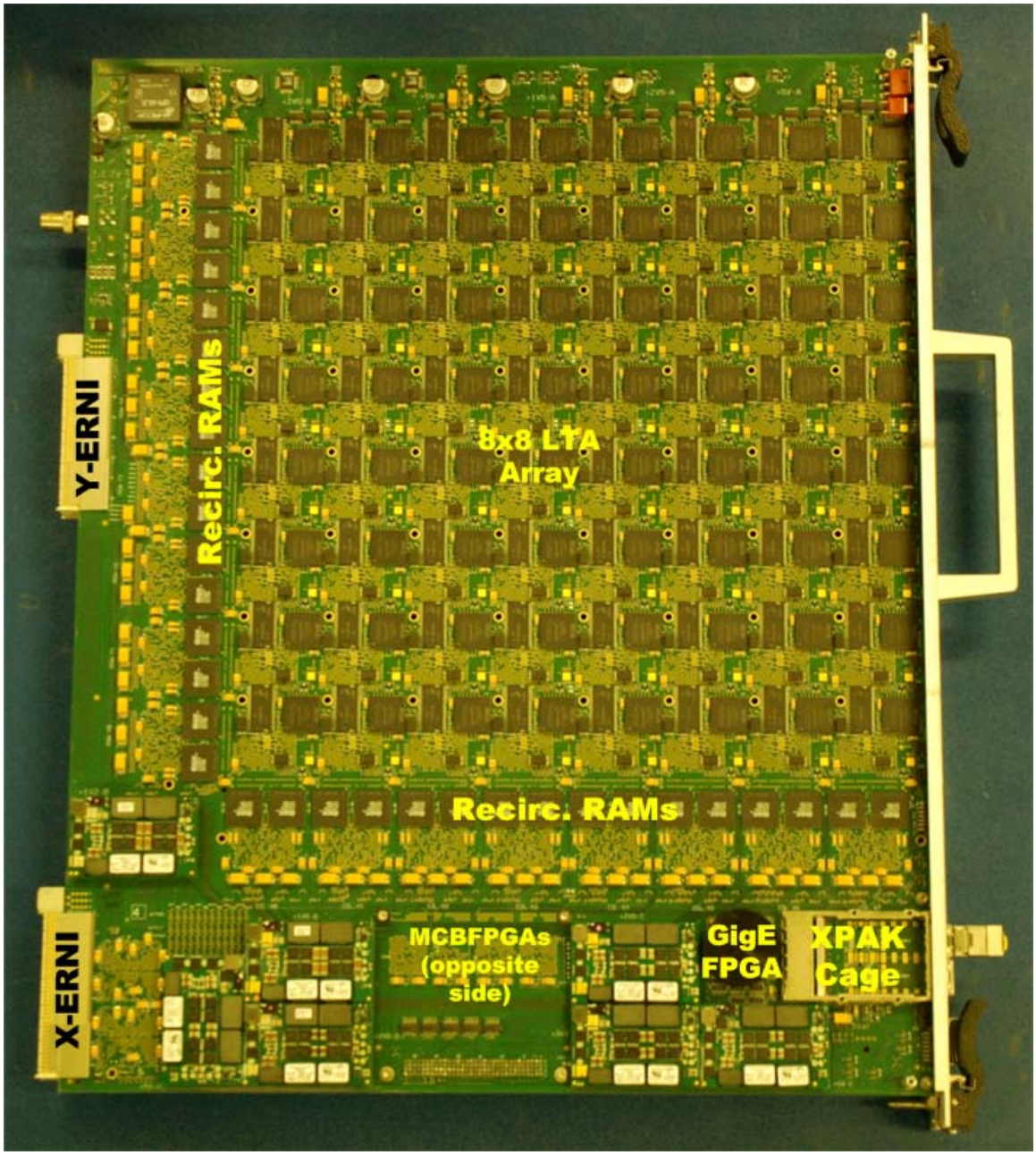

Figure 4-3 Photograph of the REAR side of the Baseline Board.

A photograph of the FRONT PANEL of Baseline Board, with annotation showing major functions/ports is shown in Figure 4-4:

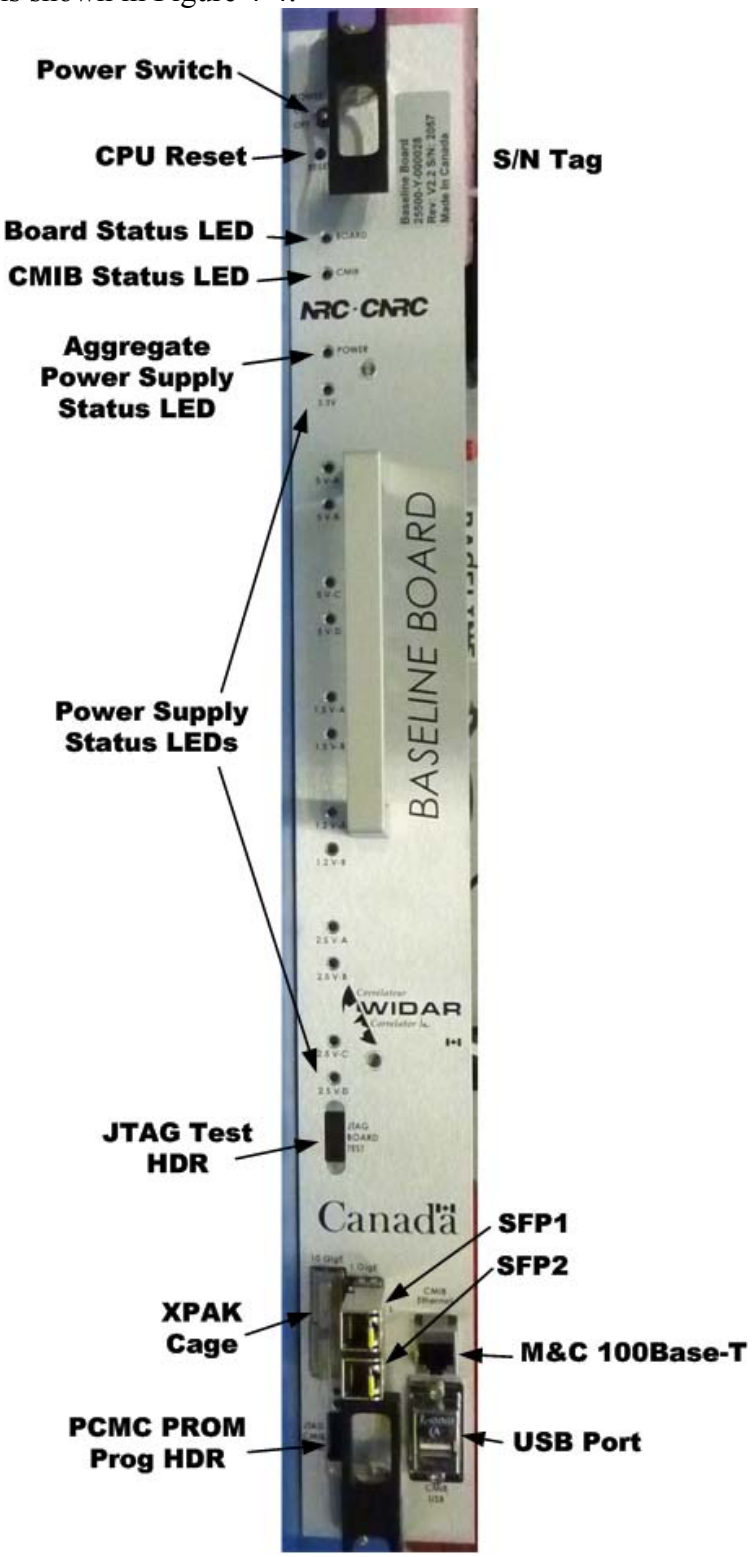

Figure 4-4 Photograph of the FRONT PANEL of the Baseline Board.

The Power Switch controls the enable lines of all of the power supplies on the board, and does not actually switch -48 VDC.

The CPU Reset is a recessed push-button switch that resets the PC104 CPU module if pressed.

The Board Status LED, when the board is fully booted and running normally, flashes green for ~100 msec, once per 1 second tick derived from the HM Gbps input TIMECODE signal. This is a CPU-driven function, and so if the CPU is not functional, this LED will be off/dark.

The CMIB Status LED is solid green once the CPU has booted successfully.

The Aggregate Power Supply Status LED is green if all of the on-board power supply monitor lines indicate that power supplies are good, and is off/dark if any single power supply monitor line indicates power supply fail or out of range.

The Power Supply Status LEDs indicate window-comparator measurements of each of the on-board power supplies, referenced to the single +3.3 V supply. If a particular LED is green, it indicates that that particular power supply output is within the required range. If a particular LED is off/dark, it indicates that that particular power supply output is out of range—which may mean its output voltage is too LOW or too HIGH.

The JTAG Test HDR is for manufacturing JTAG test of the board. Note that due to dual-use of the JTAG signals, and filters soldered after testing, this header and the JTAG test function, can never be used.

The XPAK Cage is the empty cage (slot) where a 10G XPAK module could be installed if it is desired to upgrade the board's output data rate to 10G from standard 1G. Doing this requires removal of resistors on the board, and use of the GigE FPGA 10G FPGA binary. Refer to section 8.5 for more information.

The PCMC PROM Prog HDR, is a 14-pin, 2 mm header used for programming the PCMC module's FPGA PROM. Normally, programming the PCMC PROM is required only to initialize it, or if the PROM gets corrupted and can't be programmed via the CPU interface.

SFP1 and SFP2 are the two 1 GigE 1000Base-T ports; SFP1 for correlation coefficients (and optionally VDIF frames from RXPs), and SFP2 for VDIF frames exclusively.

The M&C 100Base-T connector is for the 100 Mbps Ethernet connection to the PC104 CPU module.

The USB Port connects to the PC104 CPU module's USB interface.

5 Functional Description

This section contains a functional description of the board, borrowing top-level diagrams from the various FPGA and ASIC RFS documents, and providing simplified descriptions of main board/device GUI panes, as these GUIs are the main user interface for a top-level user. The functional description roughly follows data flow through the board.

5.1 Top-level Board GUI Description

This section contains a description of the top-level Baseline Board GUI, the layout of which maps closely to the functionality, layout, and data flow of the board. The description is limited to helping to explain board functionality rather than being an exhaustive description of all GUI capabilities. The XML protocol used to communicate with the board CMIB is defined in:

http://www.aoc.nrao.edu/asg/widar/schemata/cmib/baselineBoard/baselineBoard.html

The top-level GUI, running on any JAVA browser, communicates with the CMIB via XML in the same way as any application. Refer to Figure 5-1 for the following bulleted description.

A Icon representing both Upper and Lower RXP chips. If the LED is RED, then there is some input wafer receiver that is not locked or has detected an error. If GREEN, then wafer locked is achieved on all input wafers.

B Icon representing a single Recirculation FPGA. If the LED is RED, then there is some input wafer receiver that is not locked or has detected an error. If YELLOW, the chip is set to generate PRN Test Vectors. If GREEN, all input wafers are locked, no errors have been detected since the screen was last refreshed, and the chip is in normal mode.

C Icon representing a single Correlator Chip. LEDs indicate input signal error detectors; GREEN is the no error condition, RED is the error condition. The core voltage that the chip is running at is displayed in this icon, and it is acquired using dual on-board analog switches, controlled via the Y7 Recirc FPGA (refer to section 7.3.2). This core voltage should be between 0.90 V and 1.18 V. If the chip is set for active cross-correlation, the letters “CC” are in the middle of the chip; if set for auto-correlation, the letters “AC” are present. If not correlating (correlation disabled, or set for Test Vectors “TVEN”=1), then the chip box outline is YELLOW. If the chip box outline is RED, the CPU can’t talk to the chip on the MCB bus.

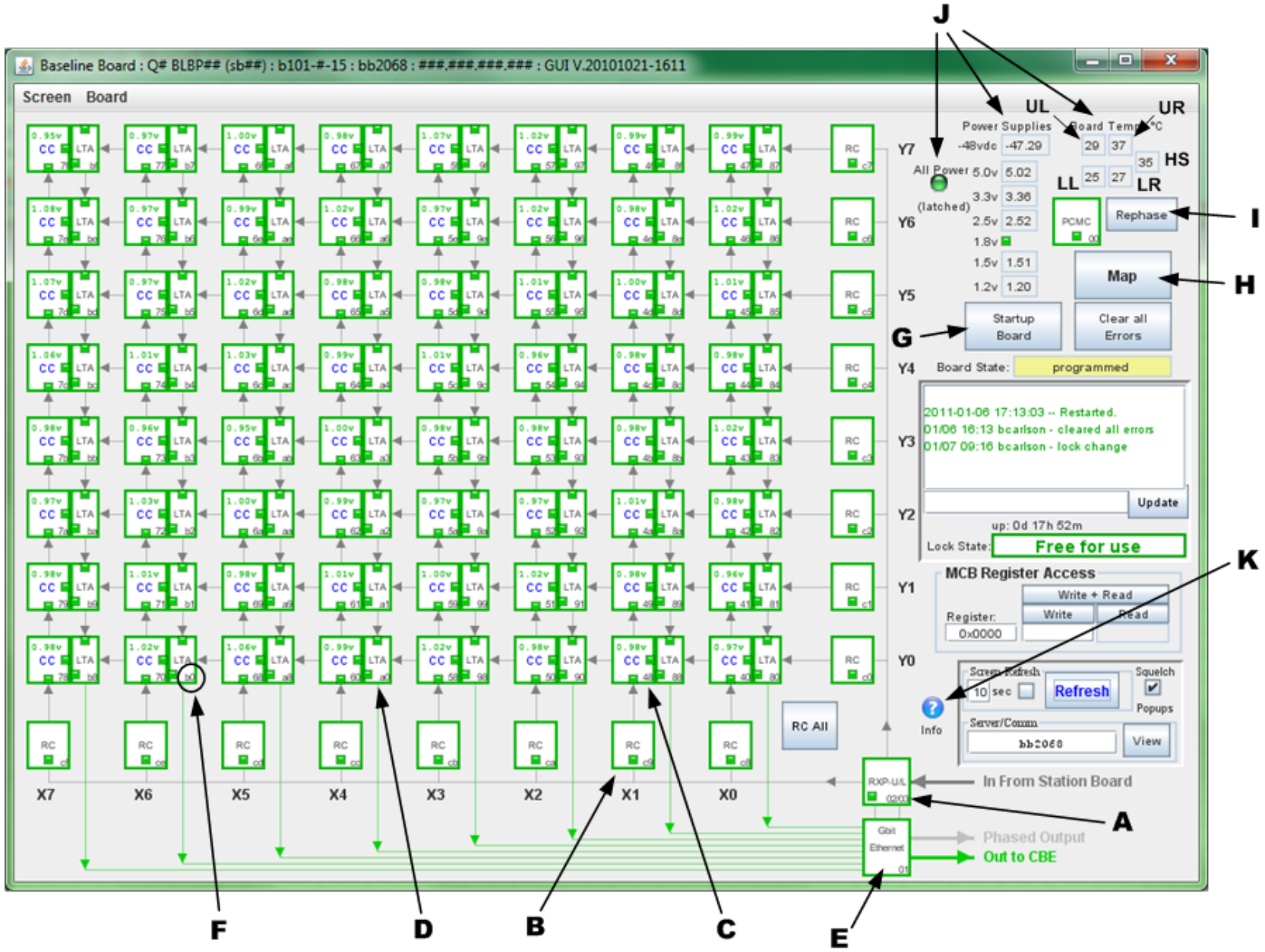

Figure 5-1 Baseline Board top-level GUI.

D Icon representing a single LTA FPGA. The top LED indicates the toggle status of the data flow from the previous chip in the daisy-chain. The left LED indicates the toggle status of data from the Correlator Chip. If either LED is RED, then the CMIB is indicating that there is some fault in a data line; if GREEN, data is flowing and all lines are toggling. If GREY, no data is flowing, but it is not expected to be flowing and is not a fault condition.

E Icon representing the GigE FPGA. The color of lines in and out indicate data flow status; GREEN=data is flowing, no faults; RED=data might/should be flowing, but there are faults; GREY=no data is flowing/data is not expected to flow.

F At the bottom-right corner of each chip icon on the board is a 2-digit hexadecimal number. This is the upper 8 bits of the MCB address of the chip. For example, to address register 1 of the X6,Y0 LTA GUI, the complete address is 0xb001.

G This icon, when pressed, brings up the "Startup Sequencer" GUI for the board. Normally in the system, startup is automatic, but for testing it can be run manually step-by-step with this GUI. The board is started up, in sequence, executing items from top to bottom in the GUI.

H This icon, when pressed, brings up a complete map of the configuration of the board.

I This icon, when pressed, causes CMIB software to re-run Correlator Chip clock phase calibration. Once calibration is complete, any affected devices are set to their previous configuration.

J This section of the board is used to indicate board power supply voltages and temperature sensor temperatures. All of these measurements are obtained with the use of the A/D converter on the PCMC module. As there are multiple board power supplies for a given voltage, the voltage measurement represents the average voltage produced. The "All Power" LED is GREEN if all power supplies on the board indicate via their monitor outputs that they are all good. The "1.8v" LED is GREEN if the 1.8 V supply is present, but it is not otherwise measured. "Board Temps" are for "UR" (Upper Right), "UL" (Upper Left), "LL" (Lower Left), "LR" (Lower Right), as viewing the front of the board (Figure 4-2), and "HS" (HeatSink).

K This Info icon, when pressed, provides a list of the FPGA binaries that went into booting the board, as well as other information such as the CMIB CPU MAC address and CMIB software task compile dates.

5.2 RXP FPGA Functions

All sampled real-time data enters the board via the 32 wafer inputs of the X-ERNI connector. The first 16 wafers (wafers 0-15) enter the "Upper" RXP FPGA, and the second 16 wafers enter the "Lower" RXP FPGA. There are high-speed "DDR" data lines connecting the Upper and Lower RXPs such that each RXP effectively has access to all of the 32 wafer inputs. Two smaller FPGAs were used instead of one larger FPGA to considerably reduce cost.

The connections to the RXP FPGAs are shown in the following Figure 5-2, borrowed from the RXP FPGA RFS document.

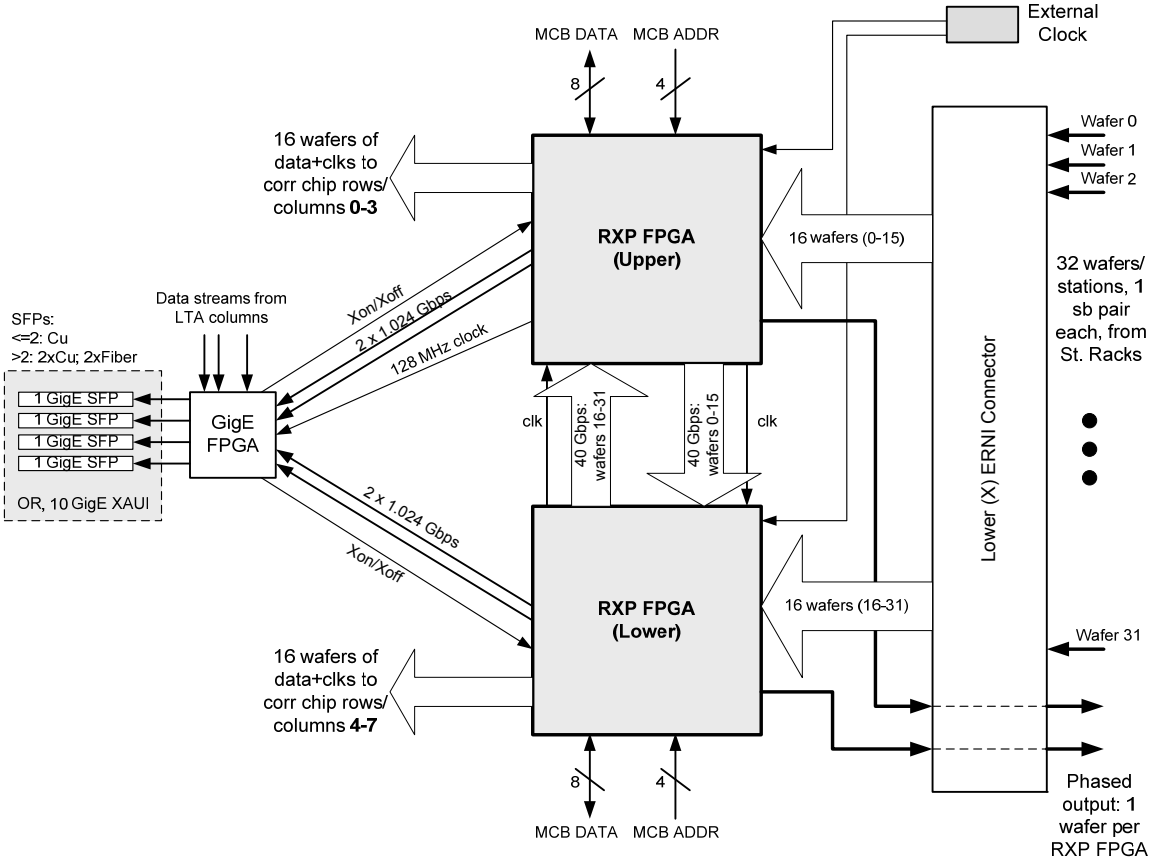

Figure 5-2 Upper and Lower RXP connections, borrowed from the RXP FPGA RFS document.

Each RXP FPGA contains a 32x16 full cross-bar switch to allow any of the 32 input wafers to be routed to any of the 16 output wafers, destined for the X/Y Recirculation FPGAs. The Upper RXP routes 16 wafers to X/Y 0-3, and the Lower RXP routes 16 wafers to X/Y 4-7. External 1:2 LVDS fanout buffers after the RXP FPGAs route identical data to X and Y Recirc inputs; i.e. X*n*/Y*n* Recirc chips get identical data.

Each RXP can select the source of the 128 MHz clock to synchronize to incoming data; either a wafer clock (Upper RXP input wafer 0, Lower RXP input wafer 16), or the

External Clock SMA connector. The receivers use "source synchronous" clocking and build the internal high-speed 1.024 GHz clock from an input 128 MHz clock rather than recovering it from the data. The phase of the 1.024 GHz clock is determined and set using Dynamic Phase Alignment (DPA) in the chip.

Each RXP has dual 1.024 Gbps lines running to the GigE FPGA, to route RXP-internally generated VDIF frames. In practise, only one 1.024 Gbps line for each RXP is used due to memory limitations in the GigE FPGA. This (and available logic in the RXP chip), restricts each RXP to phasing a single sampled data stream. The "Xon/Xoff" signals are unused.

Each RXP has 4 MCB_ADDR (address) bits, and a bi-directional 8-bit MCB_DATA bus. Refer to section 7.1 for RXP address assignments.

5.2.1 RXP GUI Description

This section contains a brief description of the RXP GUI and is relevant here as a top-level user of the board sees the RXP functionality through this GUI. The XML protocol used to communicate with the board CMIB is referenced in section 5.1; the RXP GUI, running on any JAVA browser, communicates with the CMIB via XML in the same way as any application.

Refer to Figure 5-3 on the following page for the following bullet references.

A This LED indicates the status of the status of the FPGA internal hard-block DPA (Dynamic Phase Alignment) receiver. If it is GREEN, alignment to a signal has occurred; if GREY, then it is irrelevant (in the case of DDR inputs from companion RXP), or alignment has not been achieved. Sometimes this might be GREEN for an unconnected signal, and could be due to cross-talk pickup of an adjacent channel. This should be considered a secondary indication of signal validity only.

B HM Gbps receiver lock status. This is the primary indication of HM Gbps signal lock, and is GREEN if all signals in the wafer (CTRL, BB0, BB1) are good and have receiver lock. If RED, one or more receivers for that wafer have not achieved lock.

C This LED indicates if receiver logic in the chip is actively trying to achieve signal lock. Normally this is grey when lock is achieved on all signals in the wafer, and GREEN if lock has not been achieved on at least one signal. If this is GREY and lock is not achieved, it indicates an internal problem in the chip.

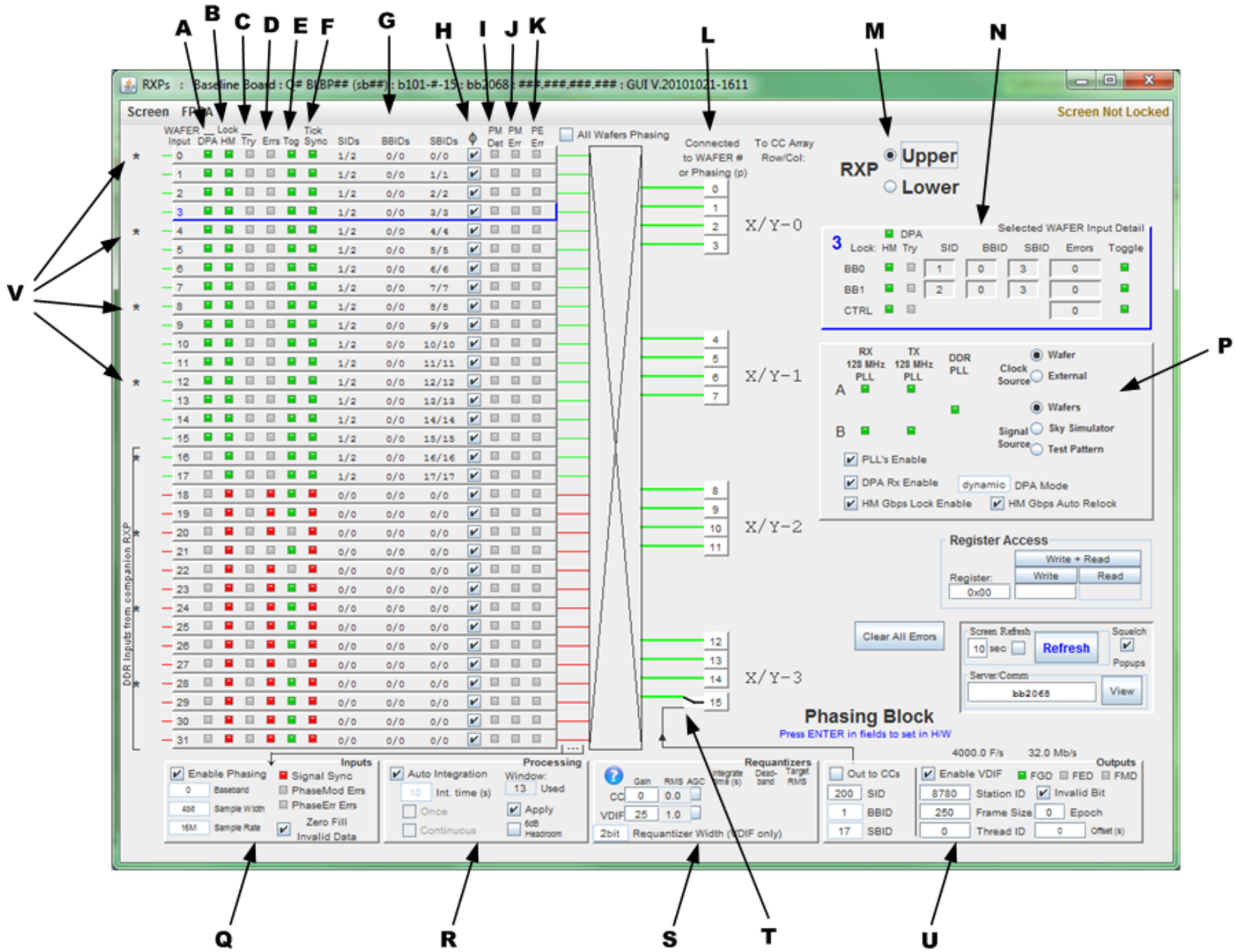

Figure 5-3 RXP FPGA GUI.

D This LED indicates if there have been any errors detected on the signals in the wafer since the last time the GUI was refreshed. GREEN of no errors, RED if errors.

E This LED indicates if the TIMECODE signal in the CTRL pair of the wafer is toggling. This is only a tertiary indication of signal presence, as it is often affected by cross-talk from other channels for unconnected inputs.

F Tick Sync. This LED indicates if the particular wafer's TIMECODE "T-bit" is time-synchronized to the currently chosen master wafer (one of 0, 4, 8, or 12 for the Upper RXP, and 16, 20, 24, 28 for the Lower RXP). Logic in the RXP chip performs a majority selection and chooses a master wafer with the fewest number of other wafers not tick-sync'd to it. Normally this is GREEN, but if RED, indicates that the upstream generator of the TIMECODE signal is not properly time-sync'd to the rest of the system. Note that tick sync has to only be within the buffer depth capability of the chip, which is +/-32, 256 MHz clock cycles (+/-125 nsec).

G Extracted IDs from BB0/BB1 in the HM Gbps BB0, BB1 signals.

H Check boxes to enable (checked) or disable (unchecked) the particular wafer for adding to the phased sum output going into the "Phasing Block".

I LED which indicates if a PHASEMOD signal in the CTRL pair of the wafer has been detected for the purposes of phased sum output. If GREY, no PHASEMOD detected, if GREEN, PHASEMOD is actively detected and used.

J LED which indicates if there has been a protocol error in the received and actively used PHASEMOD signal, for that wafer. If GREY, no error detected; if RED, an error has been detected.

K LED which indicates if there has been a protocol error in the received and actively used PHASERR signal, for that wafer. If GREY, no error detected; if RED, an error has been detected.

L The numbers in these boxes indicate the wafer input that the output to the indicated X/Y Recirc FPGA is connected to. Clicking on a box allows selection to any of the 0-31 input wafers. The color of the data flow lines indicates receiver lock status.

M These radio buttons allow quick selection of which RXP (Upper or Lower) is currently being viewed.

N This box provides more detail for the selected wafer, than provided on the left-hand side of the GUI. In the example, wafer 3 is selected (and underlined in BLUE on the left-

hand side of the GUI). It shows individual error counts, status, etc. of each signal in the wafer.

P This box contains major signal and clock source selections/status for the entire RXP FPGA. For normal operation, all of the LEDs (indicating PLL lock status) must be GREEN, all check boxes must be checked, and the "DPA Mode" should be set to "dynamic". If the RXP is to receive and decode incoming X-ERNI connector signals, the "Signal Source" is set to "Wafers", and the "Clock Source" is set to "Wafer" (but could be "External" if the "Ext-Clk" clock is present and phase-stable w.r.t. the input HM Gbps signals). To run the board standalone for testing, the signal source is set to "Test Pattern" or "Sky Simulator", and the clock source is either "Wafer" or "External". If "Test Pattern", an internal PRN generator is connected to all wafer signals, and appears in the chip and at the output as if it came from the wafer inputs. In this case correlation of these signals results in no recognizable fringes, the integration time is set for 1 second, and all signals are changing rapidly to allow for testing. If "Sky Simulator", the internal signal generator generates a low duty cycle (10 μsec every 10 msec, flagged invalid otherwise) signal that, when correlated, yields fringes with a distinct and recognizable pattern, with integration time set for 100 msec. ("HM Gbps Auto Relock" should not be checked, as there is currently a s/w bug with this feature.)

Q This is the settings/status box for the input of the phased-array processing part of the chip. The "Signal Sync" is RED if any selected-for-phasing wafer has lost lock. Note that if any signal selected for phasing is not receiver-locked, that signal is not added to the phased sum. "Zero fill Invalid Data", if checked, will insert zeros in a signal if flagged invalid; if not checked then no zeros are inserted for invalid data. The rest of the settings/status for this block should be self-evident.

R This block sets internal phased-array processing/bit selection parameters. A full description is beyond the scope of this document (i.e. refer to the RXP RFS document). Settings should normally be as indicated in the figure.

S This block sets the phased-sum output re-quantizers. Refer to the help (?) button in the GUI and the RXP RFS for more information.

T This switch allows phased-sum data to be routed to the Correlator Chip array via the indicated output "BB1". For the Upper RXP, it can be routed to X/Y-3, and for the Lower RXP it can be routed to X/Y-7. The IDs for the phased-sum stream are set in the GUI in the box as shown. Note that the RXP does not generate DUMPTRIG for this stream; it must be generated upstream and routed through the chip accordingly.

U This block contains VDIF frame settings and status. Refer to the RXP RFS Appendix I for the VDIF frame format, with one-to-one correspondence between the contents of the frame and these settings. The "Offest(s)" is a time offset in seconds added to the TIMECODE signal to produce the VDIF "Seconds from reference epoch" header field. The FGD (Frame Good Detect) LED indicates GREEN if at least one good frame was

transmitted to the GigE FPGA since the last GUI Refresh; GREY if no frame transmitted. The FED (Frame Error Detect), if RED, indicates frame generation is not properly synchronized to the TIMECODE 1 PPS epoch since the last time the GUI was "Refresh"ed. This can be likely due to not choosing a "Frame Size", sample rate, and number of bits per sample which results in an integer number of frames per second. The FMD (Frame Missing Detect), if RED, indicates missing output frames if the chosen sample rate and number of re-quantization bits is such that it exceeds the 1.024 Gbps bandwidth of the link to the GigE FPGA.

V The asterisks beside these wafers indicate the possible wafers that are the master timing/tick-sync references for internal buffer synchronization. They also demarcate the first wafer sourcing from individual Station racks in the EVLA system (e.g. wafers 0-3 source from S001, wafers 4-7 source from S002 etc.).

5.3 Recirculation FPGA Functions

There are 16 Recirculation FPGAs on the Baseline Board; 8 "X" devices feed 8 columns of the Correlator Chip array, and 8 "Y" devices feed 8 rows of the Correlator Chip array. All of the X Recirc FPGA designs are identical, but slightly different than the Y Recirc FPGA designs, which are all identical to each other. The difference is that the Y Recirc FPGAs contain circuitry to re-time and transmit all of the 4 wafer inputs to the output, for routing to the Y-ERNI connector, and potentially an adjacent board. Refer to the Recirc FPGA RFS for a more detailed description of the internal function of this chip, and its register set.

The external connections to the Recirc FPGA are shown in the following Figure 5-4, borrowed from RFS.

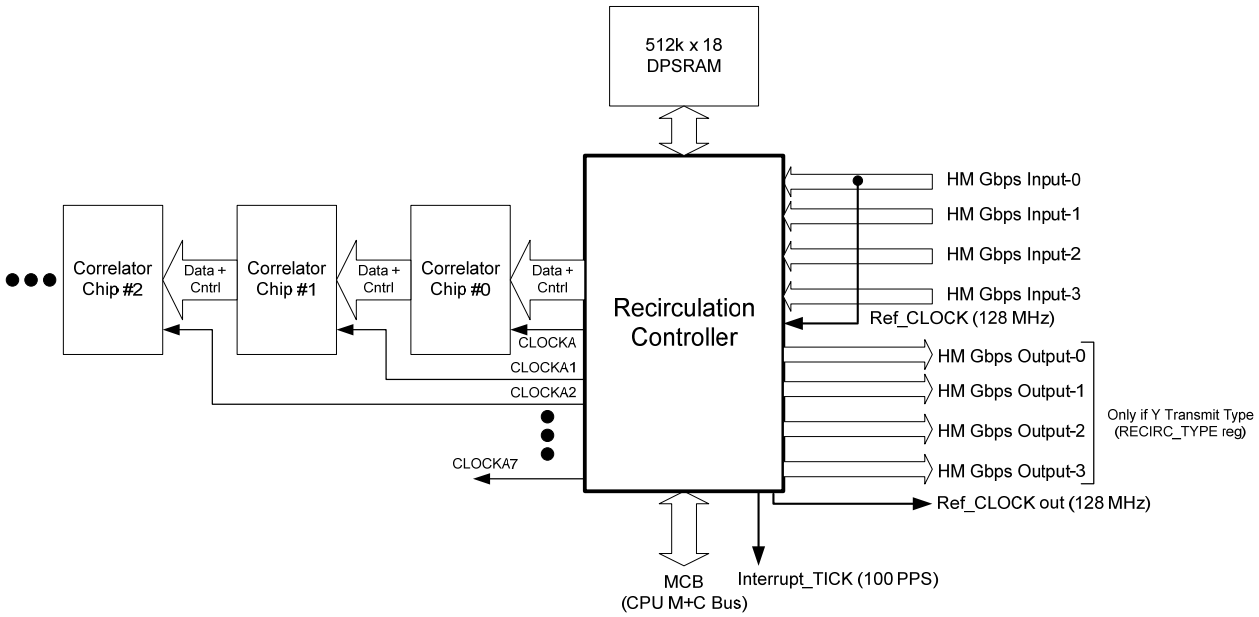

Figure 5-4 Recirculation FPGA external board connections.

The device receives 4 wafers of HM Gbps signals, sourcing from the RXP FPGAs via 1:2 LVDS fanout buffers, as well as a 128 MHz reference clock. From these signals, it builds all of the signals that are transmitted to the row or column of Correlator Chips in a daisy-chain fashion. The Recirc FPGA also produces 8 phase-controlled clocks, each clock going to one Correlator Chip in the row/column; a software-controlled "clock phase calibration" procedure is performed to get the phases of these clocks right so that each Correlator Chip is receiving properly-timed, error-free signals.

There are two external 256k x 18 synchronous SRAM chips (back of the board, see Figure 4-3) which, together, make up a 512k x 18 recirculation RAM buffer. To handle 256 Ms/s data rates, the FPGA "ping-pongs" between these two RAMs at 128 MHz. This buffer is large enough to allow for up to 262,144 spectral channels per correlation product on 4 sampled data streams with a recirculation factor of 256. Recirculation on 8 sampled data streams, with up to 16,384 channels per correlation product utilize 64k x 18 internal FPGA SRAM. As all recirculation memory buffer addresses are the same, internal logic in the chip enforces the 16,384 channel limit when more than 4 sampled data streams undergo recirculation.

5.3.1 Recirculation GUI Description

This section contains a brief description of the Recirculation GUI and is relevant here as a top-level user of the board sees the Recirculation FPGA functionality through this GUI. XML protocol used to communicate with the board CMIB is referenced in section 5.1; the Recirculation GUI, running on any JAVA browser, communicates with the CMIB via XML in the same way as any application.

Refer to Figure 5-5 on the following page for the following bullet references.

A These labels indicate the 8 BB (sampled data stream) inputs to the chip, and captured embedded IDs. There are two BBs from each wafer; BB-0 and BB-1 are from wafer 0, BB-2 and BB-3 are from wafer 1 etc. Wafer 0 sources from the first of 4 RXP outputs after the cross-bar switch (bullet L of Figure 5-3). Individual BBs are broken out in this GUI because it is possible to switch them independently.

B This "HM Gbps Rx" status box indicates status for each relevant HM Gbps signal as follows. For BBs, "CRC" and "Off" errors indicate error counts for the CRC-4 code, and for the embedded W0/W1 pattern, "Toggle" status indicates if the line is toggling or not, but is not a particularly reliable indicator if the input is not connected. For TC and DT (TIMECODE and DUMTRIG) "CRC" and "Off" are CRC and frame-end-bit errors for the currently selected "Control Input Source" (see bullet D). For PM (PHASEMOD) they are errors for any PHASEMOD frame from any CTRL input source (i.e. error detection OR function). Finally, individual error counts for PHASERR for the 4 wafers are provided. Note that individual BB lock status is displayed by the color of the data path line; RED=not locked, GREEN=locked.

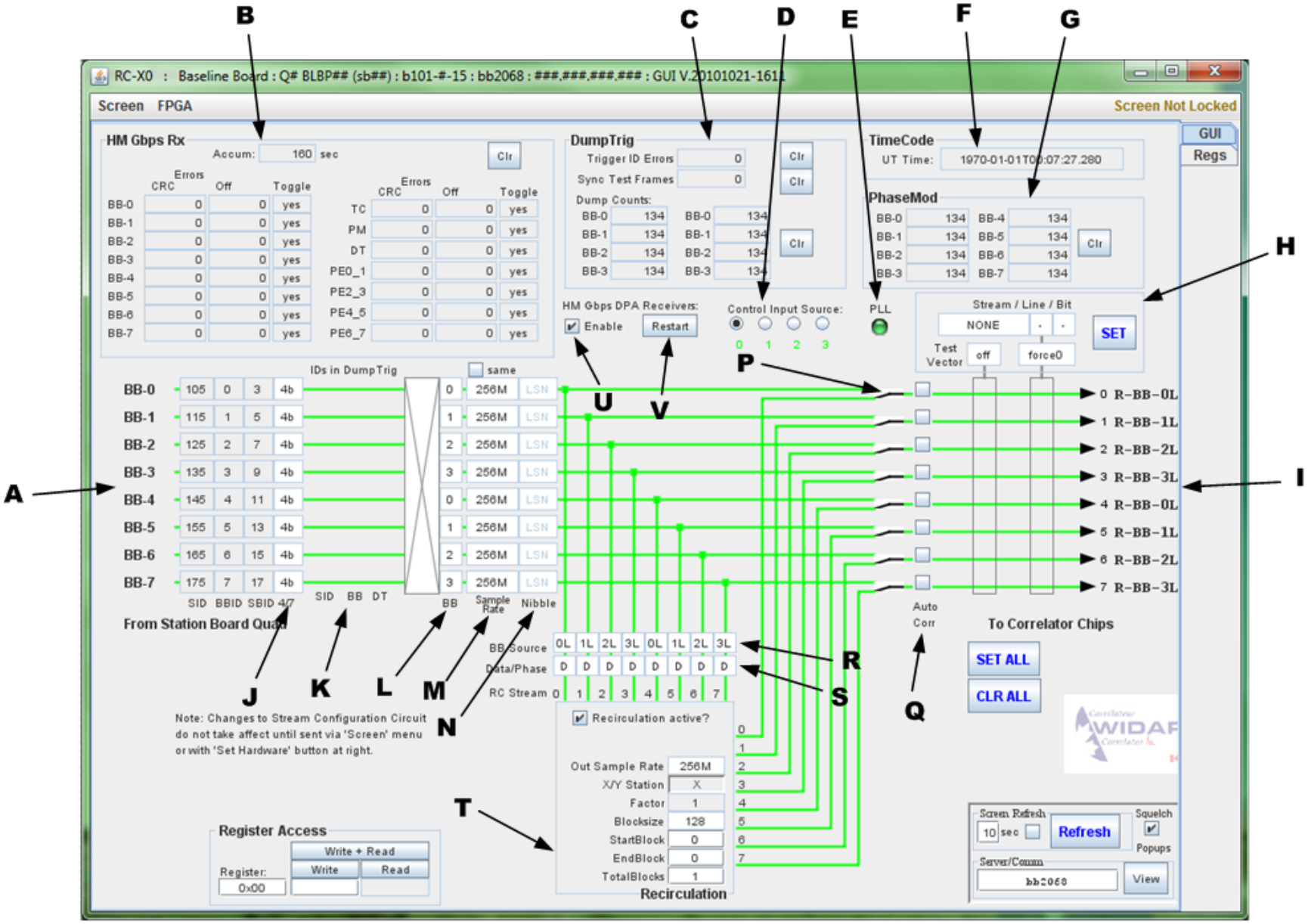

Figure 5-5 Recirculation FPGA GUI.

C This block provides pseudo-counts ("pseudo" because the chip only indicates frame detection or no detection once per 10 msec tick), of received DUMPTRIG frames, on the currently selected "Control Input Source" associated with each BB. DUMPTRIG frame error counts are displayed in the "HM Gbps Rx" block. Refer to the HM Gbps Protocol (A25022N0041) for the meaning of DUMPTRIG "Trigger ID Errors", and "Sync Test Frames" (normally these can just be ignored).

D Control Input Source. This selection allows specification of which HM Gbps CTRL input is used for the TIMECODE reference, and to extract DUMPTRIG. If the selected source has no valid signal, the chip automatically switches to selecting the next available source that contains a valid active signal.

E 128 MHz Ref_CLOCK input PLL lock status LED. For the chip to do anything useful, this LED must be GREEN.

F Current extracted and decoded TIMECODE time presented in UT YYYY-MM-DD HH:MM:SS.msec format. Refer to the HM Gbps Protocol specification (A25022N0041) for more information on the TIMECODE format and reference epoch.

G PHASEMOD frame detect counters, which indicate pseudo-counts of PHASEMOD frames detected associated with each input BB-0:7.

H This block contains some rudimentary facilities for modifying the signals going to the Correlator Chips for testing purposes. The point in the data flow where signal modification occurs is indicated in the GUI. The "Test Vector" (on/off) function allows the Recirc FPGA to be set to generate a known PRN vector pattern to the Correlator Chip (the Correlator Chip is also set for the same Test Vector—"TVN"—pattern, synchronized to the "SCHID_FRAME_" and DUMP_SYNC ticks), allowing for off-line signal-line error checking, and, most importantly, Correlator Chip clock phase calibration. When these Test Vectors are "on", the ticks going to the Correlator Chips occur every 10 μsec (and the PRN pattern repeats every tick) synchronized to the incoming TIMECODE to allow for rapid clock phase calibration, rather than every 10 msec TIMECODE tick. When Test Vectors are off, data from the chip flows normally, synchronized to the TIMECODE tick. The "Stream/Line/Bit" function allows any single signal to be forced HIGH or LOW for fault detection checking verification of the Correlator Chips.

I These labels and flow lines are representative of the output BB signals going to the Correlator Chips. The name of the signal indicates its source and content. For example "**R-BB-0L**", indicates a "**R**" recirculation stream, "**BB-0**" refers to "BB-0" on the input, and "**L**"=Least significant nibble (for 4-bit data it is always "**L**"; for 7-bit data it could be "**L**" or "**M**").

J Each of these boxes allows the user to select if the particular input stream is 4-bit ("4b"), or 7-bit ("7b") data width. If 7-bit is selected, it requires two data paths after the cross-bar icon (beside L) to process the data and so items L and N select the input and the LSN or MSN (Least/Most Significant Nibble).

K This area displays "IDs in DumpTrig" for the DUMPTRIG signal associated with adjacent input BB pairs. The DUMPTRIG frame contains these IDs when the "RRC" command is present. If no IDs are displayed, then no valid RRC DUMPTRIG frames have been detected. Refer to the HM Gbps Protocol specification (A25022N0041) for more information.

L Each box in this column allows connection of the internal data path (represented by flow lines to the right of the cross-bar graphic), to inputs.

M Each box in this column allows the sample rate for the associated data path sampled data stream to be set. This tells the chip how to decode the DATA stream rather than enforcing the sample rate. If the sample rate is not set to the same as at the originator end, garbage output will result.

N Each box in this column allows each internal data stream to be set for the MSN or LSN nibble. If the stream is 4-bit data, only LSN is allowed and is the default.

P These switch icons allow the output data stream to be connected directly to the cross-bar output, or the recirculation block output. If the first (top) four streams ONLY are connected to the recirculation block, then up to 262,144 channels per cross-correlation product may be obtained with recirculation. If ANY of the lower four streams are connected, internal logic in the chip forces the limit to 16k channels (or 8k channels depending on the setting of the R2C bit of the RBLKSIZE register in the Recirc FPGA) on ALL recirculation streams.

Q The check boxes in this column allow individual streams to be set for auto-correlator mode. If checked, then the Correlator Chip that the stream intercepts and correlates must be set for auto-correlator mode as well. In auto-correlator mode the DATA stream to the Correlator Chip contains the un-delayed sample stream, and the PHASE stream contains the delayed sample stream all set to allow the Correlator Chip in auto-correlator mode to obtain 2k spectral channels (i.e. lag-0 shows up in the edge lag [lag 0 of CCC-15]).

R The boxes in this row allow individual internal data streams to be routed to the recirculator block in the chip. Box content and GUI graphics clearly indicate the connection.

IMPORTANT NOTE: The far-left "BB Source" box is the recirculator master reference; all data streams that undergo recirculation will be driven by DUMPTRIG driving this reference stream, and must also be the same sample rate as the reference stream.

S The boxes in this row allow selection of whether the recirculated stream contains data "D" or phase "P". Normally this is set for D, and associated phase for that stream is handled serially and automatically. In this case to ensure <-50 dB spectral artefacts the phase rate f must be ≤0.05% of the sample frequency f_s, $f_s/(8f)$ must not be an integer, and f_X and f_Y must not be related in an integer fashion. Refer to the RSSR0_1 register description in the Recirculation FPGA RFS document (A25090N0000 Rev. 3.1b or higher) for more information on the calculation. If a stream is used for P for an associated D stream, then full phase resolution is available through recirculation memory.

Any stream within a "recirculation stream block" (i.e. streams 0-3 form a block, and streams 4-7 form a block), may be set to P, for a particular D within that same block, connected to the same input stream, and logic in the FPGA automatically properly matches it with the associated data stream on the output of recirculation memory. If a stream is set to P, it cannot in itself be correlated, and trying to do so will cause the LTA to discard Correlator Chip data frames.

T This is the recirculation block control icon. For "static recirculation", where "StartBlock"="EndBlock", no special DUMPTRIG signalling is required to use recirculation. When dynamic recirculation is active (StartBlock≠EndBlock), DUMPTRIG signalling must be "in concert" with settings in this box. A brief description of the items in this box is as follows:

Recirculation active? – If checked then recirculation for the current parameters, whether the P switches select recirculation or not, is active.

Out Sample Rate – Sets the output sample rate for recirculation streams going to the Correlator Chips. Normally this is "256M" for highest recirculation capability, but doesn't have to be.

X/Y Station – Automatically set and fixed by software for "X" for X Recirc chips, and "Y" for Y Recirc chips.

Factor – Calculated by software as EndBlock – StartBlock + 1. This factor indicates (the factor of) how many more channels are being obtained with recirculation rather than without. If the ratio of "Out Sample Rate" to input sample rate (M) is the same as Factor, then no SNR loss in the correlated signal occurs. If this ratio is > Factor, then no SNR loss occurs and the Correlator Chip is performing correlations on redundant data. If this ratio is < Factor, then the correlator signal is reduced in SNR by the square-root of Factor/the ratio. For example, if input sample rate is 128M, output sample rate is 256M, but "Factor" is 4, the SNR is reduced by $\sqrt{(4/2)} = \sqrt{2}$.

Blocksize – This must be set to the same number of lags being used in the downstream Correlator Chip. It is crucial information required to set recirculation memory pointers.

StartBlock – This is set to the start lag block number that is to be acquired by *this recirculator*. Refer to Figure 5-6 for lag block numbering convention in the correlator.

EndBlock – This is set to the end lag block number that is to be acquired by *this recirculator*.

TotalBlocks – This is set to the TOTAL number of lag blocks being acquired on this board or any associated board for the complete lag set. For example, if there are 256 TotalBlocks, each of 16 boards could acquire 1/16th of them (0-15, 16-31 etc.), but *each* board has its TotalBlocks parameter set to 256.

The following graphic, taken from the Recirculation FPGA RFS, indicates recirculation parameters for one particular case.

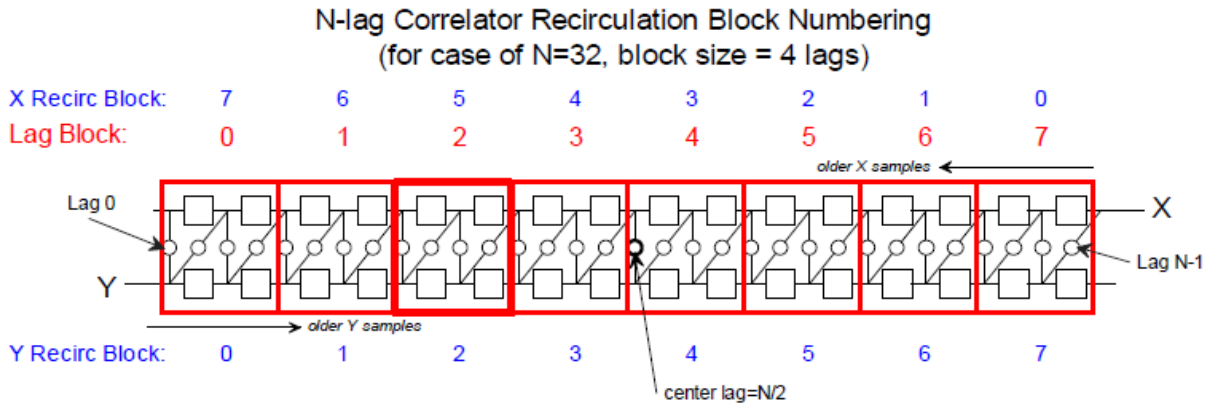

Figure 5-6 Simple example of recirculation lag block numbering. The Start Block is always the lowest-numbered Lag Block acquired by recirculation, and the End Block is always the highest numbered Lag Block acquired by recirculation. In this example, a "block size" of 4 lags is shown for clarity; in reality, the minimum block size is 128 lags.

For the special case (i.e. "optimal e-MERLIN setting") of setting recirculation such that Correlator Chips in the Lower diagonal of the board are used to acquire the "lead" lags, and Correlator Chips in the Upper diagonal of the board are used to acquire the "lag" lags, the following rules and data handling apply:

1. Both X and Y Recirculation FPGA settings are **identical**. Any combination of static and dynamic recirculation across one or more boards may be used.

2. Set the Recirculation Start and End blocks to acquire the *upper* half of blocks. For example, in Figure 5-6, the StartBlock is set to 4, and the EndBlock is set to 7, with TotalBlocks set to 8. DUMPTRIG should be set, in this example, for a recirculation factor of 4. The upper blocks must be acquired so that the zero-

delay lag ("center" in the figure) is acquired, albeit redundantly in both the Upper and Lower diagonals.

3. Set Correlator Chips in the Upper and Lower diagonals identically. i.e. **don't** try to swap around X and Y so that Upper and Lower chips are correlating the same baseline "sense".

4. When concatenating the lags from the Upper and Lower diagonals, the Upper will have correlated A*B (with B delayed), and the Lower will have correlated B*A (with A delayed). Choose one lag set as the reference (e.g. A*B), and for the other one (B*A), flip the lags end-to-end, shift-right by one lag, set the left-most (lowest, vacant) lag to 0, take the complex conjugate (flip the sign of every Quadrature lag), and concatenate in front of (i.e. lower-numbered lags) the reference. The final resulting concatenated lag set will all be for the A*B baseline, with double the total number of lags that recirculation was set for.

U This box, when checked, enables the chips DPA and HM Gbps receiver logic.

V Pressing this Restart button, resets and restarts the chip's HM Gbps receivers.

5.4 Correlator Chip ASIC Functions

A simplified context diagram of the Correlator Chip is shown in Figure 5-7 below, taken from the Correlator Chip RFS document (A25082N0000).

Each Correlator Chip receives and repeats for the next chips in the array, X and Y data, timing, and control signals. The chip contains 16, 128 complex-lag Cross-Correlator Cells (CCCs), which may be connected to the 8 sampled data stream inputs and concatenated with each other in various ways. The Correlator Chip is always correlating (unless it is in the reset condition) at 256 MHz; whether correlated data flows or not depending on dump control signalling (derived from DUMPTRIG in the Recirc FPGA), and whether correlation has been enabled in the chip. Enabling of correlation simply means that it responds to dump control signalling.

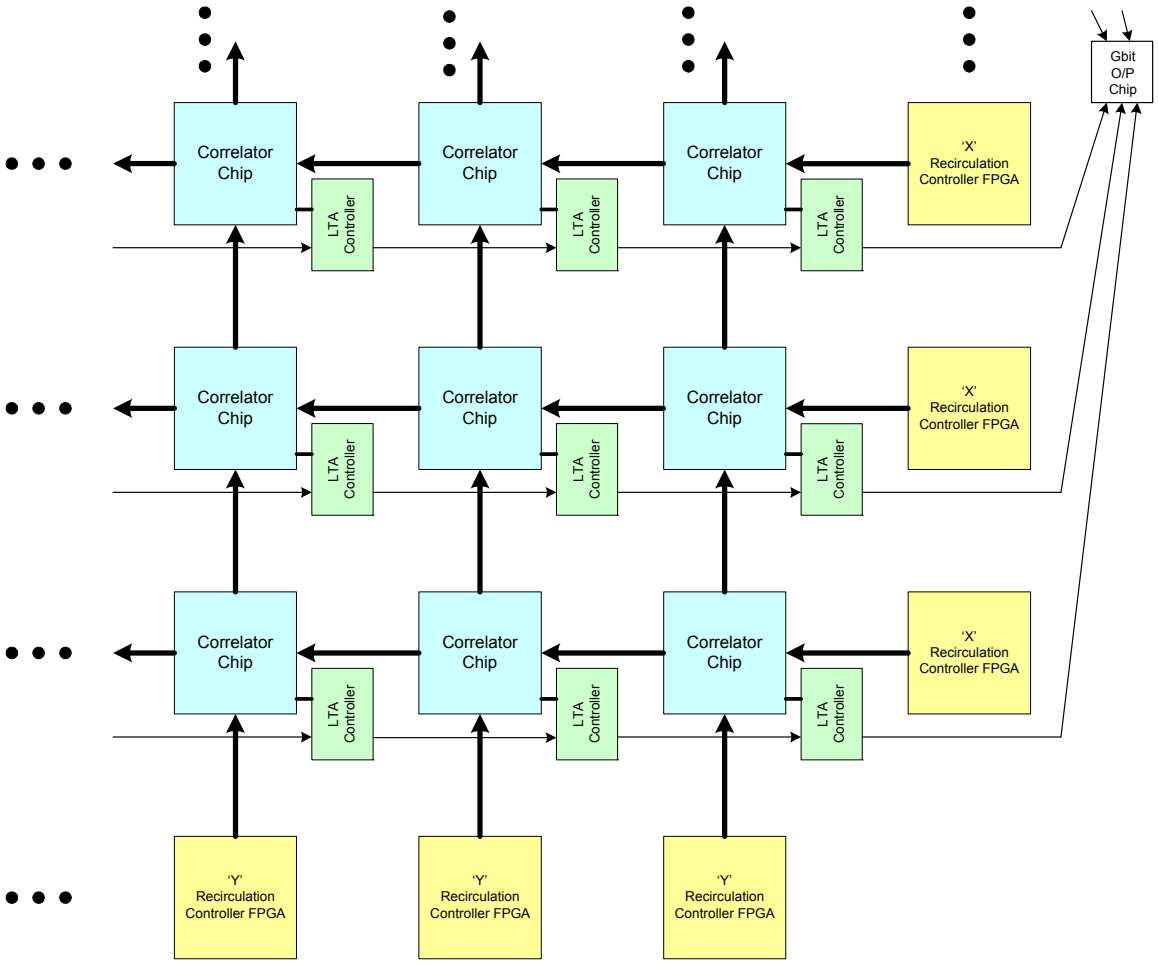

Figure 5-7 Simplified context diagram of the Correlator Chip. Note that the orientation of the X and Y Recirc FPGAs is swapped for diagram clarity.

Output Correlator Chip data is transmitted to its companion LTA FPGA over a simple parallel handshake interface. Flow control is determined by the LTA, and if overruns occur, they are flagged and handled gracefully by the chip (i.e. no corrupted data results).

The chip is designed so that it can be in the RESET state without affecting data flow to companion chips, and without interrupting the clock to the LTA. In this way, if an internal soft fault occurs in a particular chip, it may be cleared with a RESET. Also, if a chip is not being used, it is at its lowest power (without interrupting adjacent chips) when in RESET.

Each Correlator Chip on the board has its own companion point of load (POL) regulator called an Accel chip. The Correlator Chip contains a ring-oscillator, the output of which feeds the Accel chip (via the LTA), and the Accel chip operates in a feedback loop to keep the core voltage just high enough for operation. This mechanism always ensures that the Correlator Chip is operating at its lowest power, while still meeting speed requirements. The LTA also has connections and logic in place to program the Accel

chip's internal NVRAM, which sometimes gets corrupted. More information on Accel chip control by the LTA is provided in the LTA GUI description section.

Note that if, at any time, the X or Y clocks to the Correlator Chip are interrupted, the chip must be RESET and PLL RESET, otherwise its internal operation may be in an indeterminate state. Also note that the X input clock is the master reference clock for the Correlator Chip.

The Correlator Chip contains a very simplified register set, the details of which can be found in the RFS document A25082N0000. Details of the signalling from the Recirc FPGA to the Correlator Chip can be found in that RFS document Figure 5-1.

5.4.1 Correlator Chip GUI Description

This section contains a description of the Correlator Chip GUI insofar as required to understand the operation of the chip. XML protocol used to communicate with the board CMIB is referenced in section 5.1; the Correlator Chip GUI, running on any JAVA browser, communicates with the CMIB via XML in the same way as any application.

Refer to Figure 5-8 on the following page for the following bullet references.

A This is the main chip control/status register box, which maps into the chip's MCSR register and DESSR registers. A short description of each element is as follows:

"**x y**" (and "DS") – These selector boxes select whether integration/dumping is controlled by X or Y input signalling. The intent of this selection was to allow for quasi-baseline integration times (where antennas furthest from the array phase center have longer LTA integration times), but is not really utilized in practise. Thus, either "x" or "y" selection will suffice.

TVEN – This box, when selected (grey), puts the chip in Test Vector mode, where it expects the PRN sequence from the Recirc FPGA.

PhEN – This box, when selected (grey), enables phase rotation in the chip. When it is not selected, it zeros phase streams in the chip, effectively turning off phase rotation.

CEN – This box, when selected (grey), enables correlation in the chip, meaning that it responds to dump control signalling. If not enabled, no output frames will be produced.

TvER – When TVEN is selected, this bit indicates if there is any Test Vector receiver error in the chip.

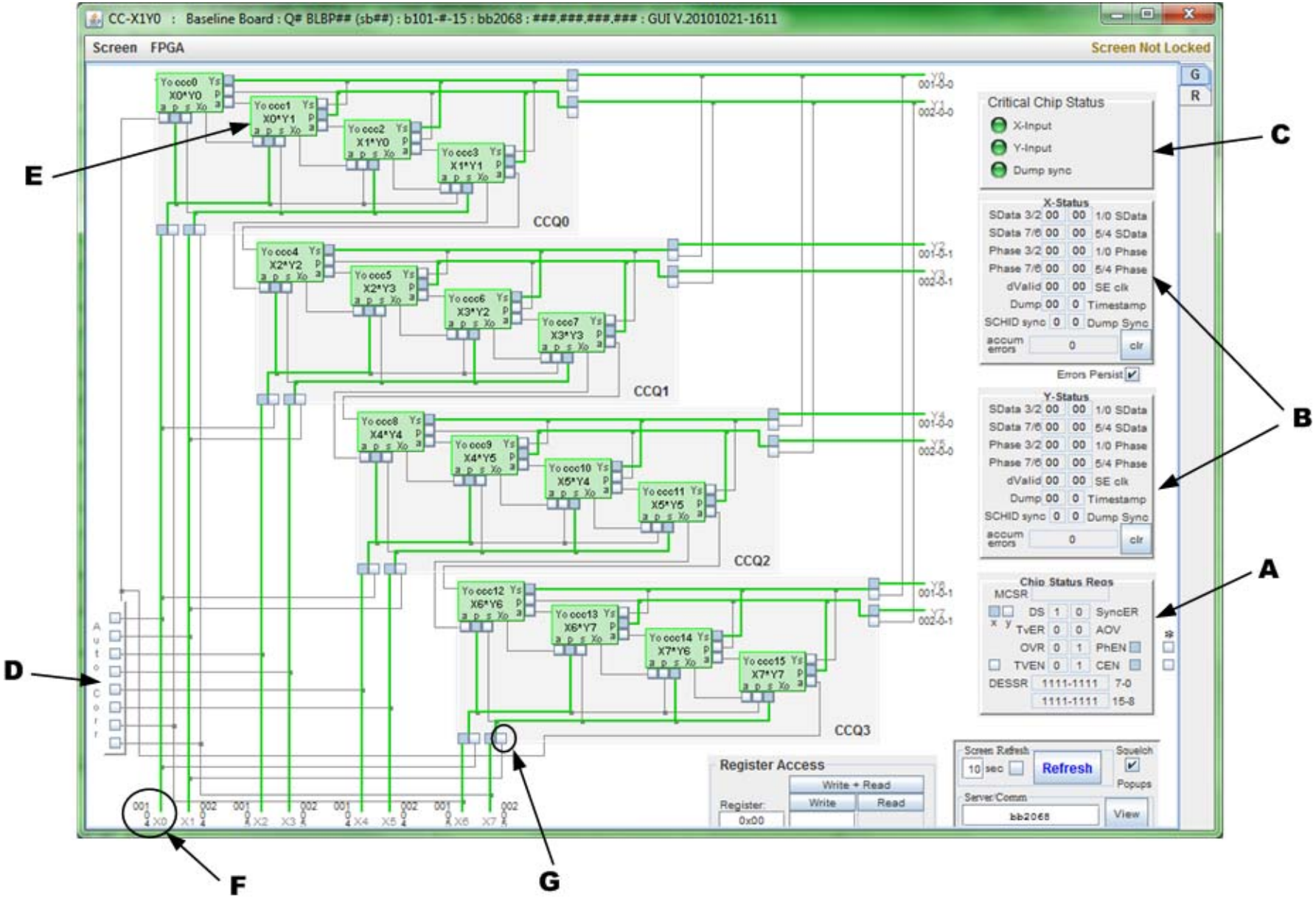

Figure 5-8 Correlator Chip GUI.

OVR – This bit gets set if there was an overrun in the chip (i.e. tried to dump data to on-chip buffer RAM, but the on-chip buffer RAM has not yet been cleared).

AOV – This bit gets set if accumulator overflow in the chip occurred and is contained in one or more output frames to the LTA.

SyncER – This bit gets set if there is an input synchronization error that affects any output data frame.

***Note:** when the chip is in normal correlation mode, the X&Y inputs must conform to the signalling protocol as defined in A25082N0000 Figure 5-1, otherwise one or more offending lines will be detected, flagged in the output frame, and this bit will be set.*

DESSR – Dump enable synchronization status register bits. These bits, if set, indicate that for a particular CCC (labelled 7-0 and 15-8 to the right of the bits), dump signalling (DUMP_SYNC) between X and Y inputs are not coincident in time. This may or may not be an error; for recirculation it is an error as it indicates that source DUMPTRIG signalling is not properly synchronized between the two stations/antennas. For normal correlation, this is not an error.

B These boxes indicate input receiver synchronization errors for the X and Y inputs for the indicated lines. These are active in Test Vector (TVEN=1) mode, or in normal mode. The hexadecimal numbers correspond to the lines as shown (mapping to the X/YSTATUS register contents in the chip RFS, section 5.4.4.6). If any hexadecimal digit is non-zero (and RED if that occurs), then it indicates an error condition. Any data path lines and "CCC" boxes (E) that are affected by an error are also turned RED in an error condition.

C These 3 LEDs provide, at one glance, and indication of X/Y input sync status, and X/Y DUMP_SYNC status.

D These boxes allow with a single click selection of the input and setting of the chip for auto-correlation mode. In auto-correlation mode, the X-inputs (DATA and PHASE contain un-delayed, and delayed data respectively) are used, but the Y-inputs are completely ignored. The top box connects to the "X0" input, the next box down connects to the "X1" input etc.

E Each of these icons represents a 128 complex-lag Correlator Chip cell (CCC), numbered and placed as shown. The X and Y inputs to each cell have several sources, which can be selected by clicking on selection boxes. Source selection is reflected in the box (e.g. for "ccc1" in the figure, it is "X0*Y1"). If the box is GREEN, then it is connected to synchronized X and Y inputs, if it is RED, then either the X or Y input has sync errors, and if it is GREY, then the CCC is unused (either the X or Y input has a null

connection). Data path lines to and between CCCs light up if they are connected, but are grey otherwise.

Note: *the GUI does not explicitly show how dump control signalling is handled in the chip. In short, the user doesn't have to worry about this as the chip automatically routes dump signalling based on data path selections; if multiple CCCs are set to be concatenated, dump signalling is also automatically routed accordingly so that all CCCs dump data in sync.*

F For each input, the generic label ("Xn", "Yn") is augmented by the "SID-BBID-SBID" of that data stream, determined by the CMIB CPU reading the captured IDs in the Recirculation FPGA.

G This is one of many switch boxes in the chip. If a switch box is selected, it is grey, otherwise it is white. Highlighted data path lines also aid in seeing what connections are made in the chip.

5.5 LTA FPGA Functions

There is a dedicated LTA FPGA associated with each Correlator Chip. The purpose of the LTA is, by definition, to provide long-term accumulation of Correlator Chip data since the Correlator Chip can only integrate on-chip for maximum 500 µsec (and in some cases, depending on data content less—250 µsec is a safer maximum integration time). The LTA also provides a very large amount of buffering (with the use of an external 512 Mbit DDR SDRAM), to enable phase binning and recirculation functions.

A simplified context diagram of the LTA FPGA, taken from the LTA RFS document A25091N0000, is shown in Figure 5-9 below:

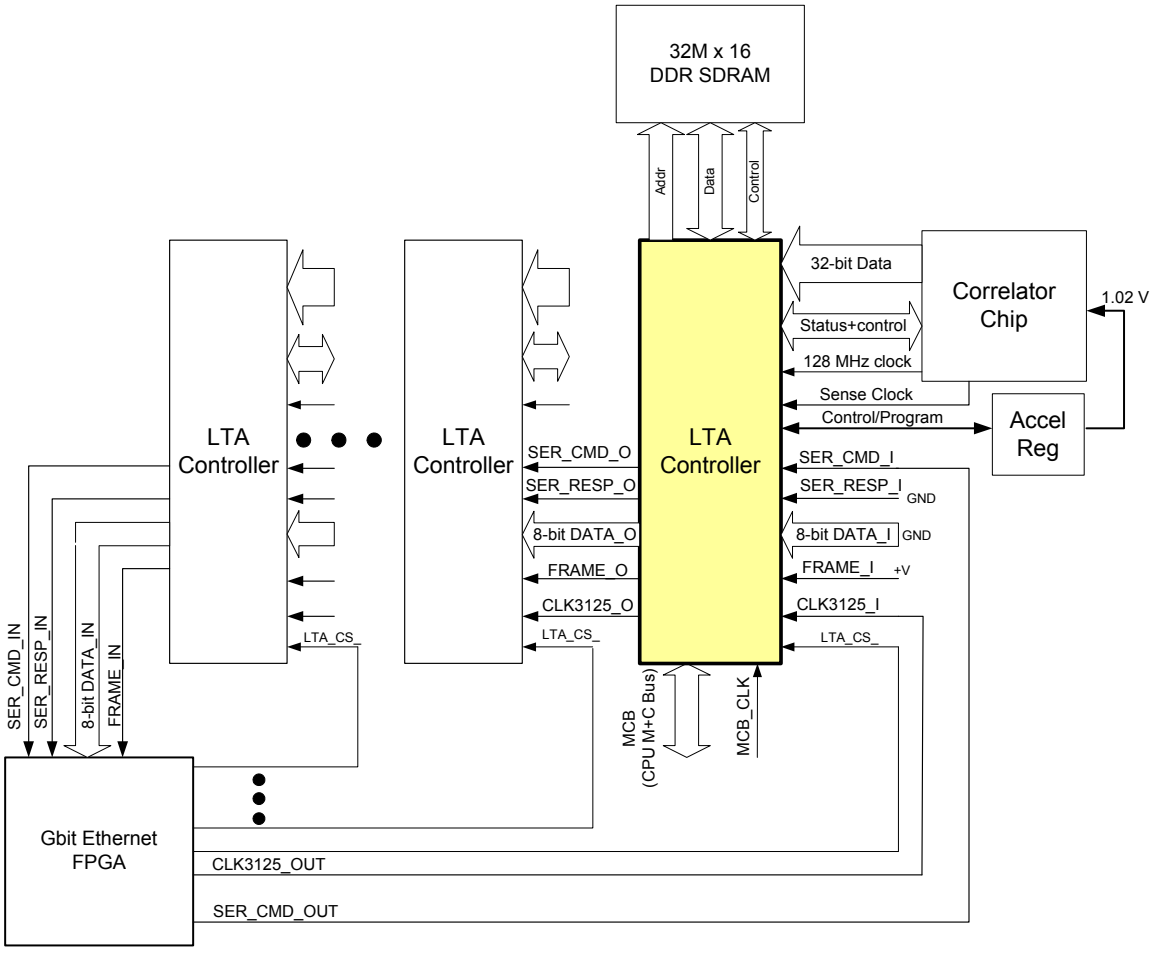

Figure 5-9 LTA FPGA context diagram.

The LTA accepts correlated data frames from the Correlator Chip via a simple handshake parallel interface (the details of which can be found in the Correlator Chip RFS document A25082N0000, Figure 5-3), and, depending on the command embedded in the data frame, does one of several things including integrating data with existing LTA data and flagging that particular data bin for readout.

The GigE FPGA is the central controller that talks to each column of LTAs in a daisy-chain command/response fashion to query LTA chips to see if integrated data is ready for readout. If the GigE FPGA has not selected a particular LTA, then that LTA just passes its input data and command/response signalling on to the next chip. If the LTA is selected (the GigE FPGA selects one and only one LTA at a time in a particular column), then only that LTA in the column responds to command signalling, and transmits data, if ready, on its output eventually finding its way to the GigE FPGA input. Simplified data flow connections are shown in Figure 5-7, with more detail shown in Figure 5-9.

There is a 512 Mbit (32M x 16) DDR SDRAM for each LTA, enough for 2 banks of 2000 accumulation bins for each Correlator Chip. In normal integrate/dump operation, these are memory buffers that may be used as desired (and determined by the phase bin "PB" number in the DUMPTRIG frame); the more buffers that are used, the more the LTA can tolerate readout latency uncertainty. In recirculation dump operation, these form recirculation buffers, and therefore the number of actual unique buffers available is reduced by a factor of the number of blocks acquired by the Correlator Chip (EndBlock – StartBlock +1 in the Recirc GUI). In pulsar phase binning operation, these bins allow for up to 2000 pulsar phase bins to be acquired with no loss of data.

For a full dump/integrate cycle into the LTA (all CCCs), it takes just shy of 200 μsec so this pretty much sets the minimum integration time of the Correlator Chip. A dump/integrate cycle entails transferring data to the LTA, whilst the LTA is fetching data from RAM, integrating the two, and writing back into RAM. A burst-dump cycle (dump data, write to the LTA, flag as ready) for all CCCs is considerably lower, and is about 50 μsec. Proportionately shorter integration times can result as the number of active CCCs is reduced.

The Correlator Chip-to-LTA interface runs at the Correlator Chip-provided clock rate of 128 MHz. All other LTA integrate and transmission functions operate at 133 MHz, this clock frequency being provided to the LTAs at 133 MHz/4 = 33.25 MHz by the GigE FPGA (the "CLK3125" in Figure 5-9, indicating 31.25 MHz, is really 33.25 MHz in the design). 133 MHz is the fastest data rate allowed for the LTA-SDRAM interface.

Note: *every time a Correlator Chip dump occurs, there is a 1 μsec blanking time while the Correlator Chip internally transfers data from active accumulators to on-chip RAM buffers. This must be borne in mind when setting smaller and smaller integration times, because blanking coupled with the dump period can beat with system frequencies, resulting in reduced anti-aliasing or false correlation (see NRC-EVLA Memo# 031).*

As previously mentioned, the LTA FPGA also provides the interface to the Correlator Chip POL regulator Accel chip, the control of which will be described more fully in the next section.

5.5.1 LTA FPGA GUI Description

This section contains a brief description of the LTA GUI and is relevant here as a top-level user of the board sees the LTA FPGA functionality through this GUI. XML protocol used to communicate with the board CMIB is referenced in section 5.1; the LTA GUI, running on any JAVA browser, communicates with the CMIB via XML in the same way as any application.

Refer to Figure 5-10 on the following page for the following bullet references.

A These LEDs indicate the toggle status of each of the lines used to transfer data from the Correlator Chip to the LTA. They are here to provide a visual indication of which line is faulty if the LTA starts reporting errors in E. If an LED is GREEN, the line is toggling; if GREY it is not toggling and is not expected to be toggling; if RED the line is not toggling but is expected to be toggling. There are some conditions under which an LED might be RED, but the associated line is ok. For example, if the Frame Abort LED is GREEN, the LTA is aborting frames, probably due to full LTA bins, in this case not many words of the ACCUM_DATA (LEDs 0-31) will have been transmitted, and it is possible that one of the LEDs is RED (in particular, "bit 28", has been found to be RED in this case).

B This is the PLL lock status for the 133 MHz clock which the chip gets from the GigE FPGA (in the form of a 33.25 MHz clock). GREEN is locked, GREY is not locked. If this LED is GREY, the chip is effectively dead as the 133 MHz clock is the primary clock for the chip.

C This is an indication of the presence of the 128 MHz clock from the Correlator Chip. It is GREEN if the clock is present, GREY if not. Due to excessive jitter, this clock does not actually go through a PLL, but rather is used in raw form; a circuit in the chip, driven by the 133 MHz clock, determines if this clock is present. Therefore, if the 133 MHz PLL status LED is not GREEN, this won't be GREEN either.

D These are toggle status lines for the signals from the previous LTA in the column that are used to transfer data to the GigE FPGA in a daisy-chain fashion. If there is a bad line somewhere in the column, the GigE FPGA will report transmission errors; these toggle status lines help to nail down where in the daisy-chain the error might have occurred.

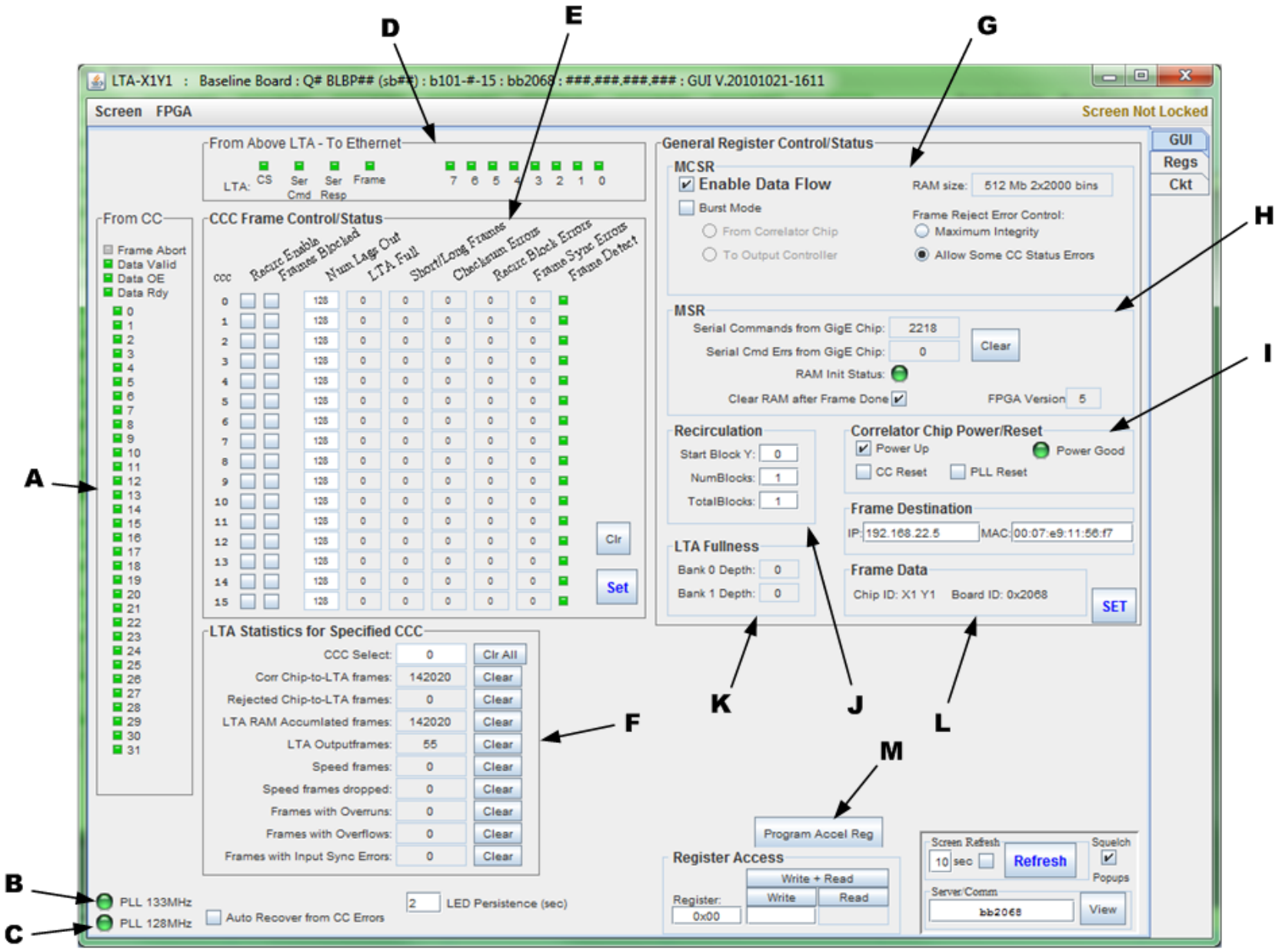

Figure 5-10 LTA FPGA GUI.

E This box contains settings that are pseudo-error counts for all 16 CCCs in the Correlator Chip. Each column is a different setting or error count, and each row is a CCC, with its number indicated on the far left of the box. Settings and error count categories are as follows, starting at the far left:

Recirc Enable – This box, if checked, "enables" recirculation on the CCC. "Enable" in this context means that the LTA performs consistency checking on the Correlator Chip frame's (refer to RFS A25082N0000 Figure 5-4) RECIRC_BLK_X and RECIRC_BLK_Y according to the parameters set in box J, and if inconsistencies are detected, rejects the frame. It also re-calculates the actual LTA memory bin that is used from the Phase Bin embedded in the DUMPTRIG frame and present in the Correlator Chip frame to ensure that each unique recirculation block has its own memory slot. This box does not have to (but could) be checked if "static recirculation" (Start Block=End Block) only is active. If dynamic recirculation is active and this box is not checked, indeterminate integrated LTA frame outputs will result.

Frames Blocked – This box, if checked, will abort Correlator Chip data frames for the CCC. This provides an alternative method for not accumulating one or more particular CCCs, and is normally only used for testing.

Num Lags Out – This is a box that can be set to "128" or "64". If set to 64, then only the center 64 lags of the CCC are transmitted, allowing for higher output frame rates.

LTA Full – This box provides a pseudo-count (maximum one count every 10 msec CPU interrupt) indicating the number of frames that were aborted because the LTA RAM memory slot for the frame is already used (i.e. flagged as "accumulation complete—ready for readout").

Short/Long Frames – This box provides a pseudo-count of the number of frames that were either too short or too long. If this count is non-zero, then it likely means that there is a problem with the Correlator Chip-to-LTA interface, or that the Correlator Chip is in an indeterminate state (see the Note box on page 42 for reasons why this might occur).

Checksum Errors – This box provides a pseudo-count of the number of frames that had checksum errors. If this count is non-zero, then it likely means that there is a problem with the Correlator Chip-to-LTA interface, or that the Correlator Chip is in an indeterminate state (see Note box page 42).

Recirc Block Errors – This box provides a pseudo-count of the number of frames that were aborted (discarded) due to inconsistent RECIRC_BLK_X and RECIRC_BLK_Y numbers with box J. This will also count the number of frames in which an OVR (overrun) has been detected if the **Recirc Enable** box is checked, which indicates that the frame was aborted because it contains data from a previous

time-burst (see the explanation for why this occurs in Appendix V "Known bugs and workarounds" of the Correlator Chip RFS document A25082N0000). In this case, the Correlator Chip integration time is likely too short (coupled with high LTA output data rates), thereby not allowing the LTA enough time to do all of the necessary memory transfers.

Frame Sync Errors – This box provides a pseudo-count of the number of frames with SYNC errors (i.e. the start or end SYNC words are not correct). If this box is non-zero, then it likely means there is a problem with the Correlator Chip-to-LTA interface, or the Correlator Chip is in an indeterminate state (see Note box page 42).

Frame Detect – This LED is GREEN if frames for the associated CCC are being detected, and GREY if frames are not being detected.

F This box contains actual error counts for a selected CCC for various categories. This box, in particular "LTA Outputframes" is useful to look at in real time to gauge the output frame rate of the LTA. Box labelling should be self-explantory. For more information on particulars of each count, refer to associated registers in the LTA RFS document A25091N0000.

G This box provides major data flow control functions for the chip as follows:

Enable Data Flow – This box must be checked, otherwise data flow from the Correlator Chip is stopped. This box can ONLY be checked if the "RAM Init Status" LED is GREEN.

Burst Mode – This box, if checked, puts the LTA in burst-mode, where the associated radio buttons control which of the indicated data paths are currently active. If burst mode is ever implemented in the correlator, it will be under automatic control, and so these selections are here for testing only.

RAM size – This box indicates the RAM capacity and mode of the associated DDR SDRAM.

Frame Reject Error Control – This section has two radio buttons. If "Maximum Integrity" is on, then any frame that has any overflow, overrun, or X/Y syncerr is rejected. If "Allow Some CC Status Errors" is on, then these kinds of frames are allowed through.

H This box (labelled "MSR" as it is associated with the MSR register of the chip) provides information on transport command signalling and DDR SDRAM status for the device. If the "Serial Commands from GigE Chip" is counting up, then the GigE output data scheduler is actively talking to the chip. "Serial Cmd Errs from GigE Chip" counts the number of detected errors on the serial command line. The "Clear RAM after Frame Done", if checked, indicates that the LTA will write zeros to LTA RAM bins once data is read out. As this takes a finite amount of time, if dumping and readout is pushed to the

limit of performance (i.e. OVR errors are starting to be detected), un-checking this box can free up some LTA RAM access time. Note that zeroing RAM ensures that if the first Command for integrating to the LTA is not "First Dump Save" (FDS), data is not corrupted; if this box is unchecked and a FDS isn't the first command (due to a temporary comm. link fault for example), then a corrupted data bin could result. The "RAM Init Status" LED must be GREEN otherwise the DDR SDRAM self-test failed (LED RED). If the LED is YELLOW, then RAM self-test is still in progress. If this happens, it is impossible for the "Enable Data Flow" box (G) to be checked, to prevent flow of corrupt data. Note that a RAM init/self-test happens on every off-to-on transition of the "PLL 128 MHz" LED, and the RAM self-test takes ~32 seconds to complete.

I This box provides power and reset control of the associated Accel POL regulator and Correlator Chip. If "Power Up" is checked, then the power on control line to the Accel regulator is enabled, which should result in the "Power Good" LED going GREEN. The "Power Good" LED reflects the state of the Accel regulator "power ok" signal, but is not necessarily indicative that the Accel regulator is producing a good voltage. Refer to the top-level Baseline Board GUI Correlator Chip icon to determine the actual Correlator Chip core voltage. The "PLL Reset" box, if checked, holds the Correlator Chip PLL in a reset state. Un-checking the box releases PLL reset and starts the PLL. The "CC Reset" box holds the Correlator Chip core logic in a reset state. Note that when this box is checked, provided proper Correlator Chip clock phase calibration has been performed, data flow to adjacent chips is not hindered, the Correlator Chip continues to provide a good 128 MHz clock to the LTA, and the chip is in its lowest power mode next to resetting the PLL and powering it down. The proper up sequence for the Correlator Chip is to check Power Up, release (un-check) PLL Reset, then release (un-check) CC Reset. Normally this sequence is handled automatically by CMIB CPU software.

J This box sets critical recirculation parameters to allow the chip to perform recirculation consistency checking and calculate the correct LTA RAM bin for a given frame of data.

Start Block Y – Referring to Figure 5-6, this is the lowest Y recirculation block number that can be expected from the connected Correlator Chip. This is effectively the same as the "StartBlock" parameter of box T of Figure 5-5.

NumBlocks – This is number of recirculation blocks acquired by this Correlator Chip LTA combination.

TotalBlocks – This is the TOTAL number of recirculation blocks acquired by any Correlator Chip that is producing the lag set that this particular recirculation is part of.

Example: 64 recirculation blocks are to be acquired on 4 different boards, of which this board is one. This particular board (and Correlator Chip/LTA combination) are acquiring blocks 32-47. For this case, Start Block Y is set to 32, NumBlocks is set to 16, and TotalBlocks is set to 64.

K This block, "LTA Fullness", is a real-time count of the number of LTA bins that are currently occupied and awaiting transfer to the GigE FPGA for each bank.

L This block sets the X/Y (column/row) coordinates of the Correlator Chip/LTA combination, and the board serial number. Although these are register settings in the LTA FPGA, they are fixed by software and unchangeable in the GUI. The coordinates and board serial number are inserted in the output LTA frame to the GigE FPGA. The board serial number is also used for Accel regulator programming (refer to the table on page 134 for IMPORTANT INFORMATION regarding regulator replacement).

M Pressing this "Program Accel Reg" button programs the NVRAM in the associated Accel regulator, which sometimes gets corrupted. This action should only have to be taken if the top-level GUI is reporting a bad Correlator Chip voltage (which normally should be handled by the Startup Sequencer). This will cause the Correlator Chip to be reset and powered down, requiring manual power up (see box I), configuration of the Correlator Chip, and setting of "Enable Data Flow" (box G). Also, other chips in the same column above it will lose their clock and have to be reset and re-configured—easily accomplished by pressing the "Rephase" button in the top-level GUI (box I, Figure 5-1).

5.6 GigE FPGA Functions

There is a single GigE FPGA on each Baseline Board. The function of the GigE FPGA is to gather correlation coefficients from LTA FPGAs, as well as VDIF packets from RXP FPGAs, encapsulate them within IEEE 802.3 frame UDP/IP packets, and transmit them out on one of the two GigE ports, SFP1 and SFP2. LTA frames are exclusively transmitted on SFP1, whereas VDIF frames may be transmitted on SFP2 or optionally SFP1. The GigE FPGA is built for speed, and has only enough on-chip buffering capability to optimize data transfer rates. The maximum LTA frame output rate is ~110 kframes/sec.

A simplified context diagram of the GigE FPGA, taken from the GBit Ethernet Chip V2 RFS document A25092N0001, is shown in Figure 5-11 below. Further details of chip operation may be found in the RFS document.

The GigE FPGA contains 8 column schedulers, each of which talks to a column of LTAs on the board, querying each chip in the column in turn to see if it has data ready to transport and if so, commanding it to transport data in the daisy-chain (see Figure 5-9) to one of 8 receive ports. Once a frame is received, it is encapsulated in an IEEE 802.3 UDP/IP frame and transmitted on SFP1 when allowed by the master scheduler (there is a "master scheduler" in the chip not shown in the figure).

A secondary receiver receives VDIF frames from the Upper and/or Lower RXP FPGAs, and transmits them on SFP2, or optionally SFP1. There is no flow control for this operation, as there is no GigE FPGA or RXP FPGA RAM buffering to do so. If another

VDIF frame comes along before the current VDIF frame is transmitted, it is simply dropped and an error is flagged.

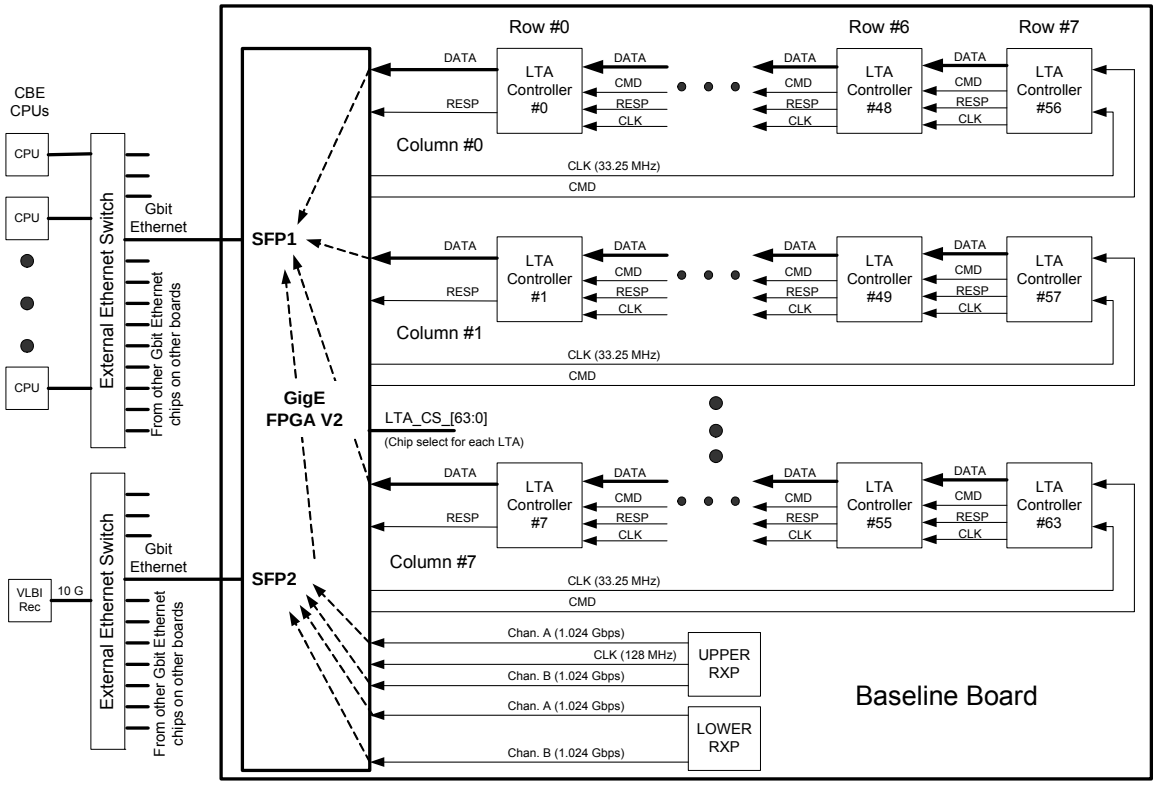

Figure 5-11 GigE FPGA context diagram.

Normal operation of the chip uses SFP1 and SFP2 ports as shown in the figure. The board design, however, supports 4 SFP ports, which could be activated with a modified FPGA design, and by removing the 10G XPAK cage, and installing SFP cages. The chip design (and RFS description) also supports a single 10G XPAK interface, and instructions on how to activate this capability are contained in section 8.1 of the A25092N0001 RFS. However, the description provided here will focus exclusively on the normal dual-1G design.

5.6.1 GigE FPGA GUI Description

This section contains a brief description of the GigE "V2" GUI and is relevant here, as a top-level user of the board sees the GigE FPGA functionality through this GUI. XML protocol used to communicate with the board CMIB is referenced in section 5.1; the GigE GUI, running on any JAVA browser, communicates with the CMIB via XML in the same way as any application.

Refer to Figure 5-12 on the following page for the following bullet references.

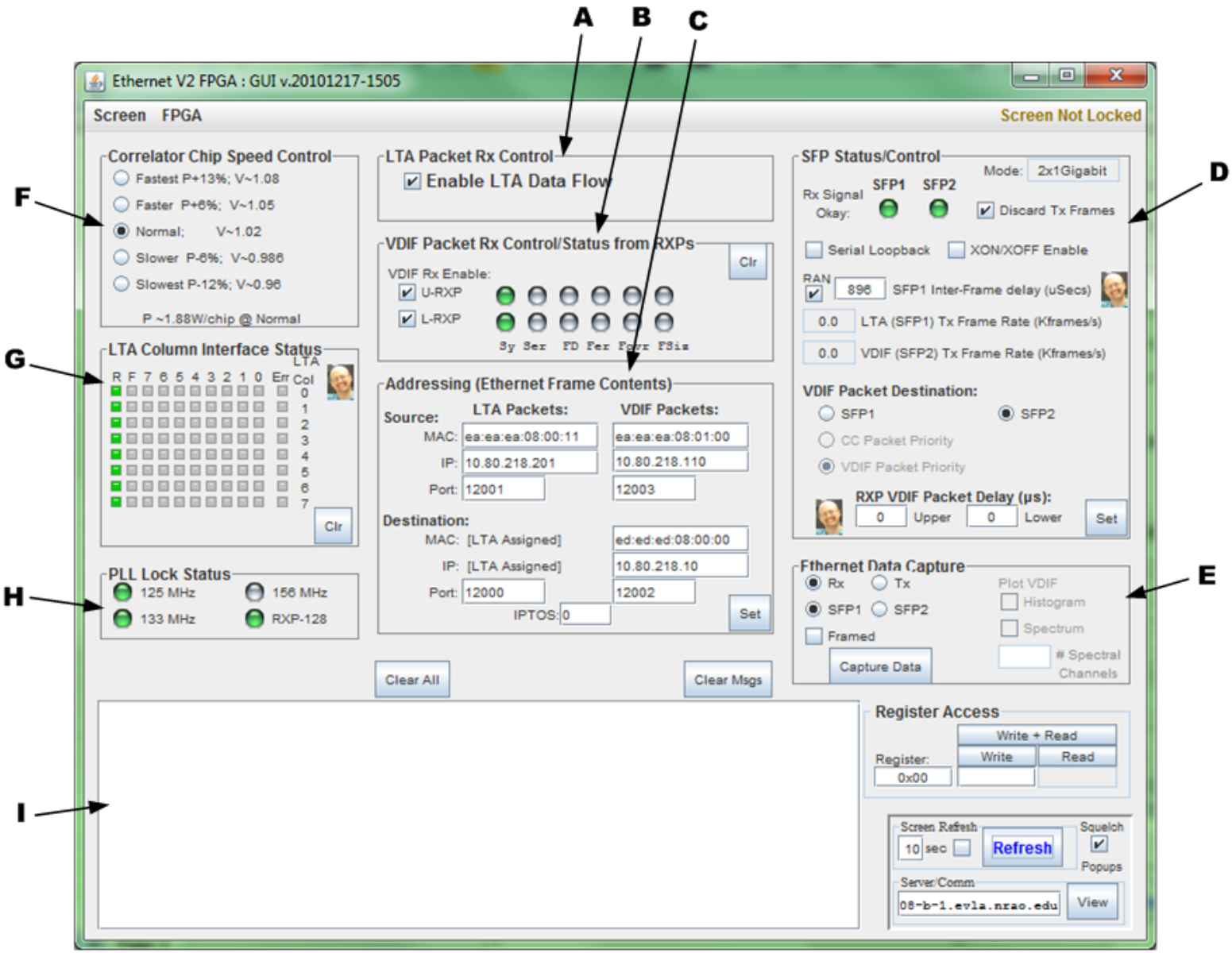

Figure 5-12 GigE FPGA GUI.

A This box contains 1 check box to enable (checked) or disable (un-checked) LTA packet data flow. If un-checked, then there are no LTA frames transferred from LTAs to the GigE FPGA, and frames will pile-up in the LTAs' RAM buffers, with frames being discarded when buffers (bins) are full.

B This box provides control and status information for the receive communications links from the RXP FPGAs. Settings and status are as follows:

VDIF Rx Enable – There are two check boxes here, one for the Upper and one for the Lower RXP. If checked, it turns on the receiver, otherwise the receiver is off. Once checked, the Sy LED will turn GREEN if the receiver syncs to the inter-frame sync codes (refer to section 5.4.4 of the GigE RFS A25092N0001) on the link, or RED if sync is not achieved. Sync should always be achieved if phasing is enabled in the RXP (Figure 5-3, box Q, "Enable Phasing"), whether or not VDIF packet transmission is enabled.

Sy LED – (Sync). Indicates GREEN if receiver sync status to the RXP is established, or RED if not. Will be GREY if the associated VDIF Rx Enable box is unchecked.

Ser LED – (Sync Error). This LED will go RED if any sync errors are detected on the link.

FD LED – (Frame Detect). This LED will go GREEN if VDIF frames are being detected on the receiver, and GREY if no frames have been detected.

Fer LED – (Frame Error). This LED will go RED if VDIF framing errors have been detected on the receiver, and GREY if no framing errors detected. A framing error is violation of the RXP-to-GigE packet protocol shown in section 5.4.4 (and Figure 5-3) of the GigE RFS A25092N0001.

Fovr LED – (Frame Overrun). This LED will go RED if the receiver is overrun by VDIF frames and some had to be discarded. This will happen if, for example, the "RXP VDIF Packet Delay" (box D) is too great, causing an overrun of the receive buffer.

FSiz LED – (Frame Size). This LED will go RED if a VDIF frame from the RXP chip was detected which exceeds the maximum size of 8192 bytes.

C This box contains Ethernet IEEE 802.3 and UDP/IP frame address settings. All of these are software settings, and the GigE FPGA in no way receives and interprets received frames to determine any addresses. The FPGA transmits packets exclusively with these settings. Source and Destination addresses, and packet applicability are self-evident in the GUI.

D Settings and status in this box provide some control of SFP1 and SFP2 packet timing, routing, and status. Settings and status are as follows:

SFP1, SFP2 LEDs – For V2.2 boards (S/N's >2008), these LEDs, if GREEN, indicate that the associated SFP module is receiving good sync codes, meaning that there is a good connection to the far end, be it a switch, or another computer. If an LED is RED, it indicates the receiver is not getting good sync codes, and that the chip is transmitting data on the link (meaning that the far end is probably not receiving it). For SFP2 only, if the LED is GREY, the receiver is not getting good sync codes, but the transmitter is not transmitting on the link anyway. As not many SFP2 connections are made, SFP2 is different in this regard as it is not necessarily an error condition if it is not connected to anything. For V2.1 boards (S/N's ≤ 2008), these LEDs do not provide a proper indication of receive link status for SFP1 (refer to ECO-A25300N0029-25080, and the BVer bit of the MCSR in the GigE RFS for more information). For these boards, this LED is GREEN if it is receiving codes from the SFP module, but is ignorant of codes from the actual link. Thus, for V2.1 boards, this SFP1 LED being GREEN is no clear indication if it is properly connected to the far end.

Mode – In normal dual-1G SFP mode, this is "2x1Gigabit". If the FPGA is booted for 10G mode, this will be "10G", and the GUI is (should be) different than that shown in Figure 5-12. This mode is determined by the state of the 10G bit of the FVSR register in the FPGA (section 5.4.3.2 of the GigE RFS).

Discard Tx Frames – If checked, then no IEEE 802.3 frames are transmitted on either SFP1 or SFP2, but rather are discarded. i.e. data from LTAs and RXPs continues to flow, but are discarded.

Serial Loopback – If checked, the 1G channels in the FPGA undergo near-end loopback, where transmit data is looped-back to the receiver. Used for testing only.

XON/XOFF Enable – If checked, the chip actively detects and acts on PAUSE frames from the far end on SFP1 (or XPAK for 10G mode). This enables far-end-controlled flow control, although a survey of switch data sheets indicates that this sort of flow control is not normally used or effective in commercial networks. In testing against a switch, even though I enabled the switch to generate PAUSE frames, and hammered it with traffic, I could not get the switch to generate PAUSE frames. If unchecked, any incoming PAUSE frames are ignored.

RAN / SFP1 Inter-Frame delay – This box, if checked, uniformly randomizes SFP1 packet transmission inter-frame delay by an amount between zero and 2X the set number of inter-frame delay microseconds, such that the average inter-frame delay is the set amount. If the set number of microseconds is zero, the RAN box MUST NOT be checked or indeterminate operation occurs. Note that the 128-lag LTA packet transmission time is ~9 µsec, and the 64-lag LTA packet transmission time is ~4.9 µsec, and so any setting must take this, as well as the calculated frame rate, into account. If VDIF packets are routed to SFP1, the RAN box should be

unchecked, and the delay should be set to zero or a small amount (i.e. < 1 packet time) to avoid losing packets. If the RAN box is checked, the delay can be set in steps of 4 µsec up to 1020 µsec, and if unchecked, the delay can be set in steps 1 µsec up to 255 µsec.

LTA (SFP1) Tx Frame Rate – This box indicates the actual counted frame rate on SFP1 in kframes/sec.

VDIF (SFP2) Tx Frame Rate – This box indicates the actual counted frame rate on SFP2 in kframes/sec.

VDIF Packet Destination – The box allows selection of where VDIF packets get routed. If SFP2 (the default), no other settings apply. If SFP1, then the radio buttons allow selection of transmit priority. Normally if SFP1 is selected, "VDIF Packet Priority" is set to ensure no VDIF packets get dropped as there is minimal VDIF packet buffering in the chip.

RXP VDIF Packet Delay – These boxes allow for the setting of a delay, in microseconds (0-255), between when a VDIF packet is received, and when it is transmitted on the selected SFP output. This should be set so that it is always at least 2 µsec less than the frame transmission period (1/VDIF Tx Frame Rate), otherwise VDIF packets could be dropped. There is a separate delay setting for VDIF packets from the Upper and Lower RXPs. The VDIF Tx Frame Rate (RXP Phasing Block settings) is:

Frame rate = (Frame size x 32 bits per word) / nbits per sample

Example: for a frame size of 250 (words) and 2-bit samples, the frame rate is 4000 frames/sec, and so the frame transmission period is 250 µsec. The maximum packet delay should therefore be 248 µsec.

Note: in any case, the combined transmission bandwidth of VDIF frames from both RXPs cannot be set greater than the 1 GigE transmission rate of 125 Mbytes/sec, and in practise must always be less due to packet transmission protocol overhead.

E This box provides some capability of capturing transmit or received packets and displaying packet contents in a separate window. This is useful for testing as a sanity check on packet contents. The radio buttons select the source (Rx, Tx, SFP1, SFP2), and the "Framed" box, if checked, captures data starting from the beginning of an IEEE 802.3 (Ethernet) frame. If the "Framed" box is un-checked, then capture happens immediately, allowing for capture of inter-frame PCS codes. The "Plot VDIF" buttons and settings (once this capability is in software), allows for some histogram and spectral display of VDIF packet contents. Note that the software frame decoder is set to decode and display LTA frames and so if VDIF frames are captured it indicates "Unrecognized Frame Type", which, presumably, will be fixed when the software is updated.

F This box contains radio buttons that allow for tweaking the Correlator Chip voltages en-masse. This is because the GigE FPGA produces the frequencies used by the Correlator Chip Accel regulators. Settings, and the effects they obtain, are as indicated in the GUI.

G LEDs in this box provide toggle status of each of the 8 indicated LTA data transmission columns coming into the FPGA. The "R" LED is the serial response communication line. The "F" LED is the data framing pulse. The "7:0" LEDs correspond to each of the 8 data lines. The "Err" LED will go RED if a receive protocol error is detected (i.e. the LTA frame CHECKSUM is bad). If any LED is RED, there is a problem (i.e. it is not toggling but is expected to be toggling because other associated lines are toggling). If any LED is GREEN, it is toggling, and if GREY it is not toggling, but is not expected to be toggling.

H The LEDs in this box provide lock status indications for the indicated PLLs. GREEN indicates the frequency is present and the PLL is locked, GREY indicates the PLL is not locked. In 4x1G mode, the 156 MHz LED is GREY, as that frequency is not used. In 10G mode, the 156 MHz LED should be GREEN, but the 125 MHz LED is GREY as it is not used.

I This box is a software message information window, which normally only contains messages if a parameter is set that is out of range or has an error.

5.7 MCB FPGA Functions

There are four small Altera Cyclone F256 FPGAs on the board (known as the "MCB FPGAs") which provide MCB address decoding and bus transceiver operations, as well as miscellaneous auxiliary functions for the board. A picture of these FPGAs (CMIB stack removed) is shown in Figure 5-13 below. They are located on the front-side of the board underneath the CMIB stack, and are referenced (left to right in the figure), U150, U151, U152, and U153.

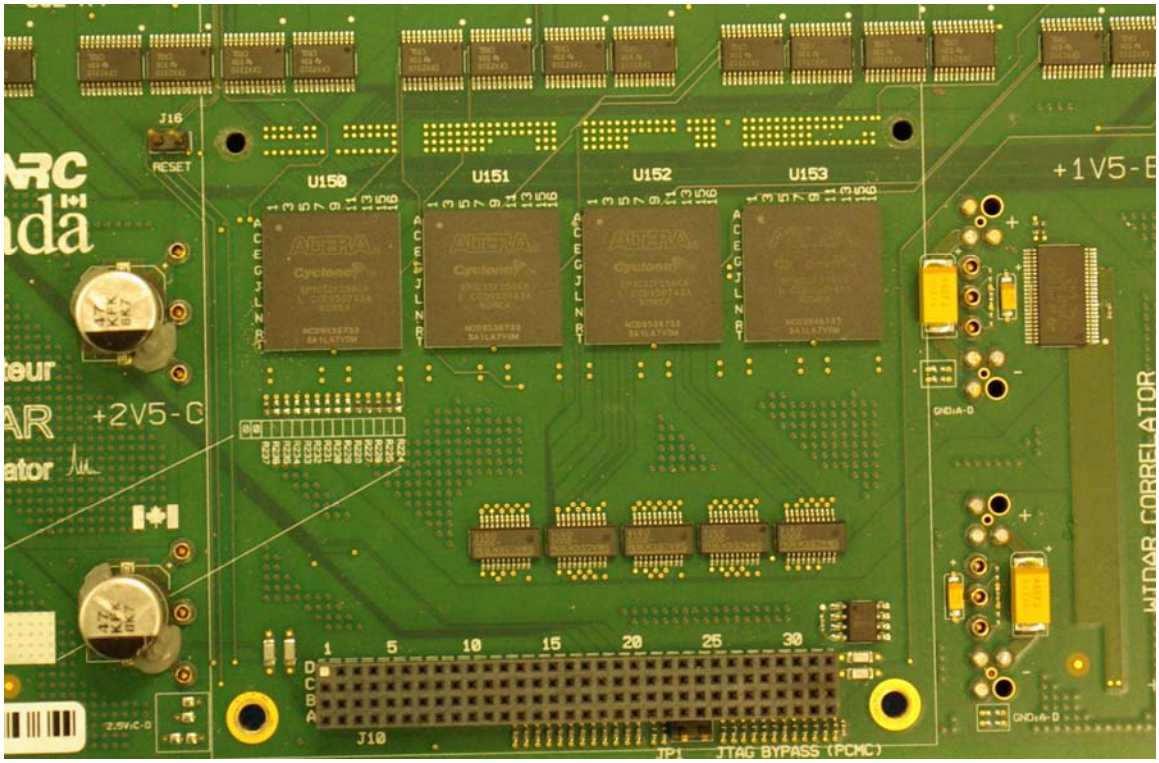

Figure 5-13 Picture of the 4 MCB FPGAs on the front-side of the board underneath the CMIB stack. They are, left to right, U150, U151, U152, and U153.

This section provides a brief description of the functionality of each FPGA. Any register set descriptions are contained in section 7.2.

The MCB on the board is a simplified 8-bit synchronous read/write interface. The PCMC FPGA on the PCMC card in the CMIB stack translates PCI bus requests to the MCB form for the motherboard. A simplified functional timing diagram of the MCB bus is shown in Figure 5-14 below:

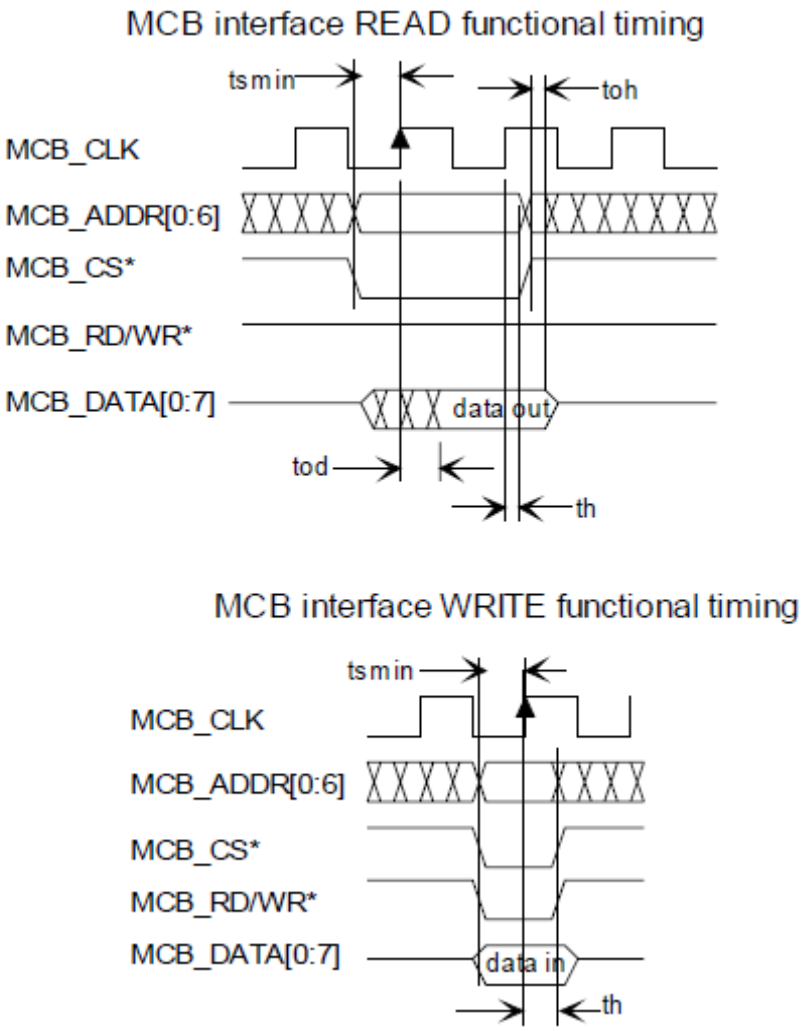

Figure 5-14 Synchronous MCB bus simplified functional timing diagram. On the read cycle, the PCMC FPGA puts in two wait states to ensure there is enough time for read data to propagate from the selected device back to the PCMC FPGA.

5.7.1 U150 "MCB Interface" FPGA

The U150 FPGA is referred to as the "**MCB Interface**" and is responsible for MCB_CLK fanout to all other devices on the board, for generating hardware reset signals for all RXP, LTA, Recirc, and GigE FPGAs; for selection of which of the Recirc FPGA-generated interrupts are used for the CPU; for reading the 14-bit board serial number; for reading the Common Backplane (X-ERNI, Y-ERNI)-settable IDs; for setting the front panel "Board Status" LED; and for reading the aggregate power supply status line. U150 is the only MCB FPGA that contains active read/write registers for the CPU.

The device core runs off the +1.5V-B power supply, and the I/O pins on all banks run off the +2.5V-D power supply.

Logical device signal descriptions are according to the following table. Refer to section 11.1 for detailed device pin-out.

Signal Name	Description
MCB_CLK_IN	33 MHz MCB clock in for CPU read/write access, sourcing from this device, MCB_CLK_F[0].
MCB_CS_IN	Active-low MCB chip select for CPU read/write access, sourcing from U151, MCB_CS_F[0].
MCB_RDWR_IN	MCB Read (high)/Write (low) signal for CPU read/write access, sourcing from U151, MCB_RDWR_F[18].
MCB_ADDR_IN[4:0]	Least-significant 5 MCB address bits for CPU read/write access. Refer to section 7.1 for MCB address allocation. Sourcing from U153, MCB_ADDR8BIT_F8[4:0].
MCB_DATA_IO[7:0]	MCB bi-directional data lines for CPU read/write access, sourcing from U152, MCB_DATAF18[7:0].
RESET	Active-low asynchronous reset from the PCMC FPGA, pin C9 of J10 (Table 6-3).
INTERRUPT_OUT	The selected INTERRUPT_IN[15:0] line, which routes to the CMIB stack connector J10 pin D25, providing the 10 msec interrupt source for the CPU.
CORR_RESET[63:0]	64 active-low reset lines going to the LTA FPGA RESET pins. [0]=X0/Y0, [1]=X0/Y1, … [7]=X0/Y7; [8]=X1Y0 etc.
RECIRC_RESET[15:0]	16 active-low reset lines going to the 16 Recirc FPGAs. [15:8] are for Recirc chips X7…0, and [7:0] are for Recirc chips Y7…Y0
GBITETHER_RESET	Single active-low reset line for the GigE FPGA.
RESYNC_RESET[1:0]	Dual active-low reset lines for the Upper [0] and Lower [1] FPGAs.
INTERRUPT_IN[15:0]	16 interrupt tick lines from the 16 Recirc FPGAs. If the particular Recirc chip is sync'd to TIMECODE, this is a 33 MHz-wide pulse every 10 msec, synchronized to the TIMECODE T-bit. [15:8] come from Recircs X7…X0; [7:0] come from Recircs Y7…Y0.
SN[13:0]	Lowest 14 bits of the board serial number. The upper 2 bits are 0.
IP[15:0]	16 bits of ID taken from the lowest row of the X and Y ERNI connector. [7:0] is from the X-ERNI connector; [15:8] is from the Y-ERNI connector.
LED_BS[1:0]	Front panel board status LED drive lines. 00=OFF; 01=RED; 10=GREEN; 11=YELLOW.
PWR_GOOD	Aggregate output of all the power supply window comparitors on the board. Same state as the front panel "Power" LED.
MCB_CLK	Reference 33 MHz CPU clock from the CMIB stack connector J10 C25.
MCB_CLK_F[30:0]	Fanned-out 33 MHz CPU clock transmitted to all other FPGAs on the board as follows: [0] – U152, U150 MCB FPGAs. [8:1] – Column 0 CC/LTAs [16:9] – Column 1 CC/LTAs [24:17] – Column 2 CC/LTAs [30:25] – Column 3 CC/LTAs
MCB_CLK_RESYNC	Fanned out 33 MHz CPU clock routed to the Upper and Lower RXP FPGAs.
DCLK, DATA0, CONFIG_n, CONF_DONE	FPGA bitstream configuration lines for this device.
TCK,TMS,TDI,TDO	JTAG test lines. Not used during normal functions.

Table 5-1 U150 "MCB Interface Chip" I/O signals.

5.7.2 U151 "MCB Control" FPGA

This FPGA is referred to as the "**MCB Control**" device, and is the main MCB address decoder for the board. It generates the 148 device chip selects (a.k.a. MCB_CS_), as well

as 19 MCB_RDWR signals, which indicate to groups of devices the data transfer direction. Device I/O signals are according to Table 5-2.

The device core runs off the +1.5V-B power supply, and device I/O runs off the +2.5V-D power supply. Refer to section 11.2 for detailed device pin-out.

Signal Name	Description
MCB_CS_F[147:0]	148 MCB chip select lines. Assignments are according to section 5.7.2.1, Table 5-3.
RES_MCB_DIR	This is a bus transceiver direction control line for the 1.8 V to 2.5 V RXP level translator bus transceiver. The RXP single-ended I/Os are 1.8 V (to meet 512 Mbps DDR speed requirements), and there is a level-translator device between the main 2.5 V referenced MCB bus, and the devices' 1.8 V MCB bus.
MCB_RDWR_F[18:0]	19 MCB_RDWR signals for banks of devices on the board. These all take on the same state at the same time. Assignments, derived from the board schematic, are as follows: [0] – Recirc Y FPGAs. [1] – Recirc X FPGAs. [9:2] – Correlator Chip columns 7:0. [17:10] – LTA FPGA columns 7:0. [18] – RXP FPGAs, MCB FPGA U150.
MCB_ADDR[15:8]	Upper 8-bits of the 16-bit MCB address from the PCMC FPGA. Address decoding functions in this chip, which generate individual chip selects, work on these addresses. Refer to section 7.1 for a complete memory map of the board.
MCB_BS	This signal goes active low when a device on the board is selected. Thus, MCB_CS_F signals are a function of this and the MCB_ADDR[15:8]
RESET	Active-low asynchronous chip reset sourcing from the PCMC FPGA via the CMIB stack connector.
DCLK, DATA0, CONFIG_n, CONF_DONE, nCE, nCEO	FPGA bitstream configuration lines for this device.
TCK, TMS, TDI, TDO	JTAG test lines. Not used during normal functions.

Table 5-2 U151 "MCB Control" FPGA device I/O signals.

5.7.2.1 U151 MCB_CS_F[147:0] Assignments

MCB_CS_F[147:0] assignments to board devices are according to Table 5-3 below:

Device	MCB_CS_F		Device	MCB_CS_F		Device	MCB_CS_F		DEVICE	MCB_CS_F
LTAc0 r0	66		LTAc5 r0	106		CCc2 r0	18		CCc7 r0	58
LTAc0 r1	67		LTAc5 r1	107		CCc2 r1	19		CCc7 r1	59
LTAc0 r2	68		LTAc5 r2	108		CCc2 r2	20		CCc7 r2	60
LTAc0 r3	69		LTAc5 r3	109		CCc2 r3	21		CCc7 r3	61
LTAc0 r4	70		LTAc5 r4	110		CCc2 r4	22		CCc7 r4	62
LTAc0 r5	71		LTAc5 r5	111		CCc2 r5	23		CCc7 r5	63
LTAc0 r6	72		LTAc5 r6	112		CCc2 r6	24		CCc7 r6	64
LTAc0 r7	73		LTAc5 r7	113		CCc2 r7	25		CCc7 r7	65
LTAc1 r0	74		LTAc6 r0	114		CCc3 r0	26			
LTAc1 r1	75		LTAc6 r1	115		CCc3 r1	27		RecircX-0	138
LTAc1 r2	76		LTAc6 r2	116		CCc3 r2	28		RecircX-1	139
LTAc1 r3	77		LTAc6 r3	117		CCc3 r3	29		RecircX-2	140
LTAc1 r4	78		LTAc6 r4	118		CCc3 r4	30		RecircX-3	141
LTAc1 r5	79		LTAc6 r5	119		CCc3 r5	31		RecircX-4	142
LTAc1 r6	80		LTAc6 r6	120		CCc3 r6	32		RecircX-5	143
LTAc1 r7	81		LTAc6 r7	121		CCc3 r7	33		RecircX-6	144
LTAc2 r0	82		LTAc7 r0	122		CCc4 r0	34		RecircX-7	145
LTAc2 r1	83		LTAc7 r1	123		CCc4 r1	35			
LTAc2 r2	84		LTAc7 r2	124		CCc4 r2	36		RecircY-0	130
LTAc2 r3	85		LTAc7 r3	125		CCc4 r3	37		RecircY-1	131
LTAc2 r4	86		LTAc7 r4	126		CCc4 r4	38		RecircY-2	132
LTAc2 r5	87		LTAc7 r5	127		CCc4 r5	39		RecircY-3	133
LTAc2 r6	88		LTAc7 r6	128		CCc4 r6	40		RecircY-4	134
LTAc2 r7	89		LTAc7 r7	129		CCc4 r7	41		RecircY-5	135
LTAc3 r0	90		CCc0 r0	2		CCc5 r0	42		RecircY-6	136
LTAc3 r1	91		CCc0 r1	3		CCc5 r1	43		RecircY-7	137
LTAc3 r2	92		CCc0 r2	4		CCc5 r2	44			
LTAc3 r3	93		CCc0 r3	5		CCc5 r3	45		Upper RXP	146
LTAc3 r4	94		CCc0 r4	6		CCc5 r4	46		Lower RXP	147
LTAc3 r5	95		CCc0 r5	7		CCc5 r5	47			
LTAc3 r6	96		CCc0 r6	8		CCc5 r6	48		GigE	1
LTAc3 r7	97		CCc0 r7	9		CCc5 r7	49		MCB U150	0
LTAc4 r0	98		CCc1 r0	10		CCc6 r0	50			
LTAc4 r1	99		CCc1 r1	11		CCc6 r1	51			
LTAc4 r2	100		CCc1 r2	12		CCc6 r2	52			
LTAc4 r3	101		CCc1 r3	13		CCc6 r3	53			
LTAc4 r4	102		CCc1 r4	14		CCc6 r4	54			
LTAc4 r5	103		CCc1 r5	15		CCc6 r5	55			
LTAc4 r6	104		CCc1 r6	16		CCc6 r6	56			
LTAc4 r7	105		CCc1 r7	17		CCc6 r7	57			

Table 5-3 MCB_CS_F[147:0] chip select assignments to devices on the board. "c" is the same as the X-coordinate; "r" is the same as the Y-coordinate.

5.7.3 U152 "MCB Data Fanout" FPGA

This FPGA is referred to as the "**MCB Data Fanout**" device, and is the MCB_DATA[7:0] fanout bus transceiver for the board. It also fans-out the FPGA configuration bitstream signal "CDATA" 9X, which feed into the 9 independent configuration bitstream paths on the board. Device I/O signals are according to Table 5-4.

The device core runs off the +1.5V-B power supply, and device I/O runs off the +2.5V-D power supply. Refer to section 11.3 for detailed device pin-out.

Signal Name	Description
MCB_DATA_F0[7:0]	Y Recirc FPGAs
MCB_DATA_F1[7:0]	X Recirc FPGAs
MCB_DATA_F2[7:0]	Corr Chips, column 0
MCB_DATA_F3[7:0]	LTAs, column 0
MCB_DATA_F4[7:0]	Corr Chips, column 1
MCB_DATA_F5[7:0]	LTAs, column 1
MCB_DATA_F6[7:0]	Corr Chips, column 2
MCB_DATA_F7[7:0]	LTAs, column 2
MCB_DATA_F8[7:0]	Corr Chips, column 3
MCB_DATA_F9[7:0]	LTAs, column 3
MCB_DATA_F10[7:0]	Corr Chips, column 4
MCB_DATA_F11[7:0]	LTAs, column 4
MCB_DATA_F12[7:0]	Corr Chips, column 5
MCB_DATA_F13[7:0]	LTAs, column 5
MCB_DATA_F14[7:0]	Corr Chips, column 6
MCB_DATA_F15[7:0]	LTAs, column 6
MCB_DATA_F16[7:0]	Corr Chips, column 7
MCB_DATA_F17[7:0]	LTAs, column 7
MCB_DATA_F18[7:0]	GigE FPGA, RXP FPGAs via the level translator.
CDATA_F[8:0]	FPGA configuration bitstream fanned-out CDATA lines.
MCB_DATA[7:0]	The bi-directional MCB_DATA bus from the PCMC FPGA.
RESET	Active-low asynchronous chip reset from the PCMC FPGA.
DCLK, DATA0, CONFIG_n, CONF_DONE, nCE, nCEO	This FPGA's bitstream configuration lines for this device.
TCK, TMS, TDI, TDO	JTAG test lines. Not used during normal functions.
MCB_ADDR[15:8]	Upper 8 bits of the MCB address sourcing from the PCMC FPGA. These address lines are needed so the device knows which MCB_DATA_F* bus is active.
MCB_CLK_IN	33 MHz MCB_CLK sourcing from U150.
MCB_BS	MCB chip select from the PCMC FPGA. This signal is also use to qualify activity of the MCB_DATA_F* lines.
MCB_RDWR	MCB RD/WR from the PCMC FPGA. The state of this signal controls the direction of the MCB_DATA_F* bus transceivers. If low, it is WRITE operation and they drive the bus. If high, it is a read operation, and they receive data from the bus, and route it to MCB_DATA[7:0]
MCB_CLK	33 MHz MCB_CLK sourcing from the PCMC FPGA.
CDATA	FPGA bitstream configuration data line sourcing from the PCMC FPGA.

Table 5-4 U152 "MCB Data Fanout" FPGA device I/O signals.

5.7.4 U153 "MCB Address Fanout" FPGA

This FPGA is referred to as the "**MCB Address Fanout**" device and is the MCB_ADDR[7:0] address fanout chip for the board. It also fans out the MCB_CLK to 43 locations on the board, augmenting the MCB_CLK fanout provided by U150, and fans-out the FPGA configuration bitstream clock "CCLK" to the 9 independent bitstream configuration paths. Device I/O signals are according to Table 5-5.

The device core runs off the +1.5V-B power supply, and device I/O runs off the +2.5V-D power supply. Refer to section 11.4 for detailed device pin-out.

Signal Name	Description
MCB_ADDR8BIT_F0[7:0]	LTAs column 0
MCB_ADDR8BIT_F1[7:0]	LTAs column 1
MCB_ADDR8BIT_F2[7:0]	LTAs column 2
MCB_ADDR8BIT_F3[7:0]	LTAs column 3
MCB_ADDR8BIT_F4[7:0]	LTAs column 4
MCB_ADDR8BIT_F5[7:0]	LTAs column 5
MCB_ADDR8BIT_F6[7:0]	LTAs column 6
MCB_ADDR8BIT_F7[7:0]	LTAs column 7
MCB_ADDR8BIT_F8[7:0]	GigE FPGA, RXP FPGAs via the level translator
MCB_ADDR6BIT_F0[5:0]	Y Recirc FPGAs
MCB_ADDR6BIT_F1[5:0]	X Recirc FPGAs
MCB_ADDR4BIT_F0[3:0]	Corr Chips column 0
MCB_ADDR4BIT_F1[3:0]	Corr Chips column 1
MCB_ADDR4BIT_F2[3:0]	Corr Chips column 2
MCB_ADDR4BIT_F3[3:0]	Corr Chips column 3
MCB_ADDR4BIT_F4[3:0]	Corr Chips column 4
MCB_ADDR4BIT_F5[3:0]	Corr Chips column 5
MCB_ADDR4BIT_F6[3:0]	Corr Chips column 6
MCB_ADDR4BIT_F7[3:0]	Corr Chips column 7
MCB_CLK_F[73:31]	Fanned-out 33 MHz MCB_CLK. Assignments are as follows: [32:31] – Column 3 CC/LTAs [40:33] – Column 4 CC/LTAs [48:41] – Column 5 CC/LTAs [56:49] – Column 6 CC/LTAs [64:57] -- Column 7 CC/LTAs [68:65] – Y Recirc FPGAs [72:69] – X Recirc FPGAs. [73] – GigE FPGA.
CCLK_F[8:0]	Fanned-out FPGA configuration bitstream configuration clock.
MCB_ADDR[7:0]	Lower 8 bits of the MCB address, sourcing from the PCMC FPGA. These get fanned-out to the MCB_ADDRnBIT_F* lines.
RESET	Active-low asynchronous chip reset sourcing from the PCMC FPGA.
MCB_ADDR[15:11]	Upper 5 bits of MCB address, sourcing from the PCMC FPGA. These address lines are used to determine which MCB_ADDRnBIT_F* lines are to be turned on.
MCB_CLK	33 MHz MCB_CLK sourcing from the PCMC FPGA.
CCLK	Bitstream configuration clock, sourcing from the PCMC FPGA, used to drive the CCLK_F[8:0] outputs.
DCLK, DATA0, Config_n, CONF_DONE, nCE, nCEO	This FPGA's bitstream configuration lines for this device.
TCK, TMS, TDI, TDO	JTAG test lines. Not used during normal functions.

Table 5-5 U153 "MCB Address Fanout" FPGA device I/O signals.

5.8 Voltage and Temperature Monitoring Functions

There are many voltage and temperature monitor points on the board, and all analog levels are fed into the PCMC board's 8-channel, 8-bit A/D converter, via the CMIB stack connector, for readout by the CPU. As there are many more monitor points than there are A/D channels, some shortcuts are taken. The first shortcut is that all ¼-brick power supplies that are the same voltage are quasi-OR'd together using resistors (refer to the Baseline Board schematic page 36). The second shortcut, or more correctly workaround, is that the 64 Correlator Chip 1.02 V core voltages, each fed with their own POL Accel regulator, are fed into analog switches, which select one source at a time (via the Y7 Recirc FPGA), and the output of which is fed to an A/D channel. The third shortcut, is that the +1.8 V supply, used to feed the RXP MCB bus level transceiver and the RXP I/Os, is not measured; it is merely fed into the U150 MCB FPGA (Monitor and Control Reg, Table 7-2) to allow the CPU to determine if it is present or not.

There are 5 temperature monitoring points on the board, one point in each of the upper-right (orientations are as looking at the front of the board, Figure 4-2) (UR), upper-left (UL), lower-right (LR), and lower-left (LL) regions of the board using a surface-mount sensor, which essentially provides a measure of the board temperature at that point. There is one final temperature monitoring point, a TO-92 device, mounted to the upper-right corner of the heatsink, which provides worst-case heatsink temperature monitoring capability.

The assignment of measurements to PCMC A/D channels, and conversion to correct value units, is according to the following table. The "**val**" in the table is the 8-bit value read from the A/D.

ADC Channel	Voltage/Temp	Location/Description	Voltage/Temp ^{o}C calculation
0	Voltage	-48 V mains supply	-(((**val**/256)x2.048)-1)/0.01333
1	Voltage	+5 V	((**val**/256)x2.048)/0.37
2	Voltage	+3.3 V	((**val**/256)x2.048)/0.5
3	Voltage	+2.5 V	((**val**/256)x2.048)/0.597
4	Voltage	+1.5 V	((**val**/256)x2.048)/0.667
5	Voltage	+1.2 V	((**val**/256)x2.048)/0.667
6	Voltage	Correlator Chip core voltage, selected by AMUX register of Recirc FPGA	((**val**/256)x2.048)
7	Temp	Heat-sink, upper right (UR)	25+(**val**-62.26)/2.4902
8	Temp	Upper left (UL)	25+(**val**-62.26)/2.4902
9	Temp	Upper right (UR)	25+(**val**-62.26)/2.4902
10	Temp	Lower left (LL)	25+(**val**-62.26)/2.4902
11	Temp	Lower right (LR)	25+(**val**-62.26)/2.4902

Table 5-6 Baseline Board monitor point to PCMC A/D channel assignment.

Refer to section 7.3.2 for information on analog-mux mapping to Correlator Chip core voltage measurements.

5.9 Dead-man Thermal Overload Protection

There are two in-series, normally-closed, thermostat/switches on the board, fastened to the heatsink with a hard-set trip temperature of 65 ^{o}C. These TO-220 packages are located in the upper-right corner of the board. If either one of them, or any wiring in-series with the trip signal path, goes open-circuit, it inhibits the power supplies on the board, preventing thermal run-away and possible destruction of the board. Refer to the Baseline Board V2.2 schematic, sheet 38.

5.10 -48 VDC Power, M&C, Transient Protection, and EMI FIltering

-48 VDC is the mains power supply for the board, and it must be within the range of -36 VDC to -58 VDC. The maximum total current requirement is ~11 A (at -48 V). DC enters the board via the two power ("PWR") connectors (Figure 4-2). Each PWR connector contains 3 contacts, 48VDC Return ("**48VR**") (i.e. power supply ground, isolated from signal ground), -48 VDC Hot ("**48V**"), and an opto-coupler-isolated TTL monitor (M) or control (C) line, referenced to signal and chassis ground with assignment to the connectors as shown in Figure 4-2.

Each PWR connector 48V and 48VR line is independent, meaning they are not connected to each other on the PCB. Each 48V line has -60 WVDC, 1500 W surface-mount transorbs, with 10 A crow-bar solder-in fuse protection, to provide transient voltage suppression. Additionally, all of the ¼-brick Artesyn/Emmerson "LQS" power supplies are capable of withstanding 100 V transients, and so the power supplies on the board are well protected.

The 48VR and 48V lines are completely isolated from signal/chassis ground on the board. A typical application will tie 48VR to earth ground at the central power supply distribution panel.

Each 48V supply input has integral EMI filtering using PICOR common-mode filters, and this filtering achieves very close to FCC Part 15 Class B conducted EMI levels, except for the switching power supply fundamental frequency of ~480 kHz, which is slightly above the level. This filtering is provided to minimize the effect of conducted common-mode power supply noise coupling into board-to-board non-isolated communications lines, rather than strictly having to meet an agency specification (i.e. HM Gbps LVDS pairs).

Each DC power supply on the board has its own 47 µF, 80 V electrolytic capacitor for line-side decoupling. The chips on the board require no special power-supply sequencing.

There is a fault in the design, in that there is no in-rush current protection for the DC supply; the many 47 µF decoupling capacitors are instantaneously charged when DC is

applied. Thus, it is recommended that the board be plugged into mating power connectors without DC present to avoid inrush currents and arcing on the power connector contacts. Even if the board is occasionally plugged into hot DC, no serious damage to the connector results.

5.11 Front-Panel Power Supply LEDs

The front-panel power supply indicator LEDs are driven by active window comparitors, powered by the single +3.3 V supply. Thus, if a particular power supply LED is dark, it indicates the voltage is out of range, either too high, or too low, and not necessarily that the power supply is dead (although this is normally the case). The front-panel "POWER" LED is the combination of all of these window comparitors, and will be dark if any power supply LED is dark. There is a bug in the design in that the window comparitors' voltages are noisy (due to the lack of filter capacitors), and sometimes these comparitors, in particular the +2.5V-A LED) will give false results (i.e. blinking out intermittently). There is an ECO (ECO-A25300N0045-25080) to fix this problem if it becomes problematic.

5.12 Front-Panel USB Port

The CMIB CPU (PC/104+) USB port is broken out via a cable to a front-panel USB connector. This function is for future considerations, and is not normally used. The cable shield is only grounded at the front-panel side, but not the CPU side, and there is some evidence that this generates noise on the USB lines causing unnecessary CPU interrupts to occur. It would seem that this problem can be mitigated by plugging a USB memory stick into the connector. The USB connector on the CPU side is very small and fragile, and so there may be problems with using this interface in practise. Refer to the PC/104+ CPU manufacturer's board User Manual for more information on this and other ports which may be available. Normally, the only CPU port that is used in practise is the 100Base-T port.

6 Interfaces

This section describes details of all physical interfaces to the Baseline Board.

6.1 X-ERNI Connector Pinouts

The 36-row X-ERNI 2 mm hardmetric connector is where sampled data and control signals enter the board. The following Table 6-1 defines pinouts, as seen looking into the board connector, where "Row 1" is the very top row.

Row/Col	H	G	F	E	D	C	B	A	Wafer#
1	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	U-CLK-	U-CLK+	**0**
2	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**1**
3	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**2**
4	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**3**
5	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term*	term*	**4**
6	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**5**
7	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**6**
8	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**7**
9	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term*	term*	**8**
10	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**9**
11	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**10**
12	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**11**
13	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term*	term*	**12**
14	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**13**
15	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**14**
16	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**15**
17	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	n/a
18	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	L-CLK-	L-CLK+	**16**
19	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**17**
20	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**18**
21	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**19**
22	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term*	term*	**20**
23	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**21**
24	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**22**
25	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**23**
26	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term*	term*	**24**
27	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**25**
28	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**26**
29	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**27**
30	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term*	term*	**28**
31	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**29**
32	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**30**
33	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	term	term	**31**
34	U-PDo-	U-PDo+	Not Active		U-Co-	U-Co+	U-CLKo-	U-CLKo+	n/a
35	L-PDo-	L-PDo+	Not Active		L-Co-	L-Co+	L-CLKo-	U-CLKo+	n/a
36	ID-7	ID-6	ID-5	ID-4	ID-3	ID-2	ID-1	ID-0	n/a

Table 6-1 X-ERNI connector pinout.

There are two outer ground shields, which mate with outer pins in the Common Backplane header. These ground shields and pins are not included in the table. Refer to the "HM Gbps Cable Physical Specification", ICD document A25022N0040 for more information on this type of connector (although note that the specification was written when there were always "quad-wafer" groups, and so its nomenclature reflects that).

Row 17 is a blank row to provide for mechanical relief for cable headers plugged into the mating Common Backplane.

Rows 34 and 35 are for phased output, and are always active if phasing in the associated RXP chip is "enabled". These contain the identical phased data and CTRL signals that are optionally routed to the Correlator Chip array.

Signals in the connector are as follows:

BB1-, BB1+ -- "BB1" sampled data stream differential pair of the wafer. HM Gbps "DATA" protocol. All pairs are DC-coupled, single-leg DC-biased to +1.2 V with a 1 k-ohm resistor. On-chip 100 ohm differentially terminated.

BB0-, BB0+ -- "BB0' sampled data stream differential pair of the wafer. All pairs are DC-coupled, single-leg DC-biased to +1.2 V with a 1 k-ohm resistor. On-chip 100 ohm differentially terminated.

CTRL-, CTRL+ -- "CTRL" stream differential pair of the wafer. Contains TIMECODE, PHASEMOD, PHASERR, DUMPTRIG, and optionally, COMMAND, and STATUS. All pairs are DC coupled, single-leg DC-biased to +1.2 V with a 1 k-ohm resistor. On-chip 100 ohm differentially terminated.

U-CLK-, U-CLK+ -- 128 MHz clock differential pair, which provides the reference clock for the Upper RXP. DC-coupled, single-leg DC biased to +1.2 V with a 1 k-ohm resistor. On-chip 100 ohm differentially terminated.

term – Unused 128 MHz clock inputs are on-board 100-ohm differentially terminated, but not otherwise routed anywhere.

term* -- Unused 128 MHz clock inputs routed to the RXP FPGAs and on-chip 100 ohm terminated. These clocks are not used, but any single one of them could be used with different RXP FPGA binaries (clock routing resources in the FPGA do not allow dynamic selection of these clock sources, unfortunately).

L-CLK-, L-CLK+ -- 128 MHz clock differential pair, which provides the reference clock for the Upper RXP. DC-coupled, single-leg DC-biased to +1.2 V with a 1 k-ohm resistor. On-chip 100 ohm differentially terminated.

U-CLKo-, U-CLKo+ -- 128 MHz clock output, sourcing from the Upper RXP (Figure 5-3, bullet T), frequency synchronous and phase stable with the other signals in this wafer. AC-coupled output.

U-Co-, U-Co+ -- Phased output CTRL (HM Gbps protocol) signal, identical to the signal routed to the Correlator Chip array, sourcing from the Upper RXP FPGA. The only relevant signal here is TIMECODE, all other signals should be ignored. AC-coupled output.

U-PDo-, U-PDo+ -- The phased HM Gbps DATA signal, identical to the signal routed to the Correlator Chip array, sourcing from the Upper RXP FPGA. Note that this signal epoch (but NOT the embedded IDs and CRC-4 codes) is delayed relative to TIMECODE by the amount of the phased signal processing path, which is sample-rate dependent. The amount of delay is approximately $(12/256 \times 10^6) + 105/fs$ seconds, where fs is the phased signal sample rate in cycles/sec. AC-coupled output.

L-CLKo-, L-CLKo+ -- 128 MHz clock output, sourcing from the Lower RXP (Figure 5-3, bullet T), frequency synchronous and phase stable with the other signals in this wafer. AC-coupled output.

L-Co-, L-Co+ -- Phased output CTRL (HM Gbps protocol) signal, identical to the signal routed to the Correlator Chip array, sourcing from the Lower RXP FPGA. The only relevant signal here is TIMECODE, all other signals should be ignored. AC-coupled output.

L-PDo-, L-PDo+ -- The phased HM Gbps DATA signal, identical to the signal routed to the Correlator Chip array, sourcing from the Lower RXP FPGA. Note that this signal epoch (but NOT the embedded IDs and CRC-4 codes) is delayed relative to TIMECODE by the amount of the phased signal processing path, which is sample-rate dependent. The amount of delay is approximately $(12/256 \times 10^6) + 105/fs$, where fs is the phased signal sample rate in cycles/sec. AC-coupled output.

ID-7…ID-0 – This last row of 8 pins is used to form the lower-part of the 16-bit ID that is fed into the U150 MCB FPGA IP[7:0] inputs. These bits form the "RID" (rack ID) for the slot the board is plugged into. Refer to A25010N0002 Figure 4-3 for encoding for Baseline racks.

Note that this connector's pins can't be probed on the board because they are covered with a ground shield. Refer to the RXP RFS document A25093N0000 appendices for complete information on the mapping between connector pins/signals and RXP FPGA pins, should such probing be required, as most RXP inputs are accessible via FPGA vias accessed at the back of the board.

6.2 Y-ERNI Connector Pinouts

The 36-row Y-ERNI 2 mm hardmetric connector is where sampled data and control signals exit the board, sourcing from the Y Recirc FPGAs. The following Table 6-2 defines pinouts, as seen looking into the board connector, where "Row 1" is the very top row. Unless otherwise specified, all signals are outputs.

Row/Col	H	G	F	E	D	C	B	A	Wafer#	Recirc Source
1	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	CLK-	CLK+	**0**	**Y7-0**
2	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**1**	**Y7-1**
3	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**2**	**Y7-2**
4	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**3**	**Y7-3**
5	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	CLK-	CLK+	**4**	**Y6-0**
6	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**5**	**Y6-1**
7	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**6**	**Y6-2**
8	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**7**	**Y6-3**
9	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	CLK-	CLK+	**8**	**Y5-0**
10	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**9**	**Y5-1**
11	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**10**	**Y5-2**
12	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**11**	**Y5-3**
13	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	CLK-	CLK+	**12**	**Y4-0**
14	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**13**	**Y4-1**
15	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**14**	**Y4-2**
16	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**15**	**Y4-3**
17	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	n/a	
18	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	CLK-	CLK+	**16**	**Y3-0**
19	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**17**	**Y3-1**
20	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**18**	**Y3-2**
21	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**19**	**Y3-3**
22	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	CLK-	CLK+	**20**	**Y2-0**
23	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**21**	**Y2-1**
24	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**22**	**Y2-2**
25	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**23**	**Y2-3**
26	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	CLK-	CLK+	**24**	**Y1-0**
27	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**25**	**Y1-1**
28	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**26**	**Y1-2**
29	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**27**	**Y1-3**
30	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	CLK-	CLK+	**28**	**Y0-0**
31	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**29**	**Y0-1**
32	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**30**	**Y0-2**
33	BB1-	BB1+	BB0-	BB0+	CTRL-	CTRL+	n/c	n/c	**31**	**Y0-3**
34	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/a	
35	GND	GND	GND	GND	GND	GND	GND	GND	n/a	
36	ID-7	ID-6	ID-5	ID-4	ID-3	ID-2	ID-1	ID-0	n/a	

Table 6-2 Y-ERNI connector pinouts.

There are two outer ground shields, which mate with outer pins in the Common Backplane header. These ground shields and pins are not included in the table. Refer to the "HM Gbps Cable Physical Specification", ICD document A25022N0040 for more

information on this type of connector (although note, that specification was written when there were always "quad-wafer" groups, and so its nomenclature reflects that).

The "Recirc Source" column indicates which Recirculation FPGA the wafer sources from, and the number following the FPGA number indicates which wafer into the Recirc FPGA it is. For example "Y6-1" sources from the Y6 Recirculation FPGA, and from wafer 1 into it (equivalent to "BB2 and BB3" of Figure 5-5).

Row 17 is a blank row to provide for mechanical relief for cable headers potentially plugged into the mating Common Backplane.

Row 34 is unused, and row 35 is all GND to allow for 2 mm jumpers to be installed to the ID bits on the next row (a similar scheme would've been nice for the X-ERNI connector, but there weren't enough pins to accommodate it).

All outputs are AC-coupled, with single-leg DC bias to +1.2 V with 1 k-ohm resistor on the device-side of the DC blocking capacitor (to allow for possible future use as an input; see section 8.6).

Signals in the connector are as follows:

BB1-, BB1+ -- "BB1" sampled data stream differential pair of the wafer. HM Gbps "DATA" protocol.

BB0-, BB0+ -- "BB0' sampled data stream differential pair of the wafer.

CTRL-, CTRL+ -- "CTRL" stream differential pair of the wafer. Contains TIMECODE, PHASEMOD, PHASERR, DUMPTRIG. Generally, no COMMAND or STATUS signals are present here.

CLK-, CLK+ -- 128 MHz reference clock, phase-stable w.r.t. BB1, BB0, and CTRL.

+5V – Connected via an 8 A fuse to the board's +5V-D power supply. The fuse is on the top of the board under the heatsink. This power supply is for future use considerations only.

ID-7…ID-0 – This last row of 8 pins is used to form the upper-part of the 16-bit ID that is fed into the U150 MCB FPGA IP[15:8] inputs. These bits form the "SLOTID" and crate ID (CID) for the slot the board is plugged into. Refer to A25010N0002 section 4.12, Table 4-5 for encoding details. Refer to Table 7-2 for information on reading U150 registers.

6.3 CMIB Stack Connector, J10

There is a 128-pin, 4 column x 32-row, 0.100" female connector on the board for mating with the male CMIB stack connector. This connector provides all signaling between the PCMC card and the motherboard. The columns are labeled A, B, C, and D, and the rows are labeled 1 to 32. The connector pins are clearly labeled on the back side of the board, with the square "pin 1" referring to pin A1.

Table 6-3 contains the pinouts for this connector.

Row/Col	A	B	C	D
1	GND	GND	GND	GND
2	GND	+5V	+3.3V	AGND
3	V/T[0]	V/T[1]	V/T[2]	V/T[3]
4	V/T[4]	V/T[5]	V/T[6]	V/T[7]
5	V/T[8]	V/T[9]	V/T[10]	V/T[11]
6	GND	+1.5V	+5V	GND
7	TCK_CFG	TMS_CFG	TDI_CFG	TDO_CFG
8	TCK_Test	TMS_Test	TDI_Test	TDO_Test
9	PCMC_Status[0]	PCMC_Status[1]	RESET	GND
10	nPCMC_PROG	CBUS_EN	GND	CCLK
11	CDATA[0]	CDATA[1]	CDATA[2]	CDATA[3]
12	CDATA[4]	CDATA[5]	CDATA[6]	CDATA[7]
13	GND	+5V	GND	GND
14	nPROG[0]	DONE[0]	nPROG[1]	DONE[1]
15	nPROG[2]	DONE[2]	nPROG[3]	DONE[3]
16	nPROG[4]	DONE[4]	nPROG[5]	DONE[5]
17	nPROG[6]	DONE[6]	nPROG[7]	DONE[7]
18	nPROG[8]	DONE[8]	nPROG[9]	DONE[9]
19	nPROG[10]	DONE[10]	nPROG[11]	DONE[11]
20	GND	+3.3V	+1.5V	GND
21	MCB_ADDR[0]	MCB_ADDR[1]	MCB_ADDR[2]	MCB_ADDR[3]
22	MCB_ADDR[4]	MCB_ADDR[5]	MCB_ADDR[6]	MCB_ADDR[7]
23	MCB_ADDR[8]	MCB_ADDR[9]	MCB_ADDR[10]	MCB_ADDR[11]
24	MCB_ADDR[12]	MCB_ADDR[13]	MCB_ADDR[14]	MCB_ADDR[15]
25	nMCB_BS	MCB_RD/nWR	MCB_CLK	MCB_INT
26	GND	+5V	GND	GND
27	MCB_DATA[0]	MCB_DATA[1]	MCB_DATA[2]	MCB_DATA[3]
28	MCB_DATA[4]	MCB_DATA[5]	MCB_DATA[6]	MCB_DATA[7]
29	MCB_DATA[8]	MCB_DATA[9]	MCB_DATA[10]	MCB_DATA[11]
30	MCB_DATA[12]	MCB_DATA[13]	MCB_DATA[14]	MCB_DATA[15]
31	GND	+3.3V	+1.5V	GND
32	BoardFunc[0]	BoardFunc[1]	BoardFunc[2]	Reserved/unused

Table 6-3 Pinouts for CMIB stack connector J10.

Note that this pinout is common to both the Baseline Board and Station Board, however the assignment and usage of some pins is different. Refer to page 125 of the Baseline Board schematic.

A description of the pins in Table 6-3, as utilized by the Baseline Board is as follows:

V/T[11:0] – Analog voltages measuring either power supply voltage or temperature. Each line is a PCMC A/D converter channel. Refer to Table 5-6 on page 67 for assignments.

AGND – Analog ground for the PCMC A/D converter. Tied to the Baseline Board analog ground, which itself is tied to digital ground at a single point via a ferrite bead (refer to the Baseline Board schematic, L610, rear side of board, upper left).

TCK_CFG, TMS_CFG, TDI_CFG, TDO_CFG – JTAG lines (all are inputs except TDO_CFG, which is the output) for programming the PCMC EEPROM via the front panel "PCMC PROM Prog HDR", Figure 4-4.

TCK_Test, TMS_Test, TDI_Test, TDO_Test – Board test JTAG lines, sourcing from the front panel "JTAG Test HDR", Figure 4-4. Note that these form no function, but may be active as TCK is used to distribute the Accel regulator reference clock from the GigE FPGA, and the TMS line contains signaling to keep chips from going into a test state.

PCMC_Status[1:0] – These status bits indicate that the PCMC FPGA configuration process has been successfully completed. These drive the front-panel "CMIB Status LED", Figure 4-4. "00"=OFF, "01"=RED, "10"=GREEN, "11"=YELLOW.

RESET – Active-low asynchronous reset from the PCMC FPGA, routing to the MCB FPGAs U150-U153.

CDATA[7:0] – FPGA bitstream configuration data bus, sourcing from the PCMC FPGA, and used to program Baseline Board FPGAs. **Only CDATA[0] is used for bit-serial configuration**; it is tied directly into the MCB FPGAs for their bitstream configuration, and is fanned-out by U152 to the rest of the FPGA serial-configuration daisy-chains on the board.

CCLK – FPGA bitstream "configuration clock". Sources from the PCMC FPGA, and gets fanned out by MCB FPGA U153 for the rest of the FPGA serial-configuration daisy-chains on the board. This also directly forms the CCLK for all MCB FPGAs U150-U153. Refer to section 5.7.

nPCMC_PROG – Goes low to re-configure the PCMC FPGA from the PCMC EEPROM on the PCMC board. This line sources from the front-panel reset switch ("CPU Reset", Figure 4-4), and is the same signal that resets the PC/104+ CPU module.

CBUS_EN – Unused on the Baseline Board.

nPROG[11:0] – These are 12 FPGA program lines, sourcing from the PCMC FPGA. When pulled low, any connected FPGAs are de-programmed. Assignments to FPGAs on the motherboard are as follows:

nPROG[0] -- used to de-program the MCB FPGAs U150-U153.

nPROG[1] – used to de-program the RXP FPGAs.

nPROG[9:2] – used to de-program LTA FPGAs in columns [7:0] (e.g. nPROG[9] is for column X7 LTAs).

nPROG[10] – used to de-program the Recirc FPGAs.

nPROG[11] – used to de-program the GigE FPGA.

DONE[11:0] – These are 12 FPGA "DONE" lines, feeding back from the FPGA daisy-chain configuration to the PCMC FPGA. After the associated nPROG line is pulled low, these lines go low, and are only released high once all FPGAs in the daisy-chain have successfully programmed. All FPGAs in the same daisy-chain drive the particular DONE line open-collector. Assignments to FPGA daisy-chains are the same as for the nPROG lines.

MCB_ADDR[15:0] – 16 MCB address lines, sourcing from the PCMC FPGA, for motherboard MCB addressing. MCB_ADDR[15:8] route exclusively to the MCB FPGAs U151, U152, U153 for address decoding/chip select generation, as well as MCB address and data bus transceiver qualification. MCB_ADDR[7:0] route to U153, for fanout to the rest of the FPGAs on the board. Refer to section 5.7.

nMCB_BS – This is an active-low chip select, sourcing from the PCMC FPGA, which indicates that an MCB bus transfer for some device on the board, including U150, is occurring. It is used by U151 to qualify the generation of chip selects for all devices on the board.

MCB_RD/nWR – This is a read/write control line, sourcing from the PCMC FPGA for MCB bus transfers. If high (and nMCB_BS is low), a read operation is occurring, if low, a write operation is occurring (refer to the MCB bus timing diagram, Figure 5-14 on page 61). This signal is fanned-out by U151 (section 5.7.2) for all other devices on the board, including U150.

MCB_CLK – This is the 33 MHz CPU clock, sourcing from the PCMC FPGA. It is fanned out to all other devices on the board by U150. Other MCB FPGAs (U153, U152) use this clock directly, but U150 uses a fanned-out MCB_CLK for its bus transactions.

MCB_INT – This is connected to a 10 msec interrupt source (Recirc FPGA), synchronized to an incoming TIMECODE signal. The choice of which Recirc FPGA is the source of this signal is determined by settings in the U150 MCB FPGA.

MCB_DATA[15:0] – This is the 16-bit bi-directional MCB data bus. It is fanned-out/in by U152 for all of the FPGAs/devices on the board, including U150. Only bits [7:0] are used by the Baseline Board.

BoardFunc[2:0] – These lines are fixed by the Baseline Board design as all low (GND), and are used to tell the CPU, via the PCMC, what motherboard it is plugged into. These 3 bits show up in bits [31:29] of the "Function-2: Monitor/Control Function" of the PCMC at address 0. Refer to section 7.1 and Table 5-10 of the PCMC RFS A25145N0000 for more information.

+5V – 5 volt power supplied to the CMIB stack from the motherboard. The PCMC card does not use this supply, but rather provides it to the PC/104+ CPU via the PCI bus connector. Total current requirement is 2 A, depending on CPU load. As there are 4 pins, the maximum load on this supply is 4 A. This supply is NOT FUSED on the motherboard, but is routed through 4 0-ohm 0805 resistors (R2001-R2002).

+3.3 V – 3.3 V power supplied to the CMIB stack from the motherboard. Used by both the PCMC and PC/104+ cards in the stack. Total current requirement is 1 A, but up to 3 A could be drawn, as there are 3 pins. This supply is NOT FUSED on the motherboard.

+1.5 V – 1.5 V power supplied to the CMIB stack from the motherboard. Used only by the PCMC for FPGA core supply. Total current requirement is 1 A, but up to 3 A could be drawn, as there are 3 pins. This supply is NOT FUSED on the motherboard.

6.4 Power Connectors, J3 and J3_6

There are two power connectors ("PWR(M)" and "PWR(C)", Figure 4-2). Both are used to deliver the -48 VDC mains power supply to the board (separately, their -48 V hot and return lines are not connected on the board, but power must be supplied to both connectors for the board to function).

The PWR(M) connector uses 1 pin as the signal/chassis-referenced GND TTL *monitor* line. If the line is high, it indicates that all power supplies on the board are operating and within range.

The PWR(C) connector uses 1 pin as the signal/chassis-referenced GND TTL *control* line. If this line is pulled high, it enables all the power supplies on the board, if pulled low, all power supplies are disabled.

Both the (M) and (C) lines are completely electrically isolated from the -48 V hot and return lines.

A picture looking into the connector, with signal assignments is shown in Figure 6-1.

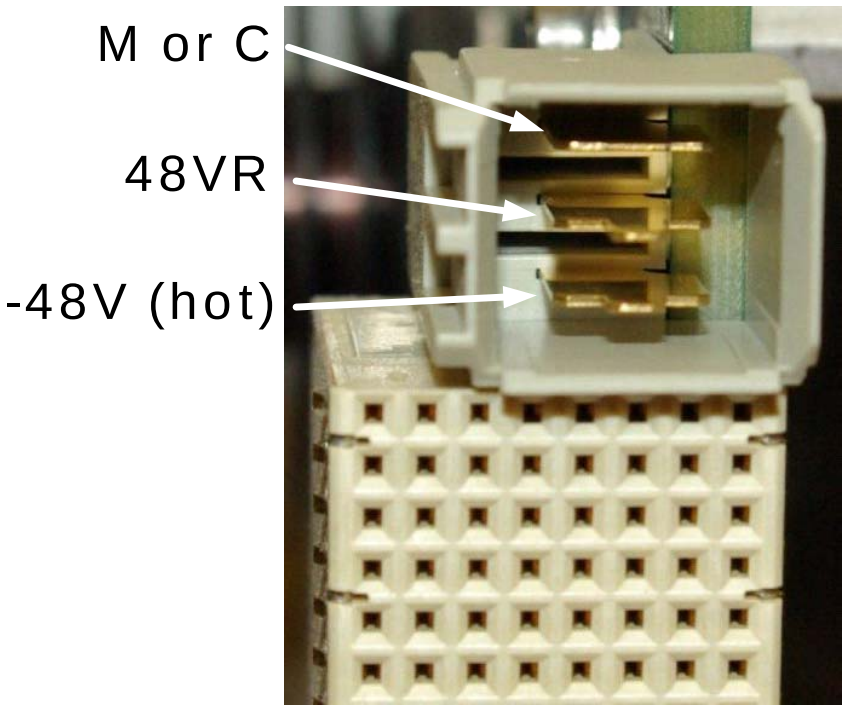

Figure 6-1 Picture looking into the PWR connector.

Note that the 48VR pin is the longest, followed by the -48V (hot), followed by the M or C pin, the idea being that when plugging in a board, the power rail is established first, before the control line connects. Unfortunately, the board does not have current in-rush protection, and so it is best to plug the board into the slot Common Backplane in before energizing -48 V mains power.

This connector pinout, and location of the M or C line ("top is control", "bottom is monitor"), is consistent with other boards in the EVLA system and so Station Board and Baseline Board test-bed connections are interchangeable without the risk of something blowing up.

6.5 Front Panel "PCMC PROM Prog HDR", J6

This 14-pin 2 mm male connector is the gateway used to program the PCMC FPGA EEPROM. Normally programming of the EEPROM must only be done once, as it can thereafter be programmed by the PC/104+ CPU module via the PCMC FPGA, unless it gets corrupted. The connector is a JTAG programming interface, and the EEPROM must be programmed using the Xilinx ISE software using JTAG, and a cable pod such as the Xilinx "Platform Cable USB II".

Pinout assignments of this connector are shown in Table 6-4.

Pin #	Pin name	Description
1, 3, 5, 7, 9, 11, 13	GND	Signal Ground
2	+3.3 V	Connected to the +3.3 V power supply rail on the motherboard.
4	TMS	Test Mode Select input to the board.
6	TCK	Test Clock input to the board
8	TDO	Test Data output from the board
10	TDI	Test Data Input to the board
12, 14	N/C	No connection

Table 6-4 Front panel, "PCMC PROM Prog HDR", J6 connector pinouts.

6.6 Front Panel "JTAG Test HDR", J7

This connector is used for pre-final assembly JTAG manufacturing test of the board. Once assembled, due to dual-use and filtering of the TCK lines stemming from this connector, this function is not available. Connector pinouts are identical to Table 6-4, except pin 2 is connected to the +2.5V-C power supply rail. Refer to section 8.3 for jumper settings which effectively disconnect this connector from board TCK and TMS lines.

6.7 External Clock SMA Connector, J17

This is a right-angle female SMA connector located pointing towards the rear of the board (i.e. same side of the board as the X/Y-ERNI connectors, see Figure 4-2). It is for connection to an external 128 MHz input (-3 to +9 dBm), AC-coupled, and 50-ohm terminated on the board. It routes through a buffer to the Upper and Lower RXP FPGAs, and may be selected as the RXP reference (and subsequently the entire board's 128 MHz clock reference) using XML or the GUI (box "P" of Figure 5-3). With just this external clock applied, and with power, CPU and GigE network connections, it is possible to completely standalone test the board, except for X-ERNI connector inputs to the RXPs, and Y-Recirc outputs to the Y-ERNI connector.

6.8 SFP1 and SFP2 Cage Connectors, J11 and J12

These two connectors mate with industry-standard SFP (Small Form-factor Pluggable) modules. Either copper or fiber modules may be used, but it is important to note that these are for 1 Gbit Ethernet ONLY, and no auto-negotiation is supported. The V2 GigE FPGA implements the IEEE 802.3 Ethernet protocol, within the Physical Coding Sub-layer (PCS) and Physical Medium Attachment (PMA) sub-layer, type 1000BASE-X of IEEE 802.3-2005, clause 36, no auto-negotiation. More information on these protocols can be found in the V2 GigE FPGA RFS A25092N0001.

SFP connector pin assignments are according to the following Table 6-5. Also, refer to pages 31-34 of the Baseline Board schematic.

Pin #	Pin Name	Description
1, 9, 10, 11, 14, 17, 20	GND	Connected to signal/chassis digital ground.
12, 13	Rx+,Rx-	1.25 Gbps receive (SFP to FPGA) pair.
15, 16	VccR, VccT	Individual, bead-isolated and filtered +3.3 V power supplies to the SFP module, sourcing from the board's +3.3 V supply.
18, 19	Tx+, Tx-	1.25 Gbps transmit (FPGA to SFP) pair.
2	SFP_TX_FAULT	Output. Pulled to +2.5 V on the board thru a 10k resistor. Feeds into the FPGA, but is unused.
3	SFP_TX_DISABLE	Input. Signal from the FPGA, which is pulled low in the FPGA.
4	SFP_MOD_DEF2	Bi-dir. Pulled to +2.5 V on the board thru a 10k resistor. Signal fed to the FPGA, but set high-impedance.
5	SFP_MOD_DEF1	Input. Signal fed to the FPGA, but set high-impedance.
6	SFP_MOD_DEF0	Output. Pulled to +2.5 V on the board thru a 10k resistor. Signal fed to the FPGA, but unused.
7	SFP_RATE_SEL	Input. Signal fed to the FPGA, held low in the FPGA design.
8	SFP_RX_LOS	Output. Pulled to +2.5 V on the board thru a 10k resistor. Signal fed to the FPGA, and helps form the "RXD" bit of the SXTCSR register. In V2.1 boards, SFP1, this signal is not connected to the FPGA.

Table 6-5 SFP connector pinouts, and assignment/use in the Baseline Board design.

6.9 10G XPAK Connector, J15

The GigE FPGA optionally supports a single 10G link for transmitting LTA frames and VDIF packets out of the board. If this link is activated, SFP1 and SFP2 modules/slots are not active. To enable 10G capability, some 0-ohm resistors must be removed (R205-R220 inclusive), an XPAK transponder module must be installed in the XPAK cage, the GigE FPGA boot binary must be used ("bb_gbitV2_10g*.rbf), and changes to software must be incorporated to un-use SPF capabilities, and use XPAK capabilities. Refer to section 8.1 of the V2 GigE FPGA RFS A25092N0001 for more detailed information.

XPAK connector J15 pin assignments are according to the following Table 6-6. Also, refer to the Baseline Board schematic page 35 for more information.

Pin #	Pin Name	Description
1, 2, 3, 33, 34, 35, 36, 37, 40, 43, 46, 49, 52, 53, 54, 57, 60, 63, 66, 69, 70	GND	Connected to signal/chassis digital ground.
4, 32	+5V	Bead-isolated +5V power supply, sourcing from the board's +5V-C power supply rail.
5, 6, 30, 31	+3.3V	Beaid-isolated +3.3V power supply, sourcing from the board's +3.3V power supply rail.
7, 8, 28, 29	APS	XPAK power supply, with sensing/feedback from the XPAK module to the power supply circuitry. This power supply is a separate switching regulator, which gets its input voltage from the board's +5V-C rail.
9	LASI_INT	Output. Pulled to +1.2V-B with a 1k resistor on the board, and going through a level translator into the GigE FPGA. Feeds into the RXD bits of the SXTCSR, indicating laser signal detect.
10	RST	Input. Active-low reset, controlled by the FPGA. Pulled high to +1.2V-B through a 1k resistor on the board.
12	TX_ON	Input. Active-high transponder enable. Controlled by the FPGA, and pulled high to +1.2V-B through a 1k resistor on the board.
14	MOD_DET_INT	Output. Fed to the FPGA, but unused.
17	MDIO_INT	Bi-directional. Fed to the FPGA but held high-impedance. Pulled high to +1.2V-B through a 1k resistor on the board.
18	MDC_INT	Bi-directional. Fed to the FPGA, but held high-impedance. Pulled high to +1.2V-B through a 1k resistor on the board.
19-23	PRTAD[4:0]	Bi-directional. Fed to the FPGA, but held high-impedance. Pulled high to +1.2V-B through a 1k resistor on the board.
25, 27	APS_SET, APS_SENSE	APS power supply sense/control lines. Not fed to the FPGA, but rather the on-board APS XPAK power supply.
50,51; 47,48; 44,45; 41,42	RX[3:0]+, RX[3:0]-	Output. 4 lanes of receive differential data lines going to the FPGA, each one running at 3.125 Gbps.
64,65; 61,62; 58,59; 55,56	TX[3:0]+, TX[3:0]-	Input. 4 lanes of transmit differential data lines sourcing from the FPGA, each one running at 3.125 Gbps.
11, 13, 15, 16, 24, 26, 38, 39, 67, 68	N/C	No connection on the board.

Table 6-6 XPAK connector pinouts, and assignment/use in the Baseline Board design.

6.10 M&C 100Base-T RJ-45 Connector

This RJ-45 connector (see Figure 4-4) is the 100Base-T Ethernet connection, which routes via cable directly to the CMIB PC/104+ CPU module. There is nothing restricting this connector to 100Base-T, it could be upgraded to 1000Base-T with an appropriate

CPU module and cable connector. Refer to industry-standard RJ-45 pinout, and the PC/104+ CPU module User Manual for more information.

6.11 Agilent Soft-Touch Probe Header, J5

There are un-populated test header locations on the board between each Recirculation FPGA, and the corresponding row or column it feeds. Each test header, referred to as J5 (page 111) of the board schematic, is built to allow for the installation of an Agilent soft-touch probe header. The solder-in header is Agilent part E5405-68702 and is shown in Figure 6-2 below:

Figure 6-2 Agilent solder-in probe header, E5405-68702.

The soft-touch probe head is Agilent E5406A and is shown in Figure 6-3 below:

Figure 6-3 Agilent soft-touch probe, E5406A.

The entire soft-touch probe pod assembly is shown in Figure 6-4 below:

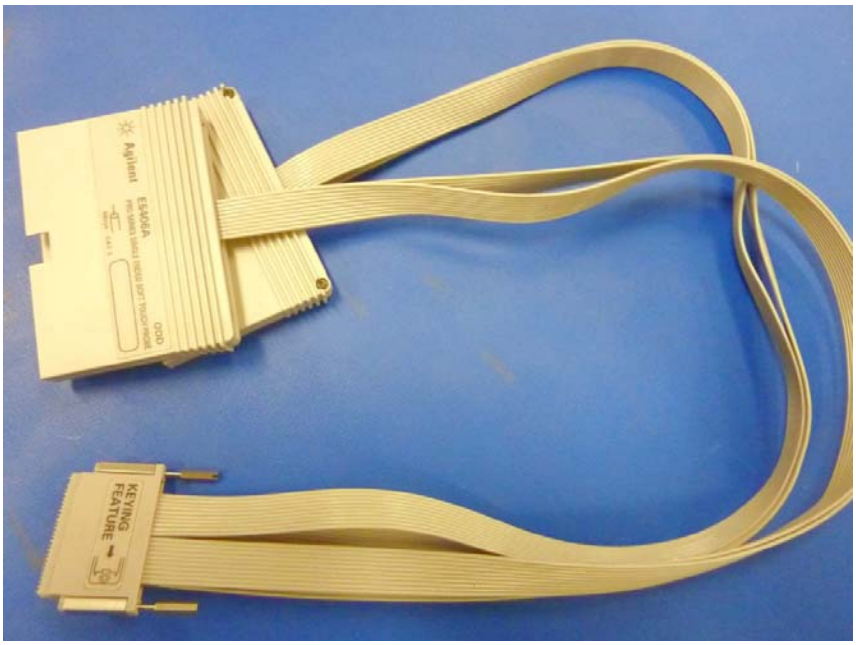

Figure 6-4 Agilent soft-touch E5406A pod assembly.

The front of the PCB, showing pads and solder in holes for the solder-in header is shown in Figure 6-5 below:

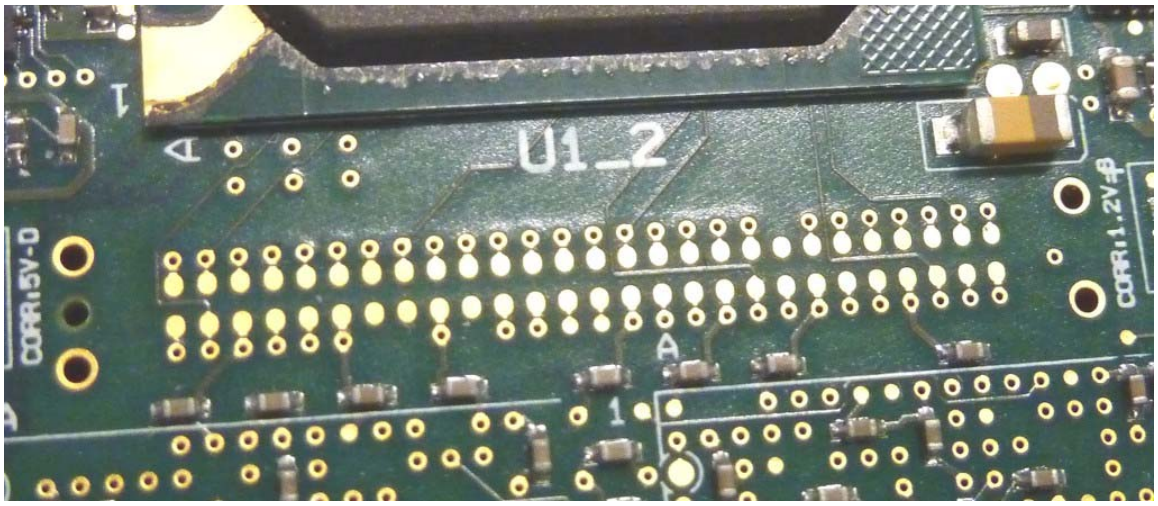

Figure 6-5 J5 header pads on the front of the Baseline Board. Pads A1-A27 run from the lower left to the lower right of the figure, and pads B1-B27 are the row above, running left to right.

The E5406A probe assembly plugs into pods exiting the Agilent 16950A card, plugged into the 16900A logic analyzer. As the clock to the Correlator Chip is running at 32 MHz, it is not possible to clock signals in on the edge of the clock (state timing) without a logic analyzer capable of multiplying the clock up to 256 MHz. Nevertheless, normal

sample timing at 600 MHz is able to clearly show select signals on this interface conforming to the specification (Figure 5-1 of the Correlator Chip RFS A25082N0000).

The pinout table for the soft-touch probe header is given in Table 6-7 below:

Pin	Signal		Pin	Signal
A1	DUMP_EN[0]		B1	GND
A2	SDATA0[3]		B2	SCHID_FRAME_
A3	GND		B3	DUMP_EN[7]
A4	TIMESTAMP		B4	GND
A5	DUMP_EN[6]		B5	SE_CLK[1]
A6	GND		B6	SDATA1[1]
A7	N/C		B7	GND
A8	N/C		B8	PHASE1[3]
A9	GND		B9	DUMP_EN[3]
A10	N/C		B10	GND
A11	PHASE1[1]		B11	SDATA0[2]
A12	GND		B12	DUMP_EN[4]
A13	PHASE0[2]		B13	GND
A14	SE_CLK[0]		B14	DUMP_EN[5]
A15	GND		B15	DVALID[0]
A16	PHASE0[1]		B16	GND
A17	DUMP_EN[2]		B17	DUMP_SYNC
A18	GND		B18	SDATA0[0]
A19	SDATA1[0]		B19	GND
A20	DVALID[1]		B20	N/C
A21	GND		B21	CLOCK (32 MHz)
A22	DUMP_EN[1]		B22	GND
A23	SDATA1[2]		B23	PHASE1[2]
A24	GND		B24	PHASE1[0]
A25	PHASE0[3]		B25	GND
A26	SDATA0[1]		B26	SDATA1[3]
A27	GND		B27	PHASE0[0]

Table 6-7 Agilent test header pads J5 pinouts.

Note that the solder-in header DOES NOT fit under the heatsink, and must be removed if/when the heatsink is installed.

6.12 J16, Reset

J16 is a two-pin 0.100" header, which routes to the front-panel reset switch (CPU Reset, Figure 4-4). When the front panel reset switch is pressed, both pins of J16 are grounded. Normally, a short wire routes from this header to the reset pin of the PC/104+ CPU module.

6.13 USB Port

This is a USB-standard port, routed by cable directly to the CMIB PC/104+ CPU module header. Refer to industry-standard pinout, and the User Manual for more information.

6.14 Front Panel LEDs

All front-panel LEDs are labeled and their association and function is self-evident. Refer to Figure 4-4, and accompanying description, as well as section 5.11 for more information.

6.15 CMIB PC/104+ CPU Module – Kontron Connectors and Problems

The PC/104+ CPU module meets industry-standard requirement for board-stack pluggable connectors, outside dimensions, and hole mounting locations. However, any non-standard connectors can be anywhere and any orientation. This makes it possible, but not without difficulty, in using other manufacturers' PC/014+ CPU modules as replacements, and so replacement manufacturer's modules must be carefully chosen.

This section contains information on the location and pinouts of non-PC/104+ standard connectors on the Kontron MOPSlcdLX module, which are used by the board, or which are used for low-level CPU setup and debug functions.

A cartoon graphic of the Kontron CPU module is shown in Figure 6-6, with connector names, locations, and pin-1 designations.

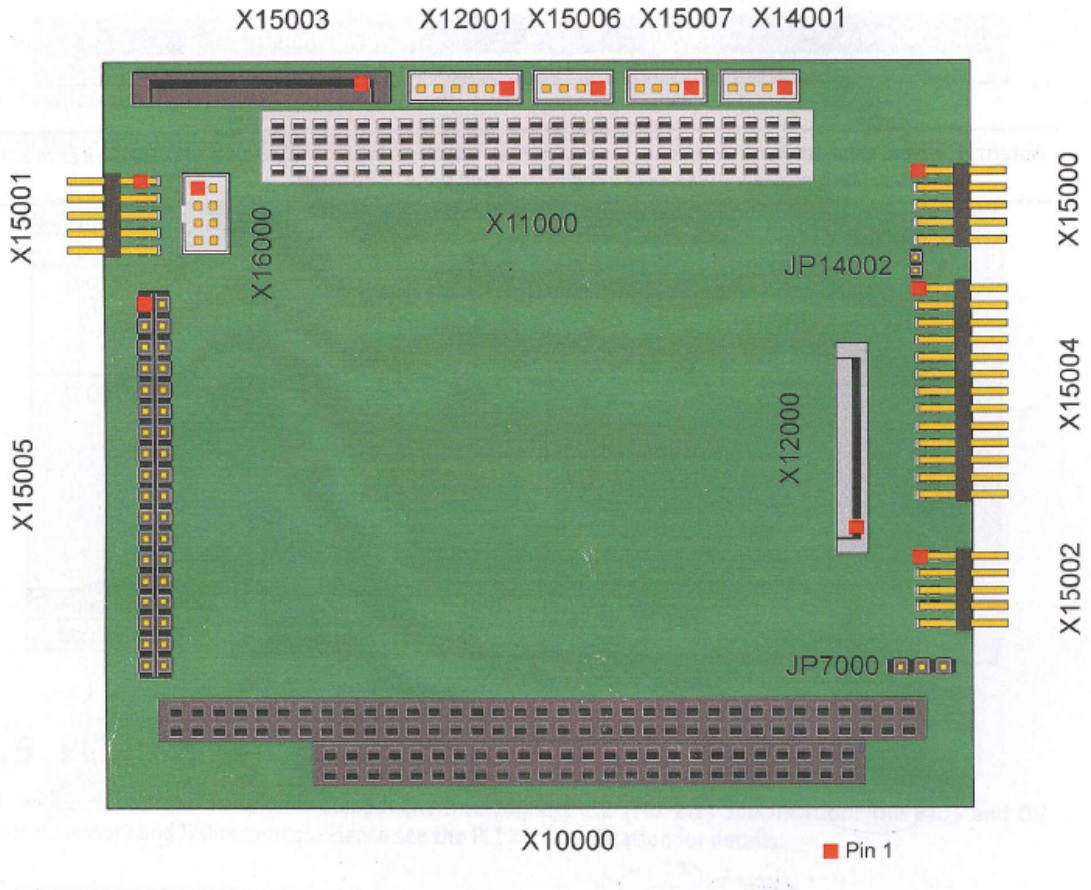

Figure 6-6 Kontron MOPSlcdLX board layout showing connector locations and names.

Connector **X16000** is the 100Base-T Ethernet connector (2 mm, 8 pos, Berg 89361-144 or compatible), which routes via a conversion cable to the front-panel RJ-45 connector.

Connector **X12001** is the CRT monitor connector (1.25 mm, 6 position, Molex 51021-0600 or compatible) and is useful for looking at low-level CPU boot states.

Connector **X15002** is the keyboard connector (0.100", 10 position, AMP 1-215882-0 or compatible) for an AT keyboard, or a PS/2 keyboard.

Connector **X15006** is the USB connector (1.25 mm, 4 position, Molex 51021-0400 or compatible) used for the front-panel USB port.

Connector pinouts are according to the following table:

Pin/Con	X16000 (Eth)	X12001 (CRT)	X15002 (kbrd)	X15006 (USB)
1	TXD+	RED	SPEAKER	VCC
2	TXD-	GRN	GND	USB00
3	RXD+	BLU	/RESIN	USB01
4	SHLDGND	GND	/KBLOCK	GND
5	SHLDGND	VSYNC	KBDAT	
6	RXD-	HSYNC	KBCLK	
7	SHLDGND		GND	
8	SHLDGND		VCC	
9			BATT	
10			PWRGOOD	

Table 6-8 Kontron PC/104+ CPU peripheral connector pinouts.

Refer to the Kontron MOPSlcdLX User's Guide for more detailed information on the board and other connector pinouts.

Additionally, note that the wizards at Kontron decided not to route the X11000 (PC/104+) connector's standard +5V pins to the +5V power supply rail on the board. The +5V pins on this connector are the mechanism the PCMC card uses to deliver +5V to the CPU module. As such, a workaround was developed to route X11000 +5V from the PCMC to the Kontron power connector (not shown in Figure 6-6). Refer to ECO-A25300N0016-25140 for more information. The X11000 connector has press-fit connectivity issues if it is the black connector (refer to ECO-A25300N0047-CPU50_1_SOLDER) and must be soldered. Finally, the X11000 pins can shed gold hairs; the connector should be inspected and cleaned of these hairs every mating cycle.

6.16 XML Protocol

The full XML schema for communicating with the Baseline Board can be found in:

http://www.aoc.nrao.edu/asg/widar/schemata/cmib/baselineBoard/baselineBoard.html

7 Monitor and Control

This section describes MCB addressing, monitor and control functions, and registers for the board, which are not already contained in FPGA or ASIC RFS documents. Refer to section 2 on page 12 for a complete list of RFS documents for devices on the board, except for the U150 MCB FPGA, which is described in this section.

7.1 Baseline Board MCB Memory Map

Chip registers on the Baseline Board, including U150, are accessed by the PC/104+ CPU module in the CMIB stack, via the PCMC FPGA. The PCMC FPGA translates PCI-bus requests to the simplified synchronous MCB bus for accessing devices on the board. The MCB bus exiting the PCMC (CMIB stack) has a chip select, a direction select, a clock, 16 bits of address, and 16 bits of data. The upper 8 bits of address are decoded by U151 to determine which device on the board is accessed. Only the lower 8 bits of the data bus are used on the board. Refer to section 5.7 starting on page 60 for more information.

The following memory map shows the start address (showing all 16 bits of the MCB address bus), for each chip on the board.

Device	Start_ Address		Device	Start Address		Device	Start Address		DEVICE	Start_ Address
LTAc0 r0	0x8000		LTAc5 r0	0xA800		CCc2 r0	0x5000		CCc7 r0	0x7800
LTAc0 r1	0x8100		LTAc5 r1	0xA900		CCc2 r1	0x5100		CCc7 r1	0x7900
LTAc0 r2	0x8200		LTAc5 r2	0xAA00		CCc2 r2	0x5200		CCc7 r2	0x7A00
LTAc0 r3	0x8300		LTAc5 r3	0xAB00		CCc2 r3	0x5300		CCc7 r3	0x7B00
LTAc0 r4	0x8400		LTAc5 r4	0xAC00		CCc2 r4	0x5400		CCc7 r4	0x7C00
LTAc0 r5	0x8500		LTAc5 r5	0xAD00		CCc2 r5	0x5500		CCc7 r5	0x7D00
LTAc0 r6	0x8600		LTAc5 r6	0xAE00		CCc2 r6	0x5600		CCc7 r6	0x7E00
LTAc0 r7	0x8700		LTAc5 r7	0xAF00		CCc2 r7	0x5700		CCc7 r7	0x7F00
LTAc1 r0	0x8800		LTAc6 r0	0xB000		CCc3 r0	0x5800			
LTAc1 r1	0x8900		LTAc6 r1	0xB100		CCc3 r1	0x5900		RecircX-0	0xC800
LTAc1 r2	0x8A00		LTAc6 r2	0xB200		CCc3 r2	0x5A00		RecircX-1	0xC900
LTAc1 r3	0x8B00		LTAc6 r3	0xB300		CCc3 r3	0x5B00		RecircX-2	0xCA00
LTAc1 r4	0x8C00		LTAc6 r4	0xB400		CCc3 r4	0x5C00		RecircX-3	0xCB00
LTAc1 r5	0x8D00		LTAc6 r5	0xB500		CCc3 r5	0x5D00		RecircX-4	0xCC00
LTAc1 r6	0x8E00		LTAc6 r6	0xB600		CCc3 r6	0x5E00		RecircX-5	0xCD00
LTAc1 r7	0x8F00		LTAc6 r7	0xB700		CCc3 r7	0x5F00		RecircX-6	0xCE00
LTAc2 r0	0x9000		LTAc7 r0	0xB800		CCc4 r0	0x6000		RecircX-7	0xCF00
LTAc2 r1	0x9100		LTAc7 r1	0xB900		CCc4 r1	0x6100			
LTAc2 r2	0x9200		LTAc7 r2	0xBA00		CCc4 r2	0x6200		RecircY-0	0xC000
LTAc2 r3	0x9300		LTAc7 r3	0xBB00		CCc4 r3	0x6300		RecircY-1	0xC100
LTAc2 r4	0x9400		LTAc7 r4	0xBC00		CCc4 r4	0x6400		RecircY-2	0xC200
LTAc2 r5	0x9500		LTAc7 r5	0xBD00		CCc4 r5	0x6500		RecircY-3	0xC300
LTAc2 r6	0x9600		LTAc7 r6	0xBE00		CCc4 r6	0x6600		RecircY-4	0xC400
LTAc2 r7	0x9700		LTAc7 r7	0xBF00		CCc4 r7	0x6700		RecircY-5	0xC500
LTAc3 r0	0x9800		CCc0 r0	0x4000		CCc5 r0	0x6800		RecircY-6	0xC600
LTAc3 r1	0x9900		CCc0 r1	0x4100		CCc5 r1	0x6900		RecircY-7	0xC700
LTAc3 r2	0x9A00		CCc0 r2	0x4200		CCc5 r2	0x6A00			

LTAc3 r3	0x9B00		CCc0 r3	0x4300		CCc5 r3	0x6B00		Upper RXP	0x0200
LTAc3 r4	0x9C00		CCc0 r4	0x4400		CCc5 r4	0x6C00		Lower RXP	0x0300
LTAc3 r5	0x9D00		CCc0 r5	0x4500		CCc5 r5	0x6D00			
LTAc3 r6	0x9E00		CCc0 r6	0x4600		CCc5 r6	0x6E00		GigE	0x0100
LTAc3 r7	0x9F00		CCc0 r7	0x4700		CCc5 r7	0x6F00		MCB U150	0x0000
LTAc4 r0	0xA000		CCc1 r0	0x4800		CCc6 r0	0x7000			
LTAc4 r1	0xA100		CCc1 r1	0x4900		CCc6 r1	0x7100			
LTAc4 r2	0xA200		CCc1 r2	0x4A00		CCc6 r2	0x7200			
LTAc4 r3	0xA300		CCc1 r3	0x4B00		CCc6 r3	0x7300			
LTAc4 r4	0xA400		CCc1 r4	0x4C00		CCc6 r4	0x7400			
LTAc4 r5	0xA500		CCc1 r5	0x4D00		CCc6 r5	0x7500			
LTAc4 r6	0xA600		CCc1 r6	0x4E00		CCc6 r6	0x7600			
LTAc4 r7	0xA700		CCc1 r7	0x4F00		CCc6 r7	0x7700			

Table 7-1 Baseline Board MCB memory map.

In Table 7-1, "LTAc*x* r*y*" designators are the array of 64 LTA FPGAs and "CCc*x* r*y*" designators are the array of 64 Correlator Chips. The "RecircX-0:7" and "RecircY-0:7" are the Recirculation Controller FPGAs in the X and Y locations according to Figure 5-1.

Note that for convenience, Start_Addresses for all chips on the board except U150 are shown in the lower right-hand corner of each chip icon of the Baseline Board GUI. Refer to Figure 5-1.

All read/write accesses to all chip registers on the board are 8-bits wide. The **final absolute address** used by application software to access chip registers is formed as follows:

application s/w address = base + (Start_Address + Register_Address) x 4

"**Start_Address**" is the address from Table 7-1.

"**Register_Address**" is the address for the particular chip register from the chip's RFS document, or for U150, from Table 7-2.

"**base**" is a dynamic value that is determined after processor boot via a system call as follows:

After reset (via the front panel hard reset button) or power cycle, the FPGA on the PCMC boots from the on-board PROM. At the same time, the processor on the PC/104+ module boots, and part of its boot process is to go out onto the PCI bus looking for devices.

The PCMC FPGA responds with 3 devices, and for each device returns a "Configuration Space Header", each of which gets stored by the operating system kernel in the /proc/devices directory. The header (refer to Table 5-2 of PCMC RFS document A25145N0000) for each device contains the "Vendor ID" (set to 0x10EE by the PCMC FPGA), the "Device ID", and most importantly the "Base Address" for that device within the processor's total memory space.

*The "**MCB bus**" function (for writing/reading all FPGA registers on the motherboard) is **Device ID 0**. (The "PCI-to-CFG" function (for programming all FPGAs with their personalities on the board) is Device ID 1. The "Monitor/Control" function (for accessing the PCMC A/D converter) is Device ID 2.)*

The upper 3 bits of the Monitor/Control Status register (bits 31:29) indicate the board type that the PCMC is plugged into:

000 – Baseline Board

*The **base** address for each device is acquired with the "pci_get_device" system call.*

For more information on the details of PCI bus to MCB bus translation and PCI devices refer to the PCMC RFS document A25145N0000. For more information on CPU booting, refer to section 7.5.

***Example:** What is the application s/w absolute address of the LTAc0r1 (LTA at column 0, row 1 location) C3SCR register if the base address is 0x20000000? The address is:*

C3SCR address = 0x20000000 + (0x8100 + 0x01) x 4

= 0x20020404

7.2 MCB FPGA U150 Registers and Addresses

The MCB FPGA U150 is the only MCB FPGA on the board that contains MCB read/write registers (refer to section 5.7.1 more detailed information on signals entering/exiting this FPGA). U150 register addresses and functionality is according to the following Table 7-2:

Register Address	Register Name	R/W	Description
0x00	U150 code revision	R	U150 personality revision number. As of this writing, this reads 0x19.
0x01	Slot ID [7:0]	R	LSByte of the slot ID for the board. Obtained from the X-ERNI connector (Table 6-1) Common Backplane.
0x02	Slot ID[15:8]	R	MSByte of the slot ID for the board. Obtained from the Y-ERNI connector (Table 6-2) Common Backplane.
0x03	S/N[7:0]	R	LSByte of the board serial number.
0x04	S/N[15:8]	R	MSByte of the board serial number.
0x05	Monitor Control Reg	R/W	B[7]—1.8 V status; B[6]—all power good flag; B[5:4]—settable status LED (00==OFF; 01==RED; 10==GREEN; 11==YELLOW; B[3:0]—choose source of interrupt: 000==RecircY-0; 001==RecircY-1; …; 100==RecircX-0; …
0x06	Reset Reg 0	R/W	Each bit, if pulled low, resets[2] the associated LTA FPGA, and consequently the Correlator Chip in

[2] Note that resetting any of the FPGAs with this or any other register does not clear the FPGA's personality; it only resets the FPGA to a known starting state and, while held reset, causes switching activity in the chip to stop.

			Column 0. Bit numbers correspond with row numbers.
0x07	Reset Reg 1	R/W	Column 1 LTA FPGA/corr chip reset.
0x08	Reset Reg 2	R/W	Column 2 LTA FPGA/corr chip reset.
0x09	Reset Reg 3	R/W	Column 3 LTA FPGA/corr chip reset.
0x0A	Reset Reg 4	R/W	Column 4 LTA FPGA/corr chip reset.
0x0B	Reset Reg 5	R/W	Column 5 LTA FPGA/corr chip reset.
0x0C	Reset Reg 6	R/W	Column 6 LTA FPGA/corr chip reset.
0x0D	Reset Reg 7	R/W	Column 7 LTA FPGA/corr chip reset.
0x0E	Recirc FPGA Reset Reg Y	R/W	Each bit, if pulled low, resets the associated 'Y' Recirculation Controller FPGA. Bit numbers correspond to row numbers.
0x0F	Recirc FPGA Reset Reg X	R/W	Each bit, if pulled low, resets the associated 'X' Recirculation Controller FPGA. Bit numbers correspond to column numbers.
0x10	GigE+RXP FPGA Reset Reg	R/W	Bit 0, if pulled low, resets the Gigabit Ethernet FPGA. Bit 1, if pulled low, resets the Upper RXP FPGA, and Bit 2, if pulled low, resets the Lower RXP FPGA.

Table 7-2 MCB FPGA U150 registers, its addresses, and functions.

7.3 Baseline Board PCMC (FPGA Programming, Voltage, Temp Monitor)

The CMIB PC/104+ CPU module communicates with board chip registers via the PCMC FPGA. The PCMC card, sandwiched between the PC/104+ and the motherboard, is the gateway for programming the FPGAs on the board, as well as containing an A/D converter for voltage and temperature monitoring.

7.3.1 FPGA Programming

The FPGAs on the Baseline Board are programmed in **1-bit serial mode**. The Correlator Chips are custom ASICs and thus are not programmable. It is possible to program every FPGA on the board with a different bitstream, as their programming data paths are all daisy-chained. In all cases, the final bitstream must contain binaries for each device in the daisy-chain, whether it has a different bitstream (i.e. design) or not. Refer to appendices for each Baseline Board FPGA RFS for information on how the final bitstream file for each type of FPGA is put together.

There are 12 "PROG" lines, PROG[11:0], originating on the PCMC that enable groups of FPGAs to be programmed. These lines are accessed by writing to the "Control" register for the Function-1 "PCI-to-CFG Bridge" function on the PCMC FPGA (Table 5-8 of the PCMC RFS A25145N0000). Asserting PROG lines (pulling the bit low in the Control register), one at a time, according to Table 7-3 (with lines entering the motherboard on the CMIB stack connector J10 as defined in Table 6-3), enables programming of the indicated FPGAs.

Once the correct PROG line is pulled low and then pulled high, configuration data is written to the PCMC "PCI-to-CFG Bridge" "Port Register" bit 0, least-significant bit first (from the bit stream file) for the FPGA or group of FPGAs that are to be programmed with the personality according to Table 7-3:

PROG	FPGA
0	MCB Fan-out
1	RXPs
9:2	LTAs (cols 7:0)
10	Recircs
11	GigE

Table 7-3 Baseline Board PROG lines indicating which FPGAs are enabled for programming.

The MCB Fan-out FPGAs must be programmed first to enable other FPGAs on the board to be programmed.

Once all of the programming bits are written for a particular group or daisy chain of FPGAs, the associated DONE line is checked by reading bits in the "Status" register of the PCI-to-CFG Bridge function on the PCMC FPGA. If the associated DONE bit is set (1), the FPGA or group of FPGAs has been successfully programmed. If not, there has been a programming problem. Once all of the DONE bits are set, all of the logic on the board is ready for configuration and operation.

Note that the CMIB CPU always looks for the FPGA binaries on a remote file system under '/opt/widar/fpga/bb' (it looks specifically for "bb_mcbfanout.bin", "bb_rxp.bin", "bb_lta.bin", bb_recirc.bin", "bb_recirc_ramtest.bin", and "bb_gbit.bin"). These then get copied to the CPU's local (RAM) filesystem at boot time into '/tmp/fpga', which are then used for programming the FPGAs. If new binaries are installed, the CPU must be rebooted to "pick them up", or the Startup Sequencer must be run with the "FPGA Bin Dir:" set to the location of the binaries (/opt/widar/fpga/bb, or another location if desired).

7.3.2 PCMC A/D Converter Readings

Acquisition of voltage and temperature monitor points on the Baseline Board is performed by reading the PCMC A/D converter. Refer to the PCMC FPGA RFS A25145N0000 "Function-2" Table 5-10 and supporting description for more information on ADC channel access.

Voltages and temperatures on the Baseline Board are assigned to PCMC A/D channels according to Table 5-6 in this document. 8-bit reading conversion factors are also provided.

The 64 Correlator Chip ASIC core voltages are obtained by routing the voltages through an analog switch (actually dual 32:1 analog switches), and then to PCMC A/D channel 6. Selection of which voltage is selected with the analog switch(es) is done by writing the

"AMUX" register of Y-7 Recirculation FPGA. Refer to Table 5-8 of the Recirculation FPGA RFS A25090N0000 for detailed information on AMUX register settings-to-Correlator Chip core voltage selection.

7.3.3 In-system Programming of the PCMC FPGA EEPROM

The PCMC card in the CMIB stack contains an FPGA and on-board EEPROM. On power-up, the FPGA boots automatically from the EEPROM. If a new binary must be installed in the EEPROM, press the "PCMC" icon on the Baseline Board GUI, to bring up the PCMC GUI. Check ON the "Enable PCMC PROM for Programming" box, and press the "Program PCMC" button. For this to work, there must be a "pcmc.svf" programming file in the mounted "/opt/widar/fpga/bb" directory that the CMIB sees. Programming takes awhile, and the GUI gives a message indicating when programming is complete. If programming fails (the EEPROM gets corrupted), then the EEPROM must be programmed via the front panel connector. See section 6.5 for more information.

7.4 Baseline Board 10 msec Interrupt

Once a particular Recirculation FPGA has acquired lock to an incoming CTRL-TIMECODE signal, it generates a 10 msec pulse, synchronous with MCB_CLK, and synchronized to the TIMECODE T-bit. All 16 of these pulses (ticks) are fed into MCB FPGA U150 (Table 5-1), and a single source is selected by the CPU by writing to the Monitor and Control Reg of U150 (Table 7-2). This single pulse is then routed to pin D25 (Table 6-3) for routing to the PCMC FPGA and, if enabled, to interrupt the PC/104+ CPU. Refer to the PCMC FPGA RFS (A25145N0000) for details on how this signal is handled and routed on the PCMC card.

7.5 CMIB PC/104+ CPU Boot

The PC/104+ CPU module (Kontron MOPSlcdLX-PC104-3 or MOPSlcdLX-PC104-5) uses "pxeboot", an Intel/DHCP protocol that allows a computer to request a boot image from the boot server. See:

http://www.pix.net/software/pxeboot/archive/pxespec.pdf

for more information.

When the board powers up, is soft-re-booted, or is reset by pressing the front-panel reset switch, the boot request goes out to the network, and provided a boot host is listening, the host returns a boot image to the board. This boot image gets the board booted to a point where it can mount a root file system (RFS). This mounted file system (Linux), contains the required startup files so the board can finish its booting and configuration onto the network.

For all of this to work, the CPU's BIOS (accessed by using the video and keyboard ports of the PC/104+ module), must be set to enable "lanboot" or "pxeboot" as the first device tried for booting.

After the board is booted and has its core OS services running, the user software (all of the software tasks that monitor and control the board), is loaded and run. This also involves loading the MCB bus device driver for the PCMC (refer to the PCMC RFS A25145N0000, for information on PCMC devices).

After the PCMC MCB bus device driver is loaded, the board type (see the note box on page 90) is determined. Next, the MCB FPGAs (U150-U153) are programmed (see section 7.3.1), and the "slot ID" information (i.e. its rack-crate-slot) is read from U150 (Table 7-2). These IDs are used to form the last two octets of the CPU's IP address, 10.80.xxx.yyy. "Crate" and "slot" are used to form the lower octet; crate-0 (upper) sets yyy=100-107, and crate-1 (lower) sets yyy=200-207, the last digit being the slot number. The "xxx" octet of the IP is based on the rack number. Baseline Boards (racks 101-108) get assigned octet 210 + rack number = 211 to 218 (Station Boards get assigned to 200 + rack number = 200-208).

A network lookup is then used to translate a non-raw IP address, to the assigned IP address. Typically a board is addressed logically as "rack-crate-slot.evla.nrao.edu" (e.g. b101-t-0.evla.nrao.edu is the board in the top crate, slot 0, of rack 101), but can also be accessed by its serial number (e.g. "bb2006.evla.nrao.edu").

7.6 Baseline Board Startup

The "Startup Sequencer" GUI, launched from the main board GUI ("Startup Board" icon of Figure 5-1) handles proper startup sequencing of the board. The basic steps are as follows:

1. Test the Recirculation FPGA external RAM. This is an optional test, and the Recirculation FPGAs (only) must be booted with a temporary bitstream (refer to section 8, Appendix I, of the Recirc FPGA RFS A25090N0000 for information on register access) to run this test. It has been found in testing that this test can pass, but other high-speed tests fail[3], and so this test only gives an indication that connection to the RAM (and the RAM itself) is ok, and is not normally run. This is "**Recirc RAM Test**" in the Startup Sequencer GUI.

2. Boot the FPGAs, in order of MCB[4], LTA, RXP, Recirc, and GigE. The GigE FPGA is booted last, as it provides the clocks for all LTAs and Correlator Chip Accel regulators on the board. This is "**FPGA Boot**" in the Startup Sequencer GUI. Refer to section 7.3.1 for information on FPGA programming.

3. Startup the RXPs, by turning on their HM Gbps receivers, and wait for lock on at least wafer 0, 4, 8, or 12 AND wafer 16, 20, 24, or 28 to be established. These wafers must be active (and wafers 0 and 16 must have 128 MHz clocks, or the

[3] Found due to malfunctioning SRAM drivers; they run ok at low speed, but not at high speed.
[4] The MCB FPGAs are automatically configured as part of the CPU boot sequence, and are re-configured in this step.

External Clock is used) to continue beyond this point. This is "**RXP Start**" in the Startup Sequencer GUI.

4. Startup the Recirc FPGA, by turning on their HM Gbps receivers, wait for lock to be established on at least one CTRL-TIMECODE and one BB input on each chip. This is "**Recirc Start**" in the Startup Sequencer GUI.

5. Sequentially startup the Correlator Chips by sequencing their power up via the LTA (refer to Figure 5-10), and releasing of PLL and then CC reset lines. This is "**LTA/CC Start**" in the Startup Sequencer GUI.

6. Turn all the Recirc FPGAs into "Test Vector" generator mode (box H Figure 5-5), and turn all Correlator Chips into Test Vector receiver mode ("TVEN" box A Figure 5-8). Run clock phase calibration by following the instructions in section 5.4.1.31 (FCPCR register) of the Recirc FPGA RFS A25090N0000. This is "**CC Array Test Vectors**" in the Startup Sequencer GUI.

7. Set the GigE FPGA for desired operating mode, source, and destination addresses. This is "**GigE Start**" in the Startup Sequencer GUI.

8. Finally, configure the board according to desired settings, optionally, from a board configuration file. This is "**CC/Recirc Config**" in the Startup Sequencer GUI. Note that this step sets *all* FPGA and Correlator Chip configurations from a file, not just the Correlator Chip and Recirc FPGAs as is indicative of the name.

8 Jumper Settings and Board Configurations

This section defines any user-settable jumpers and board configurations.

8.1 CMIB JTAG Bypass, JP1

This jumper is installed for manufacturing JTAG test only, and must be removed for normal operation. It is located on the front side of the board, lower edge, right beside the CMIB stack connector J10.

8.2 Thermal Shutdown Bypass, JP5

This jumper is located on the rear side of the board, near the top edge towards the left. If installed, it disables thermostat thermal shutdown. This jumper must never be installed for normal operation, as it overrides thermal overload protection, and could lead to board self-destruction.

8.3 JTAG TCK, TMS Source Selectors, JP6-JP9

These jumpers are located on the front side of the board, lower left, near the SFP cages. They are used to select the source of the board's TCK and TMS lines. During normal operation, the TCK line sources from the GigE FPGA and provides the Correlator Chip POL Accel regulators with their reference clocks. Also during normal operation, the TMS line sources from the GigE FPGA, and contains signaling to ensure that the attached Correlator Chips keep from going into internal test mode. JP6 and JP9, if installed ensure these signals source from the GigE FPGA.

Jumpers JP6 and JP9 MUST BE INSTALLED, and jumpers JP7 and JP8 MUST NOT BE INSTALLED for normal operation.

8.4 Board Serial Number Setting

There are 14 resistors, R224-R237, located on the front side of the board under the CMIB stack, which are used for setting the board's serial number. If a resistor is installed, then the particular bit that the resistor represents is a binary '1', and if the resistor is not installed, then the bit is a binary '0'. These 14 bits (bits 15 and 16 are set to 0), are read by the CPU via U150 registers (see Table 7-2, addresses 0x03 and 0x04).

Resistor to binary bit assignments are physically aligned on the board, reading left to right. For clarity, the assignments are as follows:

R237:R232 – bits 13:8
R231:R224 – bits 7:0

A picture of the resistors on the board is shown in Figure 8-1 below:

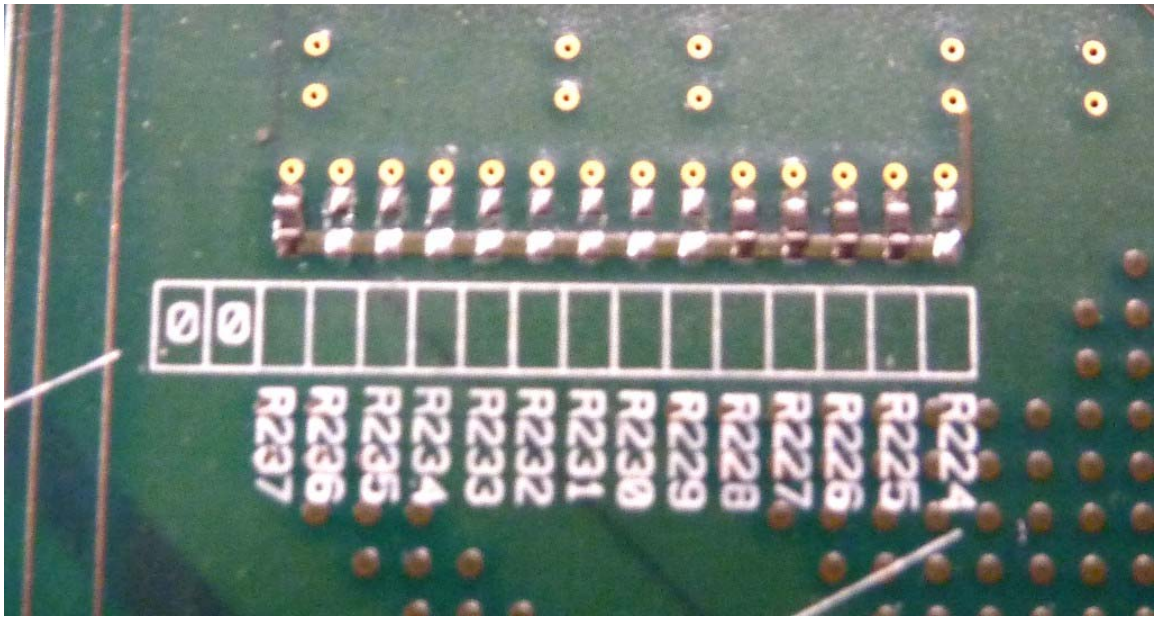

Figure 8-1 Resistors on the front side of the board, under the CMIB stack, for setting the board serial number. Binary bits in the serial number are read from left to right. If a resistor is installed, the binary bit is '1'.

8.5 Activating the 10G XPAK Interface

Refer to section 8.1 of the V2 GigE FPGA RFS document A25092N0001 for detailed information on what board modifications are required to activate the 10G XPAK interface on the board.

8.6 Setting the Y-ERNI Connector for Inputs

Refer to section 9.3.1 of the Recirculation FPGA RFS document A25090N0000 for detailed information on what board modifications are required to set the Y-ERNI connector for inputs.

9 DC and Switching Characteristics

This section contains board-level DC and switching characteristics.

9.1 Power Supply, Control, and Thermal Shutdown

Parameter	Min	Typical	Max
-48 VDC supply voltage[5]	-36 V	-48 V	-58 V
-48 VDC supply current	2 A[6]	11 A	14.7 A
-48 VDC peak voltage transient, at peak surge current of 15.5 A for 1 msec[7]. The power supply can withstand 100 V, 100 msec surges.			-97 V
Total board power dissipation	120 W[8]	480 W	530 W[9]
Input conducted ripple and noise tolerance[10]		(EN61000-4-6 10 V)	
Output conducted EMI (standard LISN)		FCC Class B; peak of 62 dBµV @ SMPS fund. of 486 kHz	
CONTROL voltage V_{IH}	3.5	4.0	5.0
CONTROL voltage V_{IL}		0.8	
CONTROL current		8 mA @ 4V	
CONTROL filter time constant		3.7 msec	
MONITOR voltage V_{OH} (1 k-ohm source impedance)		3.3 V	
MONITOR voltage V_{OL} @ -50 mA[11]		0.55 V	
Thermal shutdown heatsink trip temp	60 C	65 C	70 C
Thermal shutdown heatsink reset temp	45 C	60 C	
PWR connector, current rating per contact. (ERNI 114403 data sheet).		4.7 A[12]	12.6 A (7.3[13])

Additional notes:

1. The CONTROL pin is in the TOP power connector (Figure 4-2), and the MONITOR pin is in the BOTTOM power connector.
2. Reverse voltage protection is provided by the transorbs and 10 A fuses on each power connector; the fuse will blow with reverse voltage applied.

[5] Min: LQS100A48-1V2RE power supply data sheet; Max: 60 WVDC Bourns transorb.
[6] Quiescent power, no FPGAs booted, maximum supply voltage.
[7] Bourns CD214C-T60A transorb data sheet.
[8] Quiescent power, no FPGAs booted.
[9] RXP "Test Pattern" vectors, recirculation active.
[10] LQS100A48-1V2RE power supply data sheet.
[11] Zetex BCW60D transistor data sheet.
[12] Actual nominal case, under maximum power, 56 V operation.
[13] Actual worst-case load, under maximum power, minimum voltage conditions.

9.2 SMA External Clock In

Parameter	Min	Typical	Max
128 MHz input levels (sine)	-6 dBm	0 dBm	+9 dBm
128 MHz input levels (square) (pk-pk)	200 mV	600 mV	2400 mV
128 MHz input cycle-cycle jitter tolerance (pk-pk)[14]			1 ns
128 MHz input frequency	100 MHz	128 MHz	132[15] MHz
Termination impedance		50 ohm	

Note: this input is AC-coupled.

9.3 X-ERNI Connector

All differential inputs utilize FPGA differential 100 ohm on-chip termination, and are DC-coupled, but come complete with 1.2 V DC bias via 1 k-ohm pullup on one side to +1.2 V. All differential outputs are AC-coupled, with specifications given for a 100 ohm differential load/termination. This is in keeping with the EVLA correlator system method wherein outputs are AC-coupled, inputs are DC-coupled, and inputs also establish DC bias. Refer to section 6.1 for connector pinouts and pin names, and clock termination information.

Parameter	Min	Typical	Max
128 MHz clock input level[16] (pk-pk) (U-CLK, L-CLK)	200 mV	700 mV	1800 mV
128 MHz clock input cycle-cycle jitter tolerance (pk-pk)			1 ns
128 MHz clock input frequency	100 MHz	128 MHz	132 MHz
CTRL/BB0/BB1 inputs levels (pk-pk)	200 mV	700 mV	1800 mV
CTRL/BB0/BB1 input cycle-cycle jitter tolerance[17] (pk-pk)	0.44 UI (430 ps)		
CTRL/BB0/BB1 data rate		1024 Mbps	1056 Mbps
U/L-CLKo output clock level (pk-pk)	500 mV		900 mV
U/L-CLKo output cycle-cycle jitter (pk-pk)		100 ps	250 ps
U/L-PDo output level	500 mV		900 mV
U/L-PDo output cycle-cycle jitter (pk-pk)			200 ps

[14] Altera Stratix-II data sheet, Enhanced PLL, High Bandwidth setting.
[15] Set by the maximum timing margin achieved in the RXP and Recirc FPGA compile.
[16] Altera Stratix-II data sheet, LVDS input, 2.5 V bank.
[17] Altera defines it this way, but jitter should not exceed this limit for reliable operation.

9.4 Y-ERNI Connector

All specifications are into a 100 ohm differential load. All outputs are AC-coupled.

Parameter	Min	Typical	Max
128 MHz CLK output level[18] (pk-pk)	500 mV		900 mV
128 MHz CLK output cycle-cycle jitter (pk-pk)		100 ps	250 ps
CTRL/BB0/BB1 output level[19] (pk-pk)	800 mV	1200 mV	1600 mV
CTRL/BB0/BB1 output cycle-cycle jitter (pk-pk)			200 ps

9.5 SFP1, SFP2

These specifications apply to the signals between the SFP connectors and the GigE FPGA. The actual line output of the installed SFP module is dependent on the particular specification of the SFP module, and is therefore beyond the scope of this document.

Parameter	Min	Typical	Max
TX 1.25 Gbps differential voltage (pk-pk)	350 mV[20]	800 mV	1600 mV
TX 1.25 Gbps cycle-cycle jitter (pk-pk), measured at zero-crossing.		150 ps	136 ps[21]
TX eye opening, 400 mV pk-pk, measured.		560 ps	
RX 1.25 Gbps differential (pk-pk), from Finisar FCMJ-8520-3 SFP		800 mV	
RX 1.25 Gbps cycle-cycle jitter (pk-pk), measured at zero-crossing. From Finisar FCMJ-8520-3 SFP.		200 ps	
RX eye opening, 400 mV pk-pk, measured. From Finisar FCMJ-8520-3 SFP.		500 ps	
RX differential voltage swing pk-pk[22]	170 mV		2000 mV
RX cycle-cycle total jitter tolerance pk-pk.[23]			568 ps

[18] Altera Stratix-II data sheet, LVDS, 2.5 V bank.
[19] Altera Stratix-II data sheet, HyperTransport level.
[20] Min and max specs from the Altera Stratix-GX data sheet; typical is measured value.
[21] Max specs from the Altera Stratix-GX data sheet; typical is measured value.
[22] Altera Stratix-GX data sheet.
[23] Altera Stratix-GX data sheet.

9.6 XPAK XAUI Interface

These specifications apply to the signals between the XPAK connector (see section 6.9), and the GigE FPGA, with board modifications performed to enable the XPAK connector, and with a suitable XPAK 10GBASE-*n* transponder installed. The actual line output of the installed XPAK module is dependent on the particular specification of the XPAK module, and is therefore beyond the scope of this document.

Parameter	Min	Typical	Max
TX 3.125 Gbps differential voltage (pk-pk)	350 mV[24]	600 mV	1600 mV
TX 3.125 Gbps cycle-cycle jitter (pk-pk), measured at zero-crossing.		80 ps	102 ps[25]
TX eye opening, 400 mV pk-pk, measured.		200 ps	
RX 3.125 Gbps differential (pk-pk), from XPAK transponder.		700 mV	
RX 3.125 Gbps cycle-cycle jitter (pk-pk), measured at zero-crossing. From XPAK transponder.		75 ps	
RX eye opening, 400 mV pk-pk, measured. From XPAK transponder.		195 ps	
RX differential voltage swing pk-pk[26]	170 mV		2000 mV
RX cycle-cycle total jitter tolerance pk-pk.[27]			208 ps

9.7 M&C 100Base-T Ethernet Port

The RJ-45 front-panel connector routes directly to the CMIB PC/104+ CPU board. Refer to the CPU board manufacturer's data sheet for information on this port.

9.8 USB Port

The USB front-panel connector routes directly to the CMIB PC/104+ CPU board. Refer to the CPU board manufacturer's data sheet for information on this port.

[24] Min and max specs from the Altera Stratix-GX data sheet; typical is measured value.
[25] Max specs from the Altera Stratix-GX data sheet; typical is measured value.
[26] Altera Stratix-GX data sheet.
[27] Altera Stratix-GX data sheet.

10 Physical, Environmental, and Reliability Specifications

10.1 Baseline Board Physical Parameters

Weight with heatsink: 21.75 lbs (9.7 kgs).

Weight without heatsink: 8.25 lbs (3.7 kgs).

PCB outside dimensions: 15.748" W x 19.687" H (400 mm x 12U).

Slot width, with front panel and heatsink: 2.40"

Front panel outside dimensions: 2.40" W x 20.83" H

Front-panel left-most edge, to rear side of PCB: 0.6886"

PCB thickness: 0.125"

Critical dimensions for the baseline board, front panel, and front panel-to-PCB, are shown in Figure 10-1. Not shown on the drawing is a carrying handle attached to the front panel, the heatsink and its carrying handle, and all of the front-panel cabling, connectors and hardware. Refer to the Baseline Board exploded assembly drawing, and related mechanical drawings for more detailed physical information.

Note that there is a 0.100" copper "keep-out boundary" on all PCB layers along the top and bottom edges of the board, to prevent any possibility of PCB copper from shorting out to metal guide rails.

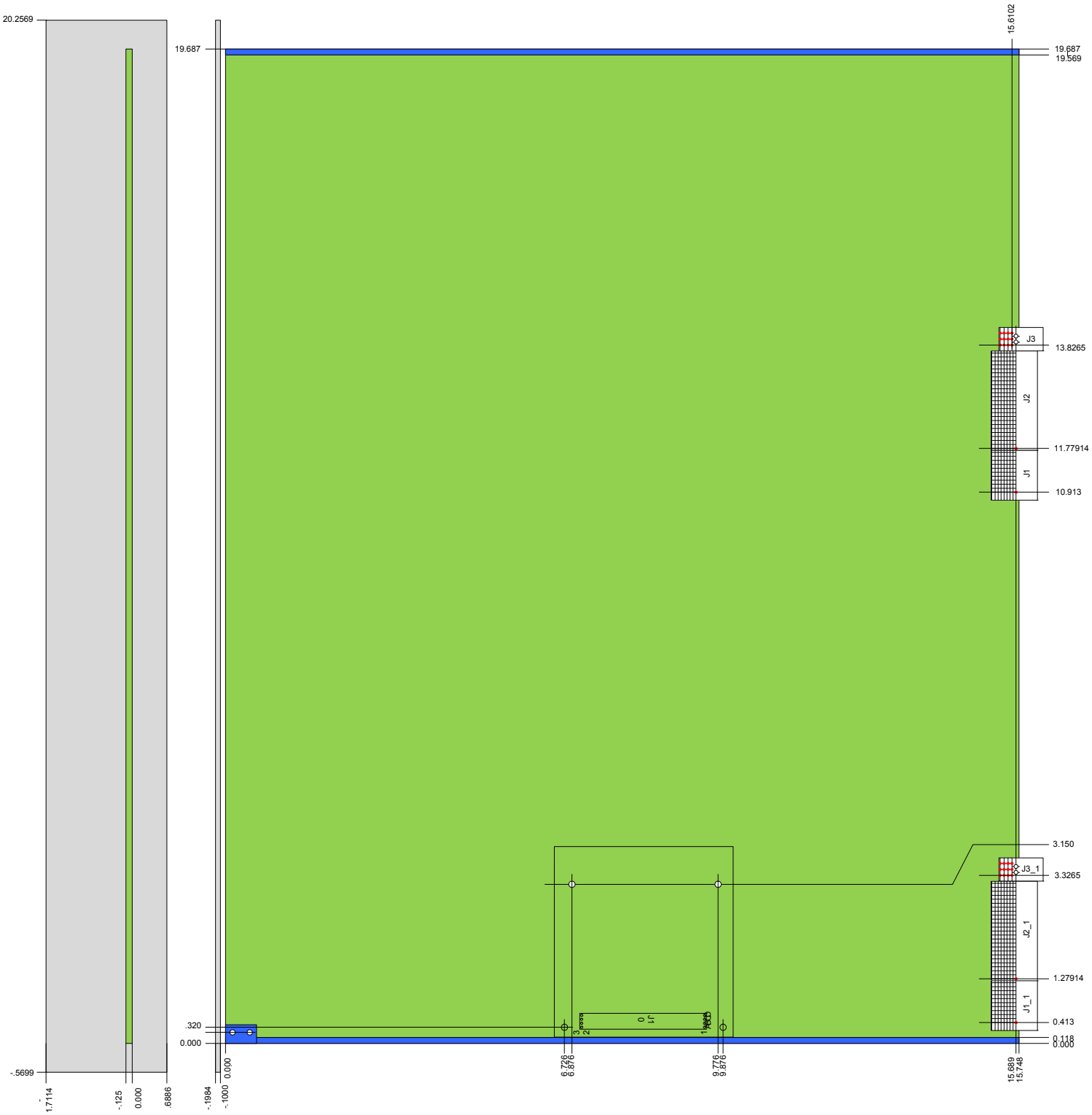

Figure 10-1 Baseline Board and front panel/location critical dimensions.

10.2 Environmental Specifications

Minimum operating ambient temperature: 0 ^{o}C, non-condensing.

Maximum operating ambient temperature: +40 ^{o}C. This limit is imposed by chips on the CMIB Kontron PC/104+ CPU module. The board itself, with heatsink attached, can withstand an ambient operating temperature of 50 ^{o}C, with adequate airflow, holding the heatsink temperature at ~60-62 ^{o}C, just below thermal shutdown. Although normally, for reliable operation, the maximum ambient temperature should not exceed 40 ^{o}C, and the measured heatsink temperature should be kept below 50 ^{o}C.

Minimum storage temperature: -10 ^{o}C.

Maximum storage temperature: +85 ^{o}C.

Nominal airflow requirement bottom to top of the board, across all surfaces: 10-15 LFM. The board (via the heatsink-mounted thermostats) and on-board power supplies are thermally protected, and so if inadequate airflow is provided, the board and/or power supplies will shutdown.

Maximum operating altitude: 10,000 ft.

Operating orientation: any.

Humidity: minimum 30%, maximum 60% R.H. For ESD risk minimization.

ESD handling protection: The board must never be handled or placed on any surfaces that are not static-dissipative, with an absolute maximum impedance of 10^{10} ohms (preferably 10^{9} ohms) to earth ground.

Dust and contamination: Should be kept to minimum to avoid possible shorting of fine pitch leads/pins. ISO 14644-1 class 8 is the required air quality specification, which is the correlator room specification requirement (RFS document A25012N0000).

10.3 Reliability Estimates

The most un-reliable components on the boards are likely the ¼-brick DC-DC power supplies. The manufacturer (Artesyn) specs these LQS-series power supplies as having an MTBF of 3.9 Mhrs, according to Telcordia Tech SR-332 standard.

A survey of FPGA manufacturers' data indicates that the nominal failure rate is ~50 FITs, or an MTBF of 20 Mhrs. The Correlator Chip ASIC original specification and reliability study indicated a similar failure rate of ~50 FITs. The Telcordia prediction for the Kontron CPU is an MTBF of ~390,000 hours.

Total approximate MTBF, including only the power supplies and FPGAs/ASICs is ~75,000 hours, or 8.5 years, not including any other devices on the board. The correlator

system reliability report #1 (A25010N0003, Report #1), based on a mixture of MIL-217B, Telcordia SR-332, and manufacturers' data, indicates an MTBF for the Baseline Board of 56,000 hours or 6.4 years, or rather there is a 60-90% chance that the MTBF is greater than 6.4 years. In the EVLA system with 128 operating boards, therefore, it would not be unexpected to have some sort of Baseline Board failure every ~18 days, if these reliability predictions are approximately correct.

An independent study [4] of the Baseline Board bare PCB (manufactured by Merix) was performed by the contract manufacturer, BreconRidge (now Sanmina-SCI), to test for compliance to IPC6012. The conclusion of the report states:

- *The IPC testing performed by Merix and data demonstrates their PWB manufacturing compliance to IPC 6012.*
- *The Merix boards had acceptable as-received bow and only slightly exceed the twist limit for one out of three PWB's (IPC 2221). This did not cause any issues during SMT assembly.*
- *After SMT assembly, the bow did increase. Whether this will have negative impact will have to be determined at the next level assembly. If this does prove to be an issue, further evaluation of the board design and SMT assembly process will be required.*
- *IST testing (Interconnect Stress Test) was performed on four types of IST coupons which included PTH, via and blind via structures. These coupons use the same drill sizes and PWB stack-up that was used for the Baseline board manufacture. No failures, significant resistance changes or interconnect cracking were found during or after testing. These results demonstrate the robustness of the PWB technology used to manufacture the Baseline boards.*

11 FPGA Pinouts, Programming, and Packaging Information

Pinouts, programming, and packaging information for all FPGAs and ASICs on the board, except for the MCB FPGAs U150-U153, can be found in the relevant RFS documents, as referenced in section 2.

11.1 U150 MCB FPGA Pinouts

This section contains an exhaustive chip pinout listing generated by the Quartus-II FPGA compiler, and the Quartus-II pin planner graphic. The U150 MCB FPGA is implemented in an Altera Cyclone EP1C12F256C6 FPGA, and compiles with the Quartus-II V9.1 compiler.

Pin Name/Usage	Location	Dir.	I/O Standard	Voltage	I/O Bank
GND	A1	gnd			
CORR_RESET_n[61]	A2	output	2.5 V		2
VCCIO2	A3	power		2.5V	2
CORR_RESET_n[58]	A4	output	2.5 V		2
GND	A5	gnd			
CORR_RESET_n[55]	A6	output	2.5 V		2
VCCINT	A7	power		1.5V	
CORR_RESET_n[52]	A8	output	2.5 V		2
IP[3]	A9	input	2.5 V		2
VCCINT	A10	power		1.5V	
IP[0]	A11	input	2.5 V		2
GND	A12	gnd			
IP[13]	A13	input	2.5 V		2
VCCIO2	A14	power		2.5V	2
IP[10]	A15	input	2.5 V		2
GND	A16	gnd			
CORR_RESET_n[63]	B1	output	2.5 V		1
CORR_RESET_n[62]	B2	output	2.5 V		2
CORR_RESET_n[60]	B3	output	2.5 V		2
CORR_RESET_n[59]	B4	output	2.5 V		2
CORR_RESET_n[57]	B5	output	2.5 V		2
CORR_RESET_n[56]	B6	output	2.5 V		2
CORR_RESET_n[54]	B7	output	2.5 V		2
CORR_RESET_n[53]	B8	output	2.5 V		2
IP[2]	B9	input	2.5 V		2
IP[1]	B10	input	2.5 V		2
IP[15]	B11	input	2.5 V		2
IP[14]	B12	input	2.5 V		2
IP[12]	B13	input	2.5 V		2
IP[11]	B14	input	2.5 V		2
IP[9]	B15	input	2.5 V		2
IP[8]	B16	input	2.5 V		3
VCCIO1	C1	power		2.5V	1
RECIRC_RESET_n[15]	C2	output	2.5 V		1
INTERRUPT_IN[14]	C3	input	2.5 V		1
RECIRC_RESET_n[14]	C4	output	2.5 V		2
INTERRUPT_IN[13]	C5	input	2.5 V		2
RECIRC_RESET_n[13]	C6	output	2.5 V		2
INTERRUPT_IN[12]	C7	input	2.5 V		2
RECIRC_RESET_n[12]	C8	output	2.5 V		2
INTERRUPT_IN[7]	C9	input	2.5 V		2

INTERRUPT_IN[6]	C10	input	2.5 V			2
INTERRUPT_IN[5]	C11	input	2.5 V			2
INTERRUPT_IN[0]	C12	input	2.5 V			2
INTERRUPT_IN[1]	C13	input	2.5 V			2
INTERRUPT_IN[2]	C14	input	2.5 V			3
INTERRUPT_IN[3]	C15	input	2.5 V			3
VCCIO3	C16	power		2.5V		3
INTERRUPT_IN[15]	D1	input	2.5 V			1
MCB_CLK_F[27]	D2	output	2.5 V			1
MCB_CLK_F[25]	D3	output	2.5 V			1
INTERRUPT_IN[11]	D4	input	2.5 V			1
MCB_CLK_F[24]	D5	output	2.5 V			2
MCB_CLK_F[23]	D6	output	2.5 V			2
MCB_CLK_F[21]	D7	output	2.5 V			2
RECIRC_RESET_n[0]	D8	output	2.5 V			2
RECIRC_RESET_n[1]	D9	output	2.5 V			2
MCB_CLK_F[19]	D10	output	2.5 V			2
MCB_CLK_F[17]	D11	output	2.5 V			2
RECIRC_RESET_n[10]	D12	output	2.5 V			2
MCB_CLK_F[15]	D13	output	2.5 V			3
MCB_CLK_F[13]	D14	output	2.5 V			3
MCB_CLK_F[10]	D15	output	2.5 V			3
INTERRUPT_IN[4]	D16	input	2.5 V			3
MCB_CLK_F[29]	E1	output	2.5 V			1
MCB_CLK_F[28]	E2	output	2.5 V			1
MCB_CLK_F[26]	E3	output	2.5 V			1
RECIRC_RESET_n[11]	E4	output	2.5 V			1
RECIRC_RESET_n[6]	E5	output	2.5 V			2
MCB_CLK_F[22]	E6	output	2.5 V			2
MCB_CLK_F[20]	E7	output	2.5 V			2
INTERRUPT_IN[8]	E8	input	2.5 V			2
MCB_CLK_F[1]	E9	output	2.5 V			2
MCB_CLK_F[18]	E10	output	2.5 V			2
INTERRUPT_IN[10]	E11	input	2.5 V			2
MCB_CLK_F[16]	E12	output	2.5 V			2
MCB_CLK_F[14]	E13	output	2.5 V			3
MCB_CLK_F[12]	E14	output	2.5 V			3
MCB_CLK_F[9]	E15	output	2.5 V			3
INTERRUPT_IN[9]	E16	input	2.5 V			3
MCB_CLK_F[30]	F1	output	2.5 V			1
RECIRC_RESET_n[3]	F2	output	2.5 V			1
RECIRC_RESET_n[4]	F3	output	2.5 V			1
RECIRC_RESET_n[5]	F4	output	2.5 V			1
CORR_RESET_n[30]	F5	output	2.5 V			1
GND	F6	gnd				
VCCIO2	F7	power		2.5V		2
GND	F8	gnd				
GND	F9	gnd				
VCCIO2	F10	power		2.5V		2
GND	F11	gnd				
MCB_CLK_F[4]	F12	output	2.5 V			3
MCB_CLK_F[5]	F13	output	2.5 V			3
MCB_CLK_F[6]	F14	output	2.5 V			3
MCB_CLK_F[7]	F15	output	2.5 V			3
RECIRC_RESET_n[9]	F16	output	2.5 V			3
RESET_n	G1	input	2.5 V			1
CORR_RESET_n[36]	G2	output	2.5 V			1
CORR_RESET_n[34]	G3	output	2.5 V			1
PWR_1V8	G4	input	2.5 V			1
CORR_RESET_n[31]	G5	output	2.5 V			1
VCCIO1	G6	power		2.5V		1
GND	G7	gnd				
VCCINT	G8	power		1.5V		
GND	G9	gnd				
VCCINT	G10	power		1.5V		

GND	G11	gnd				
CORR_RESET_n[17]	G12	output	2.5 V		3	
CORR_RESET_n[15]	G13	output	2.5 V		3	
CORR_RESET_n[13]	G14	output	2.5 V		3	
CORR_RESET_n[11]	G15	output	2.5 V		3	
IP[6]	G16	input	2.5 V		3	
MCB_CLK_IN	H1	input	2.5 V		1	
DATA0	H2	input			1	
nCONFIG	H3				1	
nCEO	H4				1	
CORR_RESET_n[48]	H5	output	2.5 V		1	
VCCA_PLL1	H6	power		1.5V		
VCCINT	H7	power		1.5V		
GND	H8	gnd				
VCCINT	H9	power		1.5V		
GND	H10	gnd				
VCCA_PLL2	H11	power		1.5V		
CORR_RESET_n[16]	H12	output	2.5 V		3	
CORR_RESET_n[14]	H13	output	2.5 V		3	
TDI	H14	input			3	
TDO	H15	output			3	
IP[7]	H16	input	2.5 V		3	
RECIRC_RESET_n[2]	J1	output	2.5 V		1	
MSEL1	J2				1	
MSEL0	J3				1	
nCE	J4				1	
GNDG_PLL1	J5	gnd				
GNDA_PLL1	J6	gnd				
GND	J7	gnd				
VCCINT	J8	power		1.5V		
GND	J9	gnd				
VCCINT	J10	power		1.5V		
GNDA_PLL2	J11	gnd				
GNDG_PLL2	J12	gnd				
nSTATUS	J13				3	
TCK	J14	input			3	
TMS	J15	input			3	
MCB_CLK_F[8]	J16	output	2.5 V		3	
CORR_RESET_n[38]	K1	output	2.5 V		1	
CORR_RESET_n[37]	K2	output	2.5 V		1	
GND*	K3				1	
DCLK	K4	bidir			1	
CORR_RESET_n[49]	K5	output	2.5 V		1	
GND	K6	gnd				
VCCINT	K7	power		1.5V		
GND	K8	gnd				
VCCINT	K9	power		1.5V		
GND	K10	gnd				
VCCIO3	K11	power		2.5V	3	
RESYNC_RESET_n[0]	K12	output	2.5 V		3	
CONF_DONE	K13				3	
CORR_RESET_n[12]	K14	output	2.5 V		3	
CORR_RESET_n[10]	K15	output	2.5 V		3	
CORR_RESET_n[9]	K16	output	2.5 V		3	
CORR_RESET_n[39]	L1	output	2.5 V		1	
CORR_RESET_n[42]	L2	output	2.5 V		1	
CORR_RESET_n[35]	L3	output	2.5 V		1	
CORR_RESET_n[32]	L4	output	2.5 V		1	
SN[0]	L5	input	2.5 V		1	
GND	L6	gnd				
VCCIO4	L7	power		2.5V	4	
GND	L8	gnd				
GND	L9	gnd				
VCCIO4	L10	power		2.5V	4	
GND	L11	gnd				

RESYNC_RESET_n[1]	L12	output	2.5 V		3	
CORR_RESET_n[1]	L13	output	2.5 V		3	
CORR_RESET_n[3]	L14	output	2.5 V		3	
CORR_RESET_n[5]	L15	output	2.5 V		3	
CORR_RESET_n[8]	L16	output	2.5 V		3	
CORR_RESET_n[40]	M1	output	2.5 V		1	
CORR_RESET_n[43]	M2	output	2.5 V		1	
CORR_RESET_n[44]	M3	output	2.5 V		1	
CORR_RESET_n[33]	M4	output	2.5 V		1	
SN[6]	M5	input	2.5 V		4	
RECIRC_RESET_n[7]	M6	output	2.5 V		4	
RECIRC_RESET_n[8]	M7	output	2.5 V		4	
CORR_RESET_n[24]	M8	output	2.5 V		4	
CORR_RESET_n[23]	M9	output	2.5 V		4	
MCB_CLK_F[2]	M10	output	2.5 V		4	
MCB_CLK_F[3]	M11	output	2.5 V		4	
SN[13]	M12	input	2.5 V		4	
CORR_RESET_n[0]	M13	output	2.5 V		3	
CORR_RESET_n[2]	M14	output	2.5 V		3	
CORR_RESET_n[4]	M15	output	2.5 V		3	
CORR_RESET_n[7]	M16	output	2.5 V		3	
CORR_RESET_n[41]	N1	output	2.5 V		1	
SN[11]	N2	input	2.5 V		1	
CORR_RESET_n[45]	N3	output	2.5 V		1	
CORR_RESET_n[46]	N4	output	2.5 V		1	
MCB_DATA_IO[4]	N5	bidir	2.5 V		4	
CORR_RESET_n[28]	N6	output	2.5 V		4	
CORR_RESET_n[26]	N7	output	2.5 V		4	
CORR_RESET_n[25]	N8	output	2.5 V		4	
CORR_RESET_n[22]	N9	output	2.5 V		4	
CORR_RESET_n[21]	N10	output	2.5 V		4	
CORR_RESET_n[19]	N11	output	2.5 V		4	
MCB_ADDR_IN[2]	N12	input	2.5 V		4	
MCB_CLK	N13	input	2.5 V		3	
MCB_DATA_IO[7]	N14	bidir	2.5 V		3	
SN[8]	N15	input	2.5 V		3	
CORR_RESET_n[6]	N16	output	2.5 V		3	
VCCIO1	P1	power		2.5V	1	
SN[7]	P2	input	2.5 V		1	
SN[4]	P3	input	2.5 V		1	
CORR_RESET_n[47]	P4	output	2.5 V		4	
SN[5]	P5	input	2.5 V		4	
CORR_RESET_n[29]	P6	output	2.5 V		4	
CORR_RESET_n[27]	P7	output	2.5 V		4	
MCB_CS_IN_n	P8	input	2.5 V		4	
SN[1]	P9	input	2.5 V		4	
CORR_RESET_n[20]	P10	output	2.5 V		4	
CORR_RESET_n[18]	P11	output	2.5 V		4	
MCB_ADDR_IN[1]	P12	input	2.5 V		4	
MCB_DATA_IO[2]	P13	bidir	2.5 V		4	
MCB_CLK_F[0]	P14	output	2.5 V		3	
SN[12]	P15	input	2.5 V		3	
VCCIO3	P16	power		2.5V	3	
LED_BS[0]	R1	output	2.5 V		1	
MCB_RDWR_IN_n	R2	input	2.5 V		4	
MCB_DATA_IO[5]	R3	bidir	2.5 V		4	
GBITETHER_RESET_n	R4	output	2.5 V		4	
LED_BS[1]	R5	output	2.5 V		4	
CORR_RESET_n[50]	R6	output	2.5 V		4	
MCB_ADDR_IN[0]	R7	input	2.5 V		4	
MCB_DATA_IO[0]	R8	bidir	2.5 V		4	
MCB_ADDR_IN[4]	R9	input	2.5 V		4	
MCB_ADDR_IN[3]	R10	input	2.5 V		4	
IP[5]	R11	input	2.5 V		4	
MCB_CLK_RESYNC	R12	output	2.5 V		4	

```
SN[10]                    : R13      : input  : 2.5 V          :         : 4         :
MCB_CLK_F[11]             : R14      : output : 2.5 V          :         : 4         :
INTERRUPT_OUT             : R15      : output : 2.5 V          :         : 4         :
MCB_DATA_IO[6]            : R16      : bidir  : 2.5 V          :         : 3         :
GND                       : T1       : gnd    :                :         :           :
SN[2]                     : T2       : input  : 2.5 V          :         : 4         :
VCCIO4                    : T3       : power  :                : 2.5V    : 4         :
SN[9]                     : T4       : input  : 2.5 V          :         : 4         :
GND                       : T5       : gnd    :                :         :           :
CORR_RESET_n[51]          : T6       : output : 2.5 V          :         : 4         :
VCCINT                    : T7       : power  :                : 1.5V    :           :
MCB_DATA_IO[1]            : T8       : bidir  : 2.5 V          :         : 4         :
SN[3]                     : T9       : input  : 2.5 V          :         : 4         :
VCCINT                    : T10      : power  :                : 1.5V    :           :
IP[4]                     : T11      : input  : 2.5 V          :         : 4         :
GND                       : T12      : gnd    :                :         :           :
PWR_GOOD                  : T13      : input  : 2.5 V          :         : 4         :
VCCIO4                    : T14      : power  :                : 2.5V    : 4         :
MCB_DATA_IO[3]            : T15      : bidir  : 2.5 V          :         : 4         :
GND                       : T16      : gnd    :                :         :           :
-------------------------------------------------------------------------------------------
 -- NC            : No Connect. This pin has no internal connection to the device.
 -- DNU           : Do Not Use. This pin MUST NOT be connected.
 -- VCCINT        : Dedicated power pin, which MUST be connected to VCC  (1.5V).
 -- VCCIO         : Dedicated power pin, which MUST be connected to VCC of its bank.
 --                              Bank 1:            2.5V
 --                              Bank 2:            2.5V
 --                              Bank 3:            2.5V
 --                              Bank 4:            2.5V
 -- GND           : Dedicated ground pin. Dedicated GND pins MUST be connected to GND.
 -- GND+          : Unused input pin. It can also be used to report unused dual-purpose pins.
 --                 This pin should be connected to GND. It may also be connected  to a
 --                 valid signal  on the board  (low, high, or toggling)  if that signal
 --                 is required for a different revision of the design.
 -- GND*          : Unused  I/O  pin.   For transceiver I/O banks (Bank 13, 14, 15, 16 and 17),
 --                 connect each pin marked GND* either individually through a 10k Ohm resistor
 --                 to GND or tie all pins together and connect through a single 10k Ohm resistor
 --                 to GND.
 --                 For non-transceiver I/O banks, connect each pin marked GND* directly to GND
 --                 or leave it unconnected.
 -- RESERVED      : Unused I/O pin, which MUST be left unconnected.
 -- RESERVED_INPUT    : Pin is tri-stated and should be connected to the board.
 -- RESERVED_INPUT_WITH_WEAK_PULLUP    : Pin is tri-stated with internal weak pull-up resistor.
 -- RESERVED_INPUT_WITH_BUS_HOLD       : Pin is tri-stated with bus-hold circuitry.
 -- RESERVED_OUTPUT_DRIVEN_HIGH        : Pin is output driven high.
-------------------------------------------------------------------------------------------
```

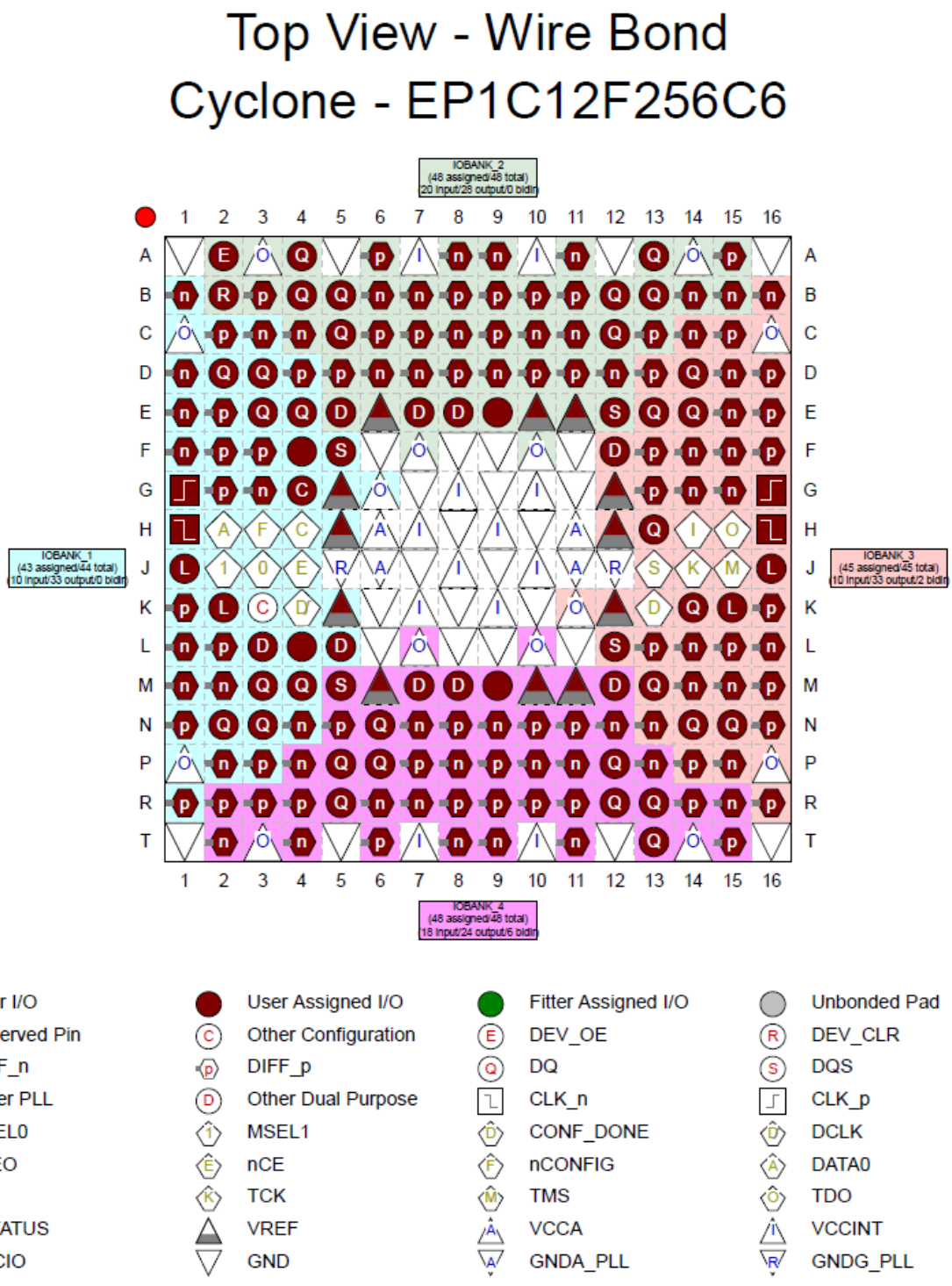

Figure 11-1 U150 MCB FPGA Quartus-II V9.1 pin planner output. This is the view looking down on the top of the chip.

11.2 U151 MCB FPGA Pinouts

This section contains an exhaustive chip pinout listing generated by the Quartus-II FPGA compiler, and the Quartus-II pin planner graphic. The U151 MCB FPGA is implemented in an Altera Cyclone EP1C12F256C6 FPGA, and compiles with the Quartus-II V9.1 compiler.

Pin Name/Usage	Location	Dir.	I/O Standard	Voltage	I/O Bank
GND	A1	gnd			
MCB_CS_F[63]	A2	output	2.5 V		2
VCCIO2	A3	power		2.5V	2
MCB_CS_F[60]	A4	output	2.5 V		2
GND	A5	gnd			
MCB_RDWR_F[9]	A6	output	2.5 V		2
VCCINT	A7	power		1.5V	
MCB_CS_F[56]	A8	output	2.5 V		2
MCB_CS_F[139]	A9	output	2.5 V		2
VCCINT	A10	power		1.5V	
MCB_CS_F[7]	A11	output	2.5 V		2
GND	A12	gnd			
MCB_CS_F[4]	A13	output	2.5 V		2
VCCIO2	A14	power		2.5V	2
MCB_RDWR_F[2]	A15	output	2.5 V		2
GND	A16	gnd			
MCB_CS_F[65]	B1	output	2.5 V		1
MCB_CS_F[64]	B2	output	2.5 V		2
MCB_CS_F[62]	B3	output	2.5 V		2
MCB_CS_F[61]	B4	output	2.5 V		2
MCB_CS_F[59]	B5	output	2.5 V		2
MCB_CS_F[58]	B6	output	2.5 V		2
MCB_CS_F[145]	B7	output	2.5 V		2
MCB_CS_F[57]	B8	output	2.5 V		2
MCB_CS_F[9]	B9	output	2.5 V		2
MCB_CS_F[8]	B10	output	2.5 V		2
MCB_CS_F[6]	B11	output	2.5 V		2
MCB_CS_F[5]	B12	output	2.5 V		2
MCB_CS_F[3]	B13	output	2.5 V		2
MCB_CS_F[2]	B14	output	2.5 V		2
MCB_CS_F[138]	B15	output	2.5 V		2
MCB_RDWR_F[1]	B16	output	2.5 V		3
VCCIO1	C1	power		2.5V	1
MCB_CS_F[125]	C2	output	2.5 V		1
MCB_CS_F[124]	C3	output	2.5 V		1
MCB_CS_F[123]	C4	output	2.5 V		2
MCB_CS_F[122]	C5	output	2.5 V		2
MCB_CS_F[127]	C6	output	2.5 V		2
MCB_RDWR_F[17]	C7	output	2.5 V		2
MCB_CS_F[128]	C8	output	2.5 V		2
MCB_CS_F[133]	C9	output	2.5 V		2
MCB_CS_F[132]	C10	output	2.5 V		2
MCB_CS_F[131]	C11	output	2.5 V		2
MCB_CS_F[130]	C12	output	2.5 V		2
MCB_CS_F[134]	C13	output	2.5 V		2
MCB_CS_F[135]	C14	output	2.5 V		3
MCB_CS_F[136]	C15	output	2.5 V		3
VCCIO3	C16	power		2.5V	3
MCB_CS_F[126]	D1	output	2.5 V		1
MCB_CS_F[39]	D2	output	2.5 V		1
MCB_CS_F[37]	D3	output	2.5 V		1

MCB_CS_F[35]	D4	output	2.5 V		1
MCB_RDWR_F[6]	D5	output	2.5 V		2
MCB_CS_F[33]	D6	output	2.5 V		2
MCB_CS_F[31]	D7	output	2.5 V		2
MCB_CS_F[129]	D8	output	2.5 V		2
MCB_RDWR_F[0]	D9	output	2.5 V		2
MCB_CS_F[25]	D10	output	2.5 V		2
MCB_CS_F[23]	D11	output	2.5 V		2
MCB_CS_F[21]	D12	output	2.5 V		2
MCB_CS_F[19]	D13	output	2.5 V		3
MCB_RDWR_F[4]	D14	output	2.5 V		3
MCB_CS_F[17]	D15	output	2.5 V		3
MCB_CS_F[137]	D16	output	2.5 V		3
MCB_CS_F[41]	E1	output	2.5 V		1
MCB_CS_F[40]	E2	output	2.5 V		1
MCB_CS_F[38]	E3	output	2.5 V		1
MCB_CS_F[36]	E4	output	2.5 V		1
MCB_CS_F[34]	E5	output	2.5 V		2
MCB_CS_F[142]	E6	output	2.5 V		2
MCB_CS_F[32]	E7	output	2.5 V		2
MCB_CS_F[29]	E8	output	2.5 V		2
MCB_RDWR_F[5]	E9	output	2.5 V		2
MCB_CS_F[141]	E10	output	2.5 V		2
MCB_CS_F[24]	E11	output	2.5 V		2
MCB_CS_F[22]	E12	output	2.5 V		2
MCB_CS_F[20]	E13	output	2.5 V		3
MCB_CS_F[18]	E14	output	2.5 V		3
MCB_CS_F[140]	E15	output	2.5 V		3
MCB_CS_F[15]	E16	output	2.5 V		3
MCB_CS_F[143]	F1	output	2.5 V		1
MCB_CS_F[43]	F2	output	2.5 V		1
MCB_CS_F[45]	F3	output	2.5 V		1
MCB_CS_F[47]	F4	output	2.5 V		1
MCB_CS_F[49]	F5	output	2.5 V		1
GND	F6	gnd			
VCCIO2	F7	power		2.5V	2
GND	F8	gnd			
GND	F9	gnd			
VCCIO2	F10	power		2.5V	2
GND	F11	gnd			
MCB_CS_F[88]	F12	output	2.5 V		3
MCB_CS_F[78]	F13	output	2.5 V		3
MCB_CS_F[10]	F14	output	2.5 V		3
MCB_CS_F[14]	F15	output	2.5 V		3
MCB_CS_F[16]	F16	output	2.5 V		3
MCB_ADDR[15]	G1	input	2.5 V		1
MCB_CS_F[44]	G2	output	2.5 V		1
MCB_CS_F[46]	G3	output	2.5 V		1
GND*	G4				1
MCB_CS_F[144]	G5	output	2.5 V		1
VCCIO1	G6	power		2.5V	1
GND	G7	gnd			
VCCINT	G8	power		1.5V	
GND	G9	gnd			
VCCINT	G10	power		1.5V	
GND	G11	gnd			
MCB_RDWR_F[12]	G12	output	2.5 V		3
MCB_CS_F[89]	G13	output	2.5 V		3
MCB_RDWR_F[3]	G14	output	2.5 V		3
MCB_CS_F[12]	G15	output	2.5 V		3
GND+	G16				3
MCB_ADDR[14]	H1	input	2.5 V		1
DATA0	H2	input			1
nCONFIG	H3				1
nCEO	H4				1

MCB_CS_F[94]	H5	output	2.5 V		1
VCCA_PLL1	H6	power		1.5V	
VCCINT	H7	power		1.5V	
GND	H8	gnd			
VCCINT	H9	power		1.5V	
GND	H10	gnd			
VCCA_PLL2	H11	power		1.5V	
MCB_RDWR_F[10]	H12	output	2.5 V		3
MCB_CS_F[66]	H13	output	2.5 V		3
TDI	H14	input			3
TDO	H15	output			3
GND+	H16				3
MCB_RDWR_F[7]	J1	output	2.5 V		1
MSEL1	J2				1
MSEL0	J3				1
nCE	J4				1
GNDG_PLL1	J5	gnd			
GNDA_PLL1	J6	gnd			
GND	J7	gnd			
VCCINT	J8	power		1.5V	
GND	J9	gnd			
VCCINT	J10	power		1.5V	
GNDA_PLL2	J11	gnd			
GNDG_PLL2	J12	gnd			
nSTATUS	J13				3
TCK	J14	input			3
TMS	J15	input			3
MCB_CS_F[13]	J16	output	2.5 V		3
MCB_CS_F[42]	K1	output	2.5 V		1
MCB_CS_F[99]	K2	output	2.5 V		1
GND*	K3				1
DCLK	K4	bidir			1
MCB_CS_F[105]	K5	output	2.5 V		1
GND	K6	gnd			
VCCINT	K7	power		1.5V	
GND	K8	gnd			
VCCINT	K9	power		1.5V	
GND	K10	gnd			
VCCIO3	K11	power		2.5V	3
MCB_CS_F[72]	K12	output	2.5 V		3
CONF_DONE	K13				3
MCB_CS_F[76]	K14	output	2.5 V		3
MCB_CS_F[74]	K15	output	2.5 V		3
MCB_CS_F[11]	K16	output	2.5 V		3
MCB_CS_F[101]	L1	output	2.5 V		1
MCB_CS_F[100]	L2	output	2.5 V		1
MCB_CS_F[103]	L3	output	2.5 V		1
MCB_CS_F[48]	L4	output	2.5 V		1
MCB_CS_F[110]	L5	output	2.5 V		1
GND	L6	gnd			
VCCIO4	L7	power		2.5V	4
GND	L8	gnd			
GND	L9	gnd			
VCCIO4	L10	power		2.5V	4
GND	L11	gnd			
MCB_CS_F[87]	L12	output	2.5 V		3
MCB_CS_F[71]	L13	output	2.5 V		3
MCB_CS_F[77]	L14	output	2.5 V		3
MCB_CS_F[75]	L15	output	2.5 V		3
RES_MCB_DIR	L16	output	2.5 V		3
MCB_CS_F[102]	M1	output	2.5 V		1
MCB_RDWR_F[15]	M2	output	2.5 V		1
MCB_CS_F[98]	M3	output	2.5 V		1
MCB_CS_F[104]	M4	output	2.5 V		1
MCB_CS_F[121]	M5	output	2.5 V		4

MCB_RDWR_F[8]	M6	output	2.5 V		4
MCB_CS_F[51]	M7	output	2.5 V		4
MCB_CS_F[30]	M8	output	2.5 V		4
MCB_CS_F[26]	M9	output	2.5 V		4
MCB_CS_F[97]	M10	output	2.5 V		4
MCB_CS_F[85]	M11	output	2.5 V		4
MCB_CS_F[82]	M12	output	2.5 V		4
MCB_CS_F[147]	M13	output	2.5 V		3
MCB_CS_F[68]	M14	output	2.5 V		3
MCB_CS_F[70]	M15	output	2.5 V		3
MCB_RDWR_F[11]	M16	output	2.5 V		3
MCB_CS_F[113]	N1	output	2.5 V		1
MCB_CS_F[111]	N2	output	2.5 V		1
MCB_CS_F[106]	N3	output	2.5 V		1
MCB_RDWR_F[14]	N4	output	2.5 V		1
MCB_CS_F[92]	N5	output	2.5 V		4
MCB_CS_F[50]	N6	output	2.5 V		4
MCB_CS_F[52]	N7	output	2.5 V		4
MCB_CS_F[53]	N8	output	2.5 V		4
MCB_CS_F[27]	N9	output	2.5 V		4
MCB_CS_F[96]	N10	output	2.5 V		4
MCB_CS_F[86]	N11	output	2.5 V		4
MCB_CS_F[73]	N12	output	2.5 V		4
MCB_RDWR	N13	input	2.5 V		3
MCB_CS_F[67]	N14	output	2.5 V		3
MCB_CS_F[69]	N15	output	2.5 V		3
MCB_CS_F[79]	N16	output	2.5 V		3
VCCIO1	P1	power		2.5V	1
MCB_ADDR[9]	P2	input	2.5 V		1
MCB_CS_F[107]	P3	output	2.5 V		1
MCB_CS_F[108]	P4	output	2.5 V		4
MCB_CS_F[93]	P5	output	2.5 V		4
MCB_CS_F[120]	P6	output	2.5 V		4
MCB_CS_F[90]	P7	output	2.5 V		4
MCB_CS_F[54]	P8	output	2.5 V		4
MCB_CS_F[28]	P9	output	2.5 V		4
MCB_CS_F[115]	P10	output	2.5 V		4
MCB_CS_F[117]	P11	output	2.5 V		4
MCB_CS_F[83]	P12	output	2.5 V		4
MCB_ADDR[12]	P13	input	2.5 V		4
MCB_CS_F[146]	P14	output	2.5 V		3
MCB_CS_F[80]	P15	output	2.5 V		3
VCCIO3	P16	power		2.5V	3
MCB_CS_F[112]	R1	output	2.5 V		1
MCB_CS_F[1]	R2	output	2.5 V		4
MCB_ADDR[8]	R3	input	2.5 V		4
MCB_CS_F[109]	R4	output	2.5 V		4
MCB_ADDR[13]	R5	input	2.5 V		4
MCB_RDWR_F[16]	R6	output	2.5 V		4
MCB_CS_F[91]	R7	output	2.5 V		4
MCB_CS_F[114]	R8	output	2.5 V		4
MCB_CS_F[55]	R9	output	2.5 V		4
MCB_CS_F[116]	R10	output	2.5 V		4
MCB_CS_F[118]	R11	output	2.5 V		4
MCB_CS_F[84]	R12	output	2.5 V		4
RESET_n	R13	input	2.5 V		4
GND*	R14				4
MCB_RDWR_F[18]	R15	output	2.5 V		4
MCB_CS_F[81]	R16	output	2.5 V		3
GND	T1	gnd			
MCB_CS_F[0]	T2	output	2.5 V		4
VCCIO4	T3	power		2.5V	4
MCB_ADDR[10]	T4	input	2.5 V		4
GND	T5	gnd			
MCB_CS_F[119]	T6	output	2.5 V		4

```
VCCINT                    : T7       : power  :                  : 1.5V    :           :
MCB_RDWR_F[13]            : T8       : output : 2.5 V            :         : 4         :
MCB_CS_F[95]              : T9       : output : 2.5 V            :         : 4         :
VCCINT                    : T10      : power  :                  : 1.5V    :           :
MCB_BS                    : T11      : input  : 2.5 V            :         : 4         :
GND                       : T12      : gnd    :                  :         :           :
GND*                      : T13      :        :                  :         : 4         :
VCCIO4                    : T14      : power  :                  : 2.5V    : 4         :
MCB_ADDR[11]              : T15      : input  : 2.5 V            :         : 4         :
GND                       : T16      : gnd    :                  :         :           :
-------------------------------------------------------------------------------------------
 -- NC            : No Connect. This pin has no internal connection to the device.
 -- DNU           : Do Not Use. This pin MUST NOT be connected.
 -- VCCINT        : Dedicated power pin, which MUST be connected to VCC  (1.5V).
 -- VCCIO         : Dedicated power pin, which MUST be connected to VCC of its bank.
 --                              Bank 1:            2.5V
 --                              Bank 2:            2.5V
 --                              Bank 3:            2.5V
 --                              Bank 4:            2.5V
 -- GND           : Dedicated ground pin. Dedicated GND pins MUST be connected to GND.
 -- GND+          : Unused input pin. It can also be used to report unused dual-purpose pins.
 --                 This pin should be connected to GND. It may also be connected  to a
 --                 valid signal  on the board  (low, high, or toggling)  if that signal
 --                 is required for a different revision of the design.
 -- GND*          : Unused  I/O  pin.   For transceiver I/O banks (Bank 13, 14, 15, 16 and 17),
 --                 connect each pin marked GND* either individually through a 10k Ohm resistor
 --                 to GND or tie all pins together and connect through a single 10k Ohm resistor
 --                 to GND.
 --                 For non-transceiver I/O banks, connect each pin marked GND* directly to GND
 --                 or leave it unconnected.
 -- RESERVED      : Unused I/O pin, which MUST be left unconnected.
 -- RESERVED_INPUT    : Pin is tri-stated and should be connected to the board.
 -- RESERVED_INPUT_WITH_WEAK_PULLUP    : Pin is tri-stated with internal weak pull-up resistor.
 -- RESERVED_INPUT_WITH_BUS_HOLD       : Pin is tri-stated with bus-hold circuitry.
 -- RESERVED_OUTPUT_DRIVEN_HIGH        : Pin is output driven high.
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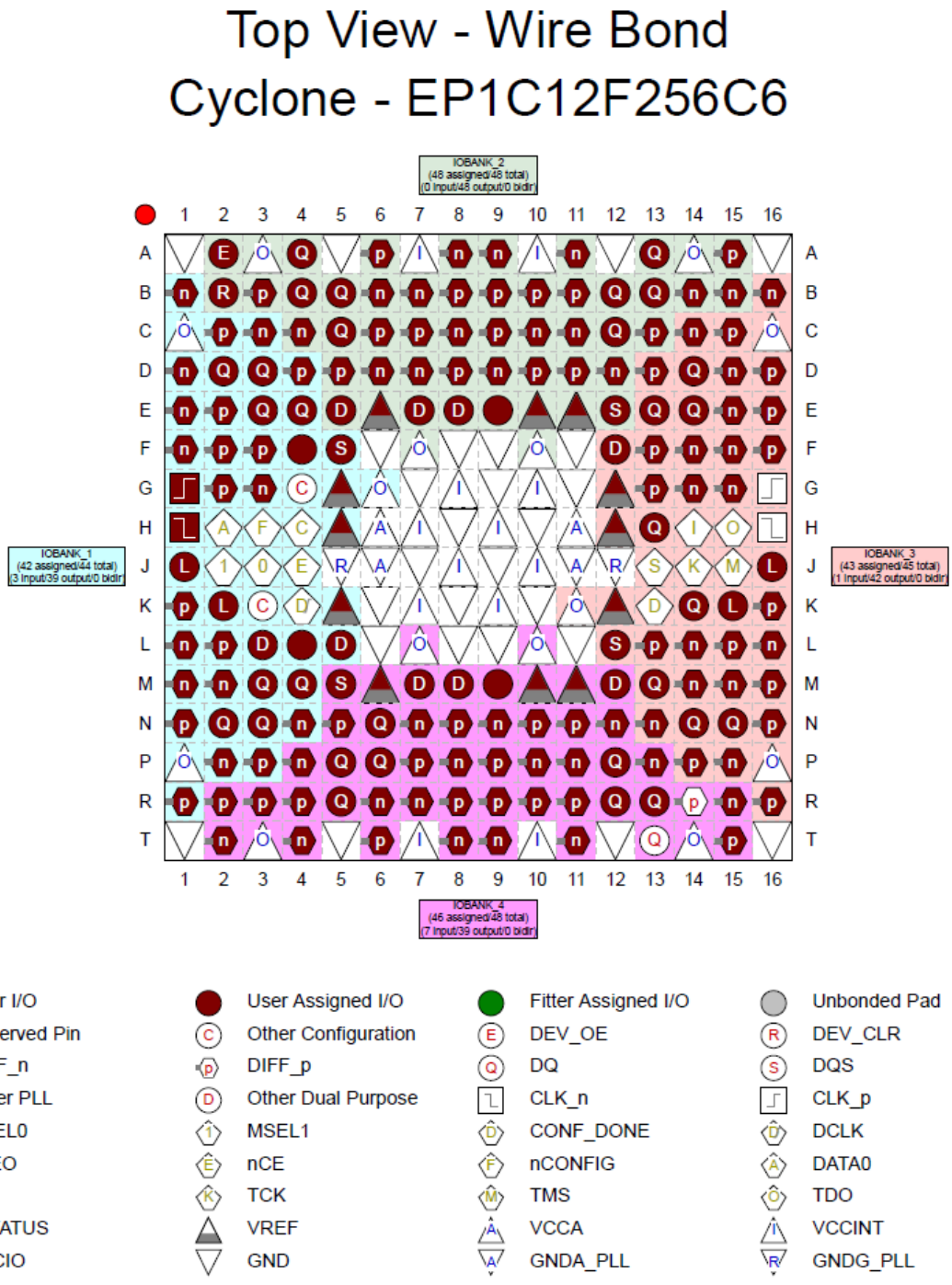


Figure 11-2 U151 MCB FPGA Quartus-II V9.1 pin planner output. This is the view looking down on the top of the chip.

11.3 U152 MCB FPGA Pinouts

This section contains an exhaustive chip pinout listing generated by the Quartus-II FPGA compiler, and the Quartus-II pin planner graphic. The U152 MCB FPGA is implemented in an Altera Cyclone EP1C12F256C6 FPGA, and compiles with the Quartus-II V**6.1** compiler.

Pin Name/Usage	Location	Dir.	I/O Standard	Voltage	I/O Bank
GND	A1	gnd			
MCB_DATA_F17[0]	A2	bidir	2.5 V		2
VCCIO2	A3	power		2.5V	2
MCB_DATA_F16[6]	A4	bidir	2.5 V		2
GND	A5	gnd			
MCB_DATA_F15[6]	A6	bidir	2.5 V		2
VCCINT	A7	power		1.5V	
MCB_DATA_F15[7]	A8	bidir	2.5 V		2
MCB_DATA_F2[5]	A9	bidir	2.5 V		2
VCCINT	A10	power		1.5V	
MCB_DATA_F1[0]	A11	bidir	2.5 V		2
GND	A12	gnd			
MCB_DATA_F1[3]	A13	bidir	2.5 V		2
VCCIO2	A14	power		2.5V	2
MCB_DATA_F0[4]	A15	bidir	2.5 V		2
GND	A16	gnd			
MCB_DATA_F17[6]	B1	bidir	2.5 V		1
MCB_DATA_F17[1]	B2	bidir	2.5 V		2
MCB_DATA_F17[7]	B3	bidir	2.5 V		2
MCB_DATA_F16[7]	B4	bidir	2.5 V		2
MCB_DATA_F16[5]	B5	bidir	2.5 V		2
MCB_DATA_F16[4]	B6	bidir	2.5 V		2
MCB_DATA_F15[1]	B7	bidir	2.5 V		2
MCB_DATA_F15[0]	B8	bidir	2.5 V		2
MCB_DATA_F2[4]	B9	bidir	2.5 V		2
MCB_DATA_F1[6]	B10	bidir	2.5 V		2
MCB_DATA_F1[4]	B11	bidir	2.5 V		2
MCB_DATA_F1[1]	B12	bidir	2.5 V		2
MCB_DATA_F0[6]	B13	bidir	2.5 V		2
MCB_DATA_F0[0]	B14	bidir	2.5 V		2
MCB_DATA_F0[1]	B15	bidir	2.5 V		2
MCB_DATA_F0[3]	B16	bidir	2.5 V		3
VCCIO1	C1	power		2.5V	1
MCB_DATA_F17[3]	C2	bidir	2.5 V		1
MCB_DATA_F17[2]	C3	bidir	2.5 V		1
MCB_DATA_F17[5]	C4	bidir	2.5 V		2
MCB_DATA_F16[3]	C5	bidir	2.5 V		2
MCB_DATA_F16[2]	C6	bidir	2.5 V		2
MCB_DATA_F16[1]	C7	bidir	2.5 V		2
MCB_DATA_F16[0]	C8	bidir	2.5 V		2
MCB_DATA_F2[1]	C9	bidir	2.5 V		2
MCB_DATA_F2[0]	C10	bidir	2.5 V		2
MCB_DATA_F1[7]	C11	bidir	2.5 V		2
MCB_DATA_F1[2]	C12	bidir	2.5 V		2
MCB_DATA_F1[5]	C13	bidir	2.5 V		2
MCB_DATA_F0[7]	C14	bidir	2.5 V		3
MCB_DATA_F0[2]	C15	bidir	2.5 V		3
VCCIO3	C16	power		2.5V	3
MCB_DATA_F17[4]	D1	bidir	2.5 V		1
MCB_DATA_F11[7]	D2	bidir	2.5 V		1

MCB_DATA_F10[6]	D3	bidir	2.5 V		1	
MCB_DATA_F10[4]	D4	bidir	2.5 V		1	
MCB_DATA_F9[1]	D5	bidir	2.5 V		2	
MCB_DATA_F9[7]	D6	bidir	2.5 V		2	
MCB_DATA_F8[6]	D7	bidir	2.5 V		2	
MCB_DATA_F15[4]	D8	bidir	2.5 V		2	
MCB_DATA_F2[2]	D9	bidir	2.5 V		2	
MCB_DATA_F6[6]	D10	bidir	2.5 V		2	
MCB_DATA_F6[4]	D11	bidir	2.5 V		2	
MCB_DATA_F6[0]	D12	bidir	2.5 V		2	
MCB_DATA_F5[6]	D13	bidir	2.5 V		3	
MCB_DATA_F5[0]	D14	bidir	2.5 V		3	
MCB_DATA_F4[7]	D15	bidir	2.5 V		3	
MCB_DATA_F0[5]	D16	bidir	2.5 V		3	
MCB_DATA_F11[1]	E1	bidir	2.5 V		1	
MCB_DATA_F11[0]	E2	bidir	2.5 V		1	
MCB_DATA_F10[7]	E3	bidir	2.5 V		1	
MCB_DATA_F10[5]	E4	bidir	2.5 V		1	
MCB_DATA_F9[6]	E5	bidir	2.5 V		2	
MCB_DATA_F9[0]	E6	bidir	2.5 V		2	
MCB_DATA_F8[7]	E7	bidir	2.5 V		2	
MCB_DATA_F8[4]	E8	bidir	2.5 V		2	
MCB_DATA_F7[7]	E9	bidir	2.5 V		2	
MCB_DATA_F6[7]	E10	bidir	2.5 V		2	
MCB_DATA_F6[5]	E11	bidir	2.5 V		2	
MCB_DATA_F6[1]	E12	bidir	2.5 V		2	
MCB_DATA_F5[1]	E13	bidir	2.5 V		3	
MCB_DATA_F5[7]	E14	bidir	2.5 V		3	
MCB_DATA_F4[6]	E15	bidir	2.5 V		3	
MCB_DATA_F4[5]	E16	bidir	2.5 V		3	
MCB_DATA_F11[6]	F1	bidir	2.5 V		1	
MCB_DATA_F12[6]	F2	bidir	2.5 V		1	
MCB_DATA_F13[7]	F3	bidir	2.5 V		1	
MCB_DATA_F13[1]	F4	bidir	2.5 V		1	
MCB_DATA_F14[4]	F5	bidir	2.5 V		1	
GND	F6	gnd				
VCCIO2	F7	power		2.5V	2	
GND	F8	gnd				
GND	F9	gnd				
VCCIO2	F10	power		2.5V	2	
GND	F11	gnd				
MCB_DATA_F5[4]	F12	bidir	2.5 V		3	
MCB_DATA_F5[2]	F13	bidir	2.5 V		3	
MCB_DATA_F2[7]	F14	bidir	2.5 V		3	
MCB_DATA_F3[0]	F15	bidir	2.5 V		3	
MCB_DATA_F4[4]	F16	bidir	2.5 V		3	
RESET_n	G1	input	2.5 V		1	
MCB_DATA_F12[7]	G2	bidir	2.5 V		1	
MCB_DATA_F13[0]	G3	bidir	2.5 V		1	
GND*	G4				1	
MCB_DATA_F14[5]	G5	bidir	2.5 V		1	
VCCIO1	G6	power		2.5V	1	
GND	G7	gnd				
VCCINT	G8	power		1.5V		
GND	G9	gnd				
VCCINT	G10	power		1.5V		
GND	G11	gnd				
MCB_DATA_F5[3]	G12	bidir	2.5 V		3	
MCB_DATA_F5[5]	G13	bidir	2.5 V		3	
MCB_DATA_F2[6]	G14	bidir	2.5 V		3	
MCB_DATA_F3[7]	G15	bidir	2.5 V		3	
MCB_ADDR[15]	G16	input	2.5 V		3	
MCB_CLK_IN	H1	input	2.5 V		1	
DATA0	H2	input			1	
nCONFIG	H3				1	

nCEO	H4				1
MCB_DATA_F9[3]	H5	bidir	2.5 V		1
VCCA_PLL1	H6	power		1.5V	
VCCINT	H7	power		1.5V	
GND	H8	gnd			
VCCINT	H9	power		1.5V	
GND	H10	gnd			
VCCA_PLL2	H11	power		1.5V	
MCB_DATA[2]	H12	bidir	2.5 V		3
MCB_DATA_F2[3]	H13	bidir	2.5 V		3
TDI	H14	input			3
TDO	H15	output			3
MCB_ADDR[14]	H16	input	2.5 V		3
MCB_DATA_F12[4]	J1	bidir	2.5 V		1
MSEL1	J2				1
MSEL0	J3				1
nCE	J4				1
GNDG_PLL1	J5	gnd			
GNDA_PLL1	J6	gnd			
GND	J7	gnd			
VCCINT	J8	power		1.5V	
GND	J9	gnd			
VCCINT	J10	power		1.5V	
GNDA_PLL2	J11	gnd			
GNDG_PLL2	J12	gnd			
nSTATUS	J13				3
TCK	J14	input			3
TMS	J15	input			3
MCB_DATA_F3[6]	J16	bidir	2.5 V		3
MCB_DATA_F12[5]	K1	bidir	2.5 V		1
MCB_DATA_F11[5]	K2	bidir	2.5 V		1
GND*	K3				1
DCLK	K4	bidir			1
MCB_DATA_F9[4]	K5	bidir	2.5 V		1
GND	K6	gnd			
VCCINT	K7	power		1.5V	
GND	K8	gnd			
VCCINT	K9	power		1.5V	
GND	K10	gnd			
VCCIO3	K11	power		2.5V	3
MCB_DATA_F18[4]	K12	bidir	2.5 V		3
CONF_DONE	K13				3
MCB_DATA[4]	K14	bidir	2.5 V		3
MCB_DATA_F4[3]	K15	bidir	2.5 V		3
MCB_DATA_F3[1]	K16	bidir	2.5 V		3
MCB_DATA_F11[3]	L1	bidir	2.5 V		1
MCB_DATA_F11[2]	L2	bidir	2.5 V		1
MCB_DATA_F10[2]	L3	bidir	2.5 V		1
MCB_DATA_F13[6]	L4	bidir	2.5 V		1
MCB_DATA_F14[0]	L5	bidir	2.5 V		1
GND	L6	gnd			
VCCIO4	L7	power		2.5V	4
GND	L8	gnd			
GND	L9	gnd			
VCCIO4	L10	power		2.5V	4
GND	L11	gnd			
MCB_DATA_F18[6]	L12	bidir	2.5 V		3
MCB_DATA_F18[2]	L13	bidir	2.5 V		3
MCB_ADDR[11]	L14	input	2.5 V		3
MCB_DATA_F4[2]	L15	bidir	2.5 V		3
MCB_DATA_F4[1]	L16	bidir	2.5 V		3
MCB_DATA_F11[4]	M1	bidir	2.5 V		1
MCB_DATA_F12[2]	M2	bidir	2.5 V		1
MCB_DATA_F10[3]	M3	bidir	2.5 V		1
MCB_DATA_F10[0]	M4	bidir	2.5 V		1

MCB_DATA_F14[1]	M5	bidir	2.5 V		4
MCB_DATA_F14[6]	M6	bidir	2.5 V		4
MCB_DATA_F8[2]	M7	bidir	2.5 V		4
MCB_DATA_F8[5]	M8	bidir	2.5 V		4
MCB_DATA_F7[0]	M9	bidir	2.5 V		4
MCB_DATA_F7[5]	M10	bidir	2.5 V		4
MCB_DATA_F6[2]	M11	bidir	2.5 V		4
CDATA_F[4]	M12	output	2.5 V		4
MCB_ADDR[8]	M13	input	2.5 V		3
MCB_ADDR[12]	M14	input	2.5 V		3
MCB_DATA_F3[2]	M15	bidir	2.5 V		3
MCB_DATA_F4[0]	M16	bidir	2.5 V		3
MCB_DATA_F12[0]	N1	bidir	2.5 V		1
MCB_DATA_F12[3]	N2	bidir	2.5 V		1
MCB_DATA_F13[5]	N3	bidir	2.5 V		1
MCB_DATA_F10[1]	N4	bidir	2.5 V		1
MCB_DATA[5]	N5	bidir	2.5 V		4
MCB_DATA_F14[7]	N6	bidir	2.5 V		4
MCB_DATA_F8[3]	N7	bidir	2.5 V		4
MCB_DATA_F7[1]	N8	bidir	2.5 V		4
MCB_DATA_F7[6]	N9	bidir	2.5 V		4
MCB_DATA_F7[2]	N10	bidir	2.5 V		4
MCB_DATA_F6[3]	N11	bidir	2.5 V		4
MCB_DATA_F18[5]	N12	bidir	2.5 V		4
MCB_ADDR[13]	N13	input	2.5 V		3
MCB_DATA[6]	N14	bidir	2.5 V		3
MCB_DATA_F3[5]	N15	bidir	2.5 V		3
MCB_DATA_F3[4]	N16	bidir	2.5 V		3
VCCIO1	P1	power		2.5V	1
CDATA_F[6]	P2	output	2.5 V		1
MCB_DATA_F13[2]	P3	bidir	2.5 V		1
MCB_DATA_F13[3]	P4	bidir	2.5 V		4
MCB_ADDR[9]	P5	input	2.5 V		4
MCB_DATA_F9[5]	P6	bidir	2.5 V		4
MCB_DATA_F15[5]	P7	bidir	2.5 V		4
MCB_DATA_F15[2]	P8	bidir	2.5 V		4
MCB_DATA_F7[3]	P9	bidir	2.5 V		4
MCB_ADDR[10]	P10	input	2.5 V		4
MCB_DATA[1]	P11	bidir	2.5 V		4
CDATA_F[3]	P12	output	2.5 V		4
CDATA_F[2]	P13	output	2.5 V		4
MCB_CLK	P14	input	2.5 V		3
MCB_DATA_F18[0]	P15	bidir	2.5 V		3
VCCIO3	P16	power		2.5V	3
MCB_DATA_F12[1]	R1	bidir	2.5 V		1
CDATA_F[7]	R2	output	2.5 V		4
CDATA_F[5]	R3	output	2.5 V		4
MCB_DATA_F13[4]	R4	bidir	2.5 V		4
MCB_DATA_F18[7]	R5	bidir	2.5 V		4
MCB_DATA_F9[2]	R6	bidir	2.5 V		4
MCB_DATA_F14[2]	R7	bidir	2.5 V		4
MCB_DATA_F8[0]	R8	bidir	2.5 V		4
MCB_DATA_F7[4]	R9	bidir	2.5 V		4
MCB_BS	R10	input	2.5 V		4
MCB_DATA[0]	R11	bidir	2.5 V		4
CDATA_F[1]	R12	output	2.5 V		4
MCB_DATA[7]	R13	bidir	2.5 V		4
CDATA_F[0]	R14	output	2.5 V		4
CDATA	R15	input	2.5 V		4
MCB_DATA_F3[3]	R16	bidir	2.5 V		3
GND	T1	gnd			
CDATA_F[8]	T2	output	2.5 V		4
VCCIO4	T3	power		2.5V	4
MCB_DATA_F18[3]	T4	bidir	2.5 V		4
GND	T5	gnd			

```
MCB_DATA_F14[3]              : T6       : bidir  : 2.5 V            :         : 4         :
VCCINT                       : T7       : power  :                  : 1.5V    :           :
MCB_DATA_F8[1]               : T8       : bidir  : 2.5 V            :         : 4         :
MCB_DATA_F15[3]              : T9       : bidir  : 2.5 V            :         : 4         :
VCCINT                       : T10      : power  :                  : 1.5V    :           :
MCB_DATA[3]                  : T11      : bidir  : 2.5 V            :         : 4         :
GND                          : T12      : gnd    :                  :         :           :
MCB_DATA_F18[1]              : T13      : bidir  : 2.5 V            :         : 4         :
VCCIO4                       : T14      : power  :                  : 2.5V    : 4         :
MCB_RDWR                     : T15      : input  : 2.5 V            :         : 4         :
GND                          : T16      : gnd    :                  :         :           :
-------------------------------------------------------------------------------------------
 -- NC             : No Connect. This pin has no internal connection to the device.
 -- DNU            : Do Not Use. This pin MUST NOT be connected.
 -- VCCINT         : Dedicated power pin, which MUST be connected to VCC  (1.5V).
 -- VCCIO          : Dedicated power pin, which MUST be connected to VCC of its bank.
 --                                Bank 1:             2.5V
 --                                Bank 2:             2.5V
 --                                Bank 3:             2.5V
 --                                Bank 4:             2.5V
 -- GND            : Dedicated ground pin. Dedicated GND pins MUST be connected to GND.
 -- GND+           : Unused input pin. It can also be used to report unused dual-purpose pins.
 --                  This pin should be connected to GND. It may also be connected  to a
 --                  valid signal  on the board  (low, high, or toggling)  if that signal
 --                  is required for a different revision of the design.
 -- GND*           : Unused  I/O  pin.   For transceiver I/O banks (Bank 13, 14, 15, 16 and 17),
 --                  connect each pin marked GND* either individually through a 10k Ohm resistor
 --                  to GND or tie all pins together and connect through a single 10k Ohm resistor
 --                  to GND.
 --                  For non-transceiver I/O banks, connect each pin marked GND* directly to GND
 --                  or leave it unconnected.
 -- RESERVED       : Unused I/O pin, which MUST be left unconnected.
 -- RESERVED_INPUT    : Pin is tri-stated and should be connected to the board.
 -- RESERVED_INPUT_WITH_WEAK_PULLUP    : Pin is tri-stated with internal weak pull-up resistor.
 -- RESERVED_INPUT_WITH_BUS_HOLD       : Pin is tri-stated with bus-hold circuitry.
 -- RESERVED_OUTPUT_DRIVEN_HIGH        : Pin is output driven high.
-------------------------------------------------------------------------------------------
```

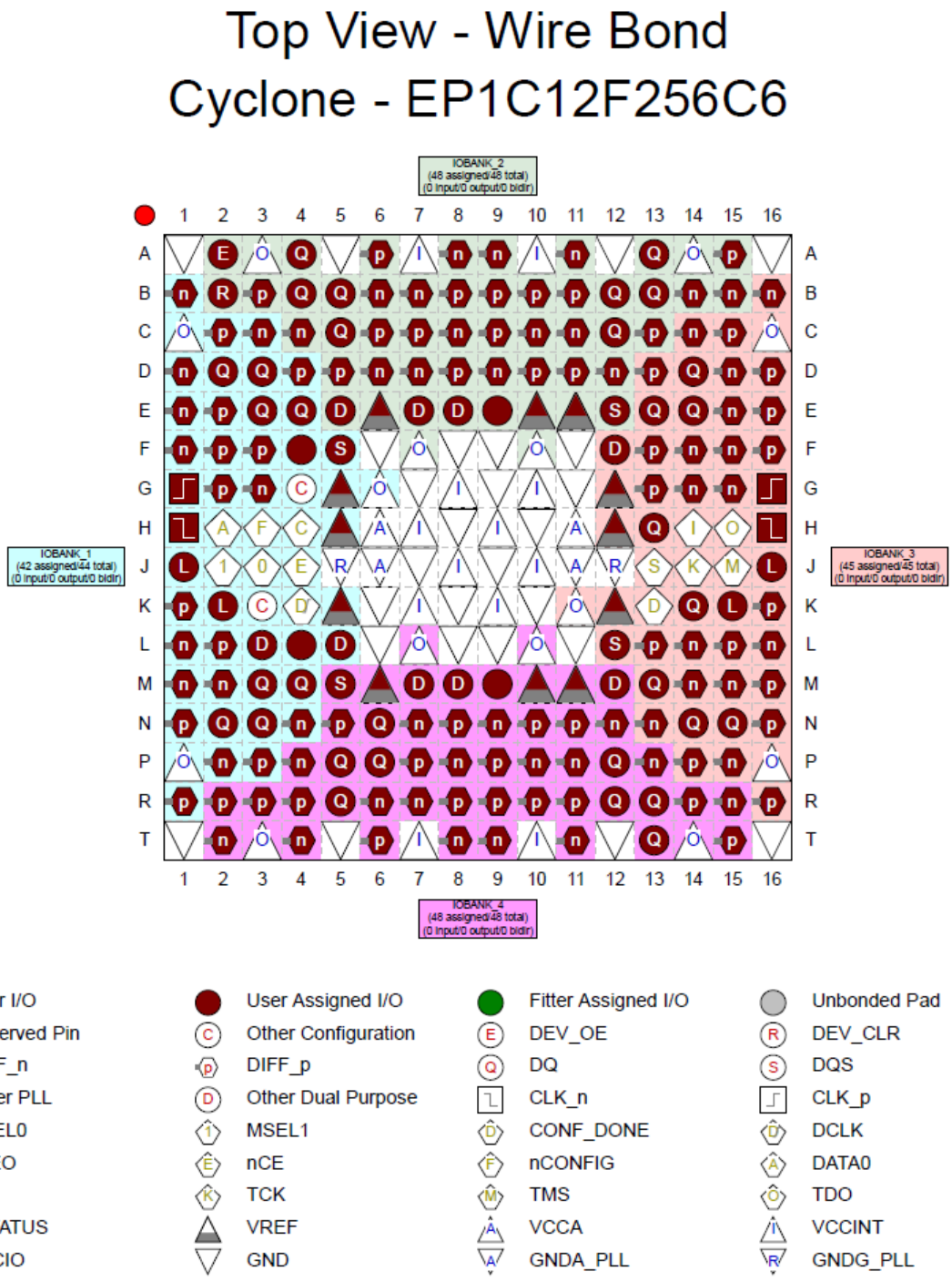


Figure 11-3 U152 MCB FPGA Quartus-II V9.1 pin planner output. This is the view looking down on the top of the chip.

11.4 U153 MCB FPGA Pinout

This section contains an exhaustive chip pinout listing generated by the Quartus-II FPGA compiler, and the Quartus-II pin planner graphic. The U153 MCB FPGA is implemented in an Altera Cyclone EP1C12F256C6 FPGA, and compiles with the Quartus-II V9.1 compiler.

Pin Name/Usage	Location	Dir.	I/O Standard	Voltage	I/O Bank
GND	A1	gnd			
MCB_ADDR8BIT_F7[5]	A2	output	2.5 V		2
VCCIO2	A3	power		2.5V	2
MCB_ADDR8BIT_F7[7]	A4	output	2.5 V		2
GND	A5	gnd			
MCB_ADDR4BIT_F7[1]	A6	output	2.5 V		2
VCCINT	A7	power		1.5V	
MCB_ADDR8BIT_F6[0]	A8	output	2.5 V		2
MCB_ADDR8BIT_F0[2]	A9	output	2.5 V		2
VCCINT	A10	power		1.5V	
MCB_ADDR8BIT_F0[3]	A11	output	2.5 V		2
GND	A12	gnd			
MCB_ADDR4BIT_F0[3]	A13	output	2.5 V		2
VCCIO2	A14	power		2.5V	2
MCB_ADDR4BIT_F0[0]	A15	output	2.5 V		2
GND	A16	gnd			
MCB_ADDR8BIT_F7[2]	B1	output	2.5 V		1
MCB_ADDR8BIT_F7[0]	B2	output	2.5 V		2
MCB_ADDR8BIT_F7[3]	B3	output	2.5 V		2
MCB_ADDR8BIT_F7[6]	B4	output	2.5 V		2
MCB_ADDR4BIT_F7[3]	B5	output	2.5 V		2
MCB_ADDR4BIT_F7[2]	B6	output	2.5 V		2
MCB_ADDR4BIT_F7[0]	B7	output	2.5 V		2
MCB_ADDR8BIT_F6[2]	B8	output	2.5 V		2
MCB_ADDR8BIT_F0[0]	B9	output	2.5 V		2
MCB_ADDR8BIT_F0[5]	B10	output	2.5 V		2
MCB_ADDR8BIT_F0[6]	B11	output	2.5 V		2
MCB_ADDR8BIT_F0[7]	B12	output	2.5 V		2
MCB_ADDR4BIT_F0[2]	B13	output	2.5 V		2
MCB_ADDR4BIT_F0[1]	B14	output	2.5 V		2
MCB_ADDR6BIT_F1[4]	B15	output	2.5 V		2
MCB_ADDR6BIT_F0[4]	B16	output	2.5 V		3
VCCIO1	C1	power		2.5V	1
MCB_ADDR8BIT_F7[4]	C2	output	2.5 V		1
MCB_CLK_F[64]	C3	output	2.5 V		1
MCB_CLK_F[63]	C4	output	2.5 V		2
MCB_CLK_F[62]	C5	output	2.5 V		2
MCB_CLK_F[61]	C6	output	2.5 V		2
MCB_CLK_F[60]	C7	output	2.5 V		2
MCB_CLK_F[59]	C8	output	2.5 V		2
MCB_ADDR6BIT_F0[1]	C9	output	2.5 V		2
MCB_ADDR6BIT_F0[3]	C10	output	2.5 V		2
MCB_ADDR6BIT_F0[5]	C11	output	2.5 V		2
MCB_ADDR6BIT_F0[0]	C12	output	2.5 V		2
MCB_ADDR6BIT_F0[2]	C13	output	2.5 V		2
MCB_CLK_F[66]	C14	output	2.5 V		3
MCB_CLK_F[67]	C15	output	2.5 V		3
VCCIO3	C16	power		2.5V	3
MCB_ADDR8BIT_F7[1]	D1	output	2.5 V		1

MCB_ADDR8BIT_F4[3]	D2	output	2.5 V		1	
MCB_ADDR8BIT_F4[7]	D3	output	2.5 V		1	
MCB_ADDR4BIT_F4[2]	D4	output	2.5 V		1	
MCB_ADDR4BIT_F4[0]	D5	output	2.5 V		2	
MCB_ADDR8BIT_F3[0]	D6	output	2.5 V		2	
MCB_ADDR8BIT_F3[3]	D7	output	2.5 V		2	
MCB_CLK_F[58]	D8	output	2.5 V		2	
MCB_CLK_F[65]	D9	output	2.5 V		2	
MCB_ADDR4BIT_F3[0]	D10	output	2.5 V		2	
MCB_ADDR8BIT_F2[3]	D11	output	2.5 V		2	
MCB_ADDR8BIT_F2[7]	D12	output	2.5 V		2	
MCB_ADDR4BIT_F2[3]	D13	output	2.5 V		3	
MCB_ADDR4BIT_F2[2]	D14	output	2.5 V		3	
MCB_ADDR4BIT_F2[1]	D15	output	2.5 V		3	
MCB_CLK_F[68]	D16	output	2.5 V		3	
MCB_ADDR8BIT_F4[0]	E1	output	2.5 V		1	
MCB_ADDR8BIT_F4[5]	E2	output	2.5 V		1	
MCB_ADDR8BIT_F4[6]	E3	output	2.5 V		1	
MCB_ADDR4BIT_F4[3]	E4	output	2.5 V		1	
MCB_ADDR4BIT_F4[1]	E5	output	2.5 V		2	
MCB_ADDR8BIT_F3[2]	E6	output	2.5 V		2	
MCB_ADDR8BIT_F3[5]	E7	output	2.5 V		2	
MCB_ADDR8BIT_F3[1]	E8	output	2.5 V		2	
RESET_n	E9	input	2.5 V		2	
MCB_ADDR4BIT_F3[1]	E10	output	2.5 V		2	
MCB_ADDR8BIT_F2[5]	E11	output	2.5 V		2	
MCB_ADDR8BIT_F2[6]	E12	output	2.5 V		2	
MCB_ADDR8BIT_F1[7]	E13	output	2.5 V		3	
MCB_ADDR6BIT_F1[2]	E14	output	2.5 V		3	
MCB_ADDR8BIT_F1[5]	E15	output	2.5 V		3	
MCB_ADDR4BIT_F2[0]	E16	output	2.5 V		3	
MCB_ADDR8BIT_F4[2]	F1	output	2.5 V		1	
MCB_ADDR4BIT_F5[2]	F2	output	2.5 V		1	
MCB_ADDR8BIT_F5[7]	F3	output	2.5 V		1	
MCB_ADDR8BIT_F5[3]	F4	output	2.5 V		1	
MCB_ADDR8BIT_F5[0]	F5	output	2.5 V		1	
GND	F6	gnd				
VCCIO2	F7	power		2.5V	2	
GND	F8	gnd				
GND	F9	gnd				
VCCIO2	F10	power		2.5V	2	
GND	F11	gnd				
MCB_ADDR4BIT_F1[3]	F12	output	2.5 V		3	
MCB_ADDR8BIT_F6[1]	F13	output	2.5 V		3	
MCB_ADDR8BIT_F1[6]	F14	output	2.5 V		3	
MCB_ADDR8BIT_F1[3]	F15	output	2.5 V		3	
MCB_ADDR8BIT_F1[2]	F16	output	2.5 V		3	
MCB_ADDR[6]	G1	input	2.5 V		1	
MCB_ADDR4BIT_F5[3]	G2	output	2.5 V		1	
MCB_ADDR8BIT_F5[6]	G3	output	2.5 V		1	
MCB_ADDR_SEL[11]	G4	input	2.5 V		1	
MCB_ADDR8BIT_F5[2]	G5	output	2.5 V		1	
VCCIO1	G6	power		2.5V	1	
GND	G7	gnd				
VCCINT	G8	power		1.5V		
GND	G9	gnd				
VCCINT	G10	power		1.5V		
GND	G11	gnd				
MCB_ADDR[4]	G12	input	2.5 V		3	
CCLK_F[8]	G13	output	2.5 V		3	
MCB_ADDR6BIT_F1[0]	G14	output	2.5 V		3	
MCB_ADDR6BIT_F1[1]	G15	output	2.5 V		3	
MCB_ADDR_SEL[15]	G16	input	2.5 V		3	
MCB_ADDR[5]	H1	input	2.5 V		1	
DATA0	H2	input			1	

nCONFIG	H3				1	
nCEO	H4				1	
MCB_ADDR8BIT_F5[5]	H5	output	2.5 V		1	
VCCA_PLL1	H6	power		1.5V		
VCCINT	H7	power		1.5V		
GND	H8	gnd				
VCCINT	H9	power		1.5V		
GND	H10	gnd				
VCCA_PLL2	H11	power		1.5V		
MCB_CLK_F[31]	H12	output	2.5 V		3	
MCB_CLK_F[57]	H13	output	2.5 V		3	
TDI	H14	input			3	
TDO	H15	output			3	
MCB_ADDR_SEL[14]	H16	input	2.5 V		3	
MCB_ADDR4BIT_F5[0]	J1	output	2.5 V		1	
MSEL1	J2				1	
MSEL0	J3				1	
nCE	J4				1	
GNDG_PLL1	J5	gnd				
GNDA_PLL1	J6	gnd				
GND	J7	gnd				
VCCINT	J8	power		1.5V		
GND	J9	gnd				
VCCINT	J10	power		1.5V		
GNDA_PLL2	J11	gnd				
GNDG_PLL2	J12	gnd				
nSTATUS	J13				3	
TCK	J14	input			3	
TMS	J15	input			3	
CCLK_F[7]	J16	output	2.5 V		3	
MCB_ADDR4BIT_F5[1]	K1	output	2.5 V		1	
MCB_ADDR8BIT_F4[4]	K2	output	2.5 V		1	
GND*	K3				1	
DCLK	K4	bidir			1	
MCB_ADDR4BIT_F6[0]	K5	output	2.5 V		1	
GND	K6	gnd				
VCCINT	K7	power		1.5V		
GND	K8	gnd				
VCCINT	K9	power		1.5V		
GND	K10	gnd				
VCCIO3	K11	power		2.5V	3	
MCB_CLK_F[56]	K12	output	2.5 V		3	
CONF_DONE	K13				3	
MCB_ADDR8BIT_F2[1]	K14	output	2.5 V		3	
CCLK_F[6]	K15	output	2.5 V		3	
CCLK_F[5]	K16	output	2.5 V		3	
MCB_CLK_F[41]	L1	output	2.5 V		1	
MCB_ADDR8BIT_F4[1]	L2	output	2.5 V		1	
MCB_CLK_F[39]	L3	output	2.5 V		1	
MCB_CLK_F[37]	L4	output	2.5 V		1	
MCB_ADDR[1]	L5	input	2.5 V		1	
GND	L6	gnd				
VCCIO4	L7	power		2.5V	4	
GND	L8	gnd				
GND	L9	gnd				
VCCIO4	L10	power		2.5V	4	
GND	L11	gnd				
MCB_ADDR8BIT_F6[4]	L12	output	2.5 V		3	
CCLK_F[0]	L13	output	2.5 V		3	
CCLK_F[4]	L14	output	2.5 V		3	
CCLK	L15	input	2.5 V		3	
CCLK_F[3]	L16	output	2.5 V		3	
MCB_CLK_F[42]	M1	output	2.5 V		1	
MCB_CLK_F[45]	M2	output	2.5 V		1	
MCB_CLK_F[40]	M3	output	2.5 V		1	

MCB_CLK_F[38]	M4	output	2.5 V		1
MCB_CLK_F[35]	M5	output	2.5 V		4
MCB_ADDR4BIT_F6[1]	M6	output	2.5 V		4
MCB_ADDR4BIT_F6[2]	M7	output	2.5 V		4
MCB_CLK_F[71]	M8	output	2.5 V		4
MCB_ADDR4BIT_F1[0]	M9	output	2.5 V		4
MCB_ADDR8BIT_F2[0]	M10	output	2.5 V		4
MCB_ADDR_SEL[12]	M11	input	2.5 V		4
MCB_ADDR8BIT_F8[7]	M12	output	2.5 V		4
MCB_ADDR_SEL[13]	M13	input	2.5 V		3
MCB_ADDR6BIT_F1[5]	M14	output	2.5 V		3
CCLK_F[2]	M15	output	2.5 V		3
CCLK_F[1]	M16	output	2.5 V		3
MCB_CLK_F[43]	N1	output	2.5 V		1
MCB_CLK_F[46]	N2	output	2.5 V		1
MCB_CLK_F[47]	N3	output	2.5 V		1
MCB_ADDR8BIT_F5[4]	N4	output	2.5 V		1
MCB_CLK_F[36]	N5	output	2.5 V		4
MCB_CLK_F[33]	N6	output	2.5 V		4
MCB_ADDR4BIT_F6[3]	N7	output	2.5 V		4
MCB_ADDR8BIT_F3[7]	N8	output	2.5 V		4
MCB_ADDR4BIT_F3[2]	N9	output	2.5 V		4
MCB_ADDR8BIT_F2[2]	N10	output	2.5 V		4
MCB_ADDR4BIT_F1[2]	N11	output	2.5 V		4
MCB_ADDR[3]	N12	input	2.5 V		4
MCB_ADDR8BIT_F8[2]	N13	output	2.5 V		3
MCB_ADDR8BIT_F2[4]	N14	output	2.5 V		3
MCB_ADDR8BIT_F0[4]	N15	output	2.5 V		3
MCB_ADDR8BIT_F1[0]	N16	output	2.5 V		3
VCCIO1	P1	power		2.5V	1
MCB_ADDR[0]	P2	input	2.5 V		1
MCB_CLK_F[48]	P3	output	2.5 V		1
MCB_ADDR8BIT_F5[1]	P4	output	2.5 V		4
MCB_CLK_F[72]	P5	output	2.5 V		4
MCB_CLK_F[34]	P6	output	2.5 V		4
MCB_CLK_F[52]	P7	output	2.5 V		4
MCB_ADDR8BIT_F3[6]	P8	output	2.5 V		4
MCB_ADDR4BIT_F3[3]	P9	output	2.5 V		4
MCB_ADDR4BIT_F1[1]	P10	output	2.5 V		4
MCB_CLK_F[32]	P11	output	2.5 V		4
MCB_ADDR[7]	P12	input	2.5 V		4
MCB_ADDR8BIT_F8[5]	P13	output	2.5 V		4
MCB_ADDR6BIT_F1[3]	P14	output	2.5 V		3
MCB_ADDR8BIT_F0[1]	P15	output	2.5 V		3
VCCIO3	P16	power		2.5V	3
MCB_CLK_F[44]	R1	output	2.5 V		1
MCB_ADDR8BIT_F8[3]	R2	output	2.5 V		4
MCB_ADDR8BIT_F8[4]	R3	output	2.5 V		4
MCB_ADDR[2]	R4	input	2.5 V		4
MCB_CLK_F[49]	R5	output	2.5 V		4
MCB_CLK_F[50]	R6	output	2.5 V		4
MCB_CLK_F[53]	R7	output	2.5 V		4
MCB_ADDR8BIT_F6[7]	R8	output	2.5 V		4
MCB_ADDR8BIT_F6[3]	R9	output	2.5 V		4
MCB_CLK_F[54]	R10	output	2.5 V		4
MCB_ADDR8BIT_F3[4]	R11	output	2.5 V		4
MCB_ADDR8BIT_F8[1]	R12	output	2.5 V		4
MCB_ADDR8BIT_F8[6]	R13	output	2.5 V		4
MCB_CLK_F[70]	R14	output	2.5 V		4
MCB_ADDR8BIT_F1[1]	R15	output	2.5 V		4
MCB_ADDR8BIT_F1[4]	R16	output	2.5 V		3
GND	T1	gnd			
MCB_CLK_F[73]	T2	output	2.5 V		4
VCCIO4	T3	power		2.5V	4
MCB_CLK	T4	input	2.5 V		4

```
GND                          : T5       : gnd    :                  :         :          :
MCB_CLK_F[51]                : T6       : output : 2.5 V            :         : 4        :
VCCINT                       : T7       : power  :                  : 1.5V    :          :
MCB_ADDR8BIT_F6[6]           : T8       : output : 2.5 V            :         : 4        :
MCB_ADDR8BIT_F6[5]           : T9       : output : 2.5 V            :         : 4        :
VCCINT                       : T10      : power  :                  : 1.5V    :          :
MCB_CLK_F[55]                : T11      : output : 2.5 V            :         : 4        :
GND                          : T12      : gnd    :                  :         :          :
MCB_ADDR8BIT_F8[0]           : T13      : output : 2.5 V            :         : 4        :
VCCIO4                       : T14      : power  :                  : 2.5V    : 4        :
MCB_CLK_F[69]                : T15      : output : 2.5 V            :         : 4        :
GND                          : T16      : gnd    :                  :         :          :
-------------------------------------------------------------------------------------------
 -- NC             : No Connect. This pin has no internal connection to the device.
 -- DNU            : Do Not Use. This pin MUST NOT be connected.
 -- VCCINT         : Dedicated power pin, which MUST be connected to VCC  (1.5V).
 -- VCCIO          : Dedicated power pin, which MUST be connected to VCC of its bank.
 --                               Bank 1:            2.5V
 --                               Bank 2:            2.5V
 --                               Bank 3:            2.5V
 --                               Bank 4:            2.5V
 -- GND            : Dedicated ground pin. Dedicated GND pins MUST be connected to GND.
 -- GND+           : Unused input pin. It can also be used to report unused dual-purpose pins.
 --                  This pin should be connected to GND. It may also be connected  to a
 --                  valid signal  on the board  (low, high, or toggling)  if that signal
 --                  is required for a different revision of the design.
 -- GND*           : Unused  I/O  pin.   For transceiver I/O banks (Bank 13, 14, 15, 16 and 17),
 --                  connect each pin marked GND* either individually through a 10k Ohm resistor
 --                  to GND or tie all pins together and connect through a single 10k Ohm resistor
 --                  to GND.
 --                  For non-transceiver I/O banks, connect each pin marked GND* directly to GND
 --                  or leave it unconnected.
 -- RESERVED       : Unused I/O pin, which MUST be left unconnected.
 -- RESERVED_INPUT    : Pin is tri-stated and should be connected to the board.
 -- RESERVED_INPUT_WITH_WEAK_PULLUP    : Pin is tri-stated with internal weak pull-up resistor.
 -- RESERVED_INPUT_WITH_BUS_HOLD       : Pin is tri-stated with bus-hold circuitry.
 -- RESERVED_OUTPUT_DRIVEN_HIGH        : Pin is output driven high.
-------------------------------------------------------------------------------------------
```

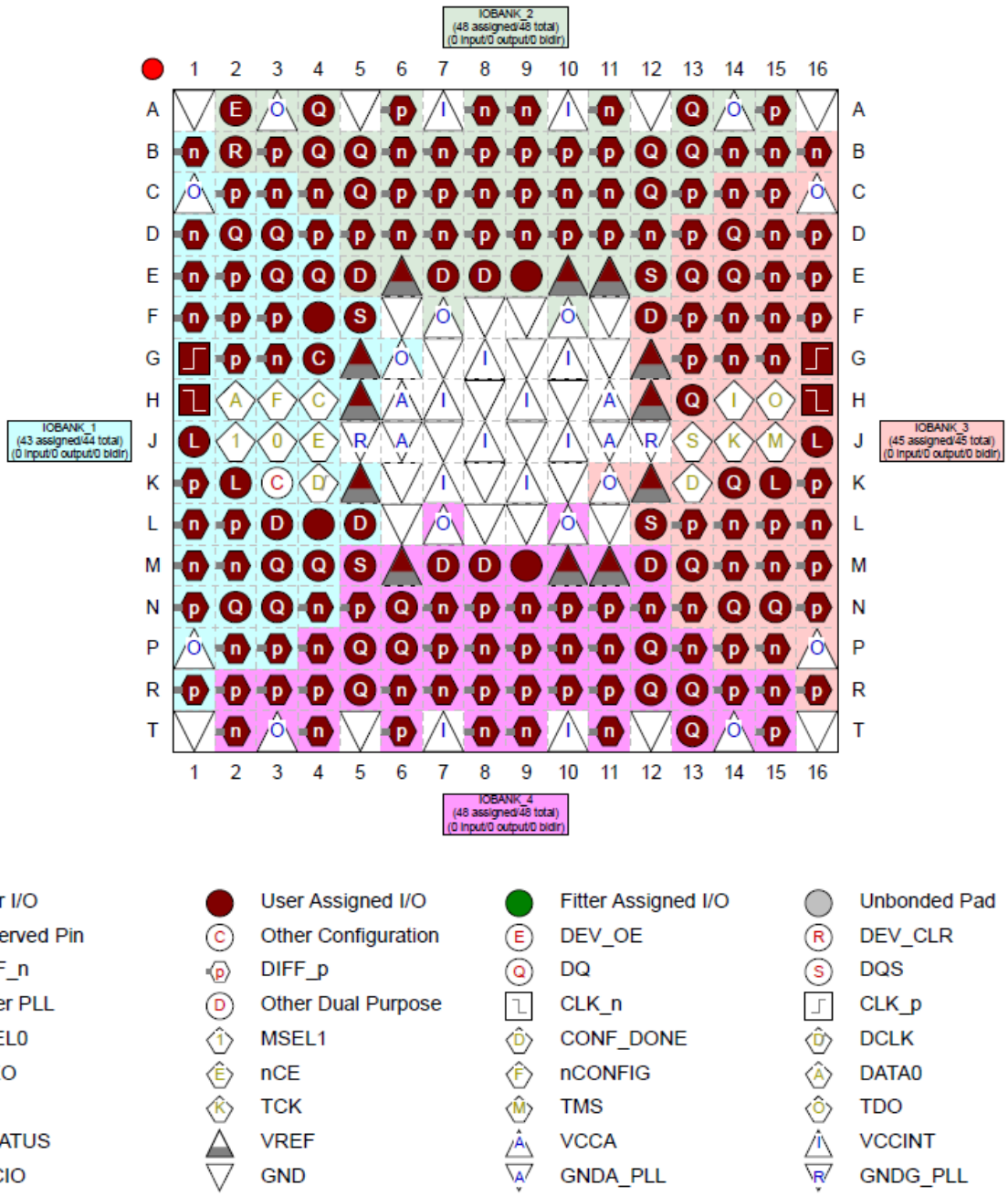
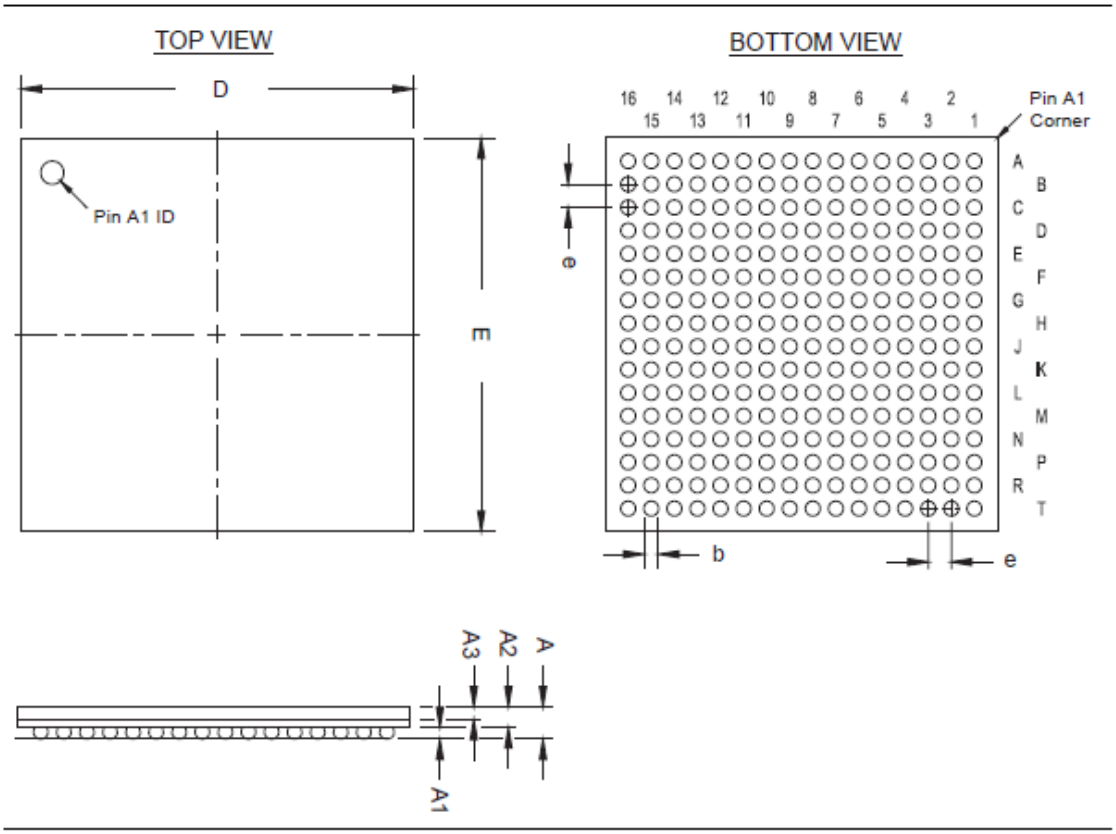


Figure 11-4 U153 MCB FPGA Quartus-II V9.1 pin planner output. This is the view looking down on the top of the chip.

11.5 Altera EP1C12F256C6 FBGA U150-U153 Package Drawing

For other package drawings, refer to the relevant FPGA or ASIC RFS documents.



Package Information	
Description	**Specification**
Ordering Code Reference	F
Package Acronym	FBGA
Substrate Material	BT
Solder Ball Composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MS-034 Variation: AAF-1
Lead Coplanarity	0.008 inches (0.20 mm)
Weight	1.5 g (Typ.)
Moisture Sensitivity Level	Printed on moisture barrier bag

Package Outline Dimension Table			
Symbol	**Millimeters**		
	Min.	**Nom.**	**Max.**
A	–	–	2.20
A1	0.30	–	–
A2	–	–	1.80
A3		0.70 REF	
D		17.00 BSC	
E		17.00 BSC	
b	0.50	0.60	0.70
e		1.00 BSC	

Figure 11-5 U150-U153 MCB FPGA Package Information.

11.6 MCB FPGA Programming Notes

For all FPGAs, except U150-U153 MCB FPGAs, refer to appendices of relevant RFS documents for information on how to put together FPGA bitstream files. Refer to section 7.3.1 for information on how the CPU programs FPGA configuration bitstreams.

The following figure is a screen-shot of the "Convert Programming Files" dialog in the Altera Quartus-II V9.1 software, showing the setup required to produce the .rbf (raw binary file) needed by the software to program the U150-U153 FPGAs.

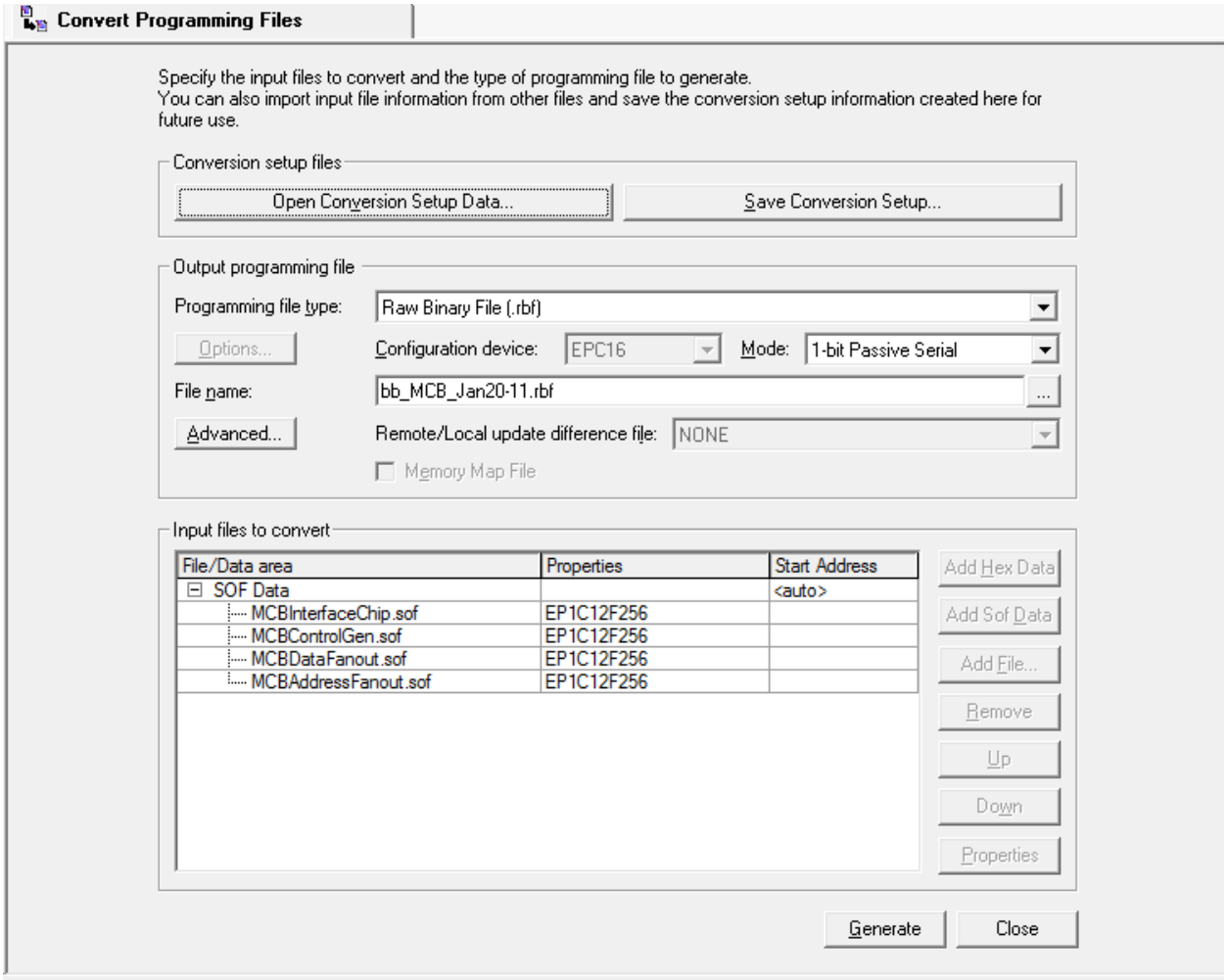


Figure 11-6 Altera Quartus-II "Convert Programming Files" screenshot showing settings necessary for generating the .rbf file for the U150-U153 MCB FPGAs.

Note that the ".sof" files listed are for U150-U153, in the order from top to bottom in the above figure. Thus, the MCB bitstream configuration daisy-chain on the board starts at U150 ("MCBInterfaceChip.sof"), then goes to U151, U152, and finally U153. Open the U150 Quartus project, and open "output_file.cof" to get this screen.

12 Troubleshooting Guide

This section contains a table to assist with troubleshooting of a board that is not functioning as intended. The board is very complex, and there are many things that can go wrong and manifest themselves in strange and bizarre ways, and so this table can, by no means, be completely exhaustive.

Problem	**Solution**
Board won't power up (indicated by all front-panel LEDs dark)	1. Ensure -48 VDC, within acceptable range and with correct polarity, is applied to both the top and bottom Power Connectors (Figure 6-1). 2. Ensure the TOP Power Connector CONTROL line has minimum +3.5 V, 8 mA source applied (w.r.t. GND-ERNI connector shields) 3. Remove power, check solder-in fuses F1 and F2 for continuity. 4. Ensure the front-panel "Power" switch is in the ON (up) position. 5. Check for damaged components on the board, in particular the power control line opto-couplers U101 and U102, and associated circuitry. 6. Check to ensure the control line on the ¼-brick Artesyn power supplies are at ~-48 V, w.r.t. the 48VR (Return) rail. The control line is the center pin on the input side of the power supply. 7. Check to ensure the thermostats mounted to the heatsink are closed-circuit. Check TO-220 legs for damage/disconnect. 8. Check to ensure the input transorbs, D42, D43, are not shorted.
One or more front-panel voltage LEDs are dark, board is malfunctioning.	Replace offending/failed power supply, check for problems as above. Note that the +3.3 V power supply is the master voltage reference, so if it has failed, all power LEDs will be dark.
The PCMC FPGA sometimes spontaneously resets (colloquially known as the "re-bootable effing problem").	This could be the single +3.3 V Artesyn power supply on the board glitching out. Replace.
The CPU suddenly can't see the PCMC FPGA PCI device (colloquially known as the "effing problem")	Check to ensure the PC/104+ CPU to PCMC connector pins are properly soldered to the CPU board (ECO-A25300N0047-CPU50_1_SOLDER), and micro-scope inspect and remove any gold hairs.

Problem	Solution
Board powers up, all power supply LEDs ok, but CMIB Status LED doesn't turn GREEN after ~2 minutes.	CPU doesn't boot properly, and this can be caused by many things: 1. Ensure the PC/104+ CPU's MAC address (found by looking up the S/N of the CPU module in the MITR database) is entered in the network DNS lookup table/ensure the CPU obtains a valid IP address for the network. 2. The PCMC FPGA's local EEPROM is corrupted, and must be re-programmed via the front-panel port. Refer to section 6.5. 3. The PC/104+ CPU module's RAM module is bad or needs to be re-seated. It is on the underside of the board; remove the CPU module from the stack, re-seat/replace, re-install, re-test. 4. The network boot server is not set properly. Refer to section 7.5. 5. The PC/104+ CPU module is malfunctioning. Replace. 6. The PCMC card is malfunctioning. Replace.
The Startup Sequencer (section 7.6) is run, but one or more FPGAs won't boot.	1. Check to ensure the CPU can find all the boot binaries. 2. Check to ensure the clock and data lines going to the offending FPGA daisy-chain are active coming out of U152, and U153 (sections 5.7.3 and 5.7.4). Trace all the way to the FPGAs. Repair board as necessary.
The Startup Sequencer is run, the FPGAs boot, but it is stuck on "RXP Start".	Check to ensure the clock source (wafer-0 and wafer-16 of the X-ERNI connector, or the SMA External Clock input) is present and valid. If, in the RXP GUI, the "PLL lock" LEDs are not all GREEN, then there is a clock source problem, or a board fault. The 1.8 V power supply may have failed (check the 1.8 V power supply LED in the top board GUI—see board schematic page 71).

Problem	Solution
One or more errors result when the Startup Sequencer is run.	There can be a myriad of causes. "Clear all Errors" on the top-level Baseline Board GUI, and see which chips are complaining: ***1.*** If a Correlator Chip icon is showing low or no voltage, try re-programming the Accel regulator (bullet M Figure 5-10). If this doesn't work, and the LTA settings are correct to power-up the chip, it could be a bad regulator. ***Be sure when replacing the Accel regulator to use the correct regulator version; board S/Ns≤2008 MUST use version "XXX"; board S/Ns>2008 MUST use version "REVC". The regulator version is marked on the package.*** 2. If one or more FPGA icons are RED, it means the CPU can't talk to them. Could be due to a malfunctioning reset line from the MCB FPGA U150 (Table 5-1). 3. If one or more comm. lines on the board are RED, it indicates an error. Drill into the chip(s) GUIs to try to nail down the problem and probe the board for the cause. Repair/replace as necessary.
Top-level board GUI Recirc icon LEDs are YELLOW.	The Recirc FPGAs are in test-vector generator mode.
One or more Correlator Chips are reporting errors on inputs.	1. Drill down into the Correlator Chip icon; if the DUMP_SYNC line is RED (bullet B, Figure 5-8), it is not necessarily an error, and indicates that the X/Y DUMP_SYNC signals coming into the chip are not coincident in time. This *is* an error if running dynamic recirculation. 2. If a number of the X-status or Y-status lines are RED, it could mean a "Re-phase" must be performed (bullet I, Figure 5-1), or that there is a mis-match between the Recirc FPGA generating Test vectors, and the Correlator Chip receiving Test vectors (TVEN). 3. There is a hard fault on the board. Repair/replace as necessary.
Tests (section 13) indicate an entire column or row of WARNings, and the test involves using the external recirculation RAM. When a test is run w/o the recirculation RAM, the problem goes away.	The Recirc FPGA feeding the row or column has a communications problem with one or both of its external recirculation RAM chips, or the recirculation RAM chip is bad or partially bad. Probe and repair/replace as necessary.

Problem	Solution
No data is flowing from one or more Correlator Chips to the associated LTA(s). This could take the form of some sort of data flowing, but frames being aborted by the LTA (i.e. the Frame Abort LED in the LTA GUI is GREEN).	1. The Correlator Chip correlation enable "CEN" button is not on (bullet A of Figure 5-8). 2. The LTA "Enable Data Flow" is not checked (bullet G of Figure 5-10). 3. If one or more LTA LEDs are RED or GREY (refer to associated descriptions of Figure 5-10), then there could be a board hard fault. 4. The Correlator Chip internal logic may be messed up due to loss of clock or a clock glitch, or bad/messed-up dump control signaling into the chip. Full reset (CC reset, and PLL reset), restart, and re-configure the chip. 5. The LTA FPGA could be experiencing a rare "soft" configuration RAM corruption. Reboot the FPGAs. 6. The Correlator Chip is bad, and must be replaced.
No LTA or VDIF frames are coming out of the GigE FPGA.	1. The "Discard Tx Frames" check-box in the GigE GUI is on (bullet D, Figure 5-12), causing frames to be tossed into the "bit bucket". 2. The GigE GUI "Enable LTA Data Flow" is not checked.
LTA and/or VDIF frames are exiting the board, but the destination computers don't detect them.	1. If the SFP1 (or SFP2) LED is RED, it indicates no good connection to the far-end computer, and could indicate an external wiring problem. Even if this is GREEN, there could be a wiring fault in the transmit data lines, and the far end port LED could be OFF, indicating the problem. 2. The LTA (or VDIF) IEEE 802.3 and/or UDP/IP source and destination addresses are not set correctly. Note that the destination MAC and destination IP addresses for LTA data, are set in the LTA, not the GigE. Note that the GigE FPGA has no capability of automatically determining destination addresses from switch signaling and must be explicitly set.

Problem	Solution
The GigE FPGA VDIF packet Rx has the "Sy" LED RED.	1. "Enable Phasing" in the RXP GUI is not checked on. 2. The 1.024 Gbps link from the RXP to the GigE FPGA is faulty. Repair as necessary.
One or more board temperature indicators are out of reasonable range.	Probably a hard board fault. Check temperature sensors for damage (see page 38 of the board schematic). On V2.1 boards, check correct application of ECO-A25300N0022-25080
One or more FPGAs are behaving strangely, and it might have been quite some time since the FPGAs on the board were booted.	On a rare (but not unusually rare) occasion, FPGA configuration SRAMs (i.e. the layer of SRAM in the chip which sets the "FPGA personality"), can get corrupted. Just resetting the chip won't clear the problem, the FPGA(s) must be re-programmed/re-booted by rebooting the board or re-running the Startup Sequencer from scratch. This is a "soft" FPGA failure.
Running "Test Pattern" vectors yields a column or row "WARN" pattern (see section 13) in lagfan output indicating bad data originating from some Correlator Chip. However, running Recirc "Test Vectors", with Correlator Chips in "TESTV" mode, indicates no connectivity issues.	This paradox has been seen in at least one board, and was found to result when a Correlator Chip output CMOS driver was malfunctioning such that the NMOS gate was turning on (i.e. driving low), but the PMOS gate was not (floating high, but high enough to mostly work).

13 Testing Procedures and Notes

The MITR database contains details of testing Procedures for Baseline Boards. These Procedures appear in every instance of a Baseline Board in the database.

Basic standalone testing, which tests everything but RXP inputs and Y-Recirc outputs, can be performed with only power, network connections to the M&C Ethernet port and the SFP1 port, and a 128 MHz External clock applied. In this case, the RXP chips are set for "External clock" (or wafer clock if there is a clock on wafer-0 and wafer-16), and "Test Pattern" generation. This setup floods the board with PRN vectors, suitable for comparison purposes but producing no sensible fringes, and has an LTA integration time of 1 second. If "Sky Simulator" is chosen as the test data source, there are 10 μseconds of sky-simulation vectors once every 10 msec (with the rest of the time marked as "invalid"), which correlate to yield fringes. Vectors are such that for every k*(k+1) correlation, where "k" are even wafers 0, 2, 4, 6, (equivalent to BBIDs) there is a continuum correlation, with k/2+1 spectral lines. If k is correlated with something other than $(k+1)$[28], then there is a spectral-line correlation only, with k/2+1 spectral lines. This provides a unique correlated signature for any combination of data stream cross-correlations. With "Sky Simulator", the LTA integration time is 100 msec.

There are 10 pre-defined tests, tests 1-10, also documented in applicable Procedures in the MITR database, with the name of the test indicative of the test setup. Each of these tests causes the board to generate LTA frames, such that there are redundant operations performed on the board. A computer hooked up to SFP1 (directly, or through a switch), with the LTAs and GigE FPGAs set for correct source and destination addresses, captures LTA UDP/IP frames and saves them to ".blf" (binary lag frame) files.

The 'lagfan' utility program is then run in the directory where the .blf files reside.

```
>lagfan –a –q –diff
```

lagfan reads files, one at a time, and performs exhaustive comparisons. Once complete, lagfan gives a clear indication if there are problems. The last part of lagfan output looks something like this:

```
***Board summary map***
        X7
   Y7   OK    OK    OK    OK    OK    OK    OK    OK
        OK    OK    OK    OK    OK    OK    OK    OK
        OK    OK    OK    OK    OK    OK    OK    OK
        OK    OK    OK    OK    OK    OK    OK    OK
        OK    OK    OK    OK    OK    OK    OK    OK
        OK    OK    OK    OK    OK    OK    OK    OK
        OK    OK    OK    OK    OK    OK    OK    OK
```

[28] Except, k*k is an auto-correlation.

```
        OK    OK    OK    OK    OK    OK    OK    OK
  END BOARD S/N: 2068
```

```
==================Finished printing TOTAL board error statistics ======================

--------------------------------------------------------------------------------
Time: 2010-045-15:49:10
TOTAL ERROR STATISTICS:
        Total X input Sync Errs: 0
        Total Y input Sync Errs: 0
        Total accumulator overflow (OV) Errs: 0
        Total accumulator overrun (OVR) Errs: 0
        Total comparison Errs: 0
--------------------------------------------------------------------------------
```

Text indicators in the X/Y matrix above indicate the status of the test for a particular chip as follows:

OK – This chip has shown no comparison errors and is completely OK.

ok? – This chip did not show any comparison errors, but a frame was not detected from every CCC.

Warn – This chip has shown some comparison errors, but is probably not the source of the problem.

WARN* – This chip has shown a large number of comparison errors, and this chip, or one feeding it is the problem.

BAD? – This chip has 100% comparison errors on all tests run, and is probably bad.

NoCmp – No comparisons performed with this chip. Something peripheral is fishy.

NoRec – No LTA frames for this chip were detected.

Note that if everything is not "OK", something is likely wrong, and the pattern of "WARN*" or "Warn", can lead a troubleshooter to determining the fault. For example a "BAD?" chip can cause a number of other chips to generate "Warn". In another example, a "WARN" in an entire row or column can be indicative of a Recirc FPGA source problem, which, if the test uses recirculation, could indicate a bad external Recirc FPGA SRAM or connection to it. An exhaustive Correlator Chip matrix printout above this summary can be used to help to pinpoint the cause of the problem, bearing in mind that data flows in a daisy-chain fashion from chip to chip, upwards in columns, and right to left in rows.

Note that the Upper and Lower RXP FPGAs generate "Test Pattern" and "Sky Simulator" vectors with wildly different TIMECODE values. This is done because there is no way, in test mode, to ensure they are *exactly* the same, and having them close to each other, could result in false comparisons and false results. This is why, in some cases one "BAD?" can make only ½ of the chips on the board show "Warn".

The lagfan program is written in 'C' and is completely portable as it contains no references to anything other than standard Linux ".h" files. lagfan is on subversion, and is in "/widar/tools/blfutils/lagfan".

lagfan also has the ability to integrate data in various ways, and produce LTA*.dat and TRACE*.dat output files to allow for "lagcomp" display, or import into other display/analysis programs. To determine lagfan help, type "lagfan" <RET> or "lagfan –h". The most common use of lagfan in this case is:

```
>lagfan –a –q –i all
```

Which integrates all data available, to produce one or more LTA*.dat files.

LTA*.dat files contain two columns of ASCII floating-point numbers, representing complex lag values vs lag number. The first column is the real part, the second column is the imaginary part. An example of the first few lines of a LTA*.dat file output is as follows:

```
DVCOUNT=1.675302300000000e+09
-1.508411228230272e-02 -7.652761534440679e-03
-6.076299184929191e-03 1.195175342384476e-04
2.052887052086062e-02 4.322912945323360e-03
1.100967747731260e-02 7.701038194718649e-03
-5.750245791461039e-03 -1.095100508129190e-02
1.619612173874530e-04 -8.440493396326144e-03
7.846641170372655e-03 -7.214611357007031e-03
```

The first line indicates the data valid count, and can be used by any program to calculate the SNR of the data.

TRACE*.dat files contain ASCII floating-point values in 3 columns. The first column is amplitude, the second column is delay (at the decimated [correlated] sample rate), and the third column is phase in degrees. Time is the record/line number. Typical lagfan use for TRACE output is:

```
>lagfan –a –q –i 1 –trace all
```

This performs no integration[29], and produces TRACE file output for as many records as are available. To limit the TRACE file output to, say, the first 100 points, use "`-trace 100`". To integrate more than one record to produce a TRACE line output, use "`-i n`". An example of the first few lines of a TRACE*.dat file output is as follows:

```
1.9844659800e+00        -1.5036865774e-02        1.2847034047e+00
1.9844659800e+00        -1.5036865774e-02        1.2847034047e+00
1.9844659800e+00        -1.5036865774e-02        1.2847034047e+00
```

[29] In the TRACE*.dat file data. However, integrated LTA*.dat files are also/still produced.

```
1.9844659800e+00        -1.5036865774e-02       1.2847034047e+00
1.9844659800e+00        -1.5036865774e-02       1.2847034047e+00
1.9844659800e+00        -1.5036865774e-02       1.2847034047e+00
1.9844659800e+00        -1.5036865774e-02       1.2847034047e+00
```

In this example each line is the same, as “Sky Simulator” vectors are correlated.

13.1 Testing W/O Heatsink Attached

If a board is to be tested without the heatsink attached, adequate airflow must be provided to prevent overheating. Overheating is the condition where any part of the board PCB exceeds 50 ^{o}C. In addition, it is important that the RXP FPGAs be affixed with temporary heatsinks, as they dissipate ~9 W each, and will quickly overheat and possibly be damaged.

14 Known Bugs, Workarounds, Anomalies

14.1 No -48 VDC In-Rush Current Protection

There is no in-rush current protection on the -48 VDC supply lines. Due to the input decoupling capacitors, if the board is plugged into a -48 VDC-powered socket arcing on the PWR connectors' contacts will occur. This is not particularly damaging unless it is done many times. Therefore, it is good practice to plug the board into the socket, and then apply power to the socket.

14.2 V2.1 Boards, GigE GUI SFP Module Status Does Not Indicate Link State

As noted on page 57, for V2.1 boards (S/Ns ≤ 2008), the SFP1 LED in the GigE GUI does not indicate the state of the GigE link.

14.3 Correlator Chip Internal State Scrambled

Anytime the X or Y input clock to the Correlator Chip gets interrupted, the internal state of the chip can get scrambled, which results in unpredictable operation of the chip. Most notably, this manifests itself as the chip not producing frames when it should, or producing garbage frames that the LTA rejects (detectable when the LTA GUI "From CC" "Frame Abort" LED is GREEN). This state can also be entered if DUMPTRIG signaling messes up normal DUMP_SYNC/DUMP_EN signaling.

15 References

[1] Carlson, B., “HM Gbps Cable Signaling Specification”, PROTOCOL Document A25022N0041, Revision 1.43, May 21, 2010.

[2] Zhang, H., “PC/104 Monitor/Control Mezzanine Card (PCMC)”, RFS Document A25145N0000, Revision 1.2, July 9, 2009.

[3] Carlson, B., “EVLA Correlator Cross-Bar Board”, USER MANUAL Document A25121N0001, Revision 1.1, June 16, 2010.

[4] “IPC 6012 PWB COMPLIANCY FOR EVLA BASELINE BOARD”, BreconRidge Corporation, Version 0.1, April 27, 2009

16 Appendices

16.1 Appendix I EVLA Baseline Rack Decal

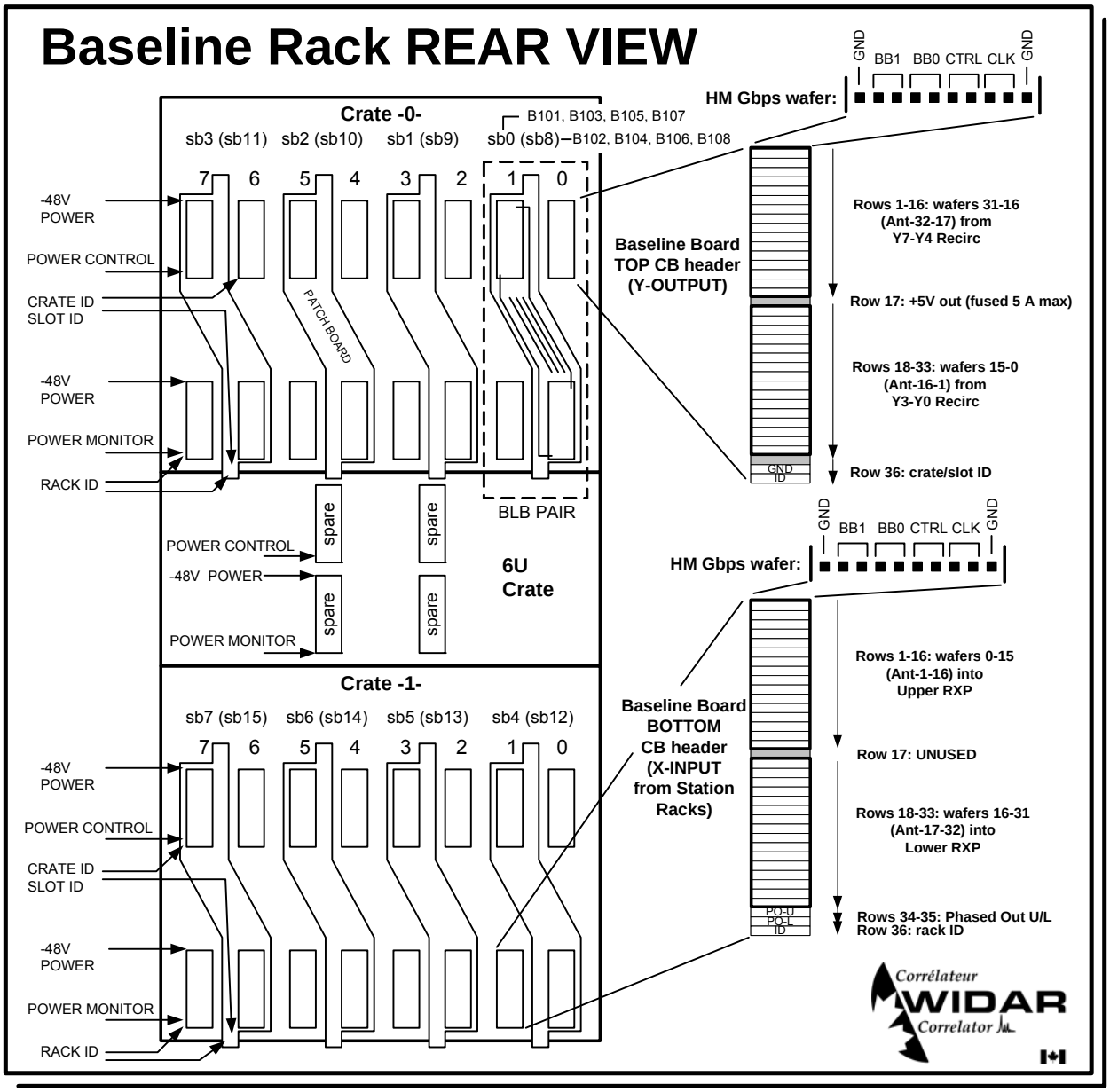


Figure 16-1 This is the decal installed at the back of every Baseline rack in the EVLA system. It shows the layout and numbering used for racks and Baseline Board pair sub-band assignements.

16.2 Appendix II EVLA Station Rack Decal

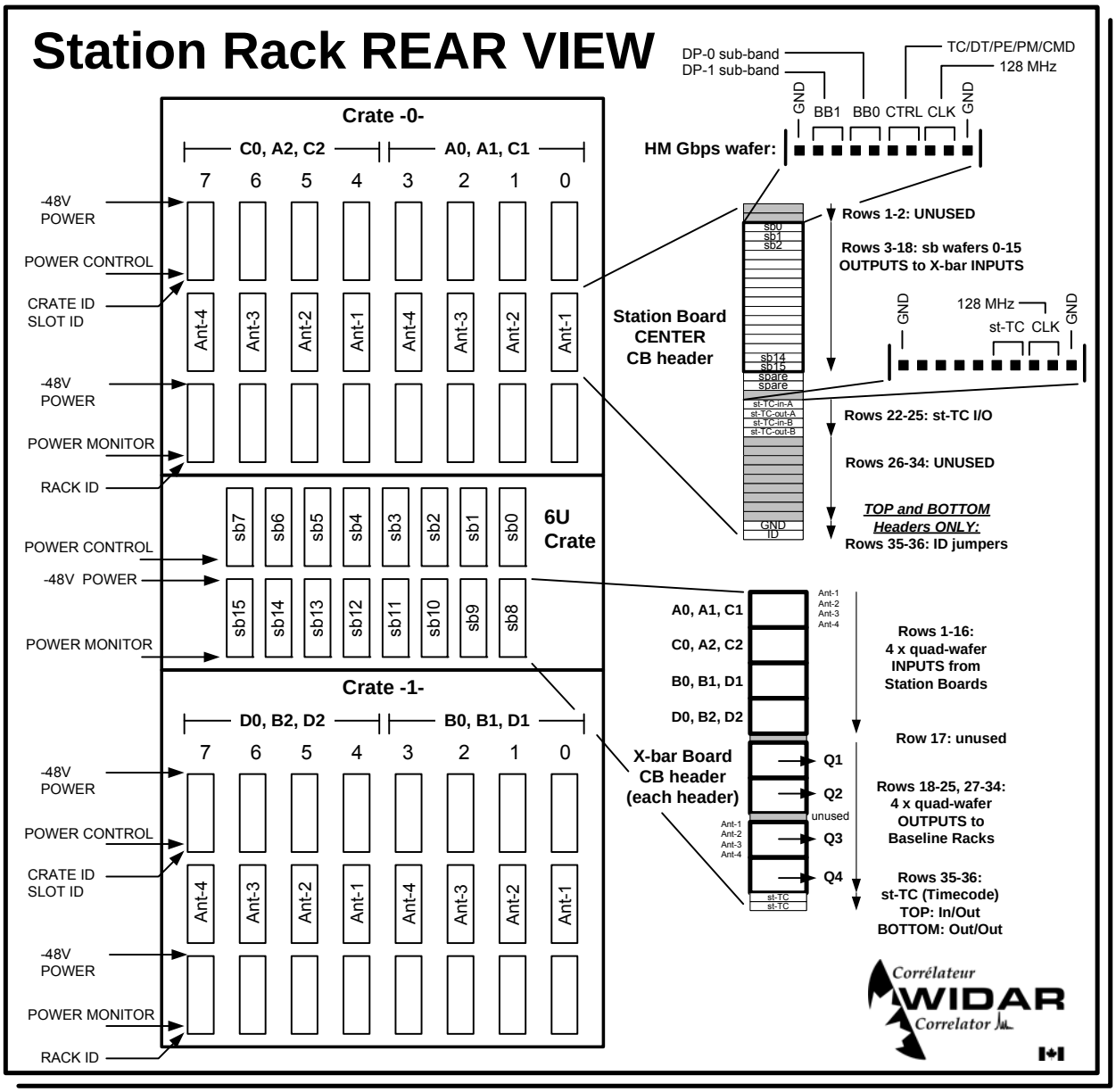


Figure 16-2 Station rack back-door decal. This decal, coupled with the Baseline rack decal, provides information on the source of data for Baseline Boards.

17 Index