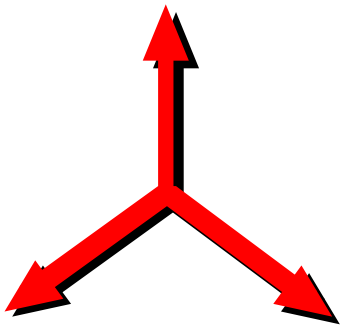
VERY LARGE ARRAY
Expansion Project



Development Specification
for the
VLA Serial Line Controller Computer Interface

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1 Introduction.

The Very Large Array (VLA) radio telescope is in the process of being upgraded to incorporate newer technology to provide expanded capability. An early phase of this upgrade, or expansion, involves the replacement of the aging Modcomp computers. The Modcomp computers provide antenna system control and monitoring functions, correlator control, and data handling functions. For the purposes of antenna system control and monitoring, the antenna hardware is interfaced to the control and monitor computers via a device called the Serial Line Controller (SLC). All commands to and monitor data from the antennas are routed through the SLC to the computers. In order to facilitate the replacement of the Modcomp control and monitor computers, the SLC interface must be adapted to the replacement computer. Subsequent phases of the expansion project will eliminate the SLC altogether.

This document describes the SLC interface and specifies the requirements necessary to connect new computers to it. It will describe the existing interface between the SLC and the Modcomp computers in terms of both hardware and software. This description will then form the basis of the requirements for the replacement computer interface which will, in turn, form the basis for the design and development of the new interface.

The intended audience for this document are the project reviewers, scientific users, and developing engineers.

1.1 Scope.

This document will describe the computer interface logic portions of the SLC and Modcomp interfaces in sufficient detail to enable design and development of custom interface hardware and/or specification of Commercial Off The Shelf (COTS) hardware and the requisite software. The complete process from requirements specification to detailed design of a Modcomp replacement interface will be presented here. This is a departure from 'common practice' where many separate documents are used to describe a project from start to finish. The reasons for this departure are as follows:

- The goal is to develop a *replacement* to an existing portion of the system. As such, much of the requirement and design specifications are already implied and just need to be gleaned from existing documentation for presentation in one convenient place (this document) which will then co-exist with the other documentation in a way that will preclude having to make changes to affected portions of the older documents.
- If the full VLA Expansion Project is realized, the control and monitor system of the VLA will probably cease to exist in its present form which means the SLC and the need to interface to it will also cease to exist. In this case, with the complete description of the Modcomp to SLC replacement interface contained in one document, we will only have one document to throw away.

Section 2 provides a general description of the whole VLA Control and Monitor System to give the reader an idea of how the SLC fits into the overall scheme. For a more detailed overall description of the VLA monitor and control system, refer to VLA Technical Report No. 44, *An Overview of the Monitor and Control System*. For an overall detailed description of the SLC, refer to VLA Technical Report No. 63, *The Serial Line Controller*.

Section 3 provides in depth functional and physical descriptions of the of the SLC to computer interface logic hardware and Modcomp software.

Section 4 specifies the requirements of the hardware and software needed to successfully interface a Modcomp replacement computer to the SLC.

Section 5 presents the detailed functional and physical descriptions of the Modcomp replacement computer and its interface to the SLC.

Section 6 provides a test plan to successfully (and with as little disruption as possible) integrate the Modcomp replacement computer and SLC interface into the existing VLA system.

1.2 Definitions, Acronyms and Abbreviations

Antenna Buffer	The hardware located in the Antenna which temporarily holds control and monitor data between the antenna end of the wave guide and the Data Sets. There are 27 Antenna Buffers (one in each antenna).
Central Buffer	The hardware located in the Control Room which temporarily holds control and monitor data between the SLC and wave guide. There are 27 Central Buffers (one for each antenna) plus one designated as the System Buffer (not associated with an antenna).
Command Mode	The portion of the VLA Machine Cycle where the SLC accepts antenna control command words from one or both of the computers attached to it.
COTS	Commercial Off The Shelf (store-bought hardware).
Data Set	The hardware located in the Antenna which distributes command data to and collects monitor data from the devices in the antenna.
DMA	Direct Memory Access. The ability of an I/O interface to get and put I/O data directly into and out of processor memory without requiring use of the processor itself.
DMP	Direct Memory Path. Modcomp's version of DMA.
Modcomp	The name of the aging computers presently being used in the VLA for correlator control and antenna control and monitoring.
Monitor Mode	The portion of the VLA Machine Cycle where the SLC collects monitor data from the Central and System Buffers and presents it to the computers.
SLC	Serial Line Controller. The NRAO built hardware interface between the control and monitor computers and the antenna hardware.

System Buffer	A Central Buffer that is used for Control Room hardware control and monitor and not associated with any one particular antenna.
VLA Machine Cycle	19.2 times a second the system goes through the cycle of sending control information to, and receiving monitor information from the antennas in a half-duplex time-shared manner. This cycle is called the VLA Machine Cycle.
VLA	Very Large Array
VLBA	Very Long Baseline Array

1.3 References

VLA Technical Report No. 44, An Overview of the Monitor and Control System, March 1980, D.W. Weber.

VLA Technical Report No. 63, *The Serial Line Controller*, 12/11/86, David Weber

VLA Drawing No. F13720L46, Serial Line Controller Model B Logic Diagram.

VLA Drawing No. D13720L78, Serial Line Controller Model C Logic Diagram.

VLA Drawing No. D13720L01, Monty Interface Logic Diagram.

VLA Drawing No. D13720L60, Bacchus Logic Diagram.

VLA Drawing No. D13720W91, SLC - Modcomp Computer Cable Wire List.

2 General System Description

The present VLA Control and Monitor System utilizes a central processing architecture where one computer controls and monitors all 27 antennas (as opposed to a distributed processing architecture where each antenna would have its own control & monitor computer). See Figure 2-1. Each of the 27 antennas contain an Antenna Buffer, LO Transceiver and MODEM, Antenna Buffer, Data Sets and associated hardware that is to be controlled and monitored. There is also a Central Buffer, Central LO Transceiver and MODEM associated with each of the 27 antennas. Additionally there is one Central Buffer called the System Buffer and associated Data Sets used for Control Room equipment control and monitor. The 27 Central Buffers and the one System Buffer interface to the single SLC (the SLC actually has enough ports to accommodate 32 buffers).

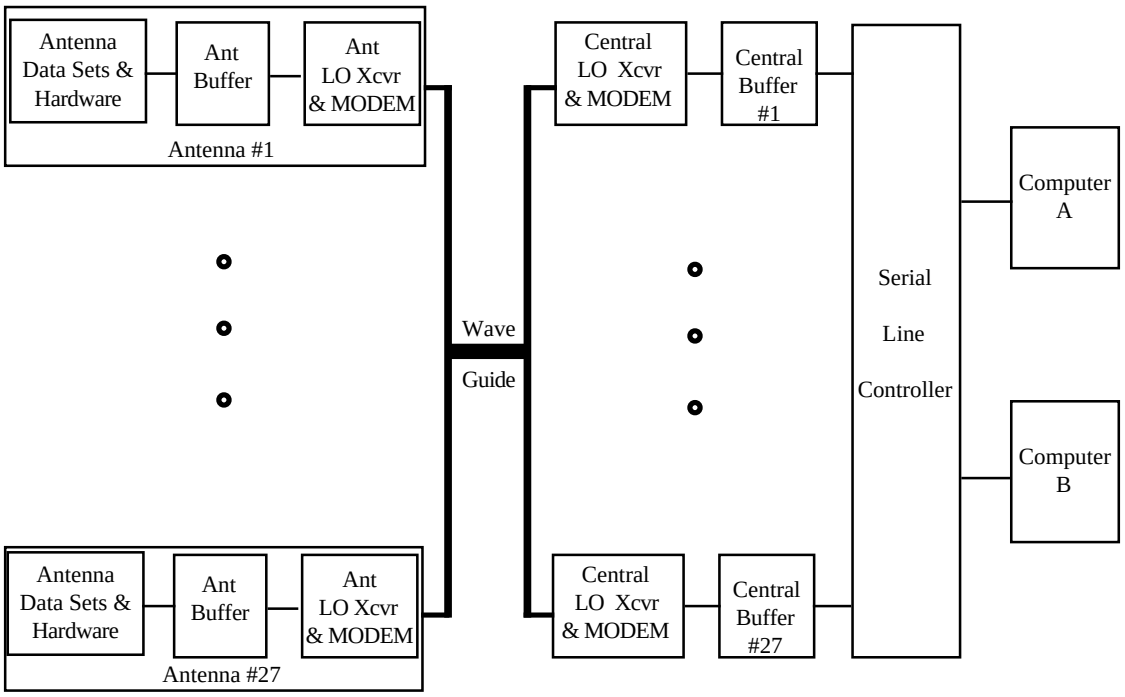


Figure 2-1. VLA Control & Monitor System Major Block Diagram.

The data to and from the 27 antennas is sent simultaneously over the wave-guide using frequency multiplexing via the LO Transceivers and MODEMs with each antenna occupying its own ‘band’.

All control and monitor data (along with the actual observation data) are passed to and from the antenna hardware via three wave-guides (one for each arm of the array) in a half-duplex mode where transmitted command data and received monitor ‘time-share’ the wave guide. This time-sharing is accomplished by allocating different times for control and monitor (transmit and receive) operations in what is called the VLA Machine Cycle. See Figure 2-2.

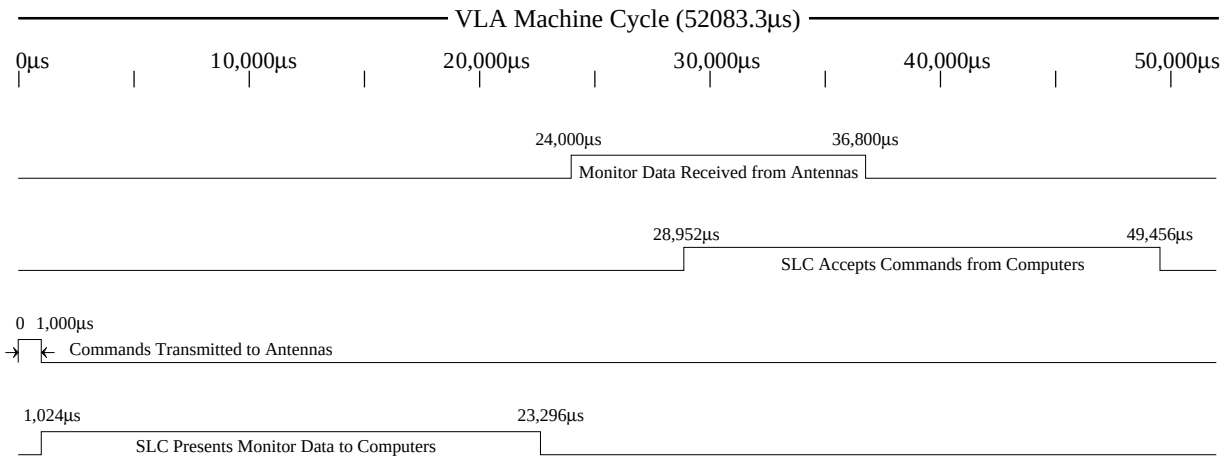


Figure 2-2. VLA Machine Cycle.

The VLA Cycles occur at a 19.2Hz rate which equates to a period of 52083µs per cycle. During time 28952µs to 49456µs of the previous cycle, command data is loaded from one or both of the control/monitor computers into the Central Buffers. Also on the previous cycle from 24000µs to 36800µs, monitor data is transmitted over the wave-guide from the Antenna Buffers into the Central Buffers. At time 0µs to 1000µs in the subsequent cycle the commands that were previously loaded into the Central Buffers are transmitted to the Antenna Buffers via the wave-guide. From 1024µs to 23296µs the SLC polls the Central Buffers for their monitor data and transfers it to the computers.

2.1 SLC General Description

The Serial Line Controller is a custom built device that provides the interface between the Modcomp computers and the Antenna Control and Monitor hardware. For command operations the SLC essentially converts parallel I/O data from the Modcomps into serial data which is RF modulated and sent to the antennas. For monitor operations, the SLC coverts the demodulated serial data from the antennas into parallel I/O data for the computers. In addition to the serial/parallel conversions, the SLC provides parity insertion, error detection and Data Set addressing error detection.

The SLC is self-contained in a rack mounted chassis with its own internal power supply. The SLC chassis provides 32 rear panel connectors that interface to the 27 Central Buffers (plus 5 for growth), eight connectors that may be connected to Data Taps to visually monitor message flow within the monitor and control system, a connector which provides a clock and other control signals and two computer interface connectors which provide 16-bit input, 16-bit output and associated handshaking signals to the Modcomp computers.

2.2 Modcomp Interface General Description

Two Modcomp computers (Monty and Bacchus) interface to the SLC via custom interface logic located on General Purpose I/O Interface boards installed in the Modcomp Peripheral Interface Chassis in the computer main frame. These are wire-wrap boards supplied by Modcomp pre-wired with logic to interface to the computer's I/O bus. The SLC interface logic portion was created by NRAO.

The Modcomp interface utilizes what is called Direct Memory Path (DMP), more commonly known as DMA (Direct Memory Access), for high-speed I/O between the SLC and the Modcomps.

It is this interface along with the Modcomp computers themselves that will be replaced in accordance with this specification.

3 SLC Detailed Description

The purpose of this section is to provide a description of the computer interface portions of the SLC at a depth sufficient to enable design of a Modcomp replacement interface. This section does not attempt to discuss the complete workings of the SLC and its interface to the antenna hardware; for a discussion of the complete SLC see VLA Technical Report No. 63, *The Serial Line Controller*, D. Weber, 12/11/86. Logic diagrams are simplified to show only components necessary for the interface circuits being discussed; for the complete SLC logic diagrams see VLA Drawing numbers F13720L46 and D13720L78; for the Modcomp Interface see VLA Drawing numbers D13720L01 and D13720L60.

3.1 System Performance Characteristics

As mentioned earlier SLC control and monitor operations take place at specific times during the VLA Machine Cycle. During this 52083μs period, up to 384 48-bit monitor words can be polled from the Central and System Buffers and sent to the two Modcomp computers. Additionally, a maximum of 128 48-bit command words can be received from the two computers during each cycle.

3.2 Hardware Functional Description

The SLC effectively acts as a serial-to-parallel interface between the control & monitor computers and the VLA antennas. Data is collected from the computers in parallel format, 48-bits per word in three 16-bit transfers, converted to serial with parity added and sent to the antenna hardware. Monitor data is polled from the antenna hardware in serial format, checked for parity and addressing errors, converted to parallel and sent to the computers.

The following subsections describe the command and monitor cycles data transfer and handshaking.

3.2.1 SLC Command Data Transfer Operation

Command operations take place during the period 28952µs - 49456µs of the VLA Cycle. During this time the two computer interfaces are queried alternately once every 160µs for one command word.

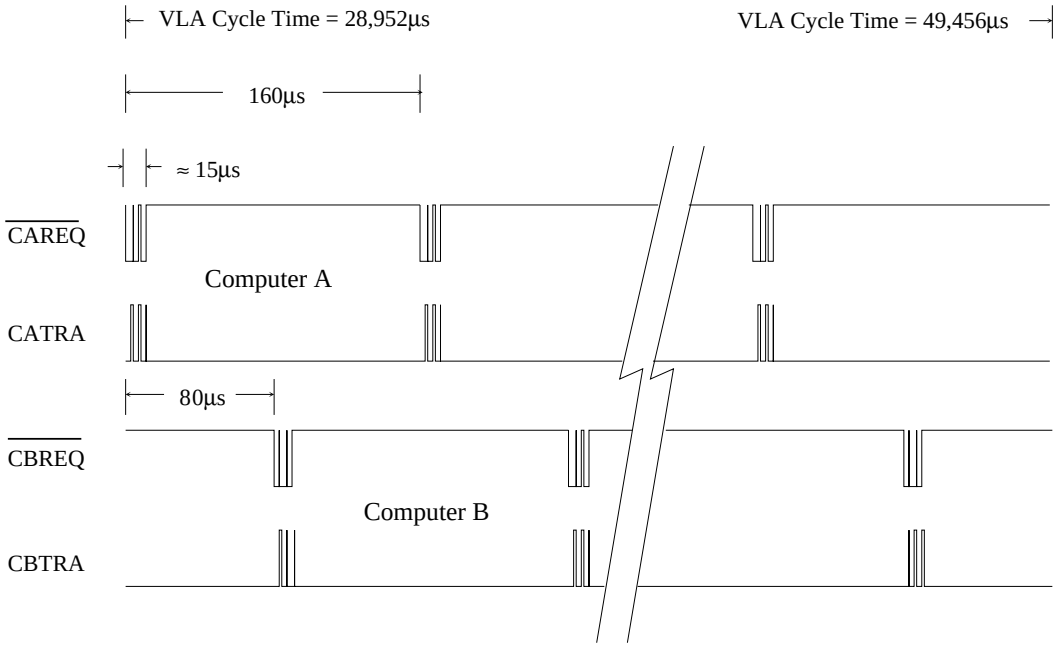


Figure 3.2.1-1. Command Cycle Timing.

This command word is 48-bits in length and is formed from three 16-bit segments generated by the computer. The three 16-bit segments are sent in a burst and must be completed within 80µs before the SLC transfer I/O to the other computer. Handshaking is accomplished by the SLC asserting CxREQ (Data Request) and the Modcomp responding CxTRA (Data Transferred).

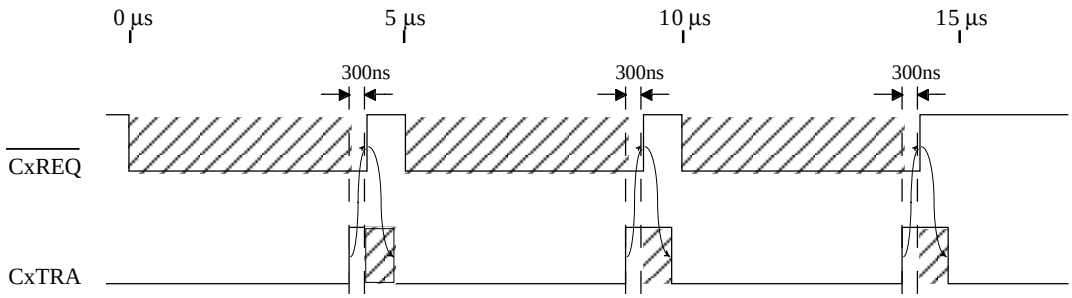


Figure 3.2.1-2. Handshaking Timing for Command Word Segment Transfers.

Refer to Figure 3.2.1-2. Typical observed transfer rates with the current SLC to Modcomp interface are on the order of 5µs per 16-bit segment thus completing a full command word transfer in approximately 15µs - well within the 80µs of allotted time. The three command word segment transfers occur as fast as the computer I/O interface (and line delays) will allow with the only speed 'governor' being a 300ns delay imposed in the SLC logic. The hash mark areas of the diagram indicate the delays imposed by the computer I/O and line delays which will vary with a different computer I/O interface.

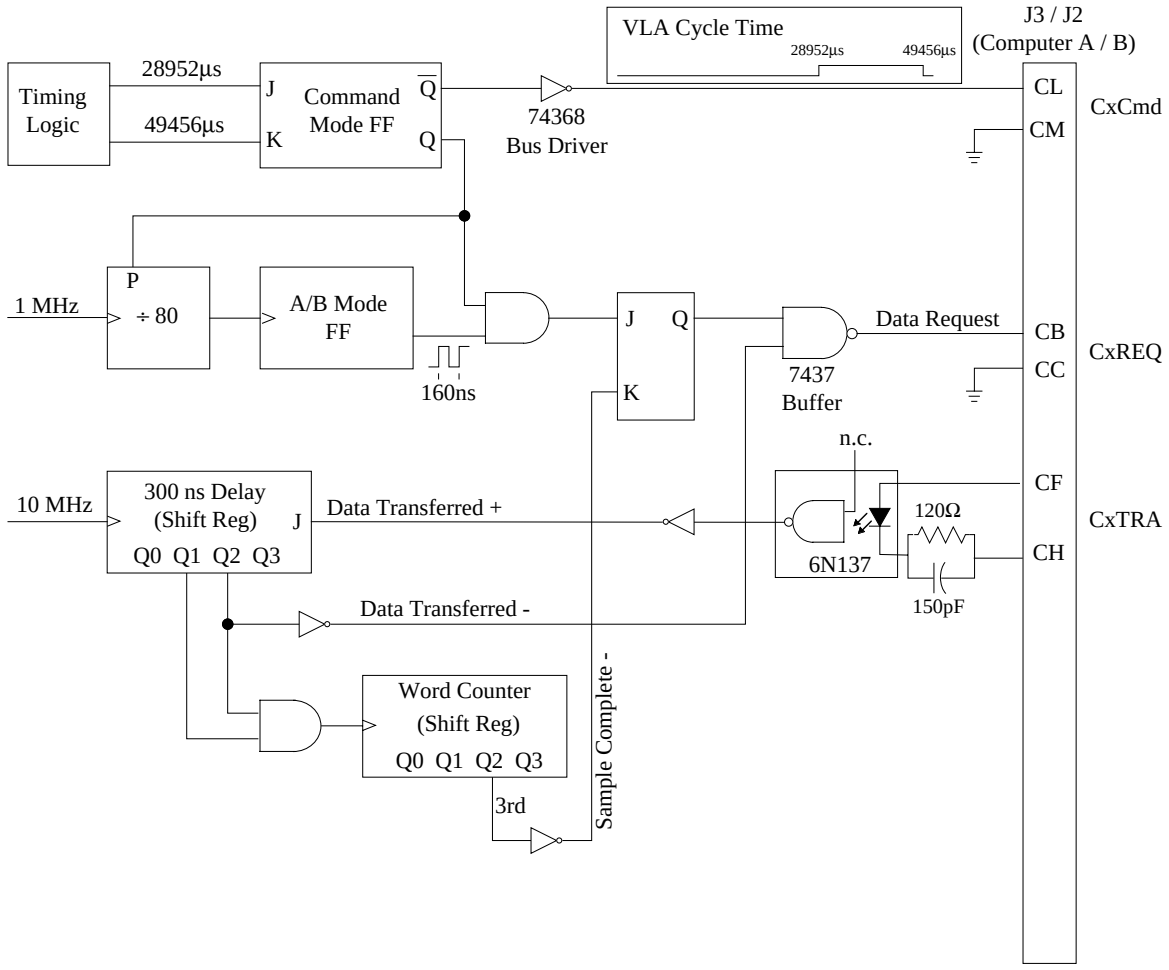


Figure 3.2.1-3. Command Word Transfer Handshaking Logic.

Refer to Figure 3.2.1-3. The figure shows the handshaking logic for one computer interface, in reality there are two identical interfaces and the signal names reflect which is which. For discussion purposes signal names such as CACMD and CBCMD are referred to as CxCMD. Timing logic in the SLC enables the Command Mode signal CxCMD at time 28952µs via the Command Mode Flip/Flop. The Command Mode Flip/Flop also enables a divide by 80 circuit fed by a 1 MHz clock which in turn toggles the A/B Mode Flip/Flop to produce the Computer A Data Request and Computer B Data Request (CxREQ) signals alternatively every 80 µs. When the computer sees CxREQ it puts the first of three 16-bit command word segments on the output data lines and raises the Data Transferred (CxTRA) line. CxTRA causes the SLC to store the

data bits in a register and starts a 300ns delay timer. After the 300ns delay, Data Xfer (-) disables CxREQ which in turn causes the computer to disable CxTRA and readies the logic for the second segment of the 3-segment command word. The second and third segments are transferred the same way with the exception that at the completion of the third segment SAMPLE COMPLETE (-) disables further CxREQs until the next 160µs period.

3.2.2 SLC Monitor Data Transfer Operation

Monitor operations take place during the period 1024µs - 23296µs of the VLA Cycle. During this time the SLC gathers monitor data from the System and Central Buffers and transfers it to the two computers concurrently at 58µs intervals.

There are 31 Central Buffers, one associated with each antenna (only 27 are in use) and one System Buffer. Each buffer has six Data Sets associated with it and two monitor words are polled from each Data Set for a total of 32 x 6 x 2 = 384 monitor data words per VLA Cycle. The first monitor data word is polled and assembled during the 58µs time period starting at time 1024µs in the VLA Cycle; during the second 58µs period, this word is transferred to the computers while the SLC simultaneously polls and assembles the second monitor data word from the Central Buffers. Thus, while the SLC is sending word n to the computers, it is gathering word n+1 from the Central Buffers.

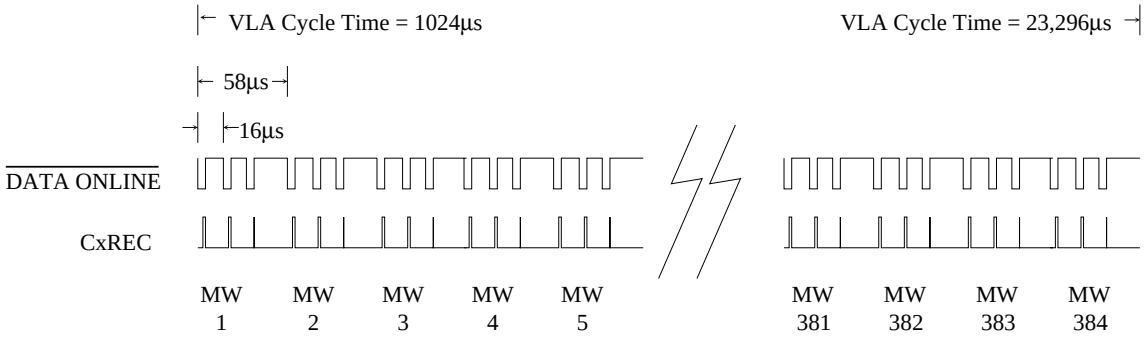


Figure 3.2.2-1. Monitor Cycle Timing.

Each monitor data word is 48 bits in length and is transferred to the computer in three 16-bit segments. Each 16-bit segment is placed on the data lines for 16µs only; the computer must accept the data within this allotted time or it will be lost. Three words are placed on the lines during each 58µs period.

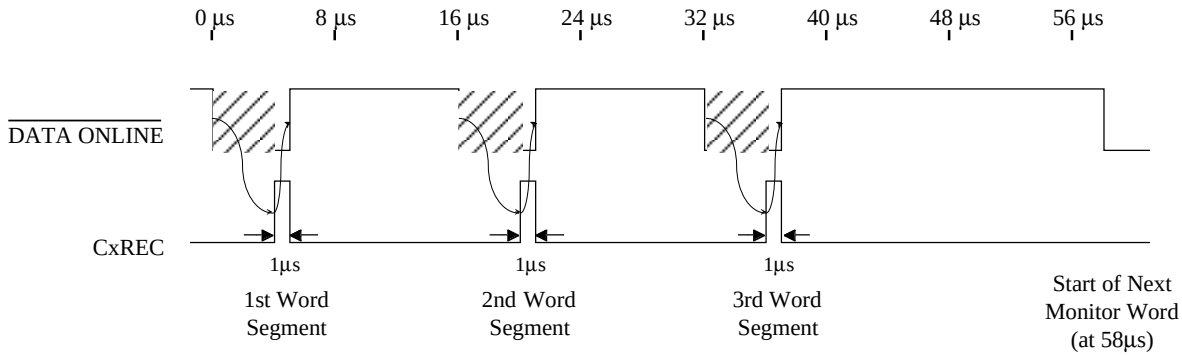
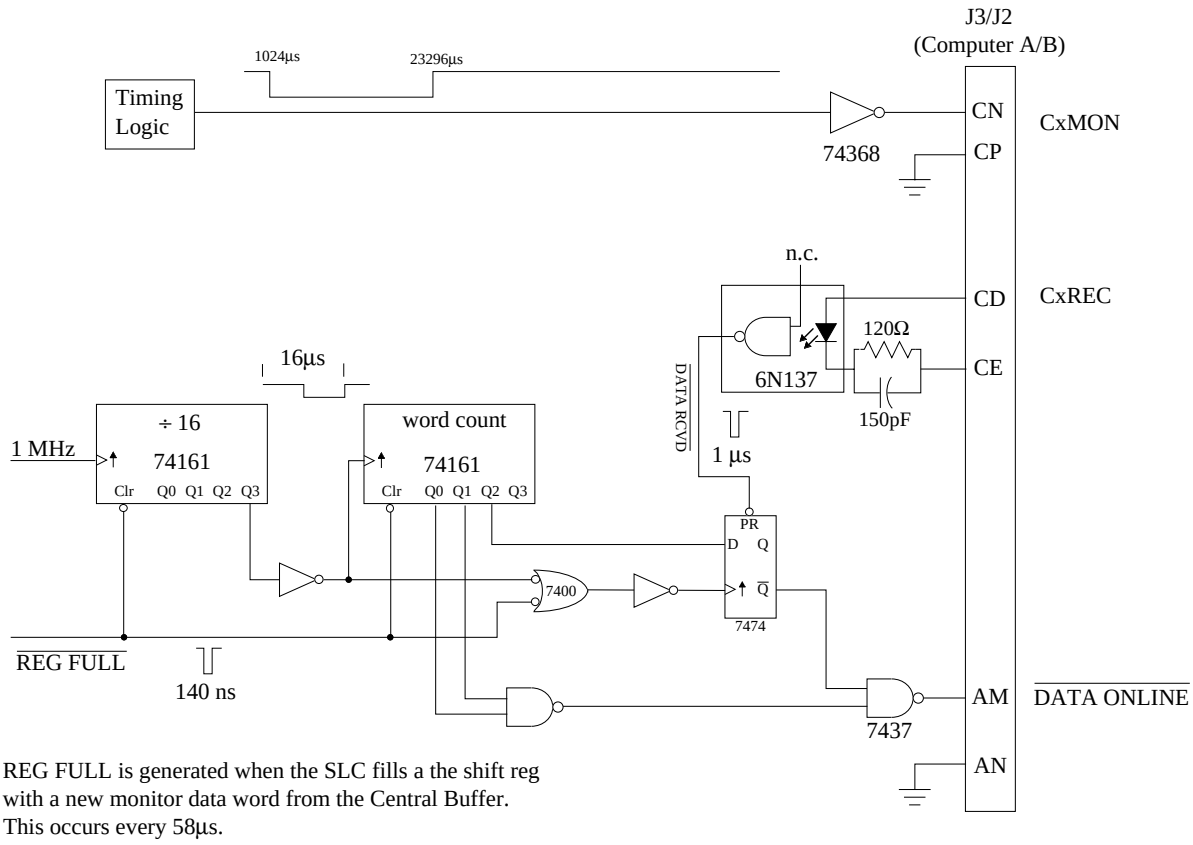


Figure 3.2.2-2. Monitor Word Transfer Detailed Timing.

The Modcomp interface takes approximately 6µs per transfer which falls well within this time. Even if the computer accepts the data faster than the 16µs allotted time, the next word will not be placed on the lines until the next 16µs period.



REG FULL is generated when the SLC fills a the shift reg with a new monitor data word from the Central Buffer. This occurs every 58µs.

Figure 3.2.2-3. Monitor Word Transfer Handshaking Logic.

Refer to Figure 3.2.2-3. Timing logic in the SLC enables CxMON at time 1024 of the VLA Cycle. This TTL signal is active HIGH and is driven by a 74368 TTL Bus Driver. CxMON remains active for the duration of the monitor word transfer portion of the VLA Cycle. After the first monitor data word is assembled from the Central Buffer and loaded into the output register, a REGISTER FULL signal is applied to initialize the monitor word transfer handshaking logic to begin a new three-word count.

A 16µs clock sequences the word counter which enables half of the DATA ONLINE output gate for the first three 16µs counts. The other half of the DATA ONLINE gate is held enabled by a D-type flip-flop. When the computer has accepted the data, it replies with CxREC which presets the flip-flop and disables the DATA ONLINE gate. CxREC is a ≈ 1µs pulse generated by a one-shot in the Modcomp interface. With the next 16µs tick from the clock, the flip-flop again

enables the DATA ONLINE gate and the cycle continues two more times (for a total of three) at which time the first half of the output gate is no longer enabled since the word count is greater than three. At the next 58μs interval, REGISTER FULL re-initializes the word count logic and the cycle repeats.

3.3 SLC Physical Description

This section describes the physical electrical and mechanical characteristics of the SLC. Its purpose is to aid in the development of a set of requirement specifications for the Modcomp replacement I/O Interface.

3.3.1 SLC Signal Electrical Characteristics

The following summarizes the handshaking and data signal characteristics associated with the SLC to computer I/O interface. The SLC specifies the computer interface (‘A’ or ‘B’) in each signal-name which is denoted by a small ‘x’ here; for example, ‘CxCMD’ would actually be seen as either ‘CACMD’ or ‘CBCMD’.

Table 3.3.1-1. SLC Signal Electrical Characteristics

CxCMD	Command Mode. Activated by the SLC during the Command Mode portion of the VLA Machine Cycle. SLC output; TTL; active HIGH; driven by a 74368 tri-state bus driver on a single fan-out.
CxMON	Monitor Mode. Activated by the SLC during the Monitor Mode portion of the VLA Machine Cycle. SLC output; TTL; active HIGH; driven by a 74368 tri-state bus driver on a single fan-out (this connector).
CxREQ	Data Request. The SLC is requesting the computer to place 16-bits of command data on the computer's output data lines. SLC output; TTL; active LOW; driven by a 7437 NAND Buffer with a fan-out of three; 1) this signal, 2) the Test Connector (J1) and 3) the PRESET input of a 7474 'D'-type Flip-Flop. This signal is active only during the Command Mode portion of the VLA Cycle and toggles to select Computer A or Computer B every 80μs (i.e. it is active Computer A for 80μs then toggles to be active for Computer B for 80μs).
CxTRA	Data Transferred. The computer tells the SLC that it has placed a 16-bit command word segment on the computer's output data lines. SLC current loop input; current required to be active ON; optically isolated input via a 6N137 Opto-isolator; typical switching delay of about 50 ns. See Optical Isolator note below.
DATA ONLINE	Data Online. The SLC has placed a monitor data word segment on the computer's input line. SLC output; TTL; active LOW; driven by a 7437 NAND Buffer with a fan-out of two; 1) this signal and 2) as a current sink for an LED on the SLC front panel Monitor Status Display - the current source is +5V through a 39Ω resistor.

Table 3.3.1-1. SLC Signal Electrical Characteristics (Cont.)

CxREC	Data Received. The computer acknowledges receipt of the monitor data word segment placed on its input lines by the SLC. SLC input; current loop input, input current required to be active ON; optically isolated via a 6N137 Opto-isolator; typical switching delay of about 50 ns. CxREC on the Modcomp side is a 1µs pulse generated from a one-shot. This pulse ends up at the PRESET pin of a 7474 flip-flop and is a pulse to ensure that the PRESET level is returned to inactive before the 16µs clock signal 'ticks' at this flip-flop (lest the clock be ignored). For this reason, it is important that CxREC arrive within 15µs to ensure the flip-flop is ready to receive the next clock. It is possible that the new interface need not generate a pulse and instead just reset CxREC when it sees DATA ONLINE go inactive. See Optical Isolator note below.
CxB01 - CxB16	Command Bits. Carry one 16-bit command word segment from the computer to the SLC. SLC optically isolated inputs via a 6N137 Opto-isolator (see note on optical isolated SLC inputs below).
IxB01 - IxB16	Monitor Bits. Carry one 16-bit monitor word segment from the SLC to the computer. SLC output; TTL active LOW driven by a 74368 tri-state bus driver with a single fan-out (this connector).

NOTE: The Optical Isolators on the input signals to the SLC employ a 120Ω current limiting resistor in series with the input diode which is a rather low value given that the 6N137 has a recommended operating current of 6.3 to 15 mA and a max of 20 mA. The Modcomp output driver for this line is a TTL level buffer so the apparent current through the input diode is about (5.0 - 1.5) / 120 = 29.2 mA. It is possible that the 150 feet of interface cable is adding the extra resistance to limit the current to a safe value.

This will have to be addressed with the new interface.

3.3.2 SLC to Computer Connector description

Figure 3.3.2-1 shows the P2 and P3 plugs which connect to J2 and J3 on the rear of the SLC chassis. This connector is the male portion of an ELCO 8016 series 90-pin connector. The view is looking into the pin side (front) of the connector.

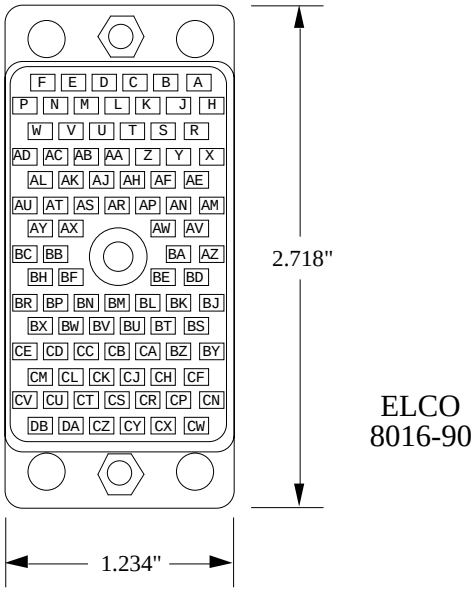


Figure 3.3.2-1. SLC Computer Interface Connector (Plug P2/P3).

3.3.3 SLC to Modcomp Wire Connection List.

Table 3.3.3-1 shows the wire connection list for the SLC to Modcomp interface cables. SLC P2 and P3 connect to J2 and J3 respectively on the rear of the SLC. Note that the 'x' in the SLC signal names denote either an 'A' or a 'B' for Computer A or Computer B. The pinouts are the same for each computer interface on P2 and P3.

Table 3.3.3-1. SLC to Modcomp Wire Connection List

SLC **P2/P3** Pin	SLC Signal Name	Modcomp **P1** Pin	Modcomp GPC Pin	Modcomp Signal Name	Remarks
A	CxB16	A13	P1-01	CMT01	
B	CxB16-R	A14	P1-14	CMT01-R	
C	CxB15	B13	P1-02	CMT02	
D	CxB15-R	B14	P1-15	CMT02-R	
E	CxB14	A11	P1-03	CMT03	
F	CxB14-R	A12	P1-16	CMT03-R	
H	CxB13	B11	P1-04	CMT04	
J	CxB13-R	B12	P1-17	CMT04-R	
K	CxB12	C11	P1-05	CMT05	
L	CxB12-R	C12	P1-18	CMT05-R	
M	CxB11	A09	P1-06	CMT06	
N	CxB11-R	A10	P1-19	CMT06-R	
P	CxB10	B09	P1-07	CMT07	
R	CxB07	B07	P1-10	CMT10	
S	CxB08	A07	P1-09	CMT09	
T	CxB08-R	A08	P1-22	CMT09-R	
U	CxB09	C09	P1-08	CMT08	
V	CxB09-R	C10	P1-21	CMT08-R	
W	CxB10-R	B10	P1-20	CMT07-R	
X	CxB07-R	B08	P1-23	CMT10-R	
Y	CxB06	C07	P1-11	CMT11	
Z	CxB06-R	C08	P1-24	CMT11-R	
AA	CxB05	A05	P1-12	CMT12	
AB	CxB05-R	A06	P1-25	CMT12-R	
AC	CxB04	B05	P1-13	CMT13	
AD	CxB04-R	B06	P1-26	CMT13-R	
AE	CxB03	H13	P2-01	CMT14	
AF	CxB03-R	H14	P2-14	CMT14-R	
AH	CxB02	J13	P2-02	CMT15	
AJ	CxB02-R	J14	P2-15	CMT15-R	
AK	CxB01	G11	P2-03	CMT16	
AL	CxB01-R	G12	P2-16	CMT16-R	

Table 3.3.3-1. SLC to Modcomp Wire Connection List (Cont.)

SLC **P2/P3** Pin	SLC Signal Name	Modcomp **P1** Pin	Modcomp GPC Pin	Modcomp Signal Name	Remarks
AM	DATA ONLINE	D11	P3-12	DOLIN	
AN	DATA ONLINE-R	D12	P3-25	DOLIN-R	
AP	IxB01	H11	P2-04	MDI01	
AR	IxB01-R	H12	P2-17	MDI01-R	
AS	IxB02	J11	P2-05	MDI02	
AT	IxB02-R	J12	P2-18	MDI02-R	
AU	+5V	E01	P4-12		
AV	IxB03	G09	P2-06	MDI03	
AW	IxB03-R	G10	P2-19	MDI03-R	
AX	IxB04	H09	P2-07	MDI04	
AY	IxB04-R	H10	P2-20	MDI04-R	
AZ	IxB05	J09	P2-08	MDI05	
BA	IxB05-R	J10	P2-21	MDI05-R	
BB	IxB06	G07	P2-09	MDI06	
BC	IxB06-R	G08	P2-22	MDI06-R	
BD	IxB07	H07	P2-10	MDI07	
BE	IxB07-R	H08	P2-23	MDI07-R	
BF	IxB08	J07	P2-11	MDI08	
BH	IxB08-R	J08	P2-24	MDI08-R	
BJ	IxB09	H05	P2-12	MDI09	
BK	IxB09-R	H06	P2-25	MDI09-R	
BL	IxB10	J05	P2-13	MDI10	
BM	IxB10-R	J06	P2-26	MDI10-R	
BN	IxB11	D17	P3-01	MDI11	
BP	IxB11-R	D18	P3-14	MDI11-R	
BR	IxB12	E17	P3-02	MDI12	
BS	IxB15	E15	P3-05	MDI15	
BT	IxB14	D15	P3-04	MDI14	
BU	IxB14-R	D16	P3-17	MDI14-R	
BV	IxB13	F17	P3-03	MDI13	
BW	IxB13-R	F18	P3-16	MDI13-R	
BX	IxB12-R	E18	P3-15	MDI12-R	
BY	IxB15-R	E16	P3-18	MDI15-R	
BZ	IxB16	F15	P3-06	MDI16	
CA	IxB16-R	F16	P3-19	MDI16-R	

Table 3.3.3-1. SLC to Modcomp Wire Connection List (Cont.)

SLC **P2/P3** Pin	SLC Signal Name	Modcomp **P1** Pin	Modcomp GPC Pin	Modcomp Signal Name	Remarks
CB	CxREQ	D07	P4-01	DAREQ	Data Request
CC	CxREQ-R	D08	P4-14	DAREQ-R	
CD	CxREC	F07	P4-02	IGOTIT	Data Rcvd
CE	CxREC-R	F08	P4-15	IGOTIT-R	
CF	CxTRA	C05	P4-03	TRANSP	Data Transferred
CH	CxTRA-R	C06	P4-16	TRANSP-R	
CJ	x-TERM	D13	P3-08	TERMTR	Terminate Transfer
CK	x-TERM-R	D14	P3-21	TERMTR-R	
CL	CxCMD	C13	P3-07	CMDMDE	Command Mode
CM	CxCMD-R	C14	P3-20	CMDMDE-R	
CN	CxMON	E13	P3-09	MONMDE	Monitor Mode
CP	CxMON-R	E14	P3-22	MONMDE-R	
CR		G13	P3-11	SSI	Select Status
CS		G14	P3-24	SSI-R	
CT	CxRES	F11	P3-13	OKRSM	OK to Resume
CU	CxRES-R	F12	P3-26	OKRSM-R	
CV		F13	P3-10	SELSL	
CW	Gnd	E02	P4-25		
CX		D01	P4-11		
CY		D02	P4-24		
CZ		D03	P4-08		
DA		D04	P4-21		
DB		F14	P3-23	SELSL-R	

3.4 Software Functional Description

TBD

4 Interface Requirement Specifications

This section specifies the requirements of an I/O Interface to provide the necessary communications between a Modcomp replacement computer and the VLA SLC. These requirements shall be used to specify a COTS I/O Interface or, in the case that one cannot be obtained to satisfy these requirements, they shall be used to design an in-house developed interface.

4.1 General

The Modcomp replacement computer will be a VME single board computer using the VxWorks Real-Time Operating System housed in a 6U VME chassis; the interface will reside in this same chassis.

4.1-1. The interface shall communicate with the processor and operating system over the standard VME backplane interface.

4.1-2. deleted.

4.1-3. The interface shall incorporate separate input (monitor) and output (command) channels.

4.1-4. Each input and output channel shall be a 16-bit parallel type with appropriate handshaking lines.

4.1-5. The interface shall be capable of storing at least 384 SLC Monitor Words x 6 bytes per word = 2304 bytes of incoming monitor data without processor involvement. This storage may be the processor board resident memory (processor memory) with access via DMA or it may be physically located on the interface itself for later transfer to the processor memory after input operations are complete.

4.1-6. The input data shall be received in 16-bit parallel fashion where three 16-bit words combine to form one 48-bit SLC monitor word as discussed in section 3 of this document.

4.1-7. The maximum time allowed for the complete transfer of one 16-bit monitor word segment input shall not exceed 16µs.

4.1-8. The interface shall be ready* to receive the next block of input data from the SLC within one VLA Machine Cycle of time (52083µs) of the start of reception of the last set.

*'ready' means that it must have an empty buffer for the incoming data. In the case of single buffering, this would mean that the previous block of monitor data must have already been delivered to the processor.

4.1-9. The interface shall also be capable of transmitting at least 128 SLC Command Words x 6 bytes per word = 768 bytes of outgoing command data without processor involvement.

4.1-10. The output data shall be sent in 16-bit parallel fashion where three 16-bit words combine to form one 48-bit SLC command word as discussed in section 3 of this document.

4.1-11. The maximum time allowed for the complete transfer of all three 16-bit command word segments shall not exceed 80μs.

4.1-12. The interface shall be ready to transmit the next block of command data within one VLA Machine Cycle of time (52083μs) of the start of transmission of the last set.

4.2 Signal Characteristics

4.2-1. deleted.

4.2-2. Input signals shall be either direct TTL coupled or optically isolated inputs.

4.2-3. All output signals that terminate in an optical isolator at the SLC shall be current limited so that $(V_O - 1.5V) \div (120\Omega + R_{line} + R_X)$ is greater than or equal to 6mA and less than or equal to 15ma with an absolute maximum rating of 20mA where R_{line} is the resistance of the connectors and wiring between the SLC and the VME interface and R_X is a series current limiting resistor added to the output signal on the VME interface (if required).

4.3 Physical Connection

4.3-1. The male plug side of an ELCO 8016-90 connector shall be used to connect the interface cable to the J2 or J3 connector jacks on the rear of the SLC.

4.3-2. The SLC cable plug shall be wired in accordance with Table 4.3-1.

Table 4.3-1. SLC Plug P2/P3 Pin Connections.

P2/P3 Pin	Signal Name
A	CxB16
B	CxB16-R
C	CxB15
D	CxB15-R
E	CxB14
F	CxB14-R
H	CxB13
J	CxB13-R
K	CxB12
L	CxB12-R
M	CxB11
N	CxB11-R
P	CxB10
R	CxB07
S	CxB08
T	CxB08-R
U	CxB09
V	CxB09-R
W	CxB10-R
X	CxB07-R
Y	CxB06
Z	CxB06-R
AA	CxB05
AB	CxB05-R
AC	CxB04
AD	CxB04-R
AE	CxB03
AF	CxB03-R
AH	CxB02
AJ	CxB02-R
AK	CxB01
AL	CxB01-R
AM	DATA ONLINE
AN	DATA ONLINE - R
AP	IxB01
AR	IxB01-R
AS	IxB02
AT	IxB02-R

P2/P3 Pin	Signal Name
AV	IxB03
AW	IxB03-R
AX	IxB04
AY	IxB04-R
AZ	IxB05
BA	IxB05-R
BB	IxB06
BC	IxB06-R
BD	IxB07
BE	IxB07-R
BF	IxB08
BH	IxB08-R
BJ	IxB09
BK	IxB09-R
BL	IxB10
BM	IxB10-R
BN	IxB11
BP	IxB11-R
BR	IxB12
BS	IxB15
BT	IxB14
BU	IxB14-R
BV	IxB13
BW	IxB13-R
BX	IxB12-R
BY	IxB15-R
BZ	IxB16
CA	IxB16-R
CB	CxREQ
CC	CxREQ-R
CD	CxREC
CE	CxREC-R
CF	CxTRA
CH	CxTRA-R
CL	CxCMD
CM	CxCMD-R
CN	CxMON
CP	CxMON-R

5 SLC to Modcomp Replacement Computer Interface Design Description

This section describes the design and development of the computer to SLC interface that replaces the existing interface between the SLC and the Modcomp computers. In a manner to similar to how Section 3 of this document described the existing SLC side of the interface in sufficient detail to develop requirements for the computer side of the interface, this section will describe the computer side of the interface in sufficient detail to create it.

5.1 Modcomp Replacement Computer System General Description

TBD

5.2 VME to SLC Interface Board Description

TBD

5.3 VME Processor Software Description

TBD

6. Test Plan

This section describes how to verify that the system described in Section 5 satisfies the requirements depicted in Section 4. It also describes how the replacement SLC interface and computer will be integrated into the existing VLA system with as little as possible disturbance to the operation of the VLA.