VERY LARGE ARRAY Expansion Project



Interim Control & Monitor Software System Overview

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1 Introduction.

An early phase of the Expanded Very Large Array (EVLA) Project is the replacement of the aging Modcomp computers currently in use. An interim Control/Monitor Processor (CMP) approach has been adopted to 1) initially take over the duties of the Modcomp computers and 2) serve in the transition phase from current VLA antenna hardware to the new EVLA hardware under control of the permanent EVLA Control/Monitor Subsystem. Using this scheme, as each VLA antenna is upgraded to an EVLA antenna, its control and monitor function responsibilities will shift from the interim CMP to the EVLA CMP with little or no visibility to the user.

The purpose of this document is to describe the software aspects of the interim Control & Monitor subsystem.

Fro a description of the current Modcomp software refer to VLA Computer Memo No. 162 "A bit level description of the Digital Control System & DCS Task".

2 Current VLA Control and Monitor System Description

This section describes the various phases proposed for the transition from the current VLA system into the EVLA system. Refer to the following diagram.



The current VLA utilizes what is called the Digital Control System (DCS) consisting of the Modcomp computers and antenna control/monitor hardware and the DCS Task software. The DCS Task communicates with the Serial Line Controller (SLC) to pass control data to and receives monitor data from the antennas. The SLC is the interface between the antenna hardware and control/monitor computers.

In the Modcomp replacement phase, an interim (to the final EVLA) processor will serve to replace the Modcomps. The interim processor will connect directly to the SLC just as the Modcomps and will control and monitor the antennas without additional hardware modification. The processing functions of the DCS Task will be emulated in the interim CMP to bring monitor data in and send control data out to the antenna. Additionally, current monitor and control applications and operator interfaces may be created to emulate those of the current Modcomps. By minimizing changes to hardware and software functionality, integration of the interim CMP processor will proceed with less unknowns and will require less regression testing.

During the transition phase, the interim CMP processor will also serve as a model and test bed for the development of the software for the ultimate EVLA Control and Monitor Subsystem. The EVLA software system will be designed using techniques to encapsulate antennas (and their requisite control/monitor methods) from the application software layer so that the application software will not be hardware specific. In this manner the same application layer of software will be used to control both the current VLA and any upgraded EVLA antennas. Utilizing this approach will allow the gradual upgrade of antennas from the current VLA types to the new EVLA types. As each antenna is upgraded, C/M functions are transparently transferred from the VLA model to the EVLA model.

3. Block Level Functional Description.

This section discusses the software functions of the Interim CMP processor. The Transition C/M Processor (MVME-162) block in the diagram above is expanded in the following diagram and each block is discussed in a little more detail in the paragraphs that follow.



The Interim C/M Processor physically consists of an MVME-162FX Embedded Controller with mezzanine connectors for up to four Industry Pack (IP) modules. Two SBS Greensprings IP-UniDig-P, 16-bit parallel I/O modules will be utilized to interface to the SLC; one for input monitor data, the other for output command data.

The first eight blocks on the left side of the diagram are low-level I/O functions who's objective is to transfer control and monitor data between the SLC and a mapped area in memory where applications can access it. This section of software will be used regardless of the higher level user applications; in other words, both the Modcomp emulation software and the EVLA model will access C/M data from the Memory Mapped C/M Data block.

Starting on the left, the I/O tasks block represents the low level interrupt handlers, DMA initialization, and etc. used to setup the IP-UniDig-P I/O modules to transfer data between the SLC and local memory of the MVME162 processor. The task(s) in this block will initialize one IP-UniDig-P module to be the transmitter and the other the receiver. Initialization will consist of

setting the proper handshaking modes for communications with the SLC and configuring DMA for communications with the MVME162.

The two DMA blocks represent the DMA processes of the MVME162. As the name suggests, these processes occur independently of the MVME162's processor. DMA transfers occur automatically under the behest of the SLC and move the SLC command and monitor data between the I/O module's input and output registers to and from the DMA buffers.

The DMA buffers reside in the MVME162's local memory and contain raw SLC data. This data is of little use to applications since it is in a specific format supported by the SLC and other antenna hardware and in no particular order. When a DMA buffer is filled (receiver) or emptied (transmitter) it represents one complete Monitor Cycle or Command Cycle data block transfer (refer to "The VLA Expansion Project - Interim Control & Monitor Processor Hardware Specification" for a more detailed description of how data is transferred to and from the SLC).

When the DMA buffers are filled or emptied interrupts are generated to request the services of the Monitor Data Demultiplexer or the Command Data Sequencer tasks.

The Monitor Data Demulitplexer converts the incoming monitor data from its SLC/antenna format into a format that application tasks can more easily digest. This involves error and validity checking and reorganizing the data from hardware addressing into a memory -mapped, monitor point, type organization. Refer to VLA Computer Memo No. 162, "A Bit-Level Description of the Digital Control System & DCS Task" for more detailed information.

The Command Data Sequencer adds the required hardware addressing information to the commands generated by the high level applications and sends the commands to the transmit DMA buffer at the required specified times (commands do not just go to the antenna when they are generated, specific command types are sent during specific VLA Machine Cycles). Refer to VLA Computer Memo No. 162, "A Bit-Level Description of the Digital Control System & DCS Task" for more detailed information.

At this point we have command and monitor data transferring to and from the SLC and being presented to user applications in an organized fashion. From here development will proceed in two directions; Modcomp Emulation and EVLA Modeling.

The purpose of Modcomp Emulation is to be able to control the VLA in the same fashion that is being done now. This is the actual Modcomp replacement phase of the VLA Expansion Project. The extent to which this phase is carried out is under discussion. In the extremes it could completely replace the Modcomp computers by fully developing all functions performed by them or it could simply be enough functionality to show that we can capture monitor data and send control data to the antenna.

The EVLA Model for VLA control phase of the development will provide a development and test bed for the design of distributed processing techniques that will be used for the EVLA. The extent to which this phase is carried out *is* known and is the complete development of a control and monitor system that will contain the functionality and structure of the final EVLA system. This system will have to be able to fully control both VLA and EVLA systems.

These final interim phases can be developed simultaneously or in sequence. As mentioned above, the extent to which Modcomp emulation is developed should be considered. On the one hand it would be beneficial to be able to have the VLA completely 'underway on MVME162 power' to ease the logistic problems associated with working concurrently with the Modcomps before we introduce new confusion with EVLA development. The cost of keeping the Modcomps on-line should also be considered if it is advantages to terminate the maintenance contract for them early. On the other hand it might be a waste of resources to develop a complete working system that will have a relatively short life-span.

Controlling the EVLA will be very different than the VLA where the nature of the control and monitoring system is based on the VLA Machine Cycle and is very time synchronous dependent. Care must be taken to avoid compromising ideal EVLA design for the sake of being able to temporarily control both systems simultaneously.