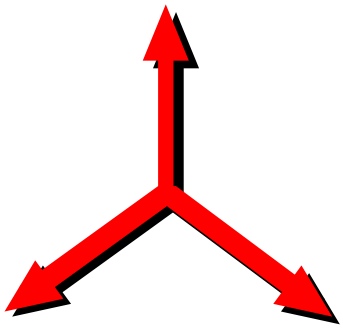
VERY LARGE ARRAY
Expansion Project



COTS Vender
Requirements Specification
for the
VLA Serial Line Controller Computer Interface

November 7, 1999

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P.O. Box 0, Socorro, New Mexico 87801

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Introduction.

This purpose of this document is to specify the electrical, mechanical and functional requirements of a COTS supplied computer to peripheral 16-bit input and 16-bit output parallel I/O **interface** with handshaking and data buffering for purchase by the National Radio Astronomy Observatory (NRAO). The **interface** will be part of the Control and Monitor subsystem of the Very Large Array (VLA) Radio Telescope. The new Control and Monitor subsystem is being developed to replace an existing subsystem and its aging computers.

Definitions, Acronyms and Abbreviations used Throughout this Document.

Antenna	A term used (in this context) interchangeably with radio telescope.
CMP	Control & Monitor Processor. A VME based single-board processor (MVME-147) running VxWorks real-time OS that is replacing the existing computers.
Interface	The parallel digital I/O interface that this document is describing. Where the word 'interface' applies to the specified device in this document, it will appear in **bold**.
SLC	Serial Line Controller. The NRAO built device that collects monitor data from, and sends command data to, the antenna array. The SLC resides between the CMP and the antenna array. The SLC will communicate with the CMP via the **interface** described in this document.
VLA Machine Cycle	19.2 times a second the system goes through the cycle of sending control information to, and receiving monitor information from the antennas in a half-duplex time-shared manner. This cycle is called the VLA Machine Cycle.
VLA	Very Large Array. A radio telescope system consisting of 27 individual radio telescopes (antennas) connected into an array. The VLA is located 60 miles west of Socorro, NM.

General Description.

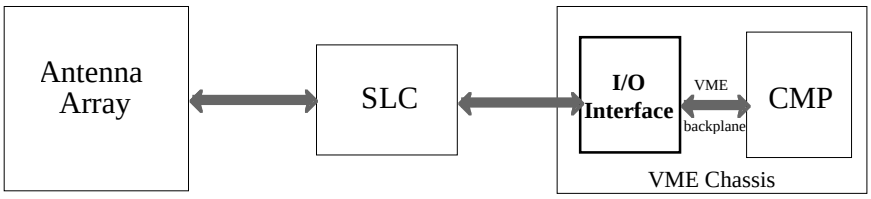
The new Control and Monitor Processor (CMP) is an MVME-147 single board computer residing in a 6U VME chassis running VxWorks Real-Time OS. The **interface** will reside in the same chassis and can occupy one or more 3U or 6U VME slots; it will communicate with the CMP over the VME backplane. The **interface** can be any of the following:

- VME board connecting directly to the VME backplane,
- Industry Pack (IP) module or modules residing on a non-intelligent VME IP Carrier board (separate modules may be used for input and output),
- PC Mezzanine Card (PMC) module or modules residing on a non-intelligent VME PMC carrier board (separate modules may be used for input and output).

The **interface** will provide parallel digital (TTL level) I/O over separate 16-bit input and 16-bit output channels with handshaking as described further in this document.

The **interface** will have the ability to transfer blocks of data without processor intervention. This can be accomplished by on-board FIFO RAM or with the MVME-147's memory using DMA provided by the **interface**. The idea is that we only want to interrupt the processor when a complete block of monitor or control data has been transferred.

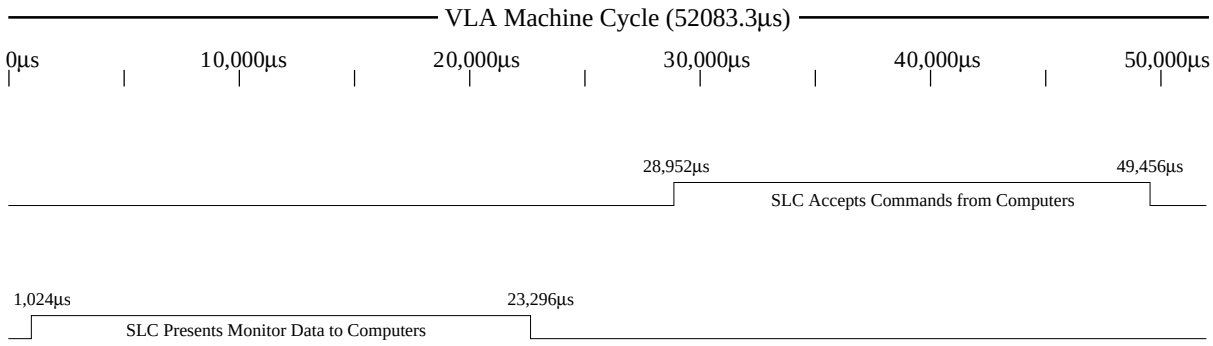
The peripheral device to which this **interface** will be connected is called the Serial Line Controller (SLC). The SLC polls monitor data from the antennas in the array and sends it to the CMP; it also accepts command data from the CMP and sends it to the antennas.



Due to the nature of how data is communicated between the SLC and the antenna array, the control and monitor data transfers are initiated by the SLC and occur at very distinct times in what is called the VLA Machine Cycle. One VLA Machine Cycle consists of:

- retrieving 384 48-bit words of monitor data from the antenna array,
- sending the monitor data to the CMP in 1152 16-bit transfers (three 16-bit words equal one 48-bit monitor data word),
- accepting 384 16-bit words of control data from the CMP,
- sending control data to the antenna array as 128 48-bit command words.

This cycle repeats 19.2 times a second for a cycle duration of 52083 µs.

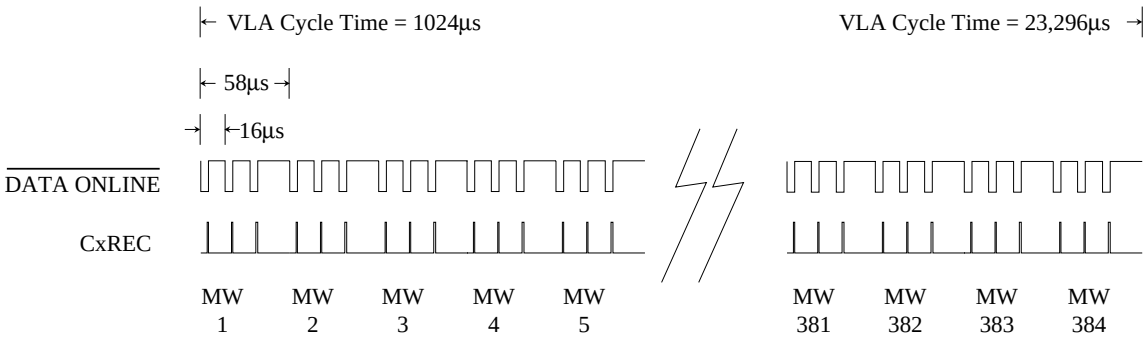


VLA Machine Cycle.

From time 1024µs to 23296µs the SLC transfers MONITOR data to the CMP and during time 28952µs to 49456µs COMMAND data is received from the CMP.

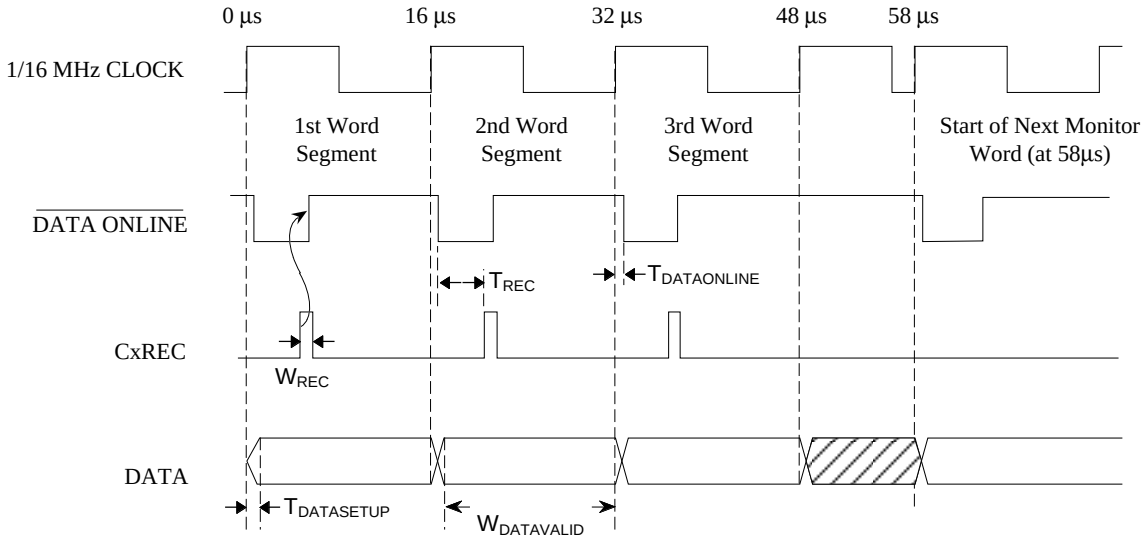
Monitor Data Transfer Operation (Data sent from SLC to Computer)

During the monitor portion of the VLA Machine Cycle, 384 monitor data words (of 48-bits per word) are sent to the CMP **interface**. Each 48-bit word is sent as a group of three 16-bit word segments.



Monitor Cycle Timing.

Each 16-bit segment is placed on the data lines for 16µs only; the CMP **interface** must accept the data within this allotted time or it will be lost. Three 16-bit segments (one 48-bit Monitor Word) are placed on the lines during each 58µs period.



Parameter	Min	Typ	Max	Notes
W_{REC}	25ns	1µs	Note 1	Note 1: WREC + TREC must not exceed 14µs
T_{REC}		Note 1		
$T_{DATASETUP}$		36ns	85ns*	* DATA ONLINE should not be used directly as a data latch since, under worst-case conditions, data may not be valid. A delay of at least 50ns should be used.
$T_{DATAONLINE}$		37µs*	108ns	
$W_{DATAVALID}$	15.9 µs			

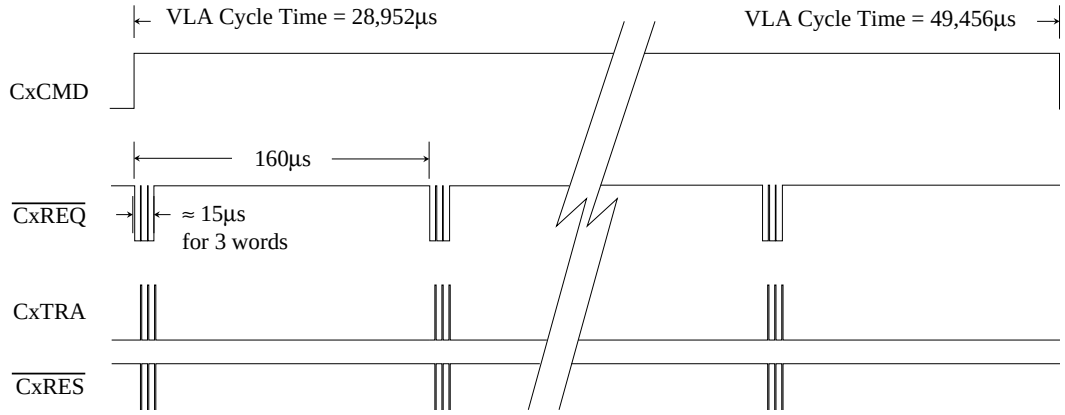
Monitor Word Transfer Detailed Timing.

The SLC asserts DATA ONLINE to let the CMP **interface** know that valid data is online. The CMP **interface** acknowledges receipt with CxREC which is a 1µs pulse. Even if the CMP **interface** accepts the data faster than the 16µs allotted time, the next word segment will not be placed on the lines until the next 16µs period.

All Monitor Cycle outputs from the SLC (CxMON, DATA ONLINE and the 16 data lines) are TTL level driven by TTL buffers or bus drivers. All signal lines into the SLC (CxREC) are terminated into a 6N137 (or equivalent) Optical Isolator.

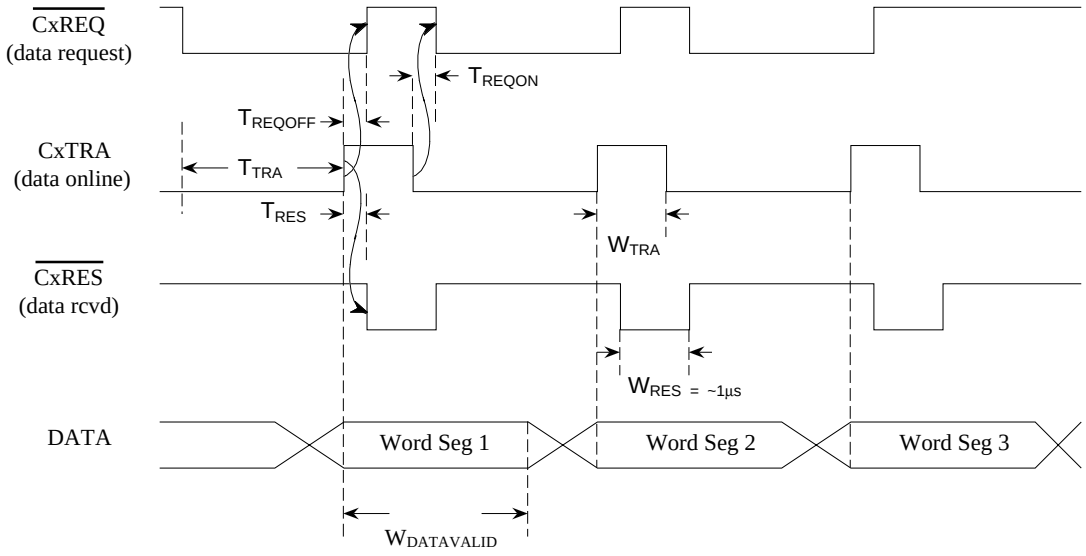
Command Data Transfer Operation (Data sent from Computer to SLC)

During the command portion of the VLA Machine Cycle, the CMP **interface** is queried every 160µs for one command word.



Command Cycle Timing.

This command word is 48-bits in length and is formed from three 16-bit segments generated by the CMP. The three 16-bit segments are sent in a 'burst' and must be completed within 80µs.



Parameter	From	To	Min	Typ	Max	Notes
T_{TRA}	CxREQ	CxTRA		Note 1		Note 1: All three word transfers must not exceed 80µs
W_{TRA}	CxTRA-ON	CxTRA-OFF	300ns	1µs	Note 1	
T_{REQOFF}	CxTRA-ON	CxREQ-OFF	200ns		400ns	
T_{REQON}	CxTRA-OFF	CxREQ-ON	200ns		400ns	
T_{RES}	CxTRA-ON	CxRES-ON	300ns		600ns	
$W_{DATAVALID}$			600ns		Note 1	

Handshaking Timing for Command Word Segment Transfers.

Handshaking is initiated by the SLC asserting CxREQ (Data Request) and the CMP **interface** responding with CxTRA (valid data online). The SLC acknowledges the data with CxRES which is a 1µs pulse.

Typical observed transfer rates with the current interface are on the order of 5µs per 16-bit segment thus completing a full command word transfer in approximately 15µs - well within the 80µs of allotted time. The three command word segment transfers occur as fast as the CMP I/O **interface** (and line delays) will allow with the only speed 'governor' being a 300ns delay imposed in the SLC logic after it receives CxTRA from the CMP **interface**.

All Command Cycle input signal lines into the SLC (CxTRA and the 16 data lines) are terminated into a 6N137 (or equivalent) Optical Isolator. All output signals (CxCMD, CxREQ and CxRES) from the SLC are TTL level buffers or bus drivers.

SLC Signal Electrical Characteristics

The following summarizes the handshaking and data signal characteristics associated with the SLC to CMP I/O **interface**.

SLC Signal Electrical Characteristics Table

Signal Name	Generated By	Remarks
CxCMD	SLC	Command Mode. Asserted by the SLC during the entire Command Mode portion of the VLA Machine Cycle. SLC output; TTL; active HIGH; driven by a 74368 tri-state bus driver on a single fan-out.
CxMON	SLC	Monitor Mode. Asserted by the SLC during the entire Monitor Mode portion of the VLA Machine Cycle. SLC output; TTL; active HIGH; driven by a 74368 tri-state bus driver on a single fan-out (this connector).
CxREQ	SLC	Data Request. The SLC is requesting the CMP **interface** to place 16-bits of command data on the output data lines. SLC output; TTL; active LOW; driven by a 7437 NAND Buffer with a fan-out of three; 1) this signal, 2) the Test Connector (J1) and 3) the PRESET input of a 7474 'D'-type Flip-Flop.
CxRES	SLC	Data Received. The SLC acknowledges receipt of data from CMP **interface**. SLC output; TTL; active LOW; ~1μs pulse driven by a 74368 tri-state bus driver on a single fan-out. This signal is available but not used in the current interface.

CxTRA	CMP	Data Transferred. The CMP **interface** tells the SLC that it has placed a 16-bit command word segment on the output data lines. SLC current loop input; current required to be active ON; optically isolated input via a 6N137 Opto-isolator; typical switching delay of about 50 ns. See Optical Isolator note below.
DATA ONLINE	SLC	Data Online. The SLC has placed a monitor data word segment on the CMP **interface**'s input lines. SLC output; TTL; active LOW; driven by a 7437 NAND Buffer with a fan-out of two; 1) this signal and 2) as a current sink for an LED on the SLC front panel Monitor Status Display - the current source is +5V through a 390Ω resistor.
CxREC	CMP	Data Received. The CMP **interface** acknowledges receipt of the monitor data word segment placed on its input lines by the SLC. SLC input; current loop input, input current required to be active ON; optically isolated via a 6N137 Opto-isolator; typical switching delay of about 50 ns. CxREC on the present interface is a 1μs pulse generated from a one-shot. This pulse ends up at the PRESET pin of a 7474 flip-flop and is a pulse to ensure that the PRESET level is returned to inactive before the 16μs clock signal 'ticks' at this flip-flop (lest the clock be ignored). For this reason, it is important that CxREC arrive within 15μs to ensure the flip-flop is ready to receive the next clock. It is possible that the new **interface** need not generate a pulse and instead just reset CxREC when it sees DATA ONLINE go inactive. See Optical Isolator note below.
CxB01 - CxB16	CMP	Command Bits. Carry one 16-bit command word segment from the CMP **interface** to the SLC. SLC optically isolated inputs via a 6N137 Opto-isolator (see note on optical isolated SLC inputs below).
IxB01 - IxB16	SLC	Monitor Bits. Carry one 16-bit monitor word segment from the SLC to the CMP **interface**. SLC output; TTL active LOW driven by a 74368 tri-state bus driver with a single fan-out (this connector).

NOTE: The Optical Isolators on the input signals to the SLC employ a 120Ω current limiting resistor in series with the input diode which is a rather

low value given that the 6N137 has a recommended operating current of 6.3 to 15 mA and a max of 20 mA. The old output driver for this line is a TTL level buffer so the apparent current through the input diode is about (5.0 - 1.5) / 120 = 29.2 mA. It is possible that the 150 feet of interface cable is adding the extra resistance to limit the current to a safe value.

The new interface cable will be less than 15 feet in length so current limiters may have to be included - this can probably be done on the SLC side if necessary.

Interface Requirement Specifications

This section specifies the requirements of an I/O **Interface** to provide the necessary communications between the CMP and the VLA SLC. These requirements shall be used to specify a COTS I/O Interface or, in the case that one cannot be obtained to satisfy these requirements, they shall be used to design an in-house developed **interface**.

The CMP will be a VME single board computer (i.e. an MVME-147) using the VxWorks Real-Time Operating System housed in a 6U VME chassis; the **interface** will reside in this same chassis.

4.1-1. The **interface** shall communicate with the CMP and operating system over the standard VME backplane interface.

4.1-2. The **interface** shall be one of the following:

1) Standalone 3U or 6U VME board,

2) Industry Pack (IP) module(s) seated in a 'dumb' 3U or 6U VME carrier board,

3) PMC module(s) seated in a 'dumb' 3U or 6U VME carrier board or,

4) 3U or 6U VME prototyping board with necessary VME backplane interface.

4.1-3. The **interface** shall incorporate separate input (monitor) and output (command) channels. If IP or PMC modules are used, two modules - one for input and one for output - may be utilized.

4.1-4. Each input and output channel shall be a 16-bit parallel type with appropriate handshaking lines.

4.1-5. The **interface** shall be capable of storing at least 384 SLC Monitor Words x 6 bytes per word = 2304 bytes of incoming monitor data without CMP involvement. This storage may be the CMP resident memory (processor memory) with access via DMA or it may

be physically located on the **interface** itself (FIFO RAM) for later transfer to CMP memory after input operations are complete.

4.1-6. The input data shall be received in 16-bit parallel fashion where three 16-bit words combine to form one 48-bit SLC monitor word as discussed earlier in this document.

4.1-7. The maximum time allowed for the complete transfer of one 16-bit monitor word segment input shall not exceed 16μs.

4.1-8. The **interface** shall be ready* to receive the next block of input data from the SLC within one VLA Machine Cycle of time (52083μs) of the start of reception of the last set.

*'ready' means that it must have an empty buffer for the incoming data. In the case of single buffering, this would mean that the previous block of monitor data must have already been delivered to the processor's memory.

4.1-9. The **interface** shall also be capable of transmitting at least 128 SLC Command Words x 6 bytes per word = 768 bytes of outgoing command data without CMP involvement.

4.1-10. The output data shall be sent in 16-bit parallel fashion where three 16-bit words combine to form one 48-bit SLC command word as discussed earlier in this document.

4.1-11. The maximum time allowed for the complete transfer of all three 16-bit command word segments shall not exceed 80μs.

4.1-12. The **interface** shall be ready to transmit the next block of command data within one VLA Machine Cycle of time (52083μs) of the start of transmission of the last set.

4.1-13 All CMP **interface** board output signals shall be at TTL levels.

4.1-14 If open collector or relay type outputs are utilized, pull-up resistors must be made available on the **interface** board.

4.1-15 If optically isolated outputs are utilized, the current loop source must be supplied by the **interface** board.

4.1-16 All CMP **interface** board input signals shall operate at TTL levels.

4.1-17 The input signals may be optically isolated but this is not required.